



**THE DATASHEET OF  
BSC0923NDI**



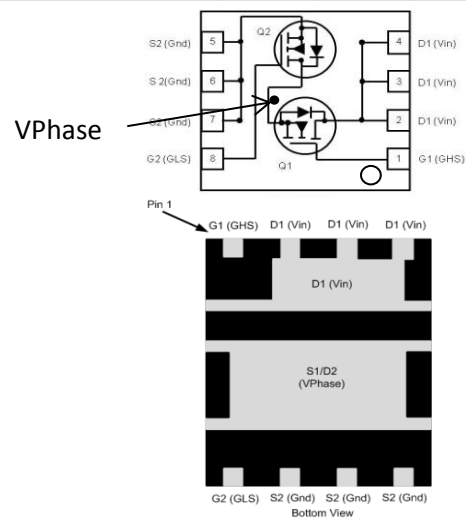
## Dual N-Channel OptiMOS™ MOSFET

### Features

- Dual N-channel OptiMOS™ MOSFET
- Optimized for high performance Buck converter
- Logic level (4.5V rated)
- 100% avalanche tested
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product Summary

		Q1	Q2	
$V_{DS}$		30	30	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	5	2.8	mΩ
	$V_{GS}=4.5\text{ V}$	7	3.7	
$I_n$		40	40	A



Type	Package	Marking
BSC0923NDI	PG-TISON-8	0923NDI

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified <sup>2)</sup>

Parameter	Symbol	Conditions	Value		Unit
			Q1	Q2	
Continuous drain current	$I_D$	$T_C=70\text{ °C}$ , $V_{GS}=10\text{V}$	40	40	A
		$T_A=25\text{ °C}$ , $V_{GS}=4.5\text{V}^{3)}$	17	32	
		$T_A=70\text{ °C}$ , $V_{GS}=4.5\text{V}^{3)}$	14	25	
		$T_A=25\text{ °C}$ , $V_{GS}=10\text{V}^{4)}$	10	15	
Pulsed drain current <sup>5)</sup>	$I_{D,pulse}$	$T_C=70\text{ °C}$	160	160	
Avalanche energy, single pulse	$E_{AS}$	Q1: $I_D=20\text{ A}$ , Q2: $I_D=20\text{ A}$ , $R_{GS}=25\text{ Ω}$	9	20	mJ
Gate source voltage	$V_{GS}$		±20		V
Power dissipation	$P_{tot}$	$T_A=25\text{ °C}^{2)}$	2.5	2.5	W
		$T_A=25\text{ °C}$ , minimum footprint <sup>3)</sup>	1.0	1.0	
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> One transistor active

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup> Device mounted on a minimum pad (one layer, 70 μm thick). One transistor active

<sup>5)</sup> See figure 3 for more detailed information.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	Q1	$R_{thJC}$		-	-	4.2	K/W
	Q2			-	-	2.6	
Thermal resistance, junction - ambient <sup>1)</sup>	Q1	$R_{thJA}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	
	Q2						
	Q1		minimal footprint, steady state <sup>3)</sup>	-	-	125	
	Q2						

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	Q1	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=10\text{ mA}$	30	-	-	V
	Q2						
Breakdown voltage temperature coefficient	Q1	$dV_{(BR)DSS}/dT_j$	$I_D=10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	-	15	-	mV/K
	Q2						
Gate threshold voltage	Q1	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1.2	-	2	V
	Q2						
Zero gate voltage drain current	Q1	$I_{DSS}$	$V_{DS}=24\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
	Q2					500	
	Q1		$V_{DS}=24\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	0.1	mA
	Q2				3	-	
Gate-source leakage current	Q1	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
	Q2						
Drain-source on-state resistance	Q1	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=20\text{ A}$	-	5.4	7.0	m $\Omega$
	Q2				3	3.7	
	Q1		$V_{GS}=10\text{ V}, I_D=20\text{ A}$	-	3.8	5.0	
	Q2				2.1	2.8	
Gate resistance	Q1	$R_G$		1.3	2.6	5.2	$\Omega$
	Q2			0.5	0.9	1.8	
Transconductance	Q1	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=20\text{ A}$	32	65	-	S
	Q2				43	86	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	Q1	$C_{iss}$	$V_{GS}=0\text{ V},$ $V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	870	1160	pF
	Q2			-	1500	2000	
Output capacitance	Q1	$C_{oss}$		-	330	439	
	Q2			-	630	838	
Reverse transfer capacitance	Q1	$C_{rss}$		-	49	-	
	Q2			-	88	-	
Turn-on delay time	Q1	$t_{d(on)}$	$V_{DD}=15\text{ V},$ $V_{GS}=10\text{ V}, R_G=1.6\ \Omega,$ $I_D=20\text{ A}$	-	4.7	-	ns
	Q2			-	4.1	-	
Rise time	Q1	$t_r$		-	3.8	-	
	Q2			-	3.6	-	
Turn-off delay time	Q1	$t_{d(off)}$		-	17	-	
	Q2			-	19	-	
Fall time	Q1	$t_f$		-	3.0	-	
	Q2			-	2.6	-	

**Gate Charge Characteristics**

Gate to source charge	Q1	$Q_{gs}$	$V_{DD}=15\text{ V},$ $I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	2.4	3.2	nC	
Gate to drain charge		$Q_{gd}$		-	2.2	2.9		
Gate charge total		$Q_g$		-	6.7	10		
Gate plateau voltage		$V_{plateau}$		-	2.8	-		V
Gate to source charge	Q2	$Q_{gs}$		-	4.0	5.3	nC	
Gate to drain charge		$Q_{gd}$		-	4.0	5.2		
Gate charge total		$Q_g$		-	12	18.4		
Gate plateau voltage		$V_{plateau}$		-	2.6	-		V
Output charge	Q1	$Q_{oss}$		$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	9	12	nC
	Q2				-	17	23	

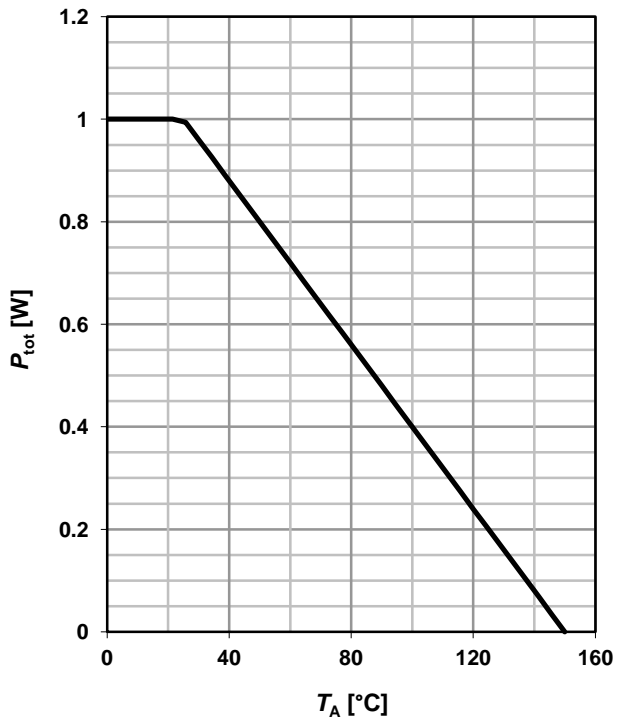
Parameter	Symbol	Conditions	Values			Unit	
			min.	typ.	max.		
<b>Reverse Diode</b>							
Diode continuous forward current	Q1	$I_S$	$T_C=25\text{ °C}$	-	-	30	A
	Q2					40	
Diode pulse current	Q1	$I_{S,pulse}$	$T_C=25\text{ °C}$	-	-	160	
	Q2			-	-	160	
Diode forward voltage	Q1	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ °C}$	-	0.9	1	V
	Q2		$V_{GS}=0\text{ V}, I_F=4\text{ A},$ $T_j=25\text{ °C}$	-	0.54	0.7	
Reverse recovery charge	Q1	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	5	-	nC
	Q2			-	5	-	nC

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> device mounted on a minimum pad (one layer, 70 μm thick)

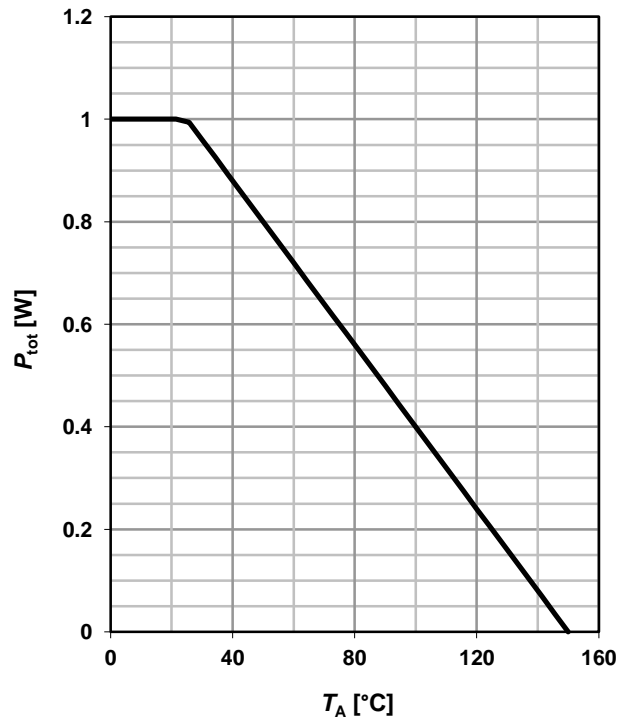
**1 Power dissipation (Q1)**

$$P_{\text{tot}}=f(T_A)^3$$



**2 Power dissipation (Q2)**

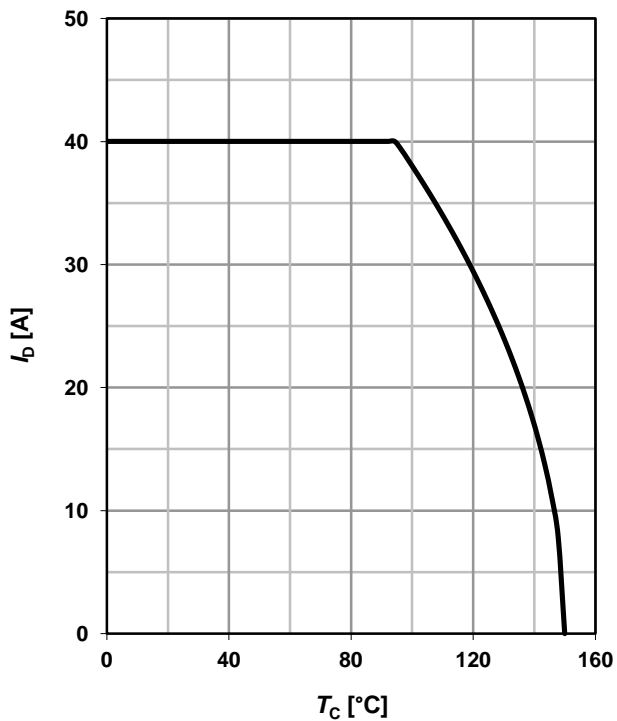
$$P_{\text{tot}}=f(T_A)^3$$



**3 Drain current (Q1)**

$$I_D=f(T_C)$$

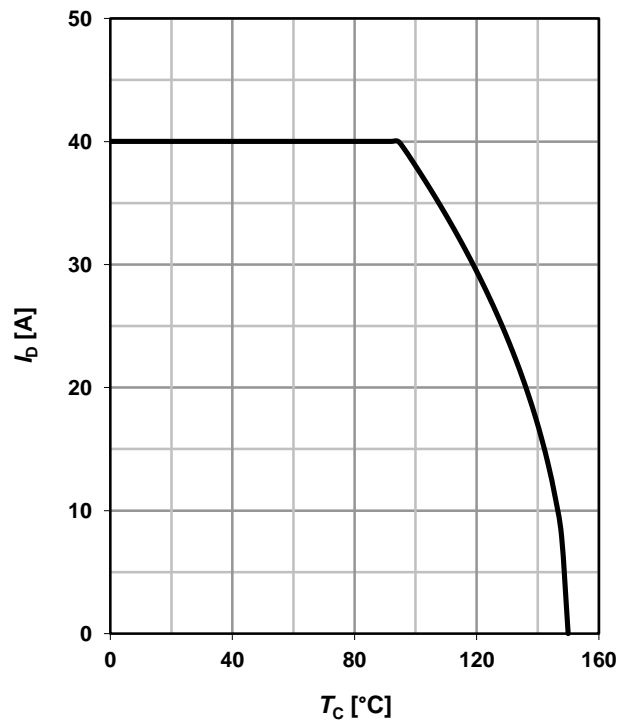
parameter:  $V_{GS} \geq 10$  V



**4 Drain current (Q2)**

$$I_D=f(T_C)$$

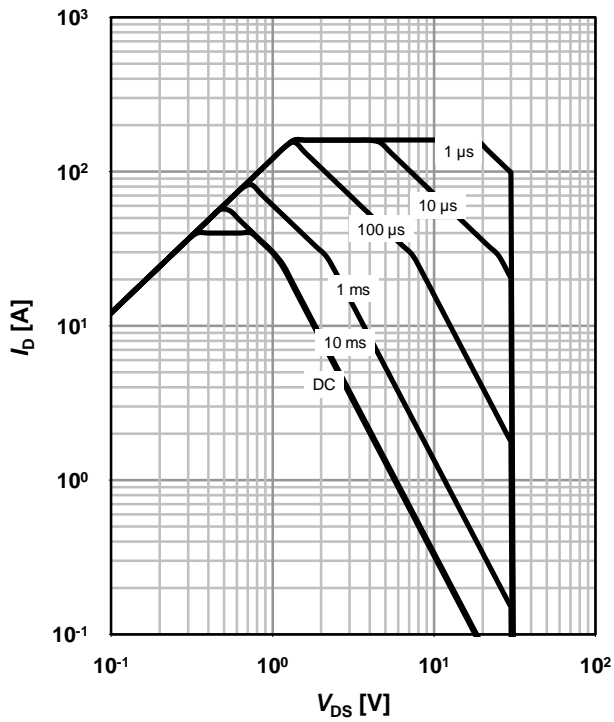
parameter:  $V_{GS} \geq 10$  V



**5 Safe operating area (Q1)**

$I_D=f(V_{DS}); T_C=25\text{ }^\circ\text{C}; D=0$

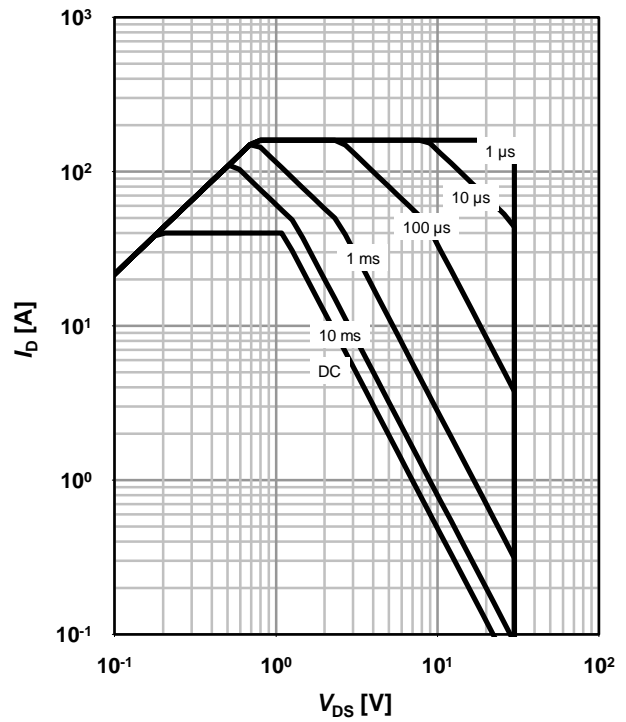
parameter:  $t_p$



**6 Safe operating area (Q2)**

$I_D=f(V_{DS}); T_C=25\text{ }^\circ\text{C}; D=0$

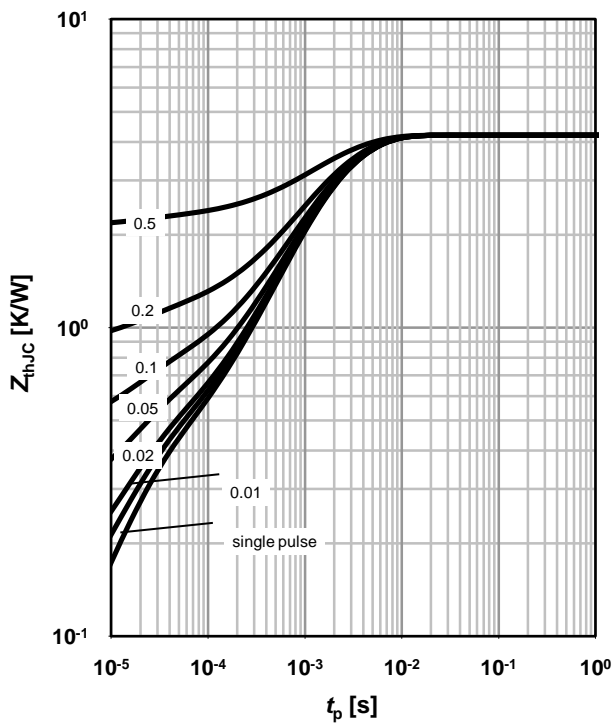
parameter:  $t_p$



**7 Max. transient thermal impedance (Q1)**

$Z_{thJC}=f(t_p)$

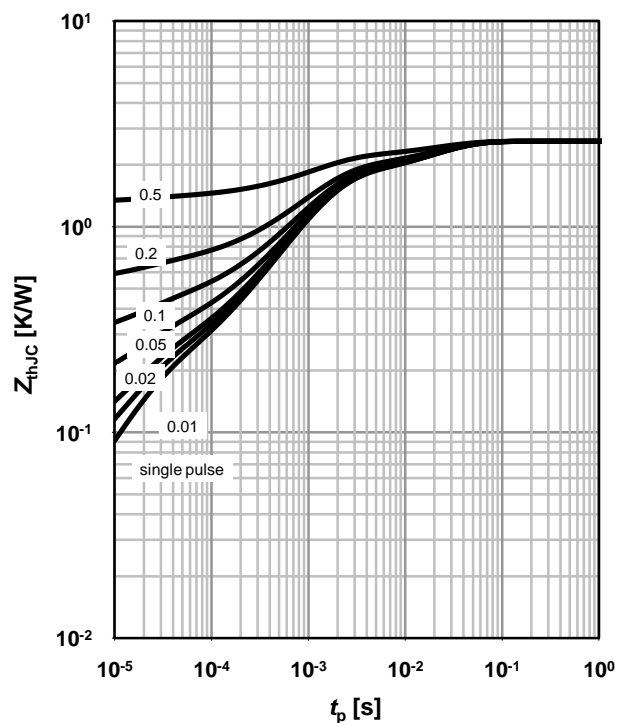
parameter:  $D=t_p/T$



**8 Max. transient thermal impedance (Q2)**

$Z_{thJC}=f(t_p)$

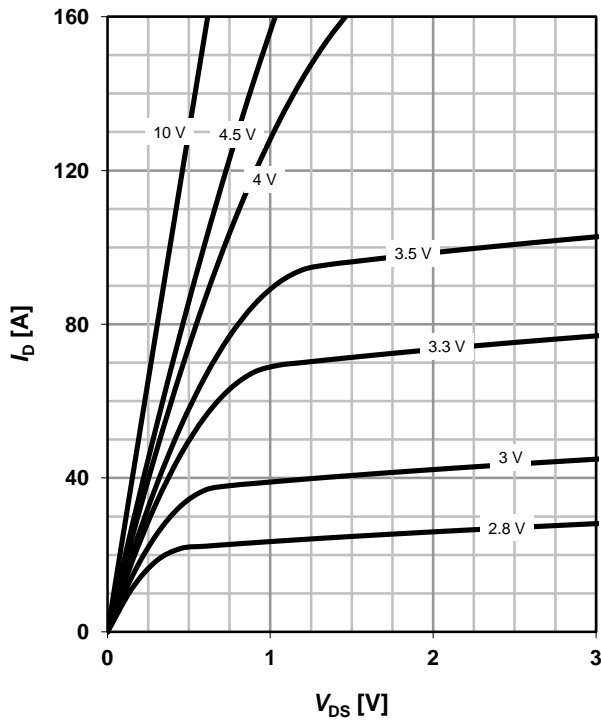
parameter:  $D=t_p/T$



**9 Typ. output characteristics (Q1)**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

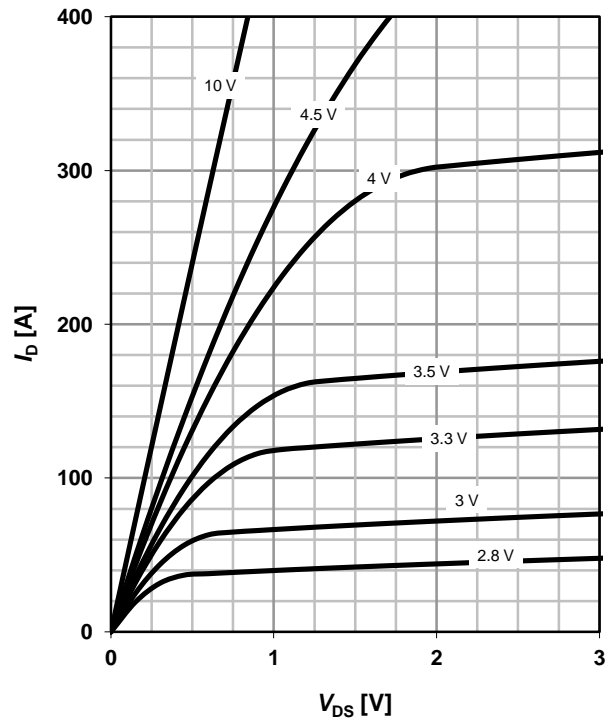
parameter:  $V_{GS}$



**10 Typ. output characteristics (Q2)**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

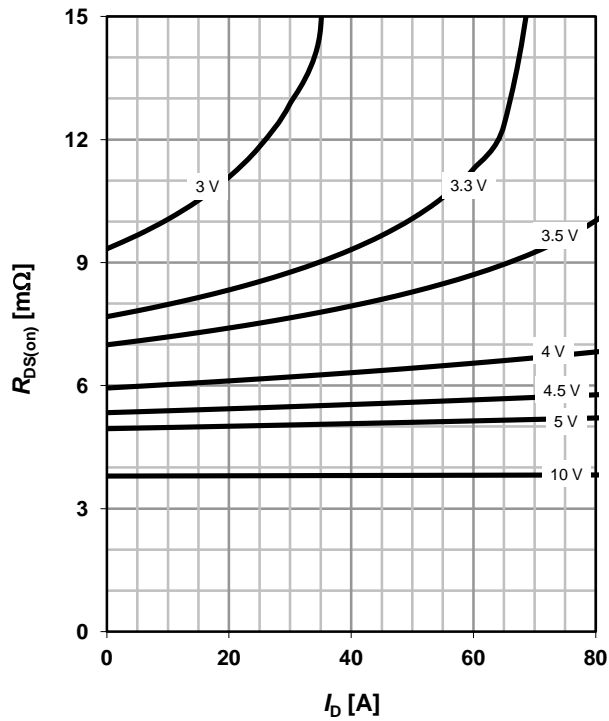
parameter:  $V_{GS}$



**11 Typ. drain-source on resistance (Q1)**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

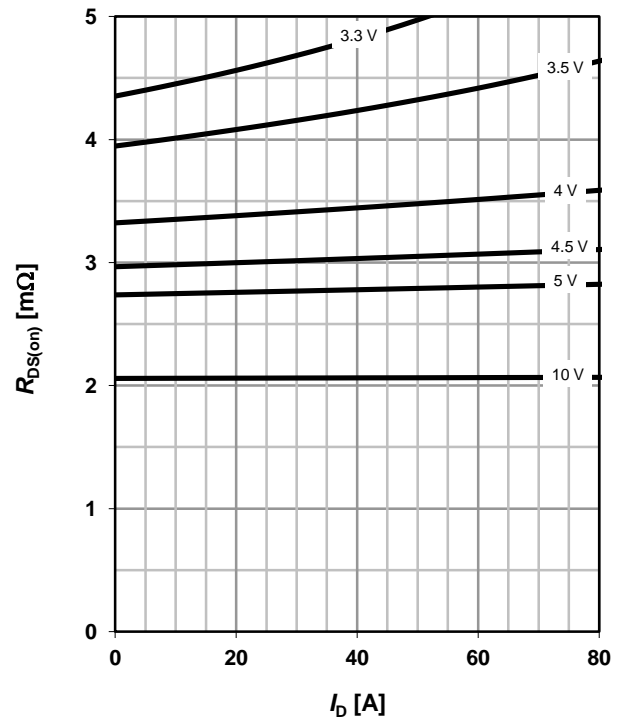
parameter:  $V_{GS}$



**12 Typ. drain-source on resistance (Q2)**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

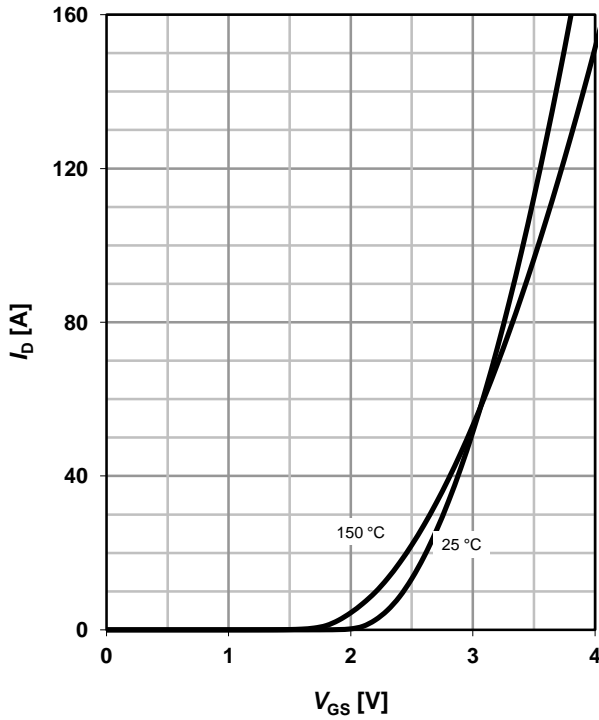
parameter:  $V_{GS}$



**13 Typ. transfer characteristics (Q1)**

$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

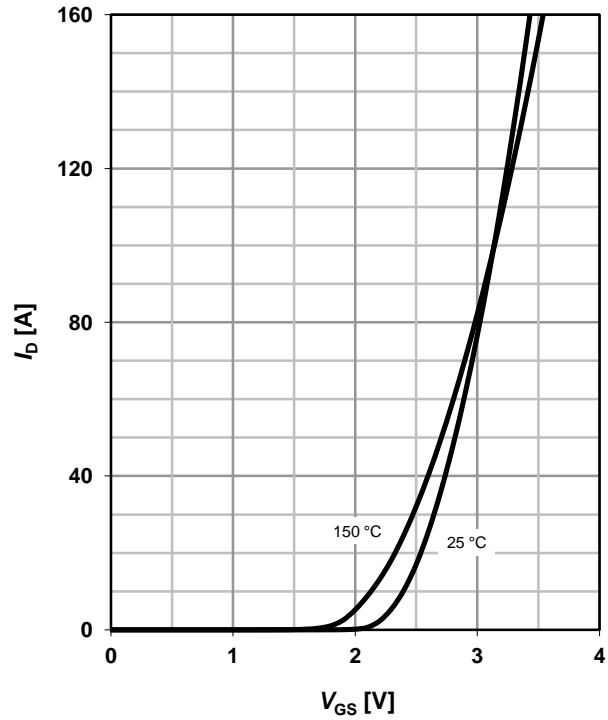
parameter:  $T_j$



**14 Typ. transfer characteristics (Q2)**

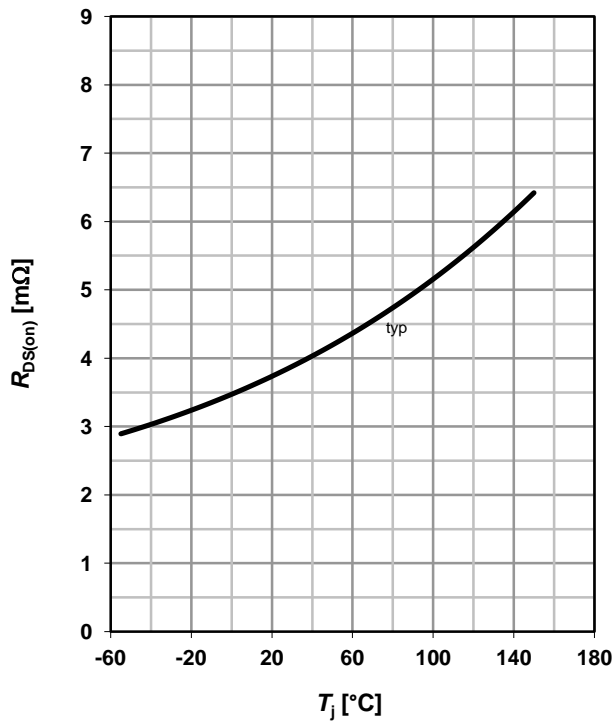
$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

parameter:  $T_j$



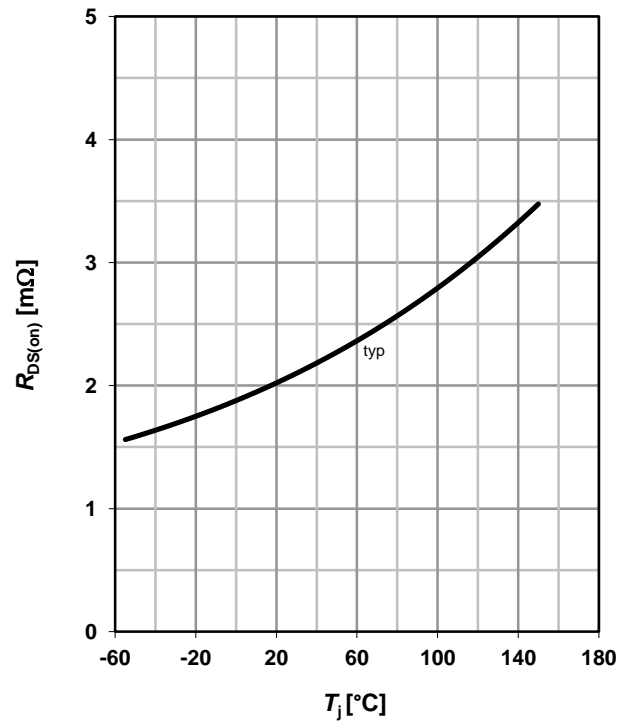
**15 Drain-source on-state resistance (Q1)**

$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$



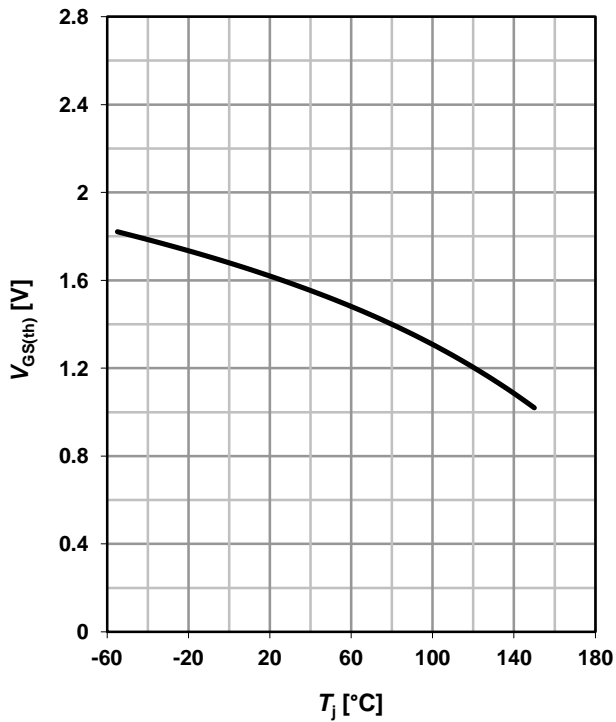
**16 Drain-source on-state resistance (Q2)**

$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$



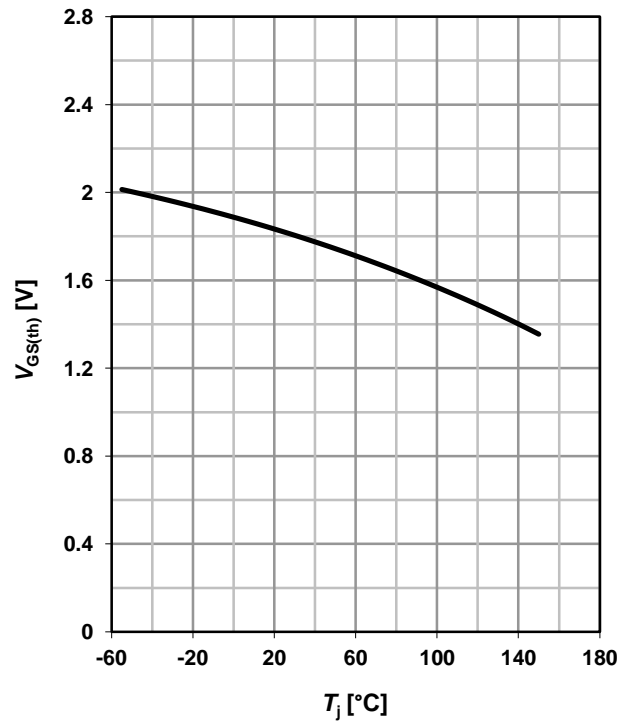
**17 Typ. gate threshold voltage (Q1)**

$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=250 \mu A$



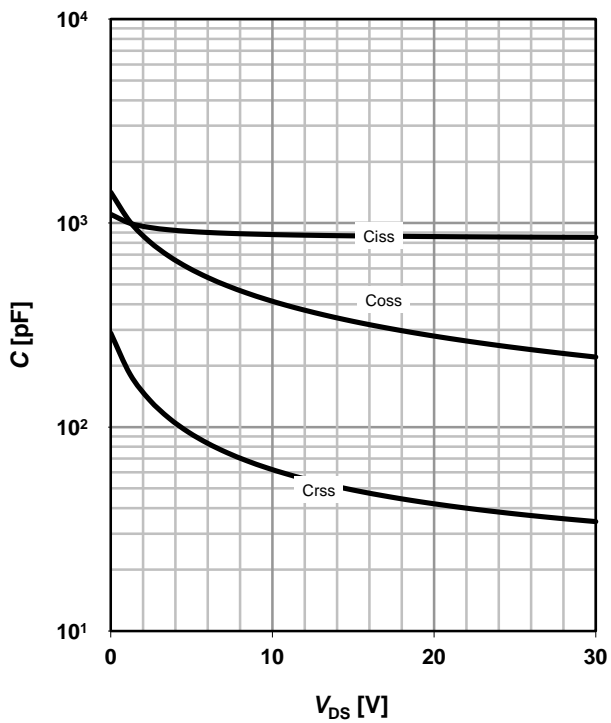
**18 Typ. gate threshold voltage (Q2)**

$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=10 \text{ mA}$



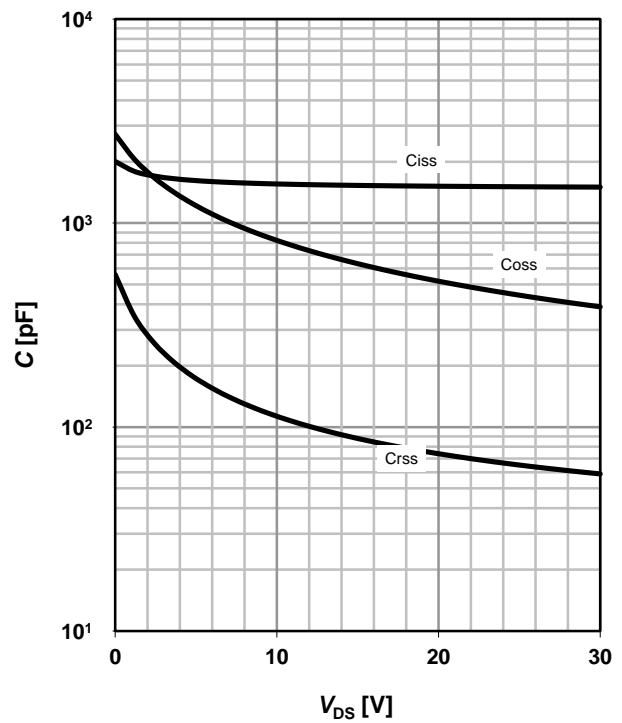
**19 Typ. capacitances (Q1)**

$C=f(V_{DS})$ ;  $V_{GS}=0 \text{ V}$ ;  $f=1 \text{ MHz}$



**20 Typ. capacitances (Q2)**

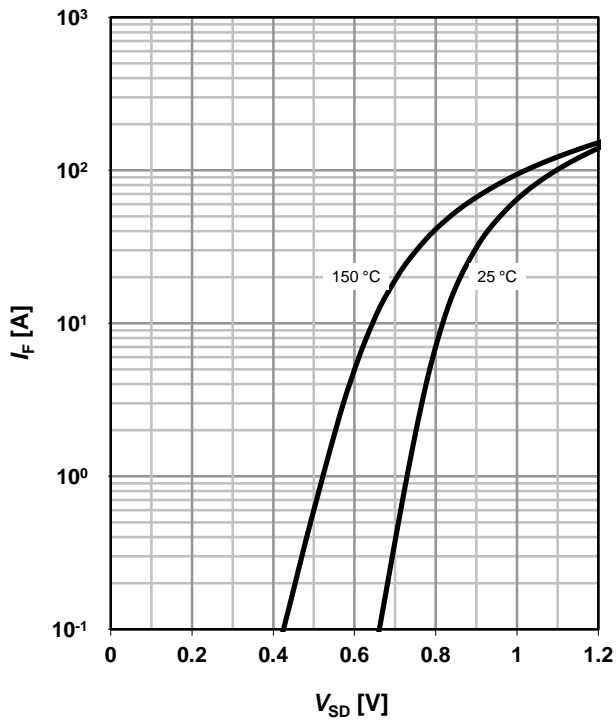
$C=f(V_{DS})$ ;  $V_{GS}=0 \text{ V}$ ;  $f=1 \text{ MHz}$



**21 Forward characteristics of reverse diode (Q1)**

$I_F=f(V_{SD})$

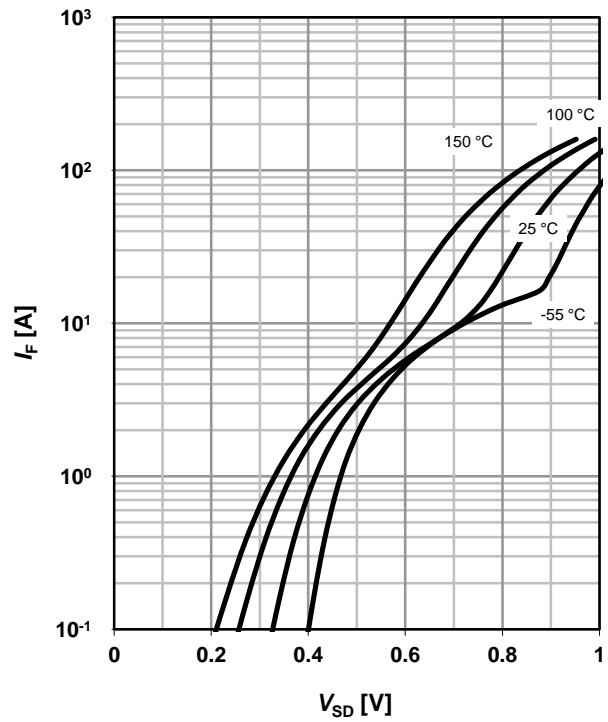
parameter:  $T_j$



**22 Forward characteristics of reverse diode (Q2)**

$I_F=f(V_{SD})$

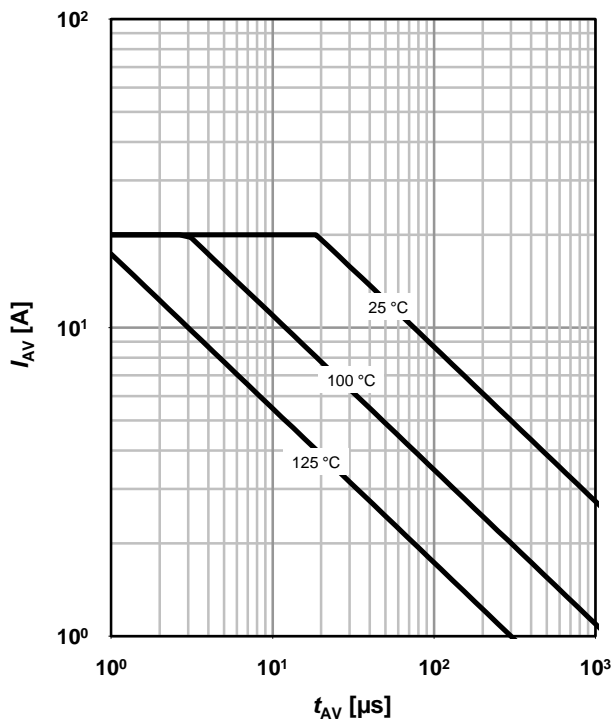
parameter:  $T_j$



**23 Avalanche characteristics (Q1)**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

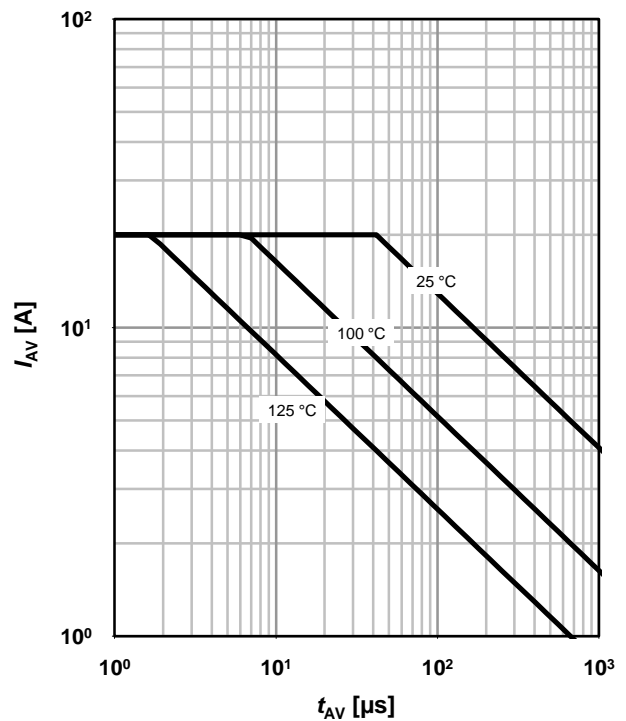
parameter:  $T_{j(start)}$



**24 Avalanche characteristics (Q2)**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

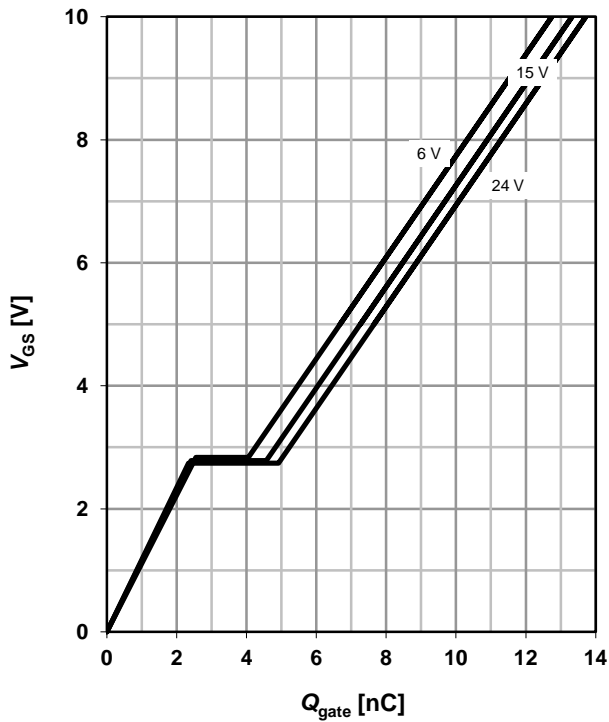
parameter:  $T_{j(start)}$



**25 Typ. gate charge (Q1)**

$V_{GS}=f(Q_{gate}); I_D=20\text{ A pulsed}$

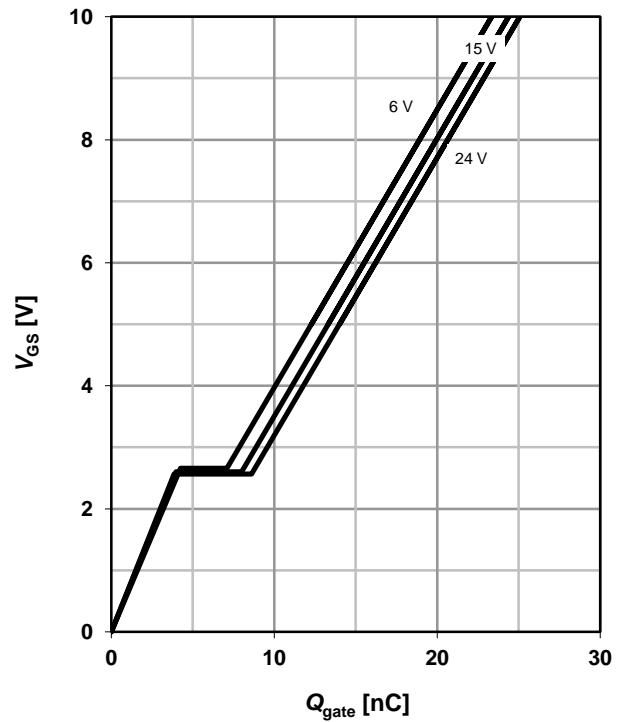
parameter:  $V_{DD}$



**26 Typ. gate charge (Q2)**

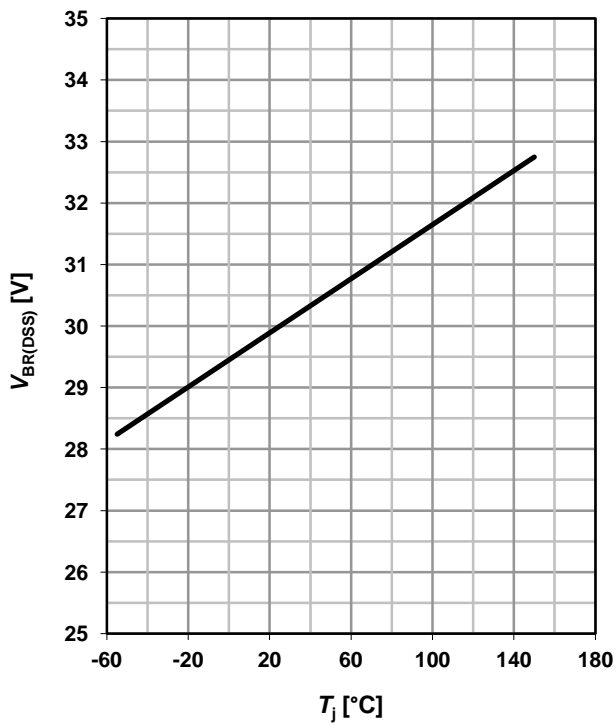
$V_{GS}=f(Q_{gate}); I_D=20\text{ A pulsed}$

parameter:  $V_{DD}$



**27 Drain-source breakdown voltage (Q1)**

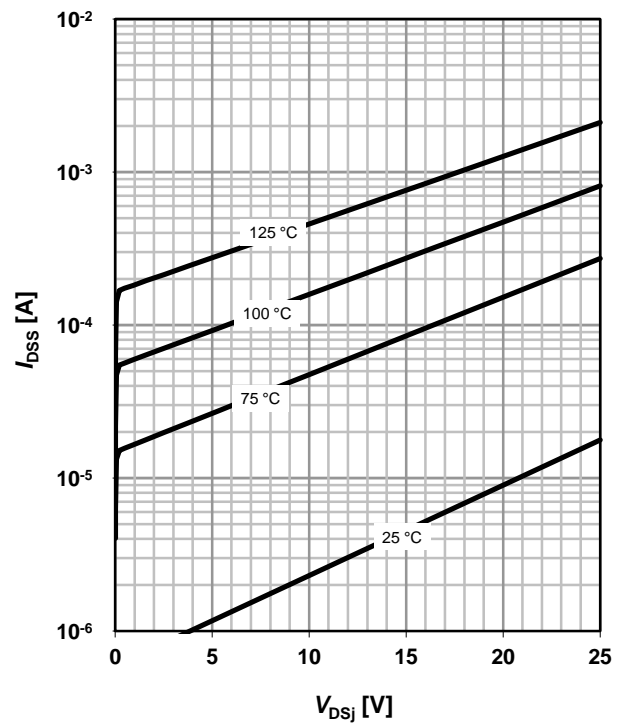
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$



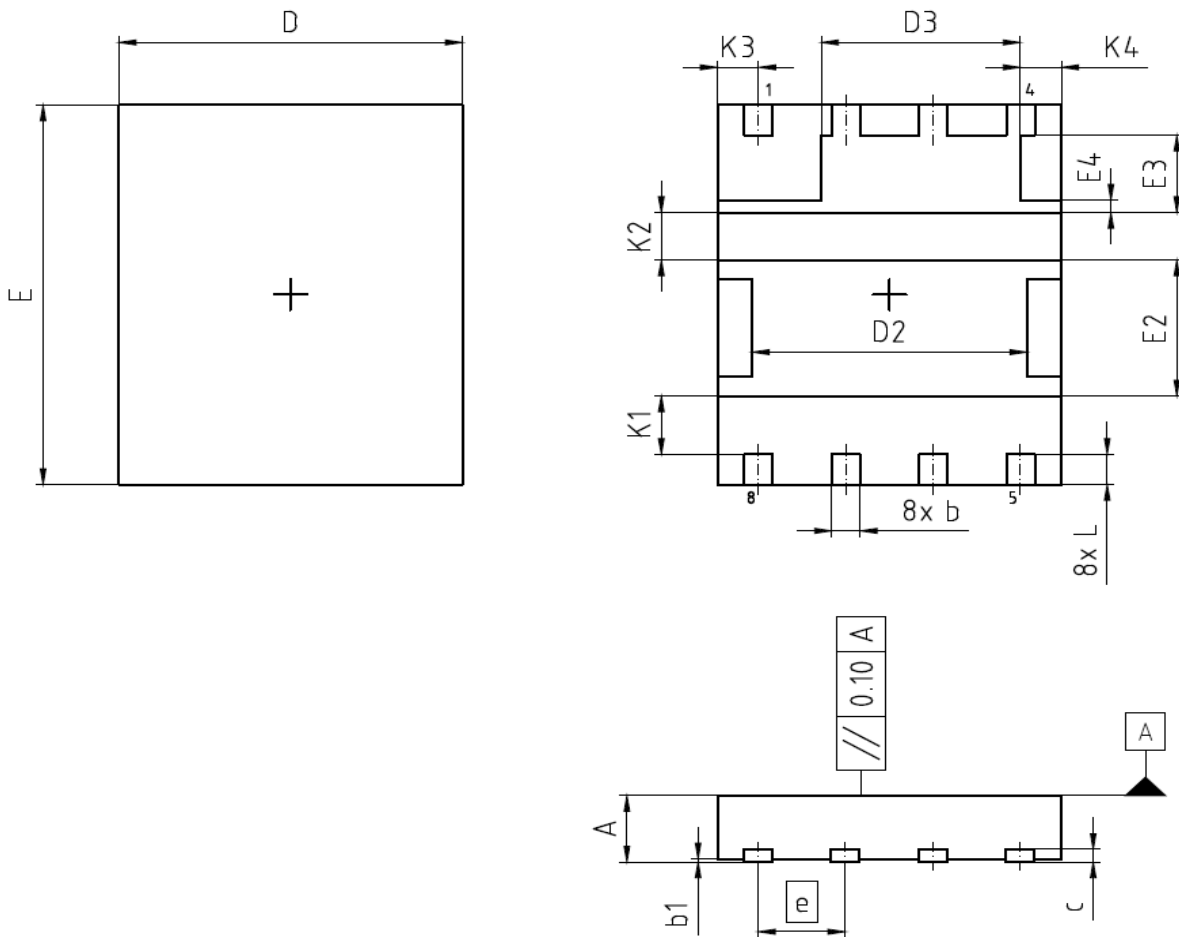
**28 Typ. drain-source leakage current (Q2)**

$I_{DSS}=f(V_{DS}); V_{GS}=0\text{ V}$

parameter:  $T_j$



PG-TISON



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.15	0.035	0.045
b	0.31	0.51	0.012	0.020
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	4.90	5.10	0.193	0.201
D2	3.90	4.10	0.154	0.161
D3	2.80	3.00	0.110	0.118
E	5.90	6.10	0.232	0.240
E2	2.05	2.25	0.081	0.089
E3	1.12	1.32	0.044	0.052
E4	0.10	0.30	0.004	0.012
e	1.27 (BSC)		0.05 (BSC)	
N	8		8	
L	0.38	0.58	0.015	0.023
K1	0.82	1.02	0.032	0.040
K2	0.65	0.85	0.026	0.033
K3 = K4	0.50	0.70	0.019	0.027

**DOCUMENT NO.**  
Z8B00162738

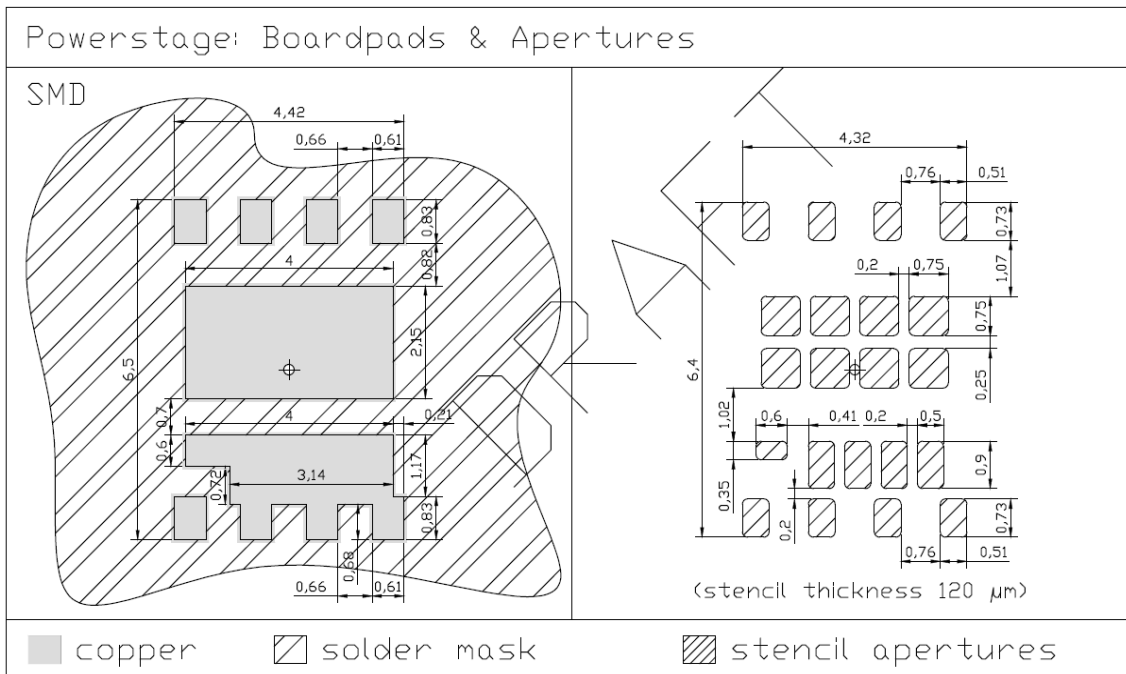
**SCALE**

**EUROPEAN PROJECTION**

**ISSUE DATE**  
21-09-2011

**REVISION**  
01

PG-TISON



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**  
**© 2012 Infineon Technologies AG**  
**All Rights Reserved.**

**Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

**Information**



For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

**Warnings**







Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View BSC0923NDI on WIN SOURCE](#)
-  [Infineon Technologies Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management