THE DATASHEET OF

AOZ5537QI

AOZ5537QI

50A Continuous Current DrMOS Power Module

General Description

The AOZ5537QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss. The compact 5mm x 5mm QFN package is optimally chosen and designed to minimize parasitic inductance for minimal EMI signature.

The AOZ5537QI is intended for use with TTL and Tri-state compatibility by using both the PWM and/or FCCM inputs for accurate control of the power MOSFET switching activities.

A number of features are provided making the AOZ5537QI a highly versatile power module: The bootstrap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pin-out is optimized for low parasitics, keeping their effects to a minimum.

Features

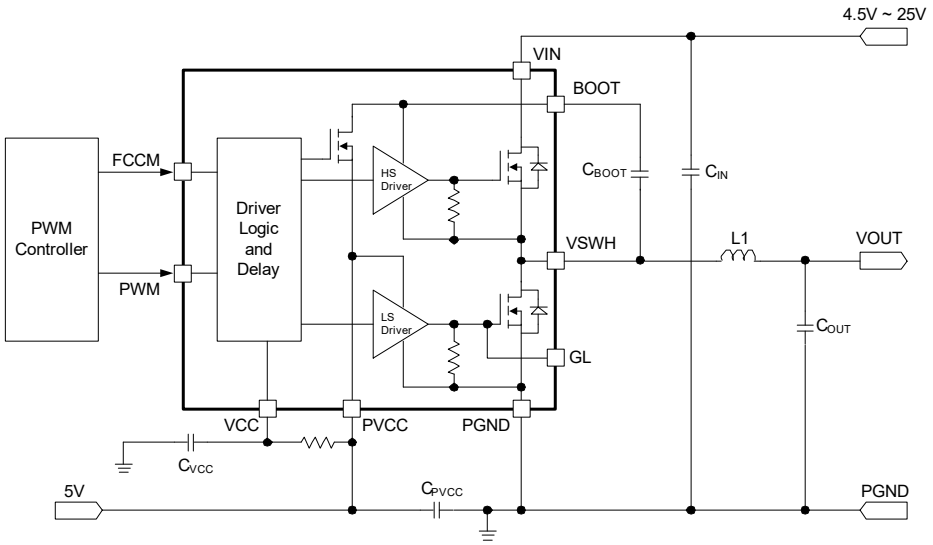
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 50A continuous output current
  - Up to 80A for 10ms on pulse
  - Up to 120A for 10us on pulse
- Integrated bootstrap schottky switch
- Up to 2MHz switching operation
- Tri-state PWM input compatible
- Under-Voltage lockout protection
- Single FCCM pin control for Shutdown / Diode Emulation / CCM operation
- Small 5mm x 5mm QFN-31L package

Applications

- Servers
- Notebook computers
- VRMs for motherboards
- Point of load DC/DC converters
- Memory and graphic cards
- Video gaming console

Green Product

Typical Application Circuit

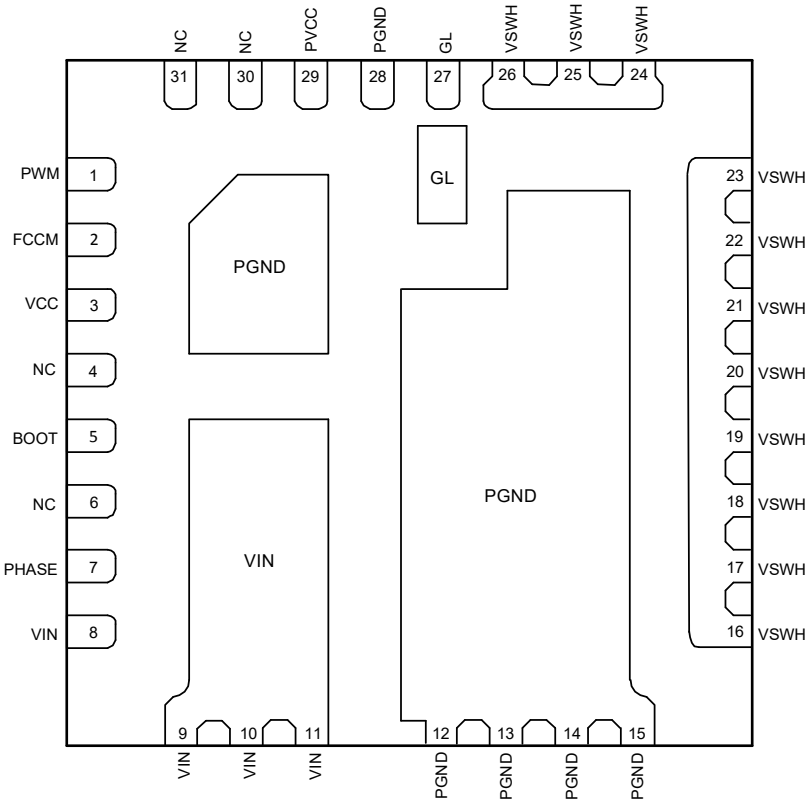


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5537QI	-40°C to 125°C	QFN5x5-31L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

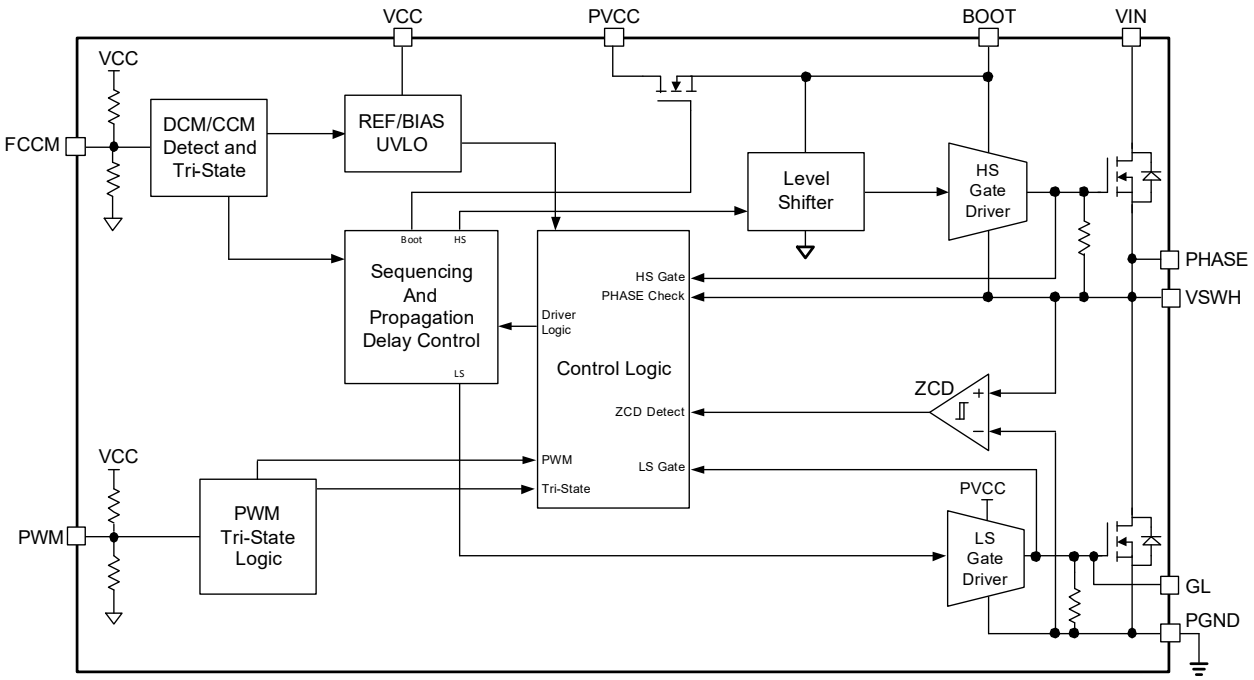


QFN5x5_31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic level Low Side.
2	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. High impedance on the input of FCCM will shutdown both High-Side and Low-Side MOSFETs.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1uF MLCC capacitor directly between VCC and PGND.
4	NC	Internally connected to PGND paddle. It can be left floating (No connect) or tied to PGND.
5	BOOT	High side MOSFET gate driver supply rail. Connect a 100nF ceramic capacitor between BOOT and PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (No connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection to BOOT (Pin 5).
8, 9, 10, 11	VIN	High voltage input for power stage (Drain Connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power ground for power stage (Source Connection of Low-Side MOSFET).
16,17,18,19, 20,21,22, 23, 24, 25, 26	VSWH	Switching node connected to the source of High-Side MOSFET and the drain of low side MOSFET. These pins are being used for zero cross detect, Anti-Overlap Control, as well as main inductor terminal.
27	GL	Low Side MOSFET Gate connection. This is for test purposes.
28	PGND	Power ground for High-Side and Low-Side MOSFET gate drivers. Ensure to position a 1uF MLCC directly between PVCC (Pin 29) to PGND.
29	PVCC	5V power rail for High-Side and Low-Side MOSFET gate drivers. Ensure to position a 1uF MLCC directly between PVCC to PGND (Pin 28).
30,31	NC	No Connect.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 33V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 38V
Low Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low Side Gate Voltage Transient(2) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	50A
VSWH Current 10ms on pulse	80A
VSWH Current 10us on pulse	120A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage/ MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics[4]

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature. VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{VIN}	Power Stage Power Supply		4.5		25	V
V_{PVCC}	Driver Power Supply		4.5		5.5	V
$R_{\theta JC}$[5]	Thermal Resistance	PCB Temp = 100°C		2.5		°C/W
$R_{\theta JA}$[5]		AOS Demo Board		13.8		°C/W
INPUT SUPPLY AND UVLO						
V_{VCC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
		VCC Hysteresis		400		mV
I_{VCC_SD}	Shutdown Bias Supply Current	FCCM = Floating PWM = Floating		3		µA
I_{PVCC}	Control Circuit Bias Current	FCCM = 5V PWM = Floating		170		µA
		FCCM = 0V PWM = Floating		180		µA
PWM INPUT						
V_{PWMH}	Logic High Input Voltage		4.1			V
V_{PWML}	Logic Low Input Voltage				0.7	V
I_{PWM}	PWM Pin Input Current	PWM = 5V		+200		µA
		PWM = 0V		-200		µA
V_{TRI}	PWM Input Tri-State Threshold Window	PWM = Floating	1.5		3.3	V
FCCM INPUT						
V_{FCCMH}	Logic High Input Voltage		3.9			V
V_{FCCML}	Logic Low Input Voltage				1.2	V
I_{FCCM}	FCCM Pin Input Current	FCCM = 5V		+50		µA
		FCCM = 0V		-50		µA
t_{PS4_EXIT}	PS4 Exit Latency	PVCC = 5V		5	15	µs
GATE DRIVER TIMING						
t_{PDLU}	PWM to High-Side Gate	PWM: H⟶L, VSWH: H⟶L		30		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L⟶H, GL: H⟶L		25		ns
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H⟶L, GH[6]: L⟶H		15		ns
t_{PDHL}	High-Side to Low-side Gate Deadtime	GH[6]: H⟶1V, GL: L⟶H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L ⟶V_{TRI}, GL: H⟶L and PWM: H⟶V_{TRI}. VSWH: H⟶L		150		ns
t_{PTS}	Tri-State Propagation Delay	PWM: V_{TRI}⟶4.1V, VSWH: L⟶H and PWM: V_{TRI}⟶<0.7V, GL: L⟶ H		45		ns
t_{LGMIN}	Low-Side Minimum On-Time	FCCM = 0V, DCM mode		350		ns

Note:

4. All voltages are specified with respect to the corresponding PGND pin.
5. Characterization value. Not tested in production.
6. GH is the internal gate pin of the high-side MOSFET.

Timing Diagram

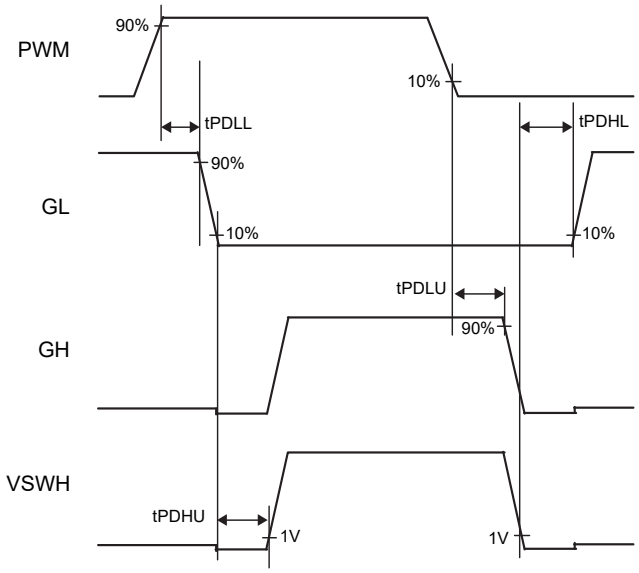


Figure 1. PWM Logic Input Timing Diagram

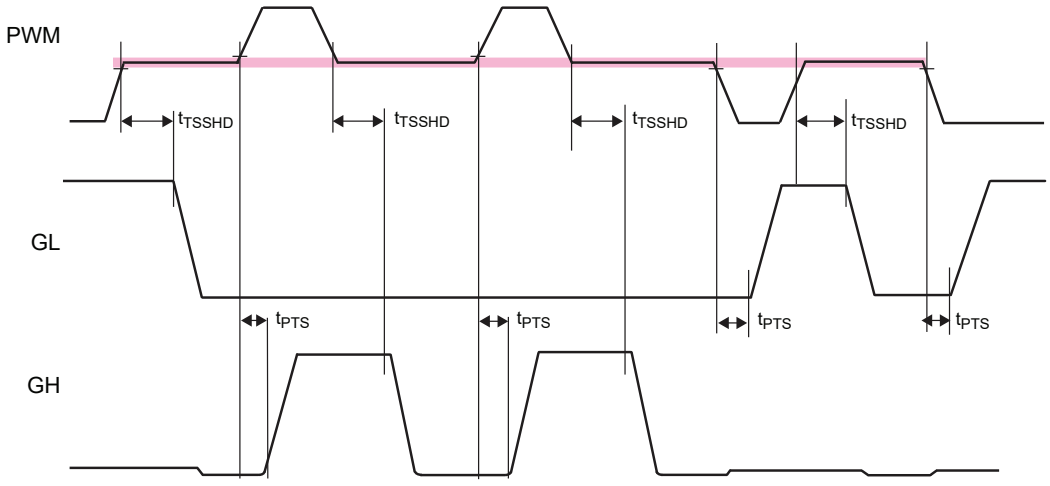


Figure 2. Tri-State Input Logic Timing Diagram

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

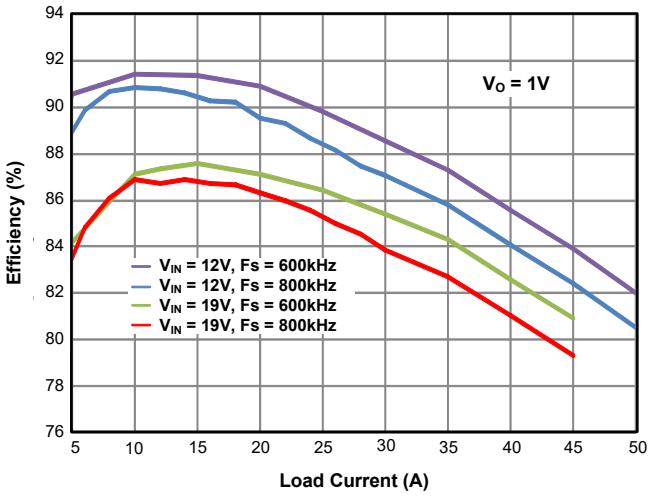


Figure 3. Efficiency vs. Load Current

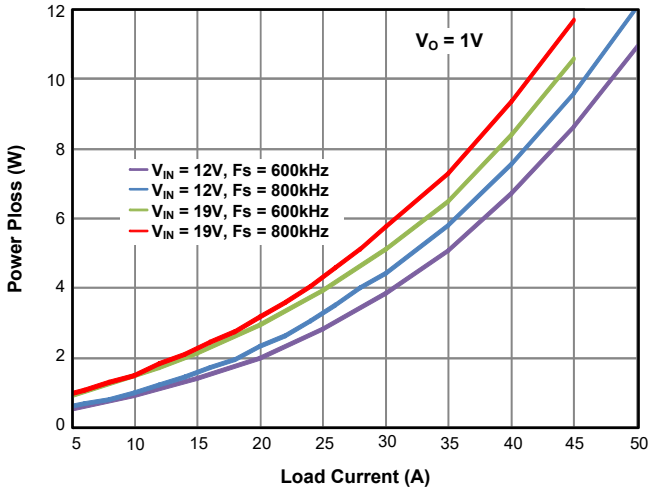


Figure 4. Power Loss vs. Load Current

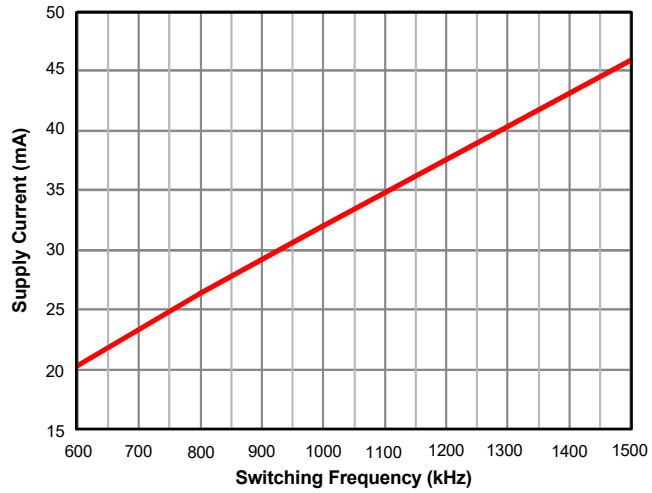


Figure 5. Supply Current vs. Switching Frequency

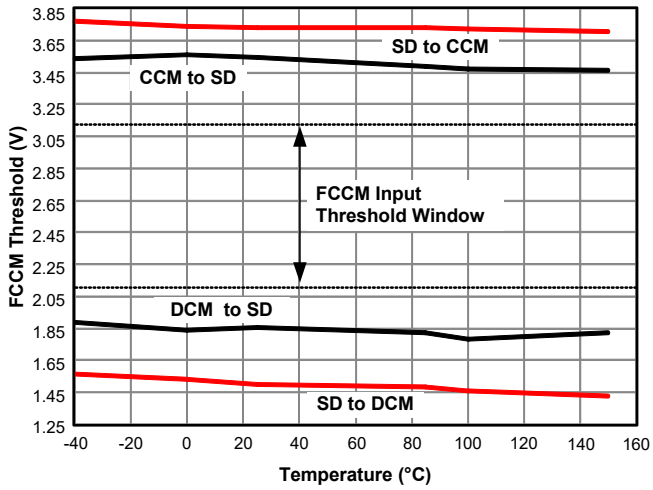


Figure 6. FCCM Input Threshold vs. Temperature

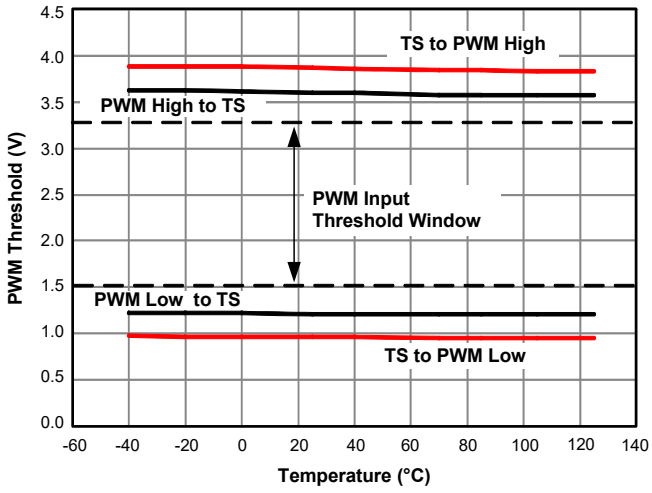


Figure 7. PWM Threshold vs. Temperature

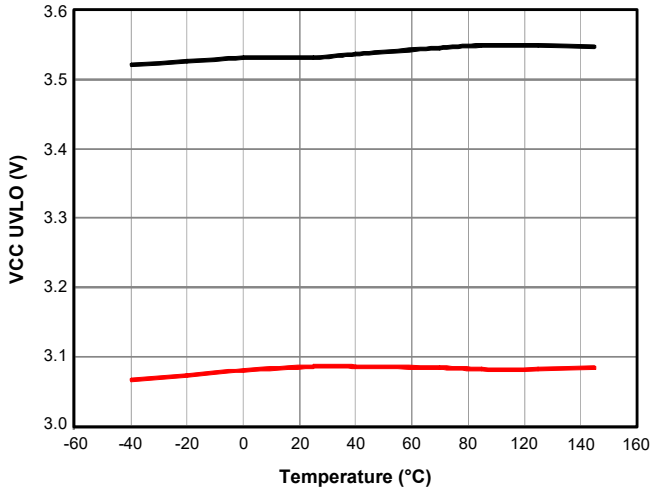


Figure 8. VCC UVLO vs. Temperature

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

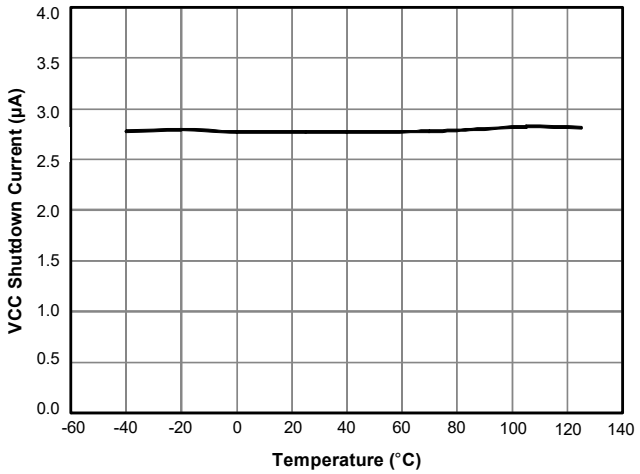


Figure 9. VCC Shutdown Current vs. Temperature

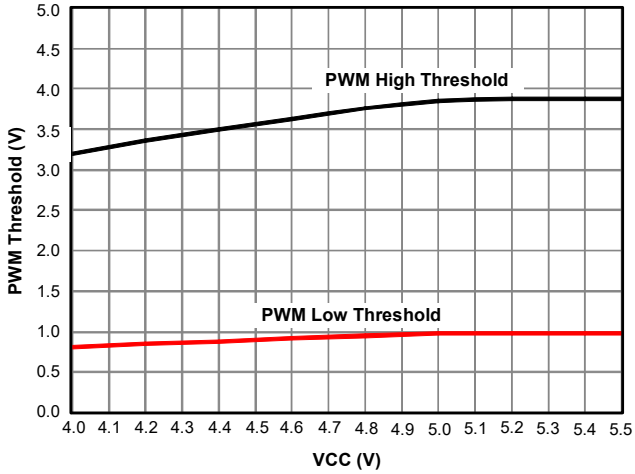


Figure 10. PWM Threshold vs. VCC

Application Information

AOZ5537QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuits. A number of desirable features make AOZ5537QI a highly versatile power module. The MOSFETs are individually optimized for efficient operation on either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also integrated in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification IMVP8(VRM13) in form fit and function.

Powering the Module and the Gate Drives

An external supply PVCC of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying large peak current into the Low Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 4.7µF or higher is recommended from PVCC to PGND. For effective filtering it is strongly recommended to directly connect this capacitor to PGND (Pin 28).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node PHASE. It is recommended that this capacitor Cboot be connected as close as possible to the device across Pin 5 and Pin 7. Boost switch is integrated into the package. A resistor Rboot in series with Cboot can be optionally used by designers to slow down the turn on speed of the High-Side MOSFET. Typically values of Rboot between 1Ω to 5Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Under-Voltage Lockout

In a UVLO event, both GH and GL outputs are actively held low until adequate gate supply becomes available. The under-voltage lockout is set to 3.5V with a 400mV hysteresis. The AOZ5537QI must be powered up before the PWM input is applied.

Since the PWM control signals are provided typically from an external controller or a digital processor, extra care must be taken during start up. It should be ensured that PWM signal goes through a proper soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. In general it should be noted that AOZ5537QI is a combination of two MOSFETs with an IMVP8 compliant driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal protection, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5537QI is rated to operate over a wide input range of 4.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality surface mount ceramic capacitors.

The High-Side MOSFET in AOZ5537QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN, the duty ratio will be higher and conduction losses in the High-Side MOSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the High-Side MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the High-Side MOSFET may be much hotter than the Low-Side MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5537QI is offered in two versions which can be interfaced with PWM logic compatible with either 5V (TTL). Refer to Figure 1 for the timing and propagation delays between the PWM input and the gate drives.

The PWM is also a tri-state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table in Table 1 lists the thresholds for high and low level transitions as well as tri-state operation. As shown in Figure 2, there is a hold off delay between the corresponding gate drive is pulled low. This delay is intended to prevent spurious triggering of the tri-state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Table 1. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5537QI	4.1 V	0.7 V	1.5 V	3.3 V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low Side MOSFET (FCCM)

AOZ5537QI can be operated in the diode emulation or skip mode using the FCCM pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If FCCM is logic high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. If the pin is logic low, the High-Side MOSFET drive is not affected but diode emulation mode is activated for the Low-Side MOSFET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions. A high impedance state at the FCCM pin shuts down the AOZ5537QI.

Table 2. Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	L
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Note: Diode emulation mode is activated when FCCM pin is held low.

Gate Drives

AOZ5537QI has an internal high current high speed driver that generates the floating gate drive for the High-Side MOSFET and a complementary drive for the Low-Side MOSFET.

Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from High to Low or Low to High, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pin GL is brought out on Pin 27 for diagnostic purpose. However this connection is not made directly to MOSFET gate pad and its voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connection is primarily for functional tests during manufacturing and no connection should be made to it in the applications.

PCB Layout Guidelines

AOZ5537QI is a high current module rated for operation up to 2MHz. This requires extremely fast switching speed to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the High-Side MOSFET, Low-Side MOSFET and the input bypass capacitor Cin. The PCB design is simplified because of the optimized pin out in AOZ5537QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by Low-Side MOSFET, output inductor and output capacitor Cout is the next critical parameter. This requires second layer or “Inner 1” should always be an uninterrupted ground plane with sufficient VIAs placed as close as possible to by-pass capacitors soldering pads.

As shown in Figure 11, the top most layer of the PCB should comprise of uninterrupted copper flooding for the primary AC current loop which runs along the VIN copper plane originating from the bypass capacitors C10, C11 and C12 which are mounted to a large PGND copper plane, also on the top most layer of the PCB. These copper planes also serve as heat dissipating elements as heat flows down to the VIN exposed pad and onto the top layer VIN copper plane which fans out to a wider area moving away from the 5x5 QFN package. Adding VIAs will only help transfer heat to cooler regions of the PCB

board through the other 3 layers (if 4 layer PCB is used) beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

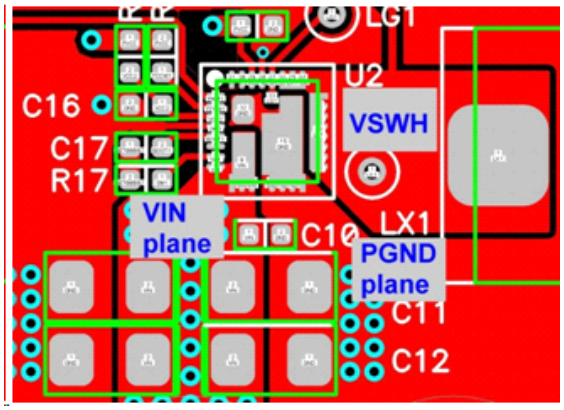


Figure 11. Top Layer of Demo Board, VIN, VSWH and PGND Copper Planes

Due to the optimized bonding technique used on the AOZ5537QI internal package, the VIN input capacitors are optimally placed for AC current activities on both the primary and complimentary current loops. The return path of the current during the complimentary period flows through a non interrupted PGND copper plane that is symmetrically proportional to the VIN copper plane.

Due to the PGND exposed pad, heat is optimally dissipated by flowing down through the vertically structured lower MOSFET, through the exposed PGND pad and down to the PCB top layer PGND copper plane that also fans outward, moving away from the package. The bottom layer of PBC layout is shown in Figure 12.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt produced through parastics inside package. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to and sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

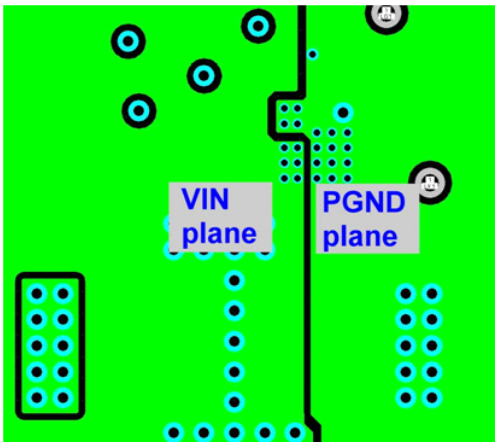
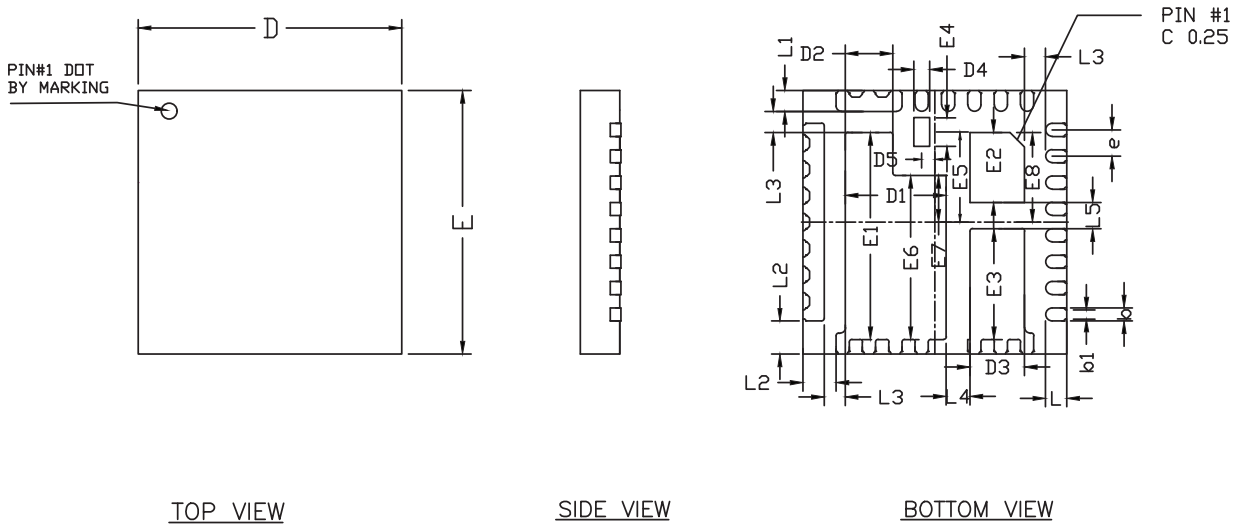
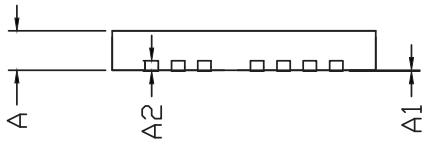


Figure 12. Bottom Layer PCB layout, VSWH Copper Plane Voided on Descending Layers

Package Dimensions, QFN5x5A-31L, EP3_S

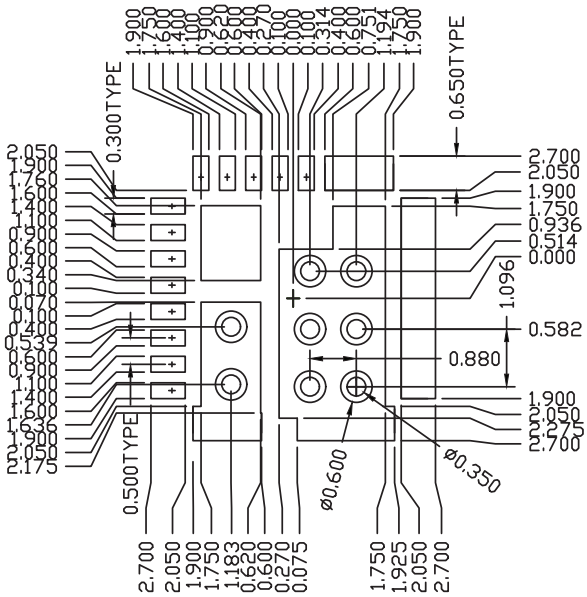


TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



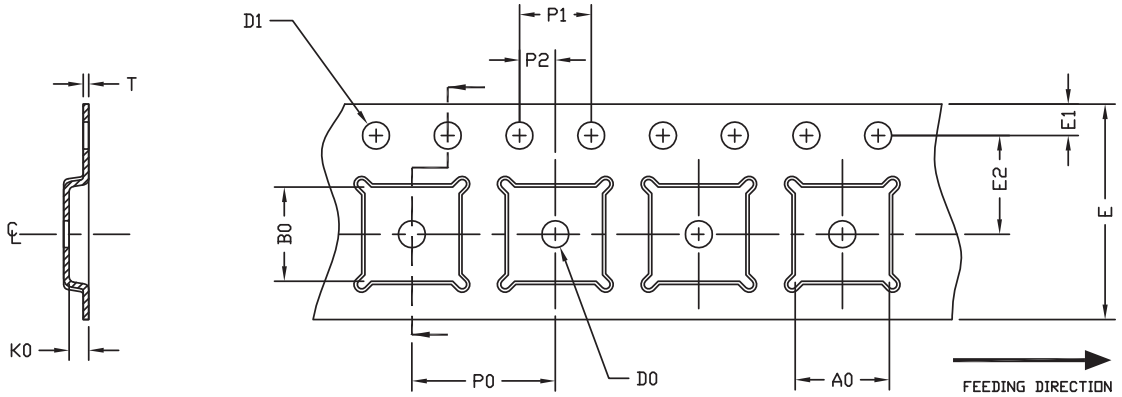
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2		0.2REF			0.008REF	
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
E6	3.061	3.111	3.161	0.121	0.122	0.124
E7	0.836	0.886	0.936	0.033	0.035	0.037
E8	1.650	1.700	1.750	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e		0.50BSC			0.02BSC	

UNIT: mm

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x5A-31L, EP3_S

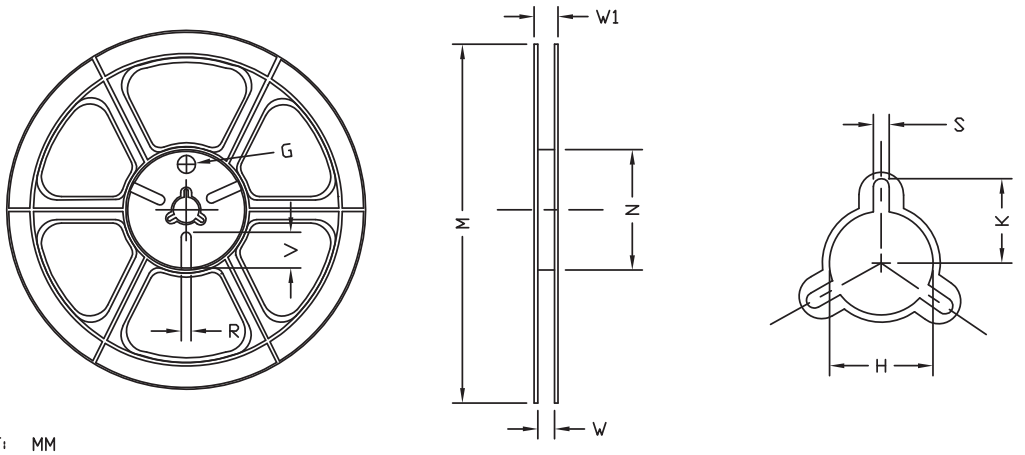
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

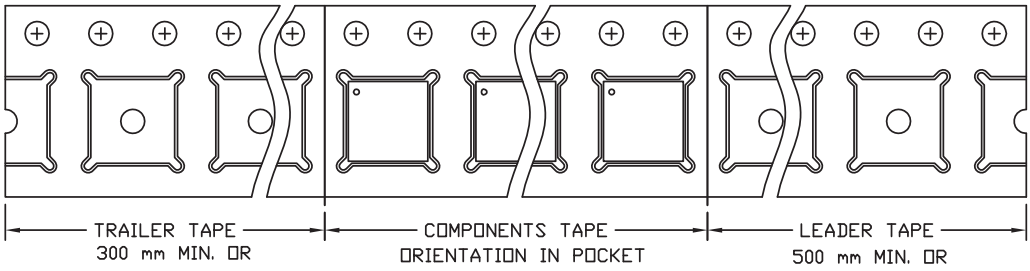


UNIT: MM

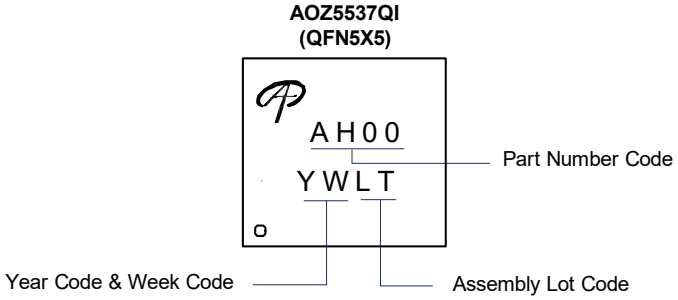
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

Leader/Trailer & Orientation

Unit Per Reel: 3000pcs



Part Marking



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