



# THE DATASHEET OF BSP250,135



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# DATA SHEET

## **BSP250**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
Supersedes data of November 1994  
File under Discrete Semiconductors, SC13b

1997 Jun 20

# P-channel enhancement mode vertical D-MOS transistor

**BSP250**

**FEATURES**

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

**APPLICATIONS**

- Low-loss motor and actuator drivers
- Power switching.

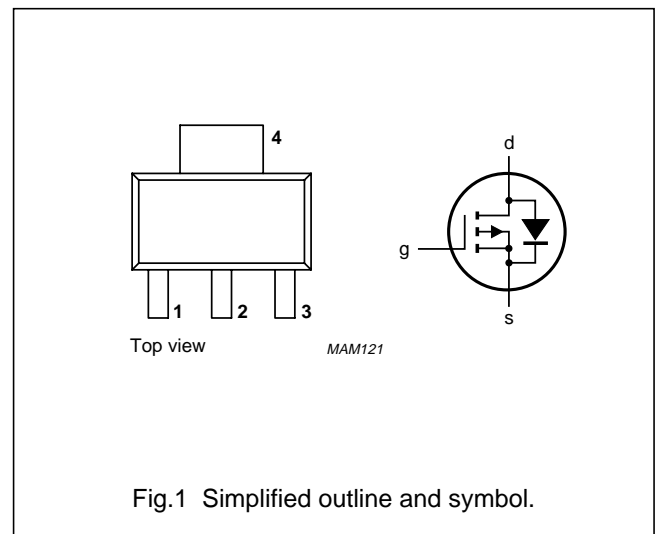
**DESCRIPTION**

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

<b>CAUTION</b>
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

**PINNING - SOT223**

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	–30	V
$V_{SD}$	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.6	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
$I_D$	drain current (DC)		–	–3	A
$R_{DSon}$	drain-source on-state resistance	$I_D = -1$ A; $V_{GS} = -10$ V	–	0.25	$\Omega$
$P_{tot}$	total power dissipation	$T_s = 100$ °C	–	5	W

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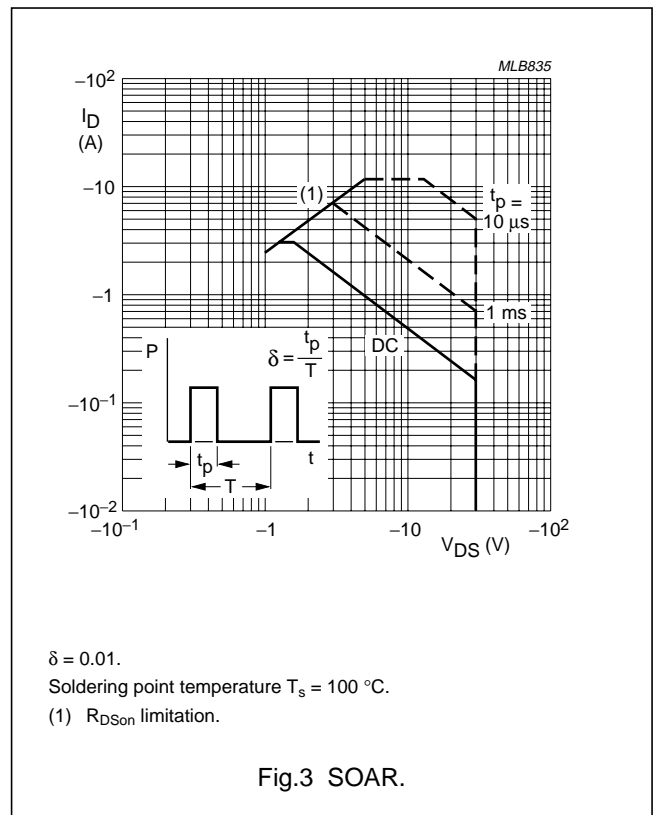
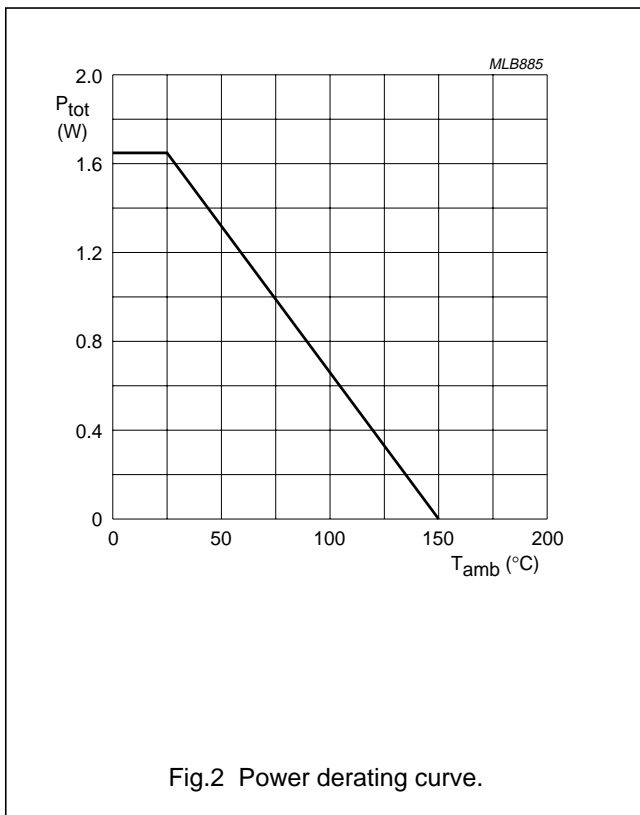
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage (DC)		–	–30	V
V <sub>GSO</sub>	gate-source voltage (DC)	open drain	–	±20	V
I <sub>D</sub>	drain current (DC)	T <sub>s</sub> ≤ 100 °C	–	–3	A
I <sub>DM</sub>	peak drain current	note 1	–	–12	A
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> = 100 °C	–	5	W
		T <sub>amb</sub> = 25 °C; note 2	–	1.65	W
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	operating junction temperature		–	150	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current (DC)	T <sub>s</sub> ≤ 100 °C	–	–1.5	A
I <sub>SM</sub>	peak pulsed source current	note 1	–	–6	A

**Notes**

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm<sup>2</sup>.



# P-channel enhancement mode vertical D-MOS transistor

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		10	K/W

### Note

1. Device mounted on an epoxy printed-circuit board,  $40 \times 40 \times 1.5$  mm; mounting pad for drain lead minimum  $6\text{ cm}^2$ .

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-1	-	-2.8	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24\ \text{V}$	-	-	-100	nA
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	-	-	$\pm 100$	nA
$I_{Don}$	on-state drain current	$V_{GS} = -10\ \text{V}; V_{DS} = -1\ \text{V}$	-3	-	-	A
		$V_{GS} = -4.5\ \text{V}; V_{DS} = -5\ \text{V}$	-1	-	-	A
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}; I_D = -0.5\ \text{A}$	-	0.33	0.4	$\Omega$
		$V_{GS} = -10\ \text{V}; I_D = -1\ \text{A}$	-	0.22	0.25	$\Omega$
$ y_{fs} $	forward transfer admittance	$V_{DS} = -20\ \text{V}; I_D = -1\ \text{A}$	1	2	-	S
$C_{iss}$	input capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	250	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	140	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	50	-	pF
$Q_G$	total gate charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	10	25	nC
$Q_{GS}$	gate-source charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	1	-	nC
$Q_{GD}$	gate-drain charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	3	-	nC

### Switching times

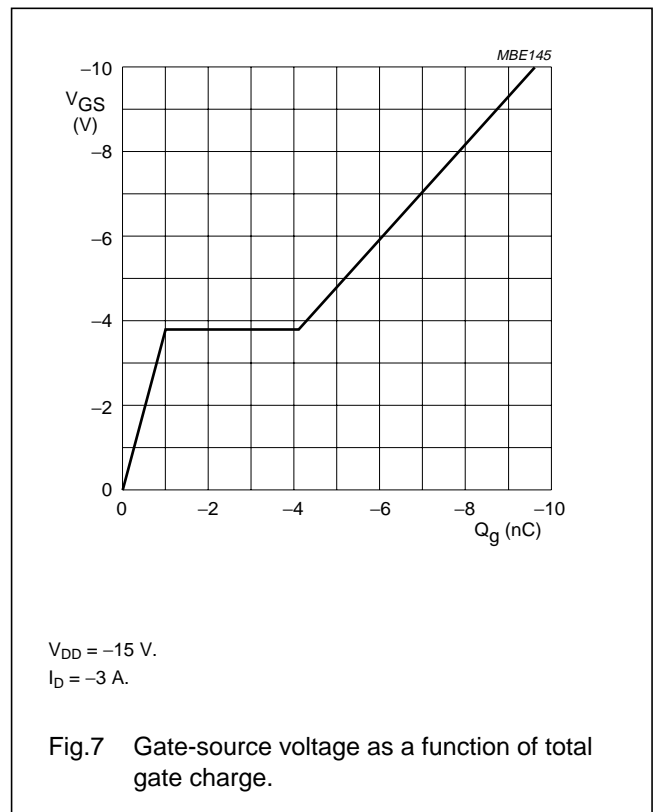
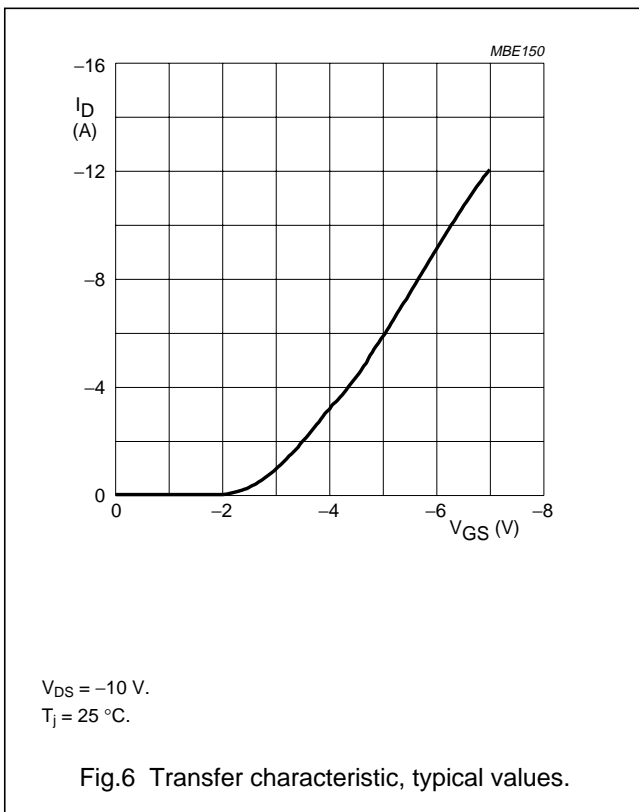
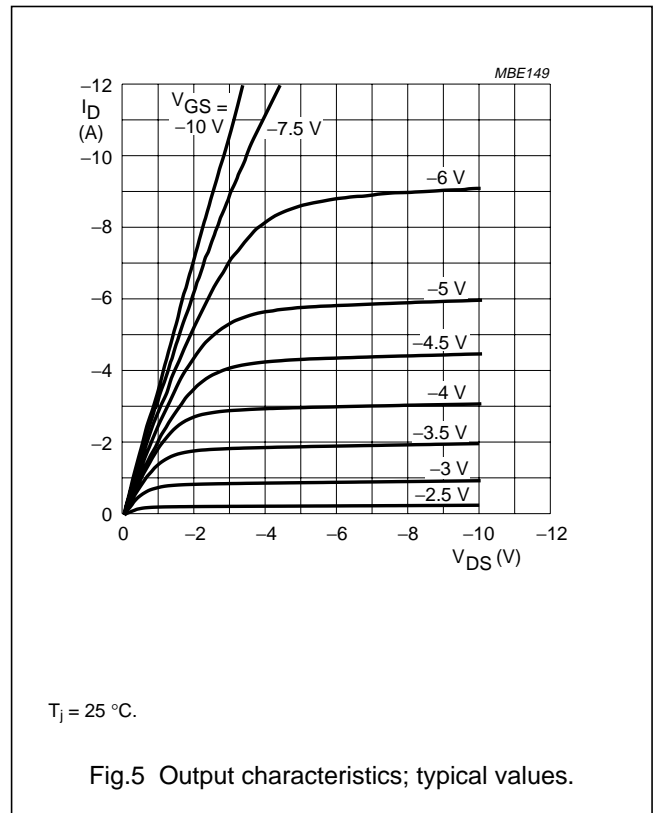
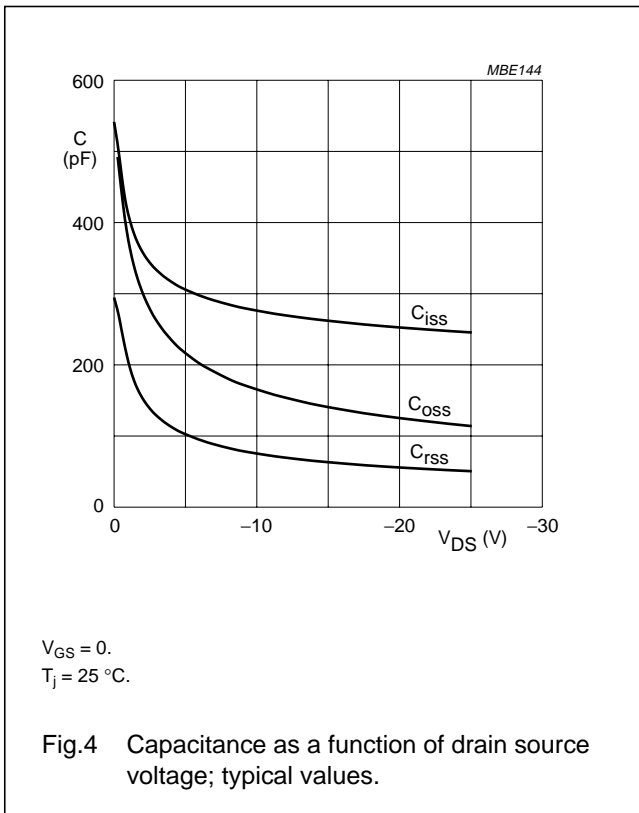
$t_{on}$	turn-on time	$V_{GS} = 0\ \text{to}\ -10\ \text{V}; V_{DD} = -20\ \text{V};$ $I_D = -1\ \text{A}; R_L = 20\ \Omega$	-	20	80	ns
$t_{off}$	turn-off time	$V_{GS} = -10\ \text{to}\ 0\ \text{V}; V_{DD} = -20\ \text{V};$ $I_D = -1\ \text{A}; R_L = 20\ \Omega$	-	50	140	ns

### Source-drain diode

$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = -1.25\ \text{A}$	-	-	-1.6	V
$t_{rr}$	reverse recovery time	$I_S = -1.25\ \text{A}; di/dt = 100\ \text{A}/\mu\text{s}$	-	150	200	ns

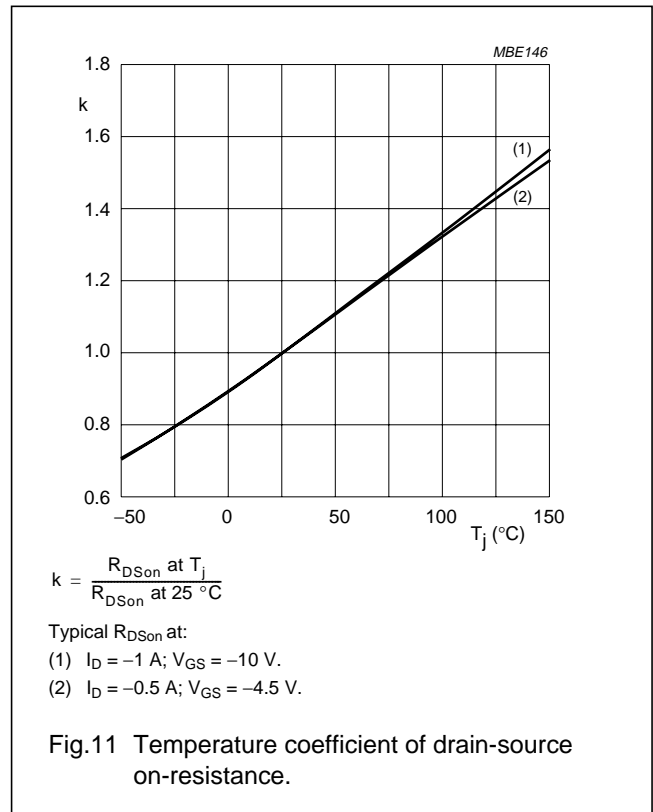
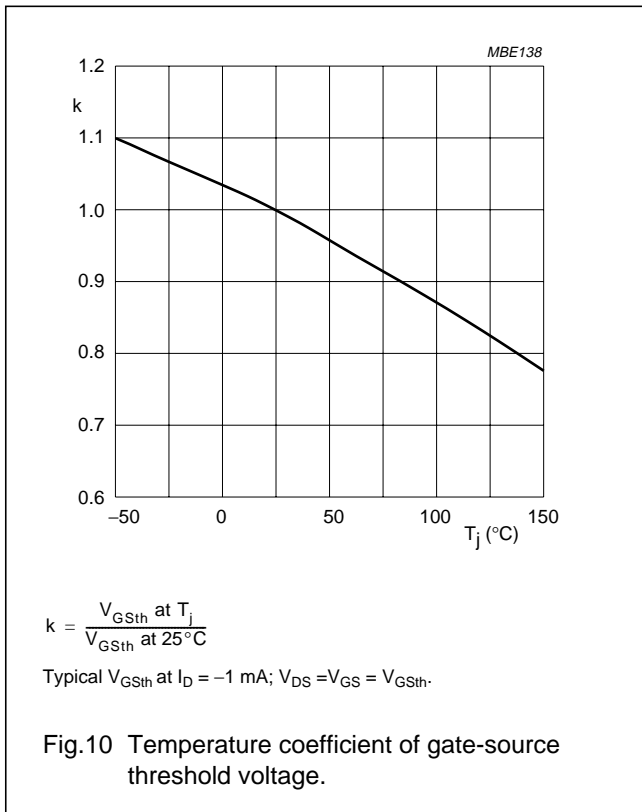
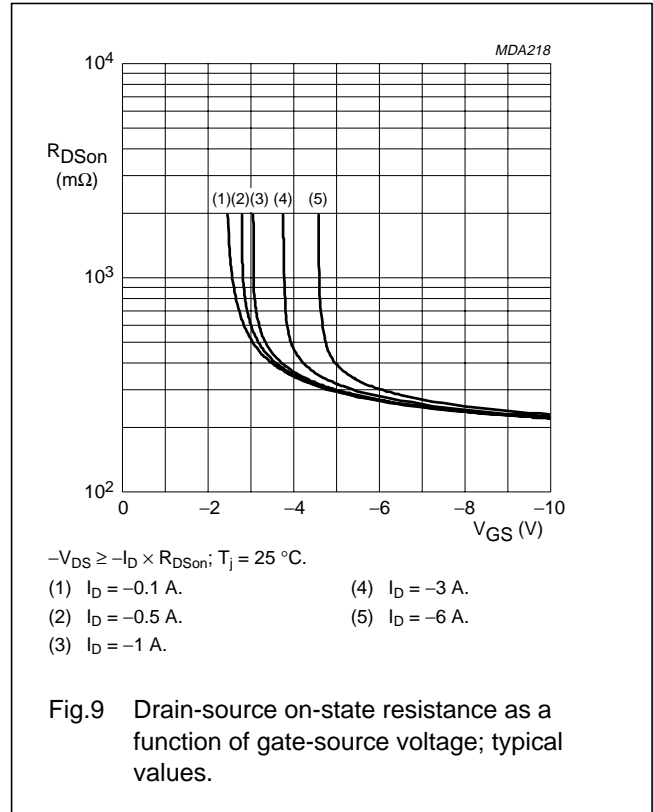
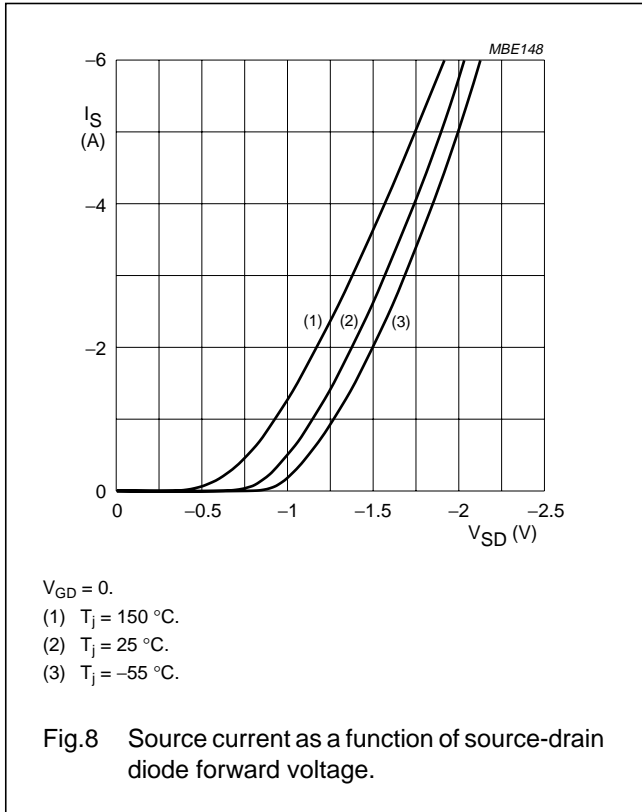
P-channel enhancement mode vertical D-MOS transistor

BSP250



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P-channel enhancement mode  
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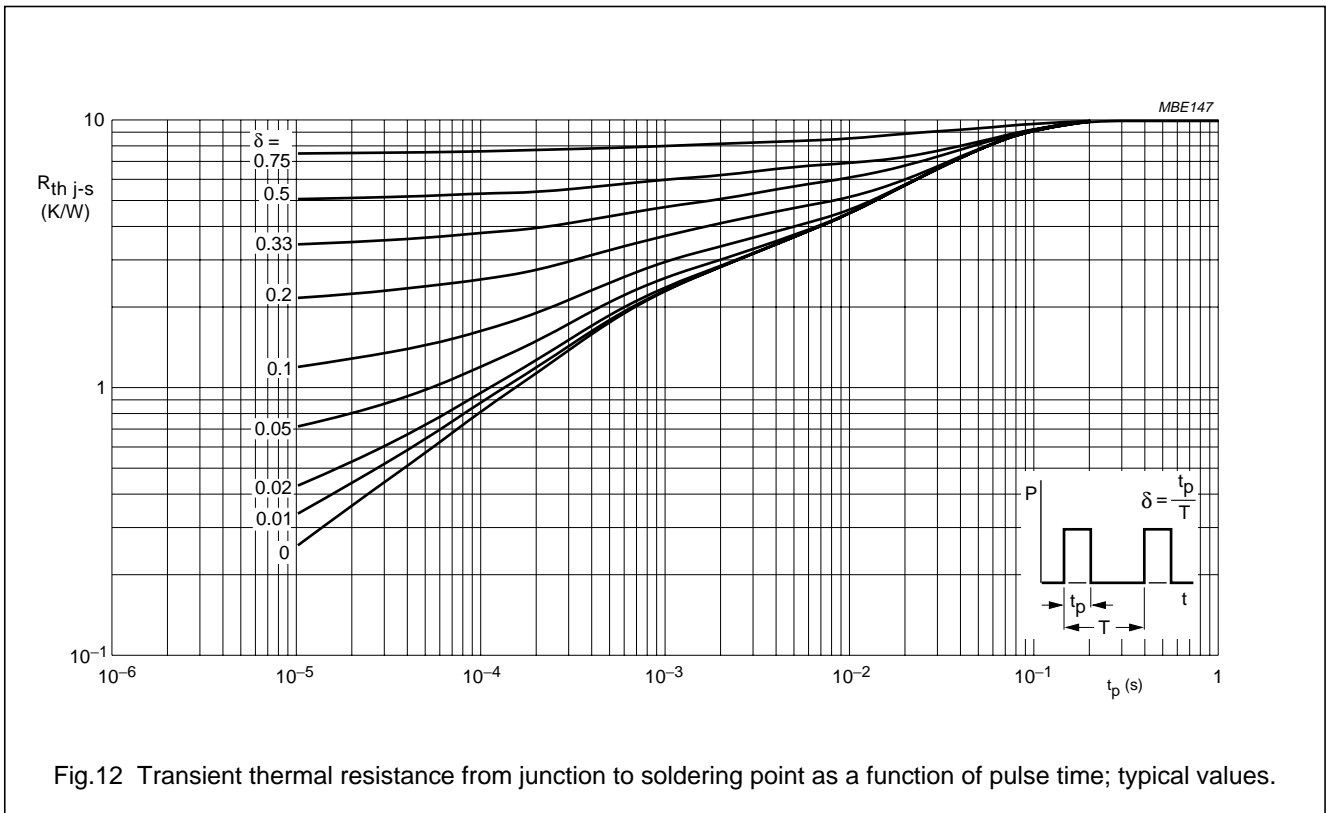


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

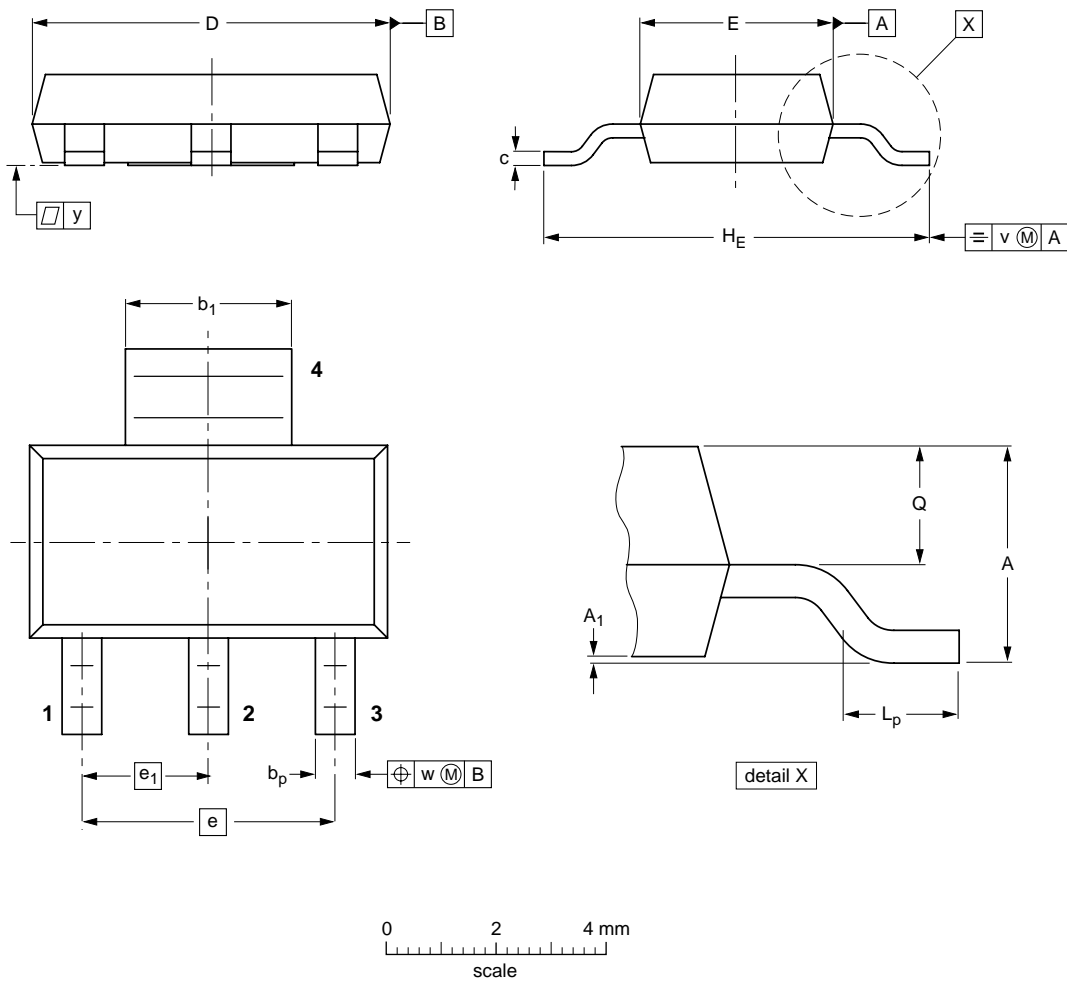
P-channel enhancement mode  
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

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**BSP250****DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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**NOTES**

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**NOTES**

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