



**THE DATASHEET OF  
BSZ076N06NS3GATMA1**



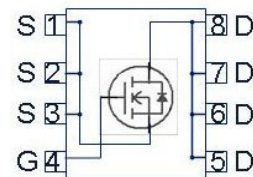
**OptiMOS™3 Power-Transistor**
**Features**

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21

**Product Summary**

$V_{DS}$	60	V
$R_{DS(on),max}$	7.6	mΩ
$I_D$	20	A

<b>Type</b>	BSZ076N06NS3 G
<b>Package</b>	PG-TSDSON-8
<b>Marking</b>	076N06N


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}^{2)}$	20	A
		$V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$	20	
		$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=50\text{K/W J41}^{3)}$	14	
Pulsed drain current <sup>4)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	80	
Avalanche energy, single pulse <sup>5)</sup>	$E_{AS}$	$I_D=20\text{ A}$ , $R_{GS}=25\text{ Ω}$	118	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Current is limited by bondwire; with an  $R_{thJC}=1.8\text{ K/W}$  the chip is able to carry 75A.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup> See figure 3 for more detailed information

<sup>5)</sup> See figure 13 for more detailed information

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	69	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=60\text{ K/W}^{3)}$	2.1	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	1.8	K/W
Device on PCB	$R_{\text{thJA}}$	minimal footprint	-	-	-	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	60	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	60	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=35\text{ }\mu\text{A}$	2	3	4	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=60\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=60\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=20\text{ A}$	-	6.1	7.6	m $\Omega$
Gate resistance	$R_{\text{G}}$		-	1	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=20\text{ A}$	20	39	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V},$ $f=1\text{ MHz}$	-	3000	4000	pF
Output capacitance	$C_{oss}$		-	660	880	
Reverse transfer capacitance	$C_{rss}$		-	24	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=3.5\ \Omega$	-	15	-	ns
Rise time	$t_r$		-	40	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	$t_f$		-	5	-	

**Gate Charge Characteristics<sup>6)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	15	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	9	-	
Gate to drain charge	$Q_{gd}$		-	3	-	
Switching charge	$Q_{sw}$		-	9	-	
Gate charge total	$Q_g$		-	37	50	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V
Output charge	$Q_{oss}$	$V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$	-	30	40	

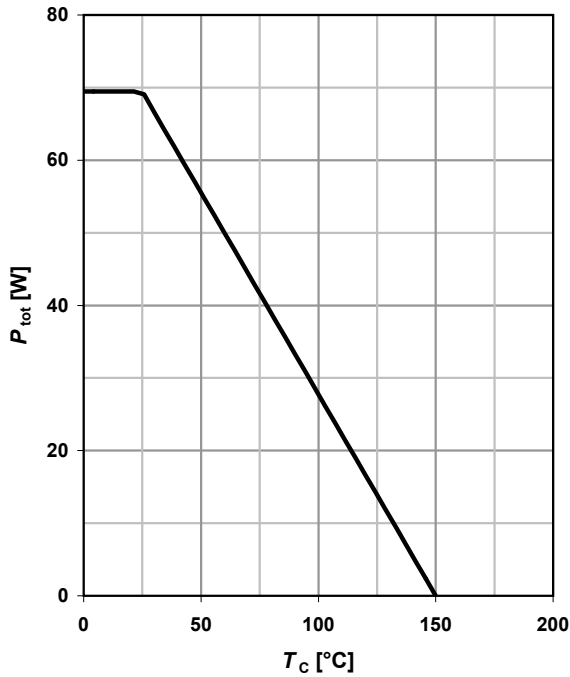
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	20	A
Diode pulse current	$I_{S,pulse}$		-	-	80	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.85	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=30\text{ V}, I_F=20\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	36	-	ns
Reverse recovery charge	$Q_{rr}$		-	32	-	nC

<sup>6)</sup> See figure 16 for gate charge parameter definition

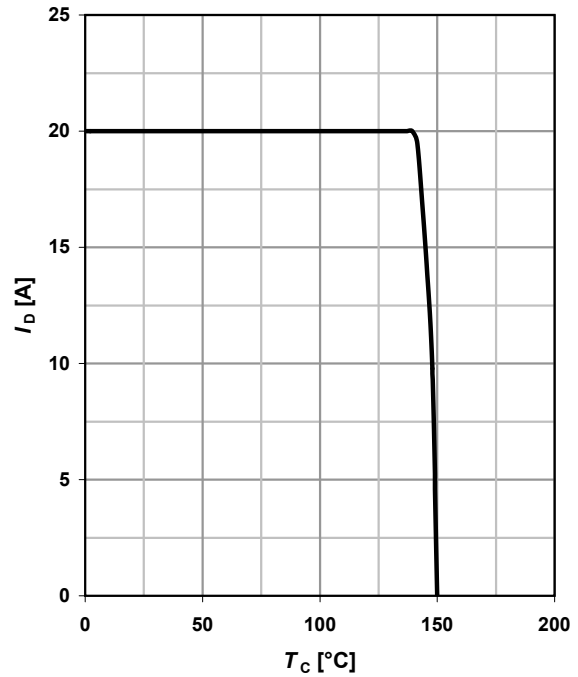
**1 Power dissipation**

$$P_{tot} = f(T_c)$$



**2 Drain current**

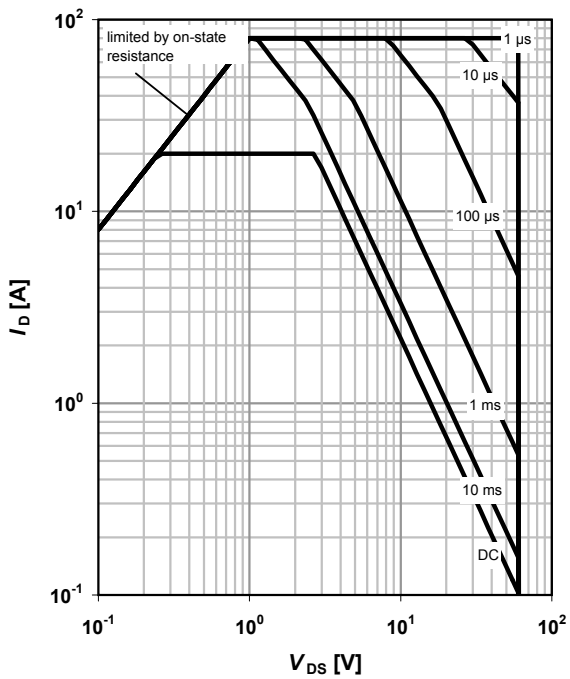
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0$$

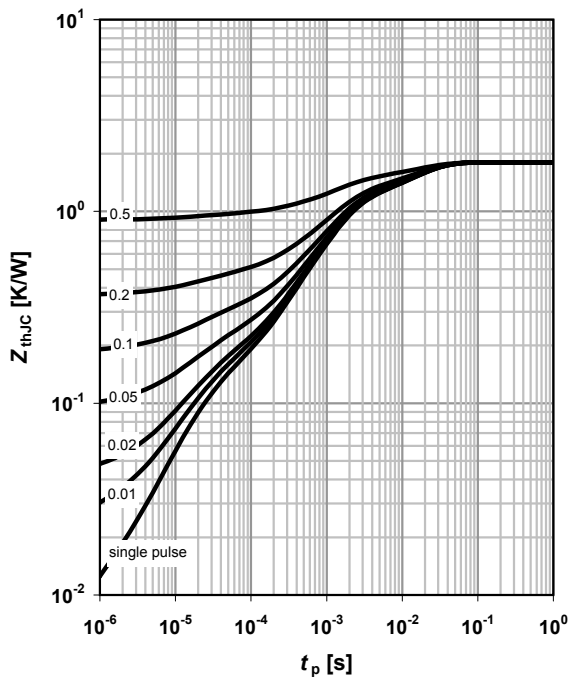
parameter:  $t_p$



**4 Max. transient thermal impedance**

$$Z_{thJC} = f(t_p)$$

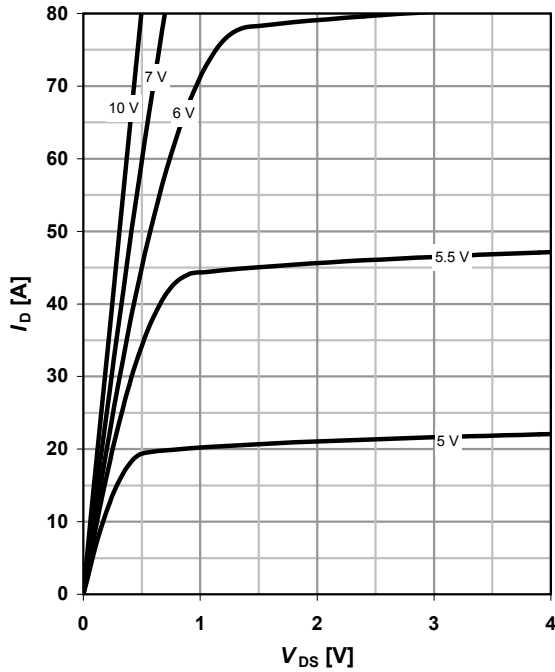
parameter:  $D = t_p / T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

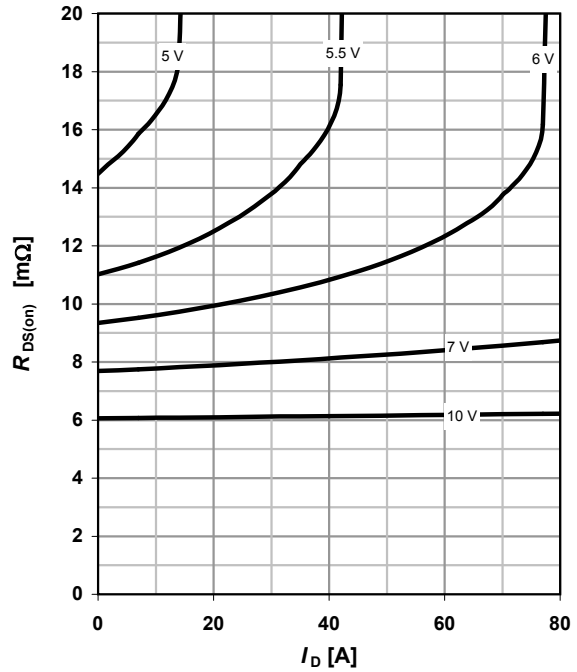
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

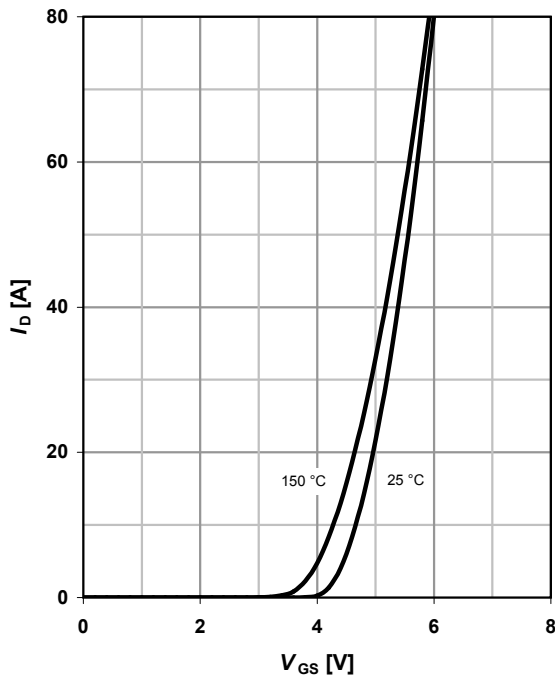
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

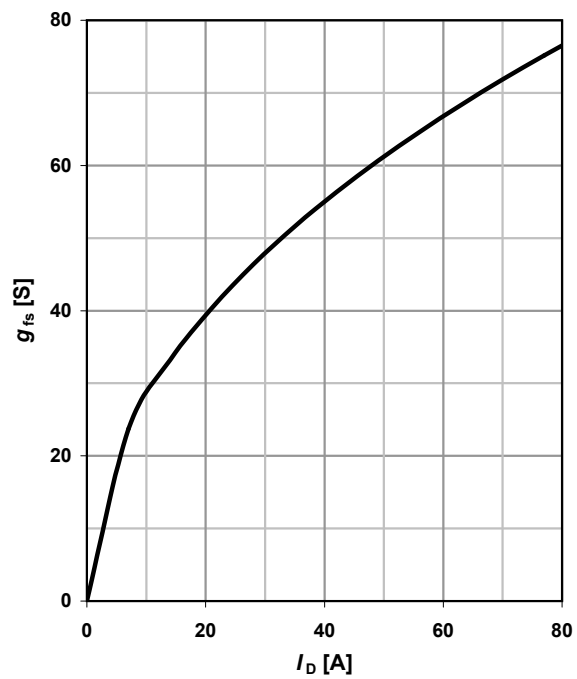
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



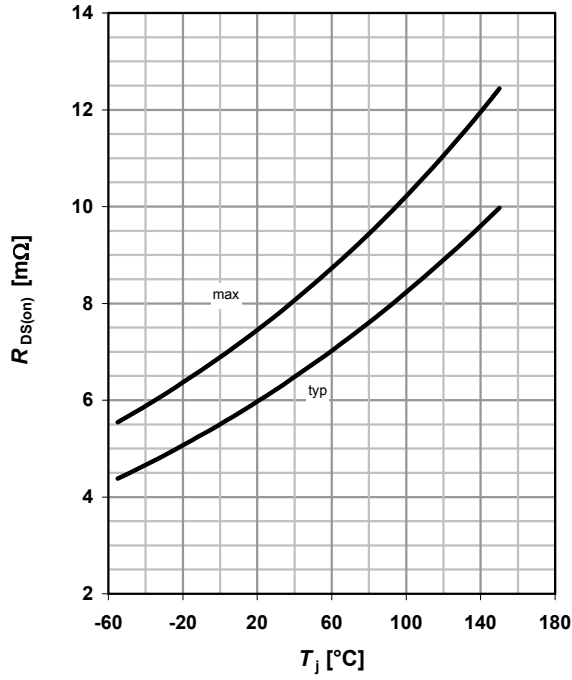
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

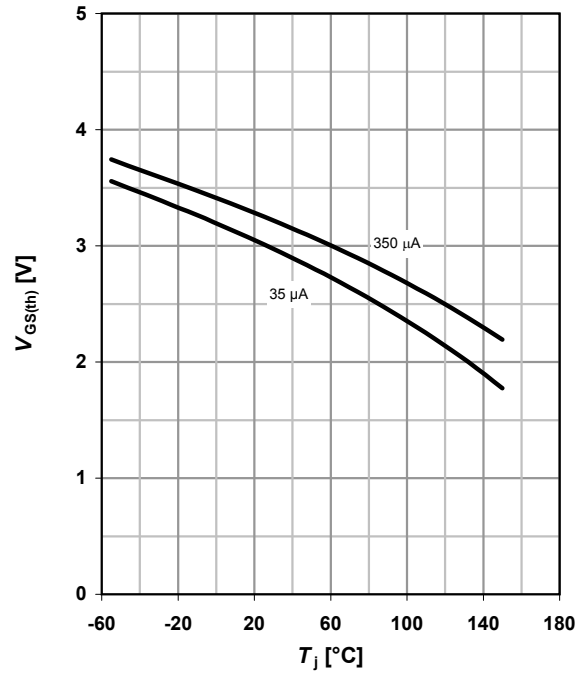


**9 Drain-source on-state resistance**

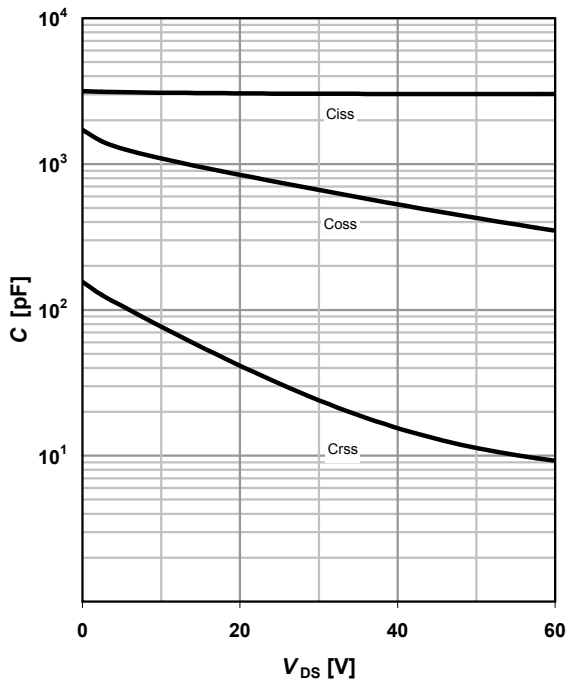
$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$


**10 Typ. gate threshold voltage**

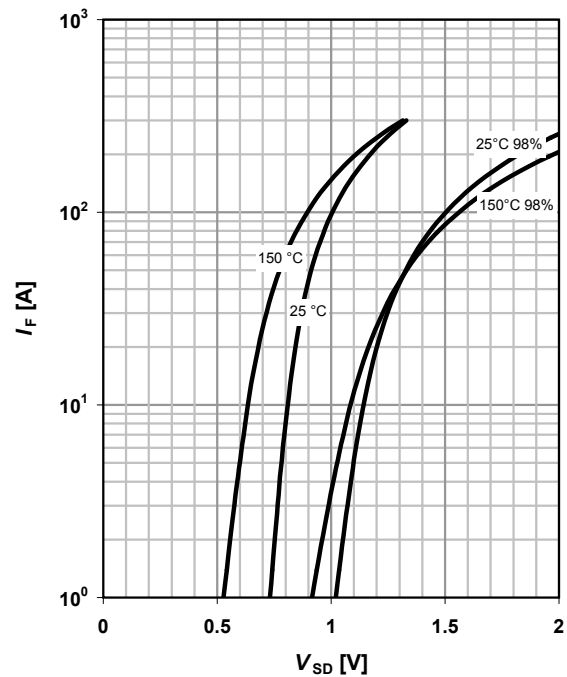
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$


**11 Typ. capacitances**

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

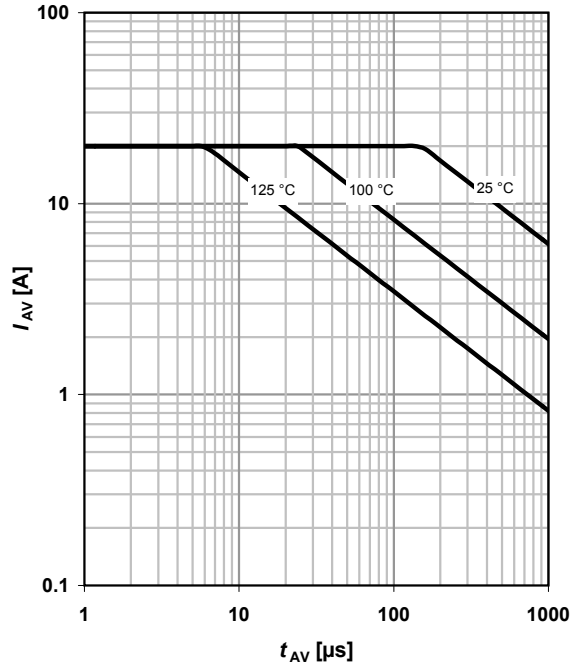

**12 Forward characteristics of reverse diode**

$$I_F = f(V_{SD})$$

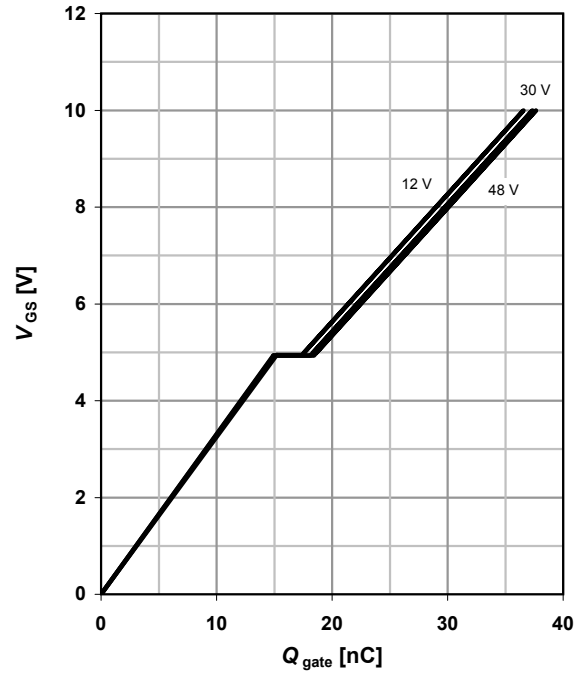
 parameter:  $T_j$ 


**13 Avalanche characteristics**

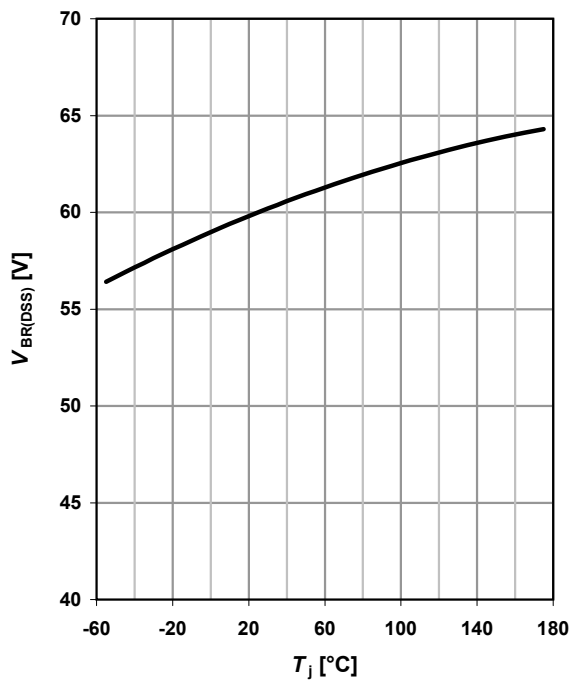
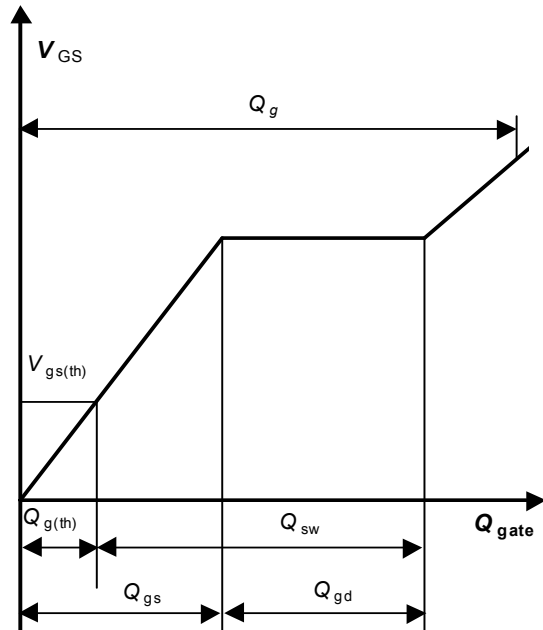
$$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$$

 parameter:  $T_{j(start)}$ 

**14 Typ. gate charge**

$$V_{GS}=f(Q_{gate}); I_D=20 \text{ A pulsed}$$

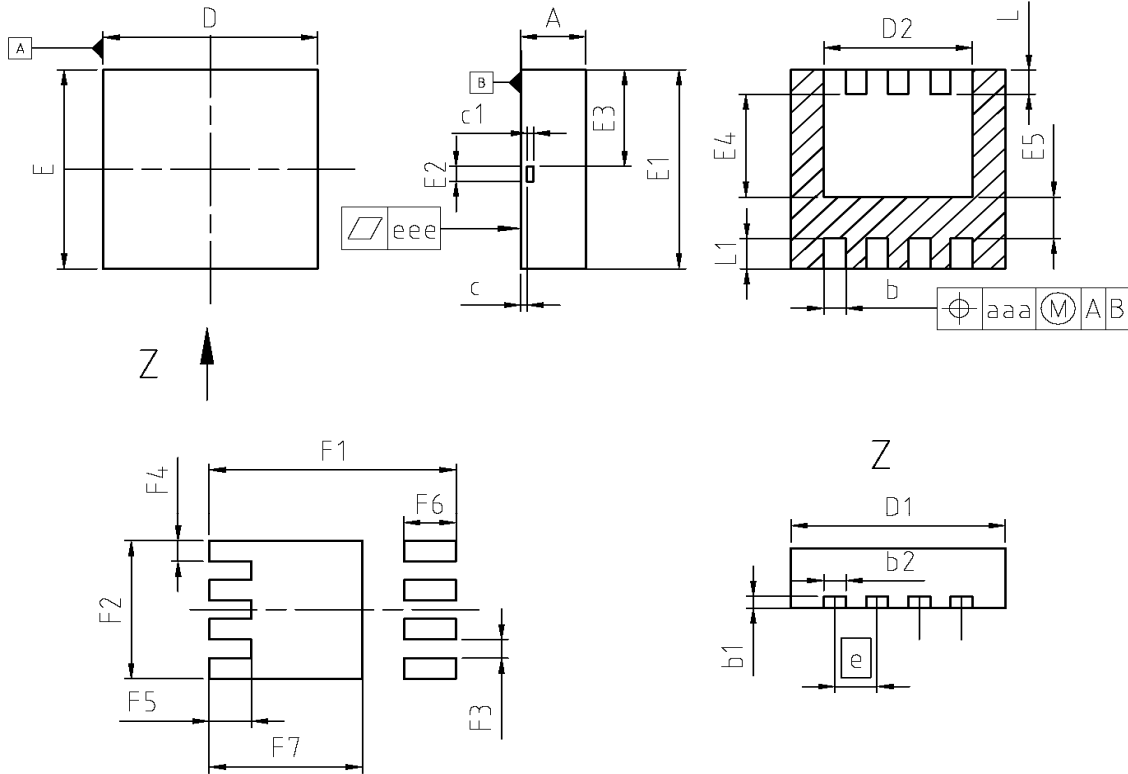
 parameter:  $V_{DD}$ 

**15 Drain-source breakdown voltage**

$$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$$


**16 Gate charge waveforms**


Package Outline

PG-TSDSON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.95	1.00	0.037	0.039
b	0.25	0.35	0.010	0.014
b1	0.10	0.30	0.004	0.012
b2	0.20	0.40	0.008	0.016
c	0.00	0.20	0.000	0.008
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.35	0.085	0.093
E=E1	3.20	3.40	0.126	0.134
E2	0.10	0.30	0.004	0.012
E3	1.35	1.55	0.053	0.061
E4	1.60	1.80	0.063	0.071
E5	0.66	0.86	0.026	0.034
e	0.60	0.70	0.024	0.028
N	8		8	
L	0.31	0.51	0.012	0.020
L1	0.33	0.53	0.013	0.021
aaa	0.25		0.010	
eee	0.05		0.002	
F1	3.70	3.90	0.146	0.154
F2	2.19	2.39	0.086	0.094
F3	0.21	0.41	0.008	0.016
F4	0.24	0.44	0.009	0.017
F5	0.55	0.75	0.022	0.030
F6	0.70	0.90	0.028	0.035
F7	2.26	2.46	0.089	0.097

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