THE DATASHEET OF

BD71850MWV-E2

Datasheet

Power Management Integrated Circuit

BD71850MWV

General Description

- BD71850MWV is a programmable Power Management IC (PMIC) for powering single-core, dual-core, and quad-core SoC's such as NXP-i.MX 8M Nano. It is optimized for low BOM cost and compact solution footprint. It integrates 6 Buck regulators and 6 LDO's to provide all the power rails required by the SoC and the commonly used peripherals.
- QFN package and pinout support low cost Type 3 (non-HDI) PCB. Programmable power sequencing and output voltages, flexible power state control for easier system design and supports a wide variety of processors and system implementations.

Features

- 6 Buck Regulators
  - 2.0 MHz Switching Frequency. (BUCK1, BUCK2, BUCK5, BUCK7, and BUCK8).
  - 1.5MHz Switching Frequency. (BUCK6)
  - Target Efficiency: 83% to 95%.
  - Output Current & Voltage.
    BUCK1: 3.0 A, 0.7 V to 1.3 V/10 mV step, DVS
    BUCK2: 3.0 A, 0.7 V to 1.3 V/10 mV step, DVS
    BUCK5: 3.0 A, 0.70 V to 1.35 V/8steps, DVS
    BUCK6: 3.0 A, 2.6 V to 3.3 V/100 mV step
    BUCK7: 1.5 A, 1.605 V to 1.995 V/8steps
    BUCK8: 3.0 A, 0.8 V to 1.4 V/10 mV step
- 6ch Linear Regulators (6 LDOs)
  - LDO1: 10 mA, 3.0 V to 3.3 V, 1.6 V to 1.9 V
  - LDO2: 10 mA, 0.9 V, 0.8 V
  - LDO3: 300 mA, 1.8 V to 3.3 V
  - LDO4: 250 mA, 0.9 V to 1.8 V
  - LDO5: 300 mA, 0.8 V to 3.3 V
  - LDO6: 300 mA, 0.9 V to 1.8 V
- Power Mux Switch
  - 1.8V Input: 500 mΩ(Max)
  - 3.3V Input: 500 mΩ(Max)
- 32.768 kHz Crystal Oscillator Driver
- Power Button Detector
- Protection and Monitoring: Soft Start, Power Rails Fault Detection, UVLO, OVP and TSD
- OTP Configurable Power Sequencing
- OTP and Software Programmable Output Voltage, Ramp rates.
- Hardware Signaling with SoC for Transition into or out of Low Power States
- Interfaces:
  - I2C: 100 kHz/400 kHz, 1 MHz
  - Power-on Reset Output: POR_B, RTC_RESET_B,
  - Watchdog Reset Input: WDOG_B:
  - Power State Control:
    PMIC_STBY_REQ, PMIC_ON_REQ, PWRON_B
  - Interrupt to SoC: IRQ_B
- Type3 PCB Applicable

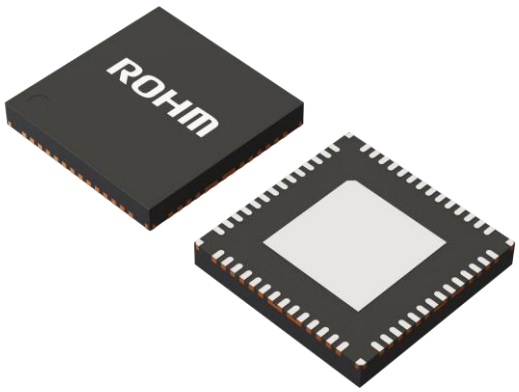
Key Specifications

- Input Voltage Range (VSYS): 2.7 V to 5.5 V
- SNVS State Current: 30 μA(Typ)
- SUSPEND State Current: 115 μA(Typ)
- IDLE State Current: 125 μA(Typ)
- RUN State Current: 125 μA(Typ)
- Operating Temperature Range: -40 °C to +105 °C

Applications

- Streaming Media Boxes and Dongles
- AV Receivers and Wireless Sound Bars
- Industrial HMI, SBC, IPC and Panel Computer

Package	W(Typ) x D(Typ) x H(Max)
UQFN56BV7070	7.00 mm x 7.00 mm x 1.00 mm



○Product structure : Silicon integrated circuit. ○This product has no designed protection against radioactive rays

Contents

Figure

Table

1. Introduction

1.1. Terminology

Table 1-1. Acronyms, Conventions and Terminology

Term	Definition
BOM	Bill Of Materials
DAC	Digital to Analog Converter
DVS	Dynamic Voltage Scaling
FET	Field Effect Transistor
I2C	Inter-Integrated Circuit
IRQ	Interrupt Request
LDO	Low Drop-Out regulator
NTC	Negative Temperature Coefficient. (a type of thermistor)
OCP	Over Current Protection
OTP	One Time Programmable memory
OVP	Over Voltage Protection
PFM	Pulse-Frequency Modulation
POR	Power On Reset
PWM	Pulse-Width Modulation
SMPS	Switched Mode Power Supply
SoC	System-On-a-Chip
UVLO	Under Voltage-LockOut
VR	Voltage Regulator

1.2. System Power Map & Typical Application Circuit

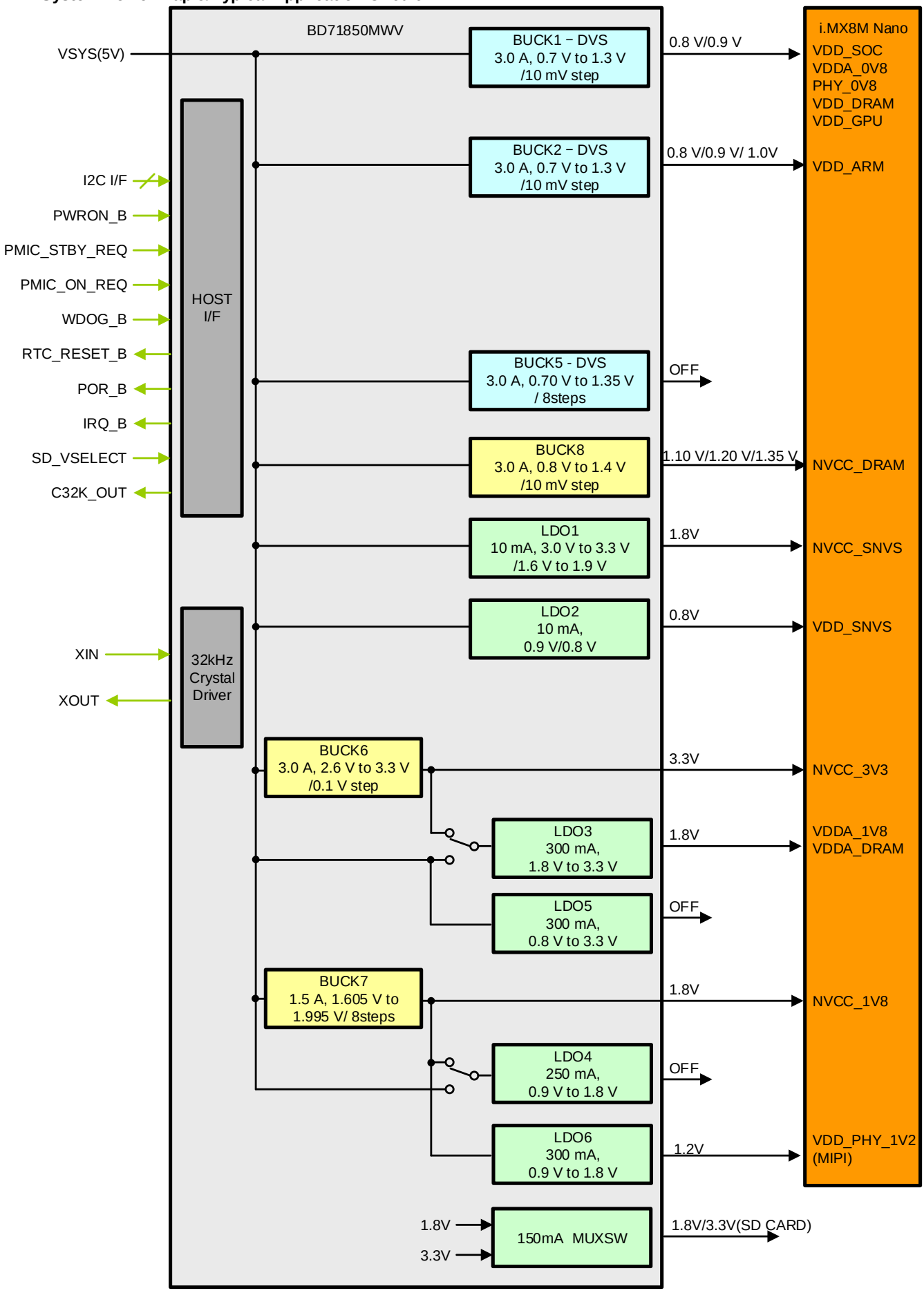
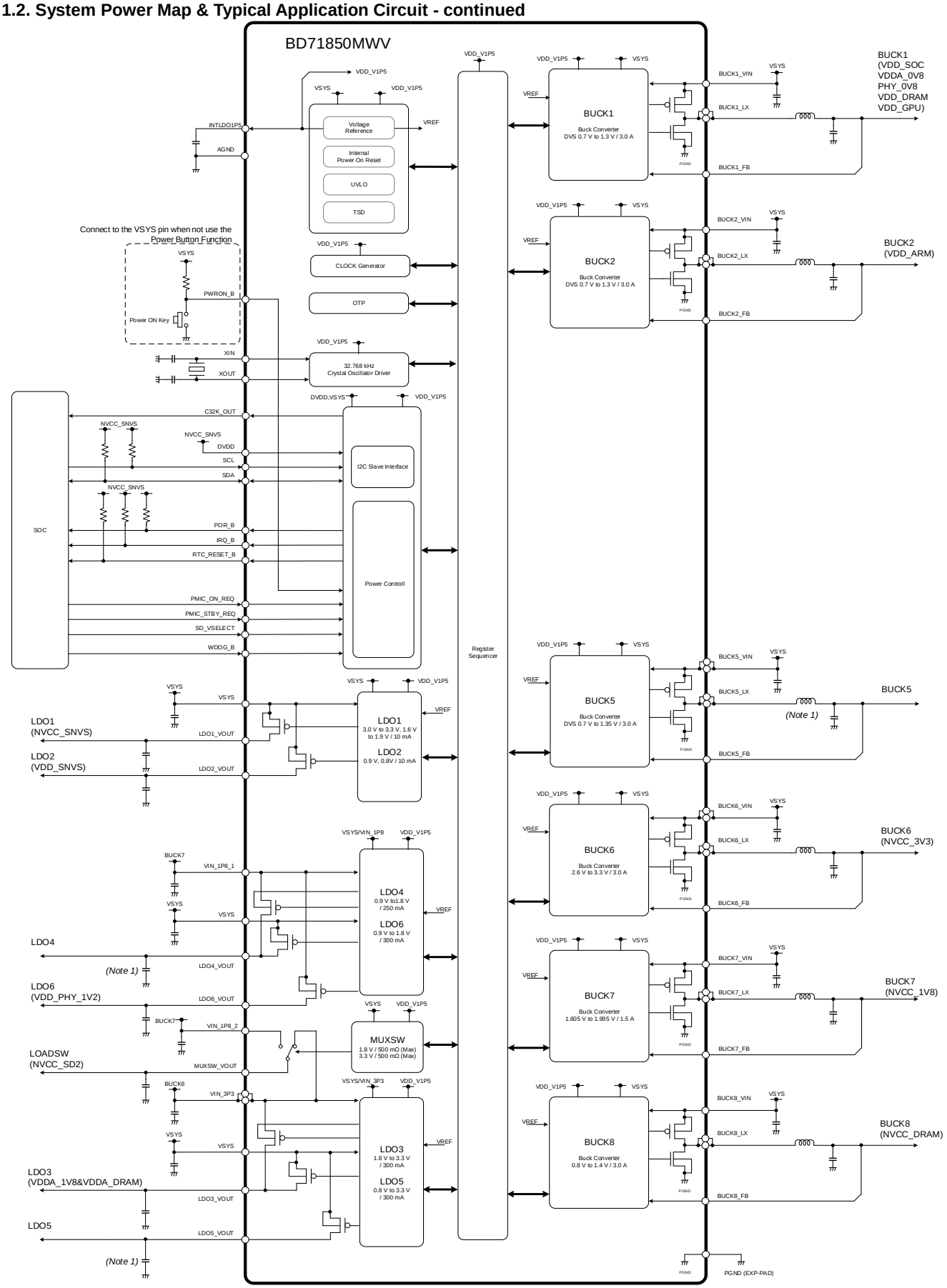


Figure 1-1. System Power Map

1.2. System Power Map & Typical Application Circuit - continued



(Note 1) Output components of BUCK5, LDO4 and LDO5 can be removed because their default settings of OTP are OFF. Other power rails output components cannot be removed. If they are removed, VR fault would be detected and PMIC would be shut down.

Figure 1-2. Typical Applications Circuit

1.3. Pin Configuration

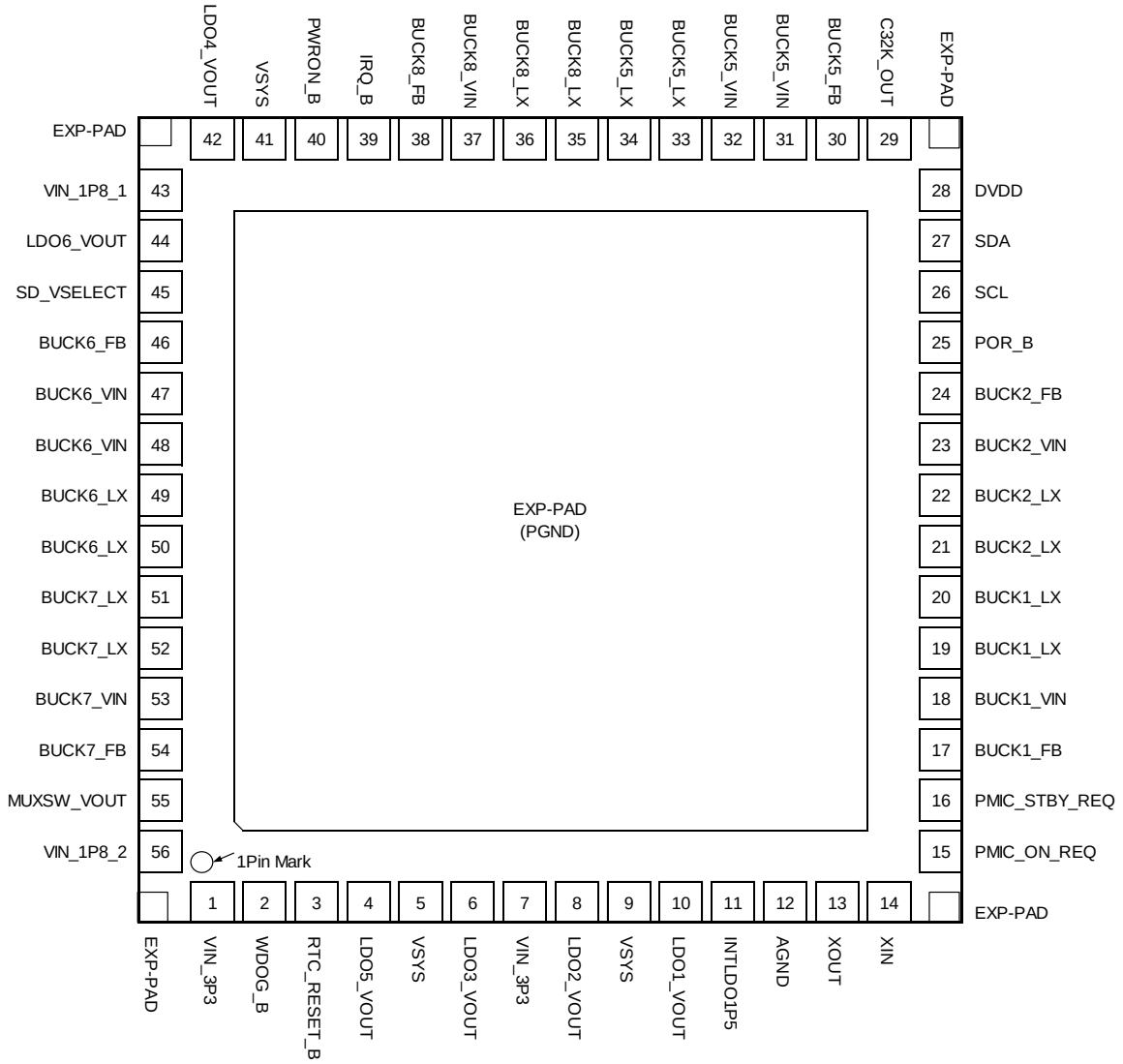


Figure 1-3. Pin Configuration (TOP VIEW)

1.4. Pin Description

Table 1-2. Pin Description

Pin#	Block Name	Pin Name	Dir	Pin Description	PWR /GND	Voltage Level	Terminal Equivalent	Internal pull-up/down
18	BUCK1	BUCK1_VIN	I	BUCK1 switcher input supply	PWR	VSYS	H1_1	No
19		BUCK1_LX	O	BUCK1 switch node connection	-	VSYS	H1_1	No
20		BUCK1_LX	O	BUCK1 switch node connection	-	VSYS	H1_1	No
17		BUCK1_FB	I	BUCK1 feedback sense	-	BUCK1	D2_1	No
23	BUCK2	BUCK2_VIN	I	BUCK2 switcher input supply	PWR	VSYS	H1_1	No
21		BUCK2_LX	O	BUCK2 switch node connection	-	VSYS	H1_1	No
22		BUCK2_LX	O	BUCK2 switch node connection	-	VSYS	H1_1	No
24		BUCK2_FB	I	BUCK2 feedback sense	-	BUCK2	D2_1	No
31	BUCK5	BUCK5_VIN	I	BUCK5 switcher input supply	PWR	VSYS	H1_1	No
32		BUCK5_VIN	I	BUCK5 switcher input supply	PWR	VSYS	H1_1	No
33		BUCK5_LX	O	BUCK5 switch node connection	-	VSYS	H1_1	No
34		BUCK5_LX	O	BUCK5 switch node connection	-	VSYS	H1_1	No
30		BUCK5_FB	I	BUCK5 feedback sense	-	BUCK5	D2_1	No
47	BUCK6	BUCK6_VIN	I	BUCK6 switcher input supply	PWR	VSYS	H1_1	No
48		BUCK6_VIN	I	BUCK6 switcher input supply	PWR	VSYS	H1_1	No
49		BUCK6_LX	O	BUCK6 switch node connection	-	VSYS	H1_1	No
50		BUCK6_LX	O	BUCK6 switch node connection	-	VSYS	H1_1	No
46		BUCK6_FB	I	BUCK6 feedback sense	-	BUCK6	D2_1	No
53	BUCK7	BUCK7_VIN	I	BUCK7 switcher input supply	PWR	VSYS	H1_1	No
51		BUCK7_LX	O	BUCK7 switch node connection	-	VSYS	H1_1	No
52		BUCK7_LX	O	BUCK7 switch node connection	-	VSYS	H1_1	No
54		BUCK7_FB	I	BUCK7 feedback sense	-	BUCK7	D2_1	No
37	BUCK8	BUCK8_VIN	I	BUCK8 switcher input supply	PWR	VSYS	H1_1	No
35		BUCK8_LX	O	BUCK8 switch node connection	-	VSYS	H1_1	No
36		BUCK8_LX	O	BUCK8 switch node connection	-	VSYS	H1_1	No
38		BUCK8_FB	I	BUCK8 feedback sense	-	BUCK8	D2_1	No
9	LDO1 LDO2	VSYS	I	LDO1, LDO2 input supply	PWR	VSYS	G1_1	No
10		LDO1_VOUT	O	LDO1 output	-	LDO1	G1_1	No
8		LDO2_VOUT	O	LDO2 output	-	LDO2	G1_1	No
43	LDO4 LDO6	VIN_1P8_1	I	LDO4, LDO6 input supply	PWR	BUCK7	G1_2,G3_1	No
41		VSYS	I	LDO4 input supply	PWR	VSYS	G1_1,G3_1	No
42		LDO4_VOUT	O	LDO4 output	-	LDO4	G3_1	No
44		LDO6_VOUT	O	LDO6 output	-	LDO6	G1_2	No
7	LDO3 LDO5	VIN_3P3	I	LDO3,MUXSW input supply	PWR	BUCK6	G3_2	No
5		VSYS	I	LDO3,LDO5 input supply	PWR	VSYS	G1_1,G3_2	No
6		LDO3_VOUT	O	LDO3 output	-	LDO3	G3_2	No
4		LDO5_VOUT	O	LDO5 output	-	LDO5	G1_1	No
1	MUXSW	VIN_3P3	I	LDO3,MUXSW input supply	PWR	BUCK6	F2_1	No
56		VIN_1P8_2	I	MUXSW input supply	PWR	BUCK7	F2_1	No
55		MUXSW_VOUT	O	LOADSW output	-	LOADSW	F2_1	No
11	REF	INTLDO1P5	O	Internal LDO for PMIC	PWR	INTLDO1P5	G1_3	No
12		AGND	I	AGND	GND	0V	Z1_1	No
14	Crystal Oscillator	XIN	I	32.768kHz crystal input	-	INTLDO1P5	E1_1	No
13		XOUT	O	32.768kHz crystal output	-	INTLDO1P5	E1_1	No
28	Interface	DVDD	I	Interface input supply	PWR	DVDD	Z1_1	No
26		SCL	I	I^2C CLOCK	-	DVDD	A1_1	No *(Note 1)*
27		SDA	I /O	I^2C DATA	-	DVDD	A3_1	No *(Note 1)*
29		C32K_OUT	O	32.768kHz clock output	-	DVDD	C1_1	No
39		IRQ_B	O	Interrupt signal to processor(Open Drain)	-	DVDD	C1_1	No *(Note 1)*
25		POR_B	O	Power on reset output(Open Drain)	-	DVDD	C1_1	No *(Note 1)*
3		RTC_RESET_B	O	Power OK signal for LDO1,2(Open Drain)	-	DVDD	C1_1	No *(Note 1)*
2		WDOG_B	I	Watchdog input from processor	-	DVDD	C1_1	No
15		PMIC_ON_REQ	I	Power on/off control Input	-	VSYS	A6_1	No
16		PMIC_STBY_REQ	I	Standby input signal	-	DVDD	C1_1	No
45		SD_VSELECT	I	Voltage select for SD	-	DVDD	C1_1	No
40		PWRON_B	I	Power Button	-	VSYS	A6_1	No
-	-	EXP-PAD (PGND)	-	Power Ground. Connect the center EXP-PAD in the Figure 1-3 to the GND plane of PCB. The EXP-PADs on the 4-corner have the same potential as the center EXP-PAD. The EXP-PADs on the 4-coner are recommended to be soldered to PCB (GND or open).	GND	0V	Z1_1	No

(Note 1) Need to pull-up external resistance to DVDD

1.5. I/O Equivalence Circuit

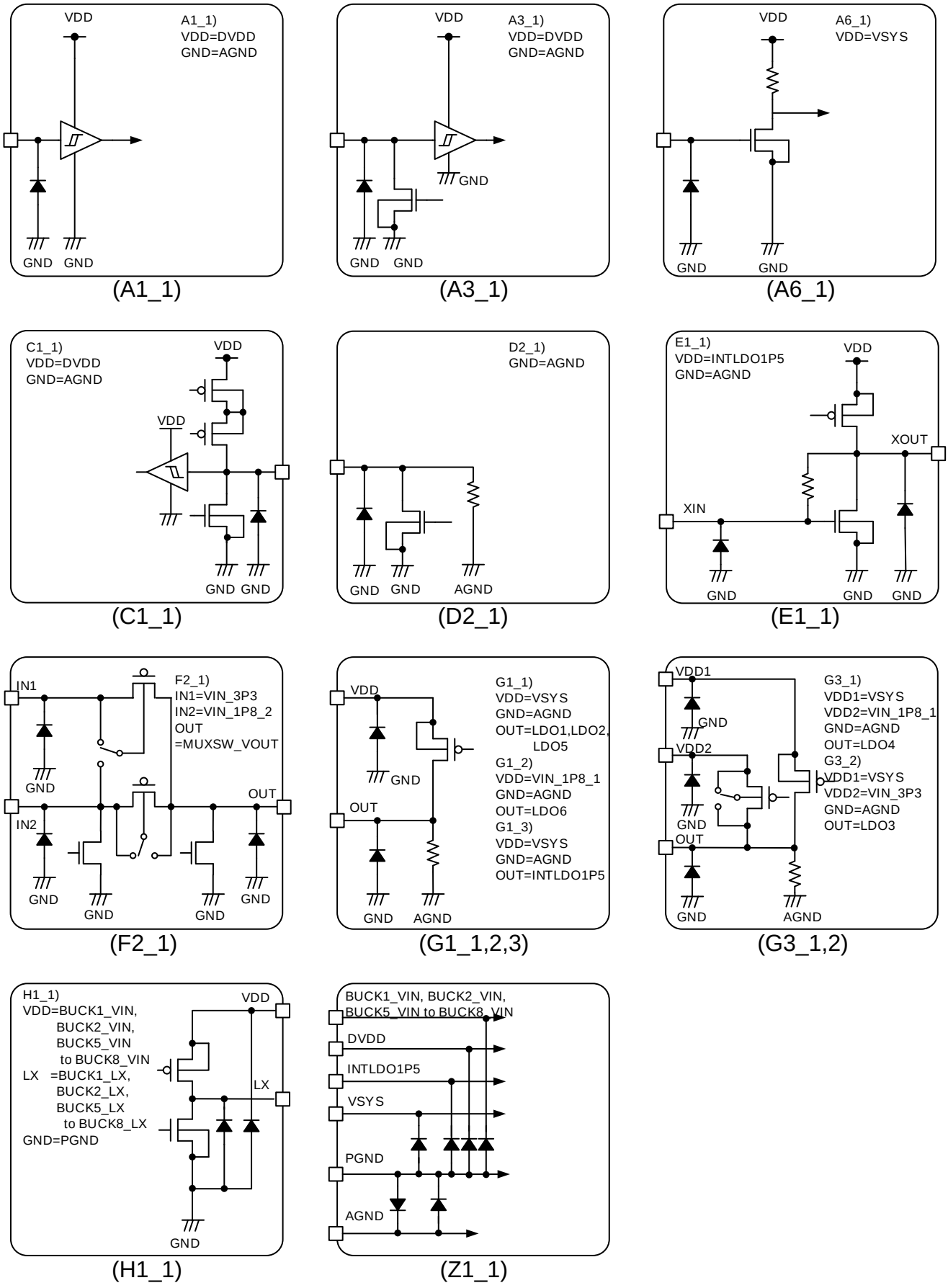


Figure 1-4. I/O Equivalence Circuit 1

1.6. Power Rail

Table 1-3. Power Rails and Output Signals

Sequence Order	Function	Rail/Signal Name	Type	Input Rail	Output Voltage Initial Value [V]	Output Voltage Adjustable Range [V]	DVS	I_{OMAX} [A]
1	NVCC_SNVS	LDO1	Source LDO	VSYS	1.8	3.0 to 3.3,1.6 to 1.9 (100 mV step)	-	0.01
2	VDD_SNVS	LDO2	Source LDO	VSYS	0.8	0.9, 0.8	-	0.01
3	RTC_RESET_B	RTC_RESET_B	Open drain	-	-	-	-	-
4	32K_OUT	C32K_OUT	CMOS	DVDD	-	-	-	-
5	VDD_SOC, VDDA_0V8, PHY_0V8, VDD_DRAM, VDD_GPU	BUCK1	SMPS	VSYS	0.8	0.7 to 1.3 (10 mV step)	DVS	3.0
6	VDD_ARM	BUCK2	SMPS	VSYS	0.9	0.7 to 1.3 (10 mV step)	DVS	3.0
6	VDDA_1V8, VDDA_DRAM	LDO3	Source LDO	VSYS/ BUCK6	1.8	1.8 to 3.3 (100 mV step)	-	0.3
7	NVCC_1V8	BUCK7	SMPS	VSYS	1.8	1.605,1.695,1.755, 1.800,1.845,1.905, 1.950,1.995	-	1.5
8	NVCC_DRAM	BUCK8	SMPS	VSYS	1.1	0.8 to 1.4 (10 mV step)	-	3.0
9	NVCC_3V3	BUCK6	SMPS	VSYS	3.3	2.6 to 3.3 (100mVstep)	-	3.0
9	NVCC_SD2	MUXSW	MUX Switch	BUCK6/ BUCK7	3.3/1.8	-	-	0.15
10	VDD_PHY_1V2	LDO6	Source LDO	BUCK7	1.2	0.9 to 1.8 (100 mV step)	-	0.3
11	POR_B	POR_B	Open drain	-	-	-	-	-
-	-	BUCK5	SMPS	VSYS	0.9	0.70,0.80,0.90,1.00 1.05,1.10,1.20,1.35	DVS	3.0
-	-	LDO4	Source LDO	VSYS/ BUCK7	0.9	0.9 to 1.8 (100 mV step)	-	0.25
-	-	LDO5	Source LDO	VSYS	3.3	0.8 to 3.3 (100 mV step)	-	0.3

1.7. Register Map

Table 1-4. Register Map

Address (Hex)	Reset Condition *(Note 1)*	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value (Hex)	Access (R, W, R/W)	OTP	Write Access Lock *(Note 2)*
00	NA	REV	MAJREV[3:0]				MINREV[3:0]				A1	R	No	-
01	UVLO	SWRESET	-	-	-	-	-	SWRESET_SEL[1:0]		SWRESET	04	R/W	No	-
02	UVLO	I2C_DEV	-	-	-	-	-	-	I2C_DEV_ADRS[1:0]		03	R	Yes	-
03	UVLO	PWRCTRL0	DEBUG_STATE[1:0]		RELOAD_REG	-	-	-	WDOGB_SEL[1:0]		A2	R/W	Yes	PWRSEQ
04	UVLO	PWRCTRL1	-	-	-	-	-	-	-	IDLE_MODE	00	R/W	Yes	-
05	READY	BUCK1_CTRL	BUCK1_RAMPRATE[1:0]		-	-	BUCK1_PWM_FIX	-	BUCK1_SEL	BUCK1_EN	40	R/W	Yes	VREG
06	READY	BUCK2_CTRL	BUCK2_RAMPRATE[1:0]		-	-	BUCK2_PWM_FIX	-	BUCK2_SEL	BUCK2_EN	40	R/W	Yes	VREG
07	-	-	-	-	-	-	-	-	-	-	-	-	-	-
08	-	-	-	-	-	-	-	-	-	-	-	-	-	-
09	READY	BUCK5_CTRL	-	-	-	-	BUCK5_PWM_FIX	-	BUCK5_SEL	BUCK5_EN	02	R/W	Yes	VREG
0A	READY	BUCK6_CTRL	-	-	-	-	BUCK6_PWM_FIX	-	BUCK6_SEL	BUCK6_EN	00	R/W	Yes	VREG
0B	READY	BUCK7_CTRL	-	-	-	-	BUCK7_PWM_FIX	-	BUCK7_SEL	BUCK7_EN	00	R/W	Yes	VREG
0C	READY	BUCK8_CTRL	-	-	-	-	BUCK8_PWM_FIX	-	BUCK8_SEL	BUCK8_EN	00	R/W	Yes	VREG
0D	READY	BUCK1_VOLT_RUN	-	BUCK1_VOLT_RUN[6:0]							0A	R/W	Yes	VREG
0E	READY	BUCK1_VOLT_IDLE	-	BUCK1_VOLT_IDLE[6:0]							0A	R/W	Yes	VREG
0F	READY	BUCK1_VOLT_SUSP	-	BUCK1_VOLT_SUSP[6:0]							0A	R/W	Yes	VREG
10	READY	BUCK2_VOLT_RUN	-	BUCK2_VOLT_RUN[6:0]							14	R/W	Yes	VREG
11	READY	BUCK2_VOLT_IDLE	-	BUCK2_VOLT_IDLE[6:0]							0A	R/W	Yes	VREG
12	-	-	-	-	-	-	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-	-	-	-	-	-	-
14	READY	BUCK5_VOLT	BUCK5_VOLT_SEL[1:0]		-	-	-	BUCK5_VOLT[2:0]			02	R/W	Yes	VREG
15	READY	BUCK6_VOLT	-	BUCK6_VOLT_SEL	-	-	-	-	BUCK6_VOLT[1:0]		03	R/W	Yes	VREG
16	READY	BUCK7_VOLT	-	-	-	-	-	BUCK7_VOLT[2:0]			03	R/W	Yes	VREG
17	READY	BUCK8_VOLT	-	BUCK8_VOLT[6:0]							1E	R/W	Yes	VREG
18	READY	LDO1_VOLT	LDO1_SEL	LDO1_EN	LDO1_VOLT_SEL	-	-	-	LDO1_VOLT[1:0]		22	R/W	Yes	VREG
19	READY	LDO2_VOLT	LDO2_SEL	LDO2_EN	LDO2_VOLT_SEL	-	-	-	-	-	20	R/W	Yes	VREG
1A	READY	LDO3_VOLT	LDO3_SEL	LDO3_EN	-	-	LDO3_VOLT[3:0]				00	R/W	Yes	VREG
1B	READY	LDO4_VOLT	LDO4_SEL	LDO4_EN	-	-	LDO4_VOLT[3:0]				80	R/W	Yes	VREG
1C	READY	LDO5_VOLT	LDO5_SEL	LDO5_EN	LDO5_VOLT_SEL	-	LDO5_VOLT[3:0]				8F	R/W	Yes	VREG
1D	READY	LDO6_VOLT	LDO6_SEL	LDO6_EN	-	-	LDO6_VOLT[3:0]				03	R/W	Yes	VREG
1E	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1F	UVLO	TRANS_COND0	C1_ VSYS_3P0_ ONLY_EN	C1_ PMIC_ON_ REQ_EN	C1_ SHORT_ PUSH_EN	C1_ LONG_ PUSH_EN	C0_ VSYS_3P0_ ONLY_EN	C0_ PMIC_ON_ REQ_EN	C0_ SHORT_ PUSH_EN	C0_ LONG_ PUSH_EN	48	R/W	Yes	PWRSEQ
20	UVLO	TRANS_COND1	PONT[3:0]				PWRON_ POFF_TO_ READY	WDOG_ POFF_TO_ READY	SWRST_ POFF_TO_ READY	ON_REQ_ POFF_TO_ READY	C0	R/W	Yes	PWRSEQ
21	UVLO	VRFAULTEN	-	-	-	-	-	-	-	VRFLTEN	01	R/W	Yes	-
22	UVLO	MVRFLTMASK0	MBUCK8_ VOUTOKH	MBUCK8_ VOUTOKL	MBUCK7_ VOUTOKH	MBUCK7_ VOUTOKL	MBUCK6_ VOUTOKH	MBUCK6_ VOUTOKL	MBUCK5_ VOUTOKH	MBUCK5_ VOUTOKL	00	R/W	Yes	-
23	UVLO	MVRFLTMASK1	-	-	-	-	MBUCK2_ VOUTOKH	MBUCK2_ VOUTOKL	MBUCK1_ VOUTOKH	MBUCK1_ VOUTOKL	00	R/W	Yes	-
24	UVLO	MVRFLTMASK2	-	-	MLDO6_ VOUTOKL	MLDO5_ VOUTOKL	MLDO4_ VOUTOKL	MLDO3_ VOUTOKL	MLDO2_ VOUTOKL	MLDO1_ VOUTOKL	00	R/W	Yes	-
25	UVLO	RCVCFG	RCVLMT[3:0]				RCVDT[3:0]				4C	R/W	Yes	-
26	UVLO	RCVNUM	-	-	-	-	RCVNUM[3:0]				00	R/W	No	-
27	UVLO	PWRONCONFIG0	-	-	PBDBNCT[1:0]		SHORTT[3:0]				16	R/W	Yes	-
28	UVLO	PWRONCONFIG1	-	-	-	-	LONGT[3:0]				00	R/W	Yes	-
29	UVLO	RESETSRC	RPWRON	RWDOG	RSWRST	RPMIC_ON_REQ	RVSYS_2P7	RTEMP	ROCP	RVR_FAULT	00	R/W	No	-
2A	UVLO	MIRQ	-	MSWRST	MPWRON_S	MPWRON_L	MPWRON	MWDOG	MON_REQ	MSTBY_REQ	7F	R/W	No	-
2B	UVLO	IRQ	-	SWRST	PWRON_S	PWRON_L	PWRON	WDOG	ON_REQ	STBY_REQ	00	R/W	No	-
2C	UVLO	IN_MON	-	-	-	-	STAT_PWRON	STAT_WDOG	STAT_ON_REQ	STAT_STBY_REQ	00	R	No	-
2D	UVLO	POW_STATE	POW_ST[3:0]				-	-	POW_SUB[1:0]		00	R	No	-
2E	READY	OUT32K	-	-	-	-	-	-	-	OUT32K_EN	01	R/W	Yes	-
2F	READY	REGLOCK	-	-	-	VREG	-	-	-	PWRSEQ	11	R/W	No	-
30	READY	MUXSW_EN	-	-	-	-	-	-	-	MUXSW_EN	01	R/W	Yes	-
FF	NA	OTPVER	OTPVER[7:0]								C3	R	Yes	-

(Note 1) Reset Condition of each register is classified as follows.
UVLO: When INTLDO1P5_UVLO=0, register values are reset to the default value.
READY: When Power State enters READY, register values are reset to the default value.

(Note 2) Regarding registes labeled in this column, its write access is disabled as follows.
PWRSEQ: When PWRSEQ in REGLOCK register is set to 1, write access is disabled.
VREG: When VREG in REGLOCK register is set to 1, write access is disabled.

Table 1-5. REV - Revision Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REV	R	MAJREV[3:0]				MINREV[3:0]				0xA1	0x00

Bit	Name	Function	Initial
D[7:4]	MAJREV[3:0]	Major Revision	1010
D[3:0]	MINREV[3:0]	Minor Revision	0001

1.7. Register Map – continued

Table 1-6. REGLOCK - Lock Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REGLOCK	R/W	-	-	-	VREG	-	-	-	PWRSEQ	0x11	0x2F

Bit	Name	Function	Initial
D[4]	VREG	Write access to following 21 registers is controlled by this bit. 0 = Enable the write access 1 = Disable the write access BUCK1_CTRL, BUCK2_CTRL, BUCK5_CTRL, BUCK6_CTRL, BUCK7_CTRL, BUCK8_CTRL BUCK1_VOLT_RUN, BUCK1_VOLT_IDLE BUCK1_VOLT_SUSP, BUCK2_VOLT_RUN BUCK2_VOLT_IDLE, BUCK5_VOLT, BUCK6_VOLT, BUCK7_VOLT BUCK8_VOLT, LDO1_VOLT, LDO2_VOLT, LDO3_VOLT LDO4_VOLT, LDO5_VOLT, LDO6_VOLT	1
D[0]	PWRSEQ	Write access to following 3 registers is controlled by this bit. 0 = Enable the write access 1 = Disable the write access PWRCTRL0, TRANS_COND0, TRANS_COND1	1

Table 1-7. OTPVER – OTP Version Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OTPVER	R	OTPVER[7:0]								0xC3	0xFF

Bit	Name	Function	Initial
D[7:0]	OTP_VER[7:0]	OTP Version	0xC3

1.8. ESD

Table 1-8. ESD

Parameter	Minimum Limit	Unit
Human Body Model(HBM)	±2000	V
Charged Device Model(CDM)	±1000	V

2. Operating Conditions

2.1. Absolute Maximum Ratings (Ta=25 ˚C)

Table 2-1. Absolute Maximum Ratings

Parameter	Symbol	Limit		Unit
		Min	Max	
Voltage Range in PINs: VSYS, BUCK1_VIN, BUCK2_VIN, BUCK5_VIN to BUCK8_VIN, VIN_1P8_1, VIN_1P8_2, VIN_3P3, PWRON_B, PMIC_ON_REQ	V_{AMR_1}	-0.3	+6.0	V
Voltage Range in PIN: DVDD	V_{AMR_2}	-0.3	+4.5	V
Voltage Range in PIN: INTLDO1P5	V_{AMR_3}	-0.3	+2.1	V
Voltage Range in PINs: BUCK1_LX, BUCK2_LX, BUCK5_LX to BUCK8_LX	V_{AMR_4}	-1.0(DC) -2.0(10 ns)	+7.0	V
Voltage Range in PINs: SCL,SDA,IRQ_B,POR_B,WODG_B, RTC_RESET_B PMIC_STBY_REQ,SD_VSELECT,C32K_OUT	V_{AMR_5}	-0.3	+4.5	V
Voltage Range in PINs: BUCK1_FB, BUCK2_FB, BUCK5_FB to BUCK8_FB, LDO1_VOUT to LDO6_VOUT, MUXSW_VOUT	V_{AMR_6}	-0.3	+4.5	V
Voltage Range in PINs: XIN, XOUT	V_{AMR_7}	-0.3	+2.1	V
Maximum Junction Temperature	Tjmax	-	150	°C
Storage Temperature Range	Tstg	-55	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

2.2. Thermal Resistance

Table 2-2. Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
UQFN56BV7070				
Junction to Ambient	θ_{JA}	76.8	28.1	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	6	6	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

2.3. Recommended Operating Conditions

Table 2-3. Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Voltage Range in PINs: VSYS, BUCK1_VIN, BUCK2_VIN, BUCK5_VIN to BUCK8_VIN *(Note 1)*	V_{OPR_1}	2.70	5.00	5.50	V
Voltage Range in PIN: VIN_3P3 *(Note 2)*	V_{OPR_2}	2.70	3.30	3.60	V
Voltage Range in PIN: VIN_1P8_1 *(Note 3)*	V_{OPR_3}	1.71	1.80	5.50	V
Voltage Range in PIN: VIN_1P8_2 *(Note 3)*	V_{OPR_4}	1.71	1.80	1.89	V
Voltage Range in PIN: DVDD	V_{OPR_5}	1.71	1.80	3.60	V
Operating Temperature	Topr	-40	+25	+105	°C

(Note 1) It is necessary to supply the same voltage to the VSYS pin and the BUCK1_VIN, BUCK2_VIN, and BUCK5_VIN to BUCK8_VIN pins.
(Note 2) The VIN_3P3 pin is recommended to connect with BUCK6 outputs.
(Note 3) The VIN_1P8_1 pin and the VIN_1P8_2 pin are recommended to connect with BUCK7 outputs.

2.4. Current Consumption

Table 2-4. Current Consumption

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
VSYS Circuit Current 1	I_{Q_VSYS1}	-	14	23	μA	READY State *(Note 1)*
VSYS Circuit Current 2	I_{Q_VSYS2}	-	30	50	μA	SNVS State *(Note 1)*
VSYS Circuit Current 3	I_{Q_VSYS3}	-	115	180	μA	SUSPEND State *(Note 1)*
VSYS Circuit Current 4	I_{Q_VSYS4}	-	125	185	μA	IDLE State *(Note 1)*
VSYS Circuit Current 5	I_{Q_VSYS5}	-	125	185	μA	Run State *(Note 1)*
DVDD Circuit Current 1	I_{Q_DVDD1}	-	-	2	μA	DVDD static current (OUT32K_EN=0)
DVDD Circuit Current 2	I_{Q_DVDD2}	-	4	-	μA	DVDD oparation current (OUT32K_EN=1) *(Note 2)*

(Note 1) When DVDD is connected with LDO1, total circuit current is the value that added VSYS and DVDD circuit current of this table.
(Note 2) This circuit current is affected by parasitic capacitance of the board.

2.5. Power Reference and Detectors (UVLO)

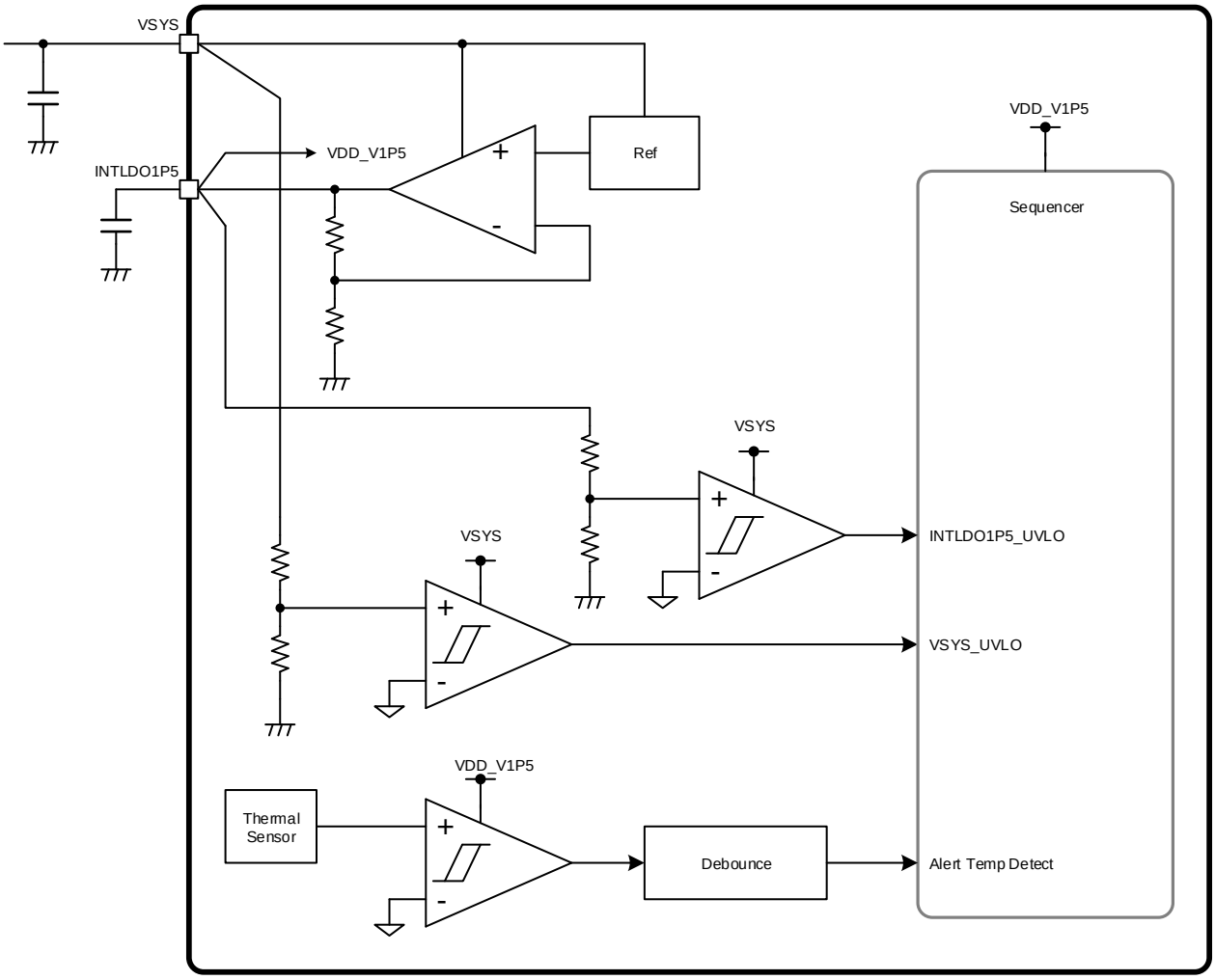


Figure 2-1. Power Reference and Detectors Block Diagram

Table 2-5. Power Reference and Detectors Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Remarks
		Min	Typ	Max		
Voltage Detector - VSYS under voltage(VSYS_UVLO)						
Release Voltage	V_{UVLORL}	2.65	3.00	3.35	V	VSYS=Sweep up
Detect Voltage	V_{UVLODT}	2.65	2.70	2.75	V	VSYS =Sweep down
Hysteresis Voltage	$V_{UVLOHYS}$	-	0.3	-	V	
Voltage Detector - INTLDO1P5 under voltage(INTLDO1P5_UVLO)						
Release Voltage	$V_{INTUVLORL}$	-	1.39	-	V	VSYS=Sweep up
Detect Voltage	$V_{INTUVLODT}$	-	1.35	-	V	VSYS =Sweep down
PMIC Die Critical Temperature Detector (Thermal Shutdown factor)						
Detect Temperature	T_{CTD}	-	150	-	°C	Die Temperature=Sweep up
Power Reference						
INTLDO1P5 Output Voltage	V_{LDO15}	-	1.5	-	V	This output voltage is for internal use only.
COUT Capacitor	C_{O_LDO15}	0.5	1.0	5.0	µF	

3. Power State Control

3.1. Power Control Signals

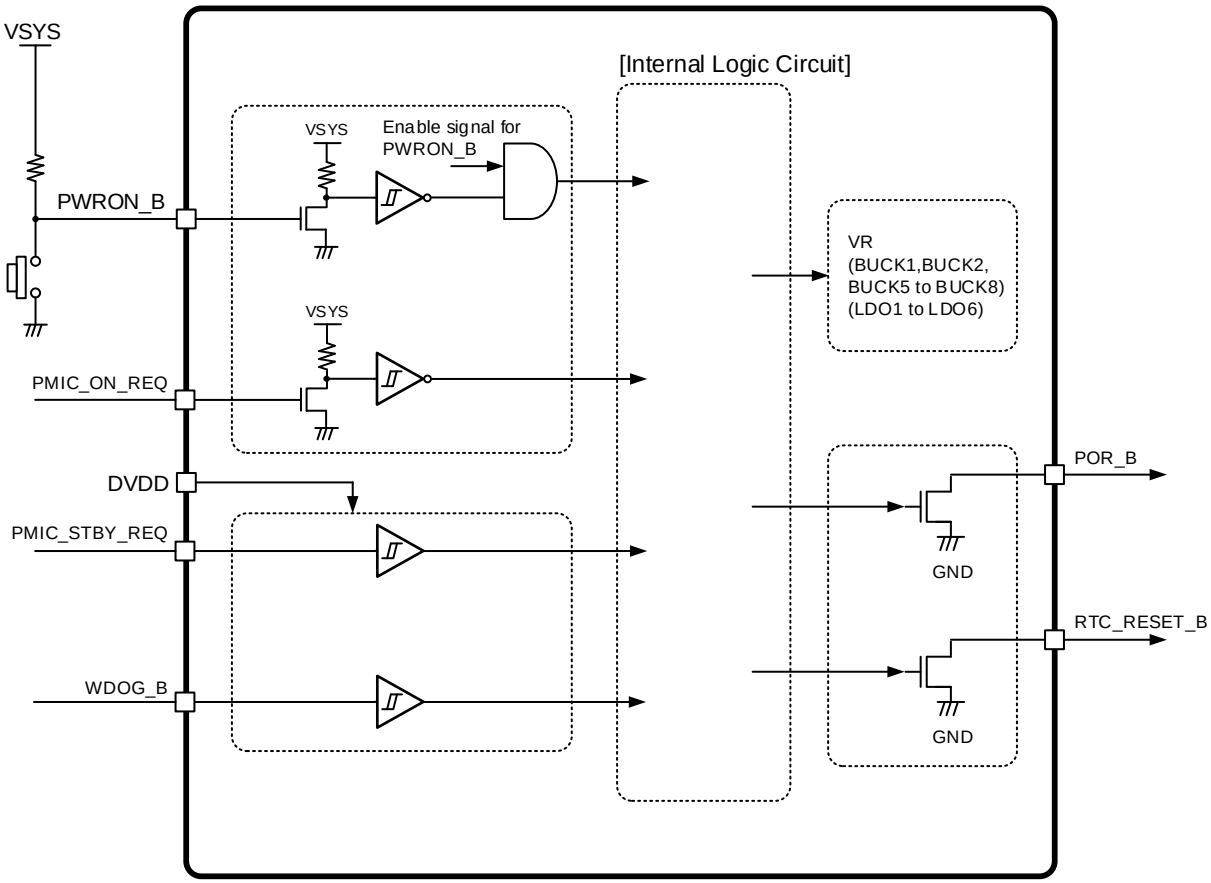


Figure 3-1. Power Control Signals of BD71850MWV

3.1.1. PWRON_B

PWRON_B is an active-low input for triggering the system to power on or off. Normally, PWRON_B is connected to a power button.

Table 3-1. PWRON_B Electrical Characteristics

(Unless otherwise specified, Ta= +25°C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Input "H" Level	V_{IH_PWRON}	1.44	-	-	V	
Input "L" Level	V_{IL_PWRON}	-	-	0.40	V	

3.1.2. PMIC_ON_REQ

PMIC_ON_REQ is an active-high input for going to RUN state.

Table 3-2. PMIC_ON_REQ Electrical Characteristics

(Unless otherwise specified, Ta= +25°C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Input "H" Level	V_{IH_ONREQ}	1.44	-	-	V	
Input "L" Level	V_{IL_ONREQ}	-	-	0.40	V	

3.1.3. PMIC_STBY_REQ

PMIC_STBY_REQ is an active-high input for going to SUSPEND state.

Table 3-3. PMIC_STBY_REQ Electrical Characteristics

(Unless otherwise specified, Ta= +25 °C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Input "H" Level	$V_{IH\_STBYREQ}$	DVDD x 0.75	-	-	V	
Input "L" Level	$V_{IL\_STBYREQ}$	-	-	DVDD x 0.25	V	

3.1.4. WDOG_B

WDOG_B is an active-low input for triggering Cold Reset or Warm Reset.

Table 3-4. WDOG_B Electrical Characteristics

(Unless otherwise specified, Ta= +25 °C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Input "H" Level	V_{IH_WDOG}	DVDD x 0.75	-	-	V	
Input "L" Level	V_{IL_WDOG}	-	-	DVDD x 0.25	V	

3.1.5. RTC_RESET_B

RTC_RESET_B is an active-low output for RTC.

Table 3-5. RTC_RESET_B Electrical Characteristics

(Unless otherwise specified, Ta= +25 °C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output "L" Level Voltage	$V_{OL\_RTCRESET}$	-	-	DVDD x 0.2	V	I_{OL}=3 mA Sink
Output Off Leak Current	$I_{OLK\_RTCRESET}$	-1	-	+1	µA	

3.1.6. POR_B

POR_B is an active-low output for the reset of SoC.

Table 3-6. POR_B Electrical Characteristics

(Unless otherwise specified, Ta= +25 °C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output "L" Level Voltage	V_{OL_POR}	-	-	DVDD x 0.2	V	I_{OL}=3 mA Sink
Output Off Leak Current	I_{OLK_POR}	-1	-	+1	µA	

3.2. Power States

3.2.1. Power State Diagram

BD71850MWV has eight power states or modes: OFF, READY, SNVS, RUN, IDLE, SUSPEND, PWROFF and EMG. Figure 3-2 shows the state transition diagram along with the conditions to enter and exit each state.
READY_TO_SNVS Condition is described in 3.2.5.2. This condition is configurable by TRANS_COND0 registers.
SNVS_TO_RUN Condition is described in 3.2.5.3. This condition is configurable by TRANS_COND0 registers.
BD71850MWV has Thermal Shutdown, OCP, VR Fault, and VSYS_UVLO=0 as Emergency Shutdown events.
Emergency Shutdown Condition is described in 3.2.5.9. EMG_TO_READY Condition is described in 3.2.5.12. EMG_STAY Condition is described in 3.2.5.13.
BD71850MWV has WDOG_B, SWRESET, and PWRON_B long detection as Cold Reset events. COLD_RESET Condition is described in 3.2.4.1. After cold reset events or PMIC_ON_REQ=0, BD71850MWV is configurable that it returns to READY or SNVS state. POFF_TO_READY Condition is described in 3.2.5.16. POFF_TO_SNVS Condition is described in 3.2.5.17. Concerning VSYS_UVLO and INTLDO1P5_UVLO, please refer to 2.5.

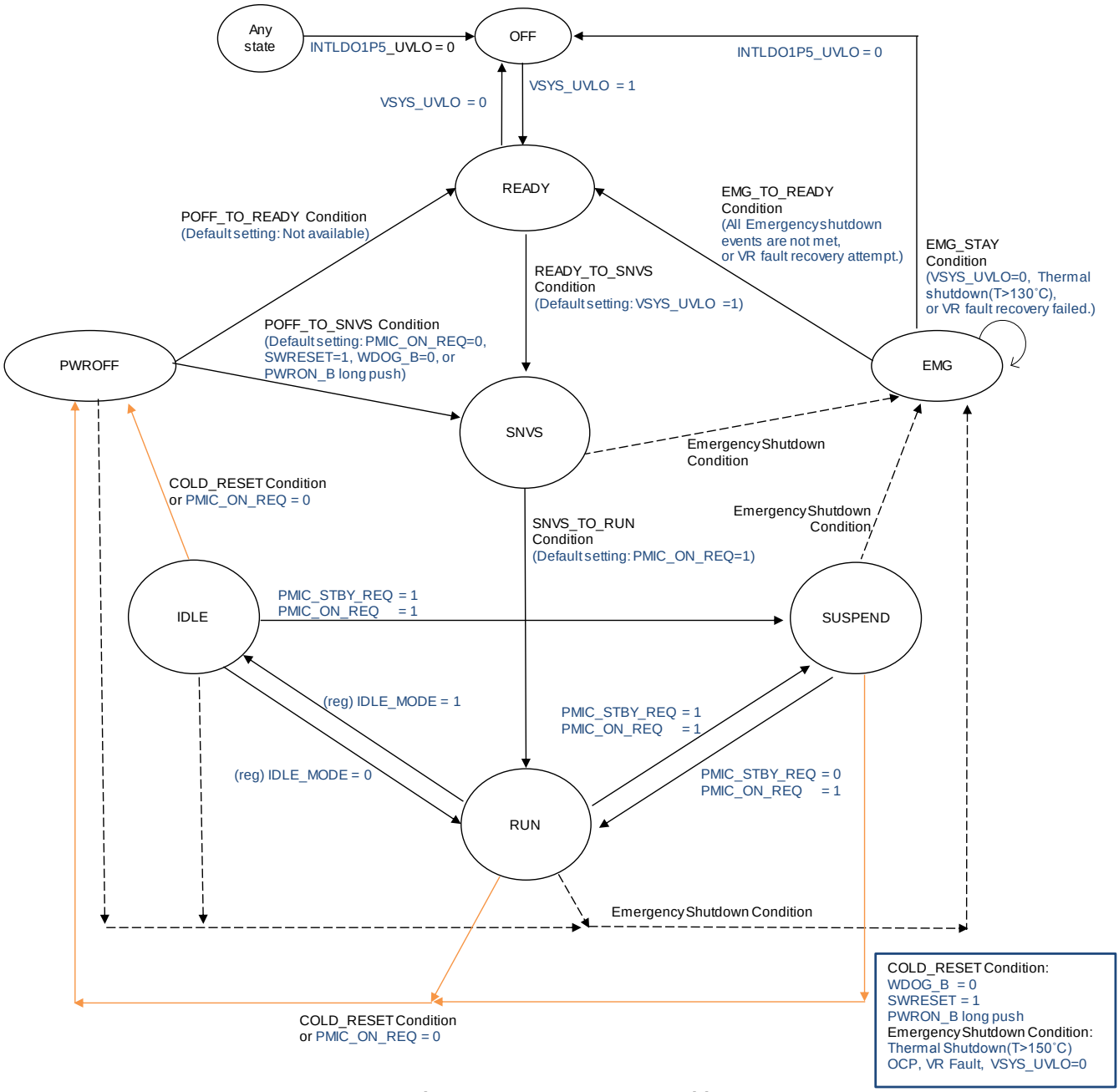


Figure 3-2. Power State Transition

3.2.2. Power State Register

The POW_STATE register shows current power state and power sub state in Table 3-7. The power sub state definition is illustrated in Figure 3-3.

Table 3-7. POW_STATE – Power State Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
POW_STATE	R	POW_ST[3:0]				-	-	POW_SUB[1:0]		0x00	0x2D

Bit	Name	Function	Initial
D[7:4]	POW_ST[3:0]	This bit field shows current power state. 0x0 = OFF 0x1 = READY 0x2 = SNVS 0x8 = RUN 0x9 = IDLE 0xA = SUSPEND 0xB = PWROFF 0xC = EMG	0000
D[1:0]	POW_SUB[1:0]	This bit field shows current power sub state. 00 = Stable 01 = Up 10 = Down 11 = Counting Cold Reset duration time (set by PONT[3:0])	00

3.2.2. Power State Register – continued

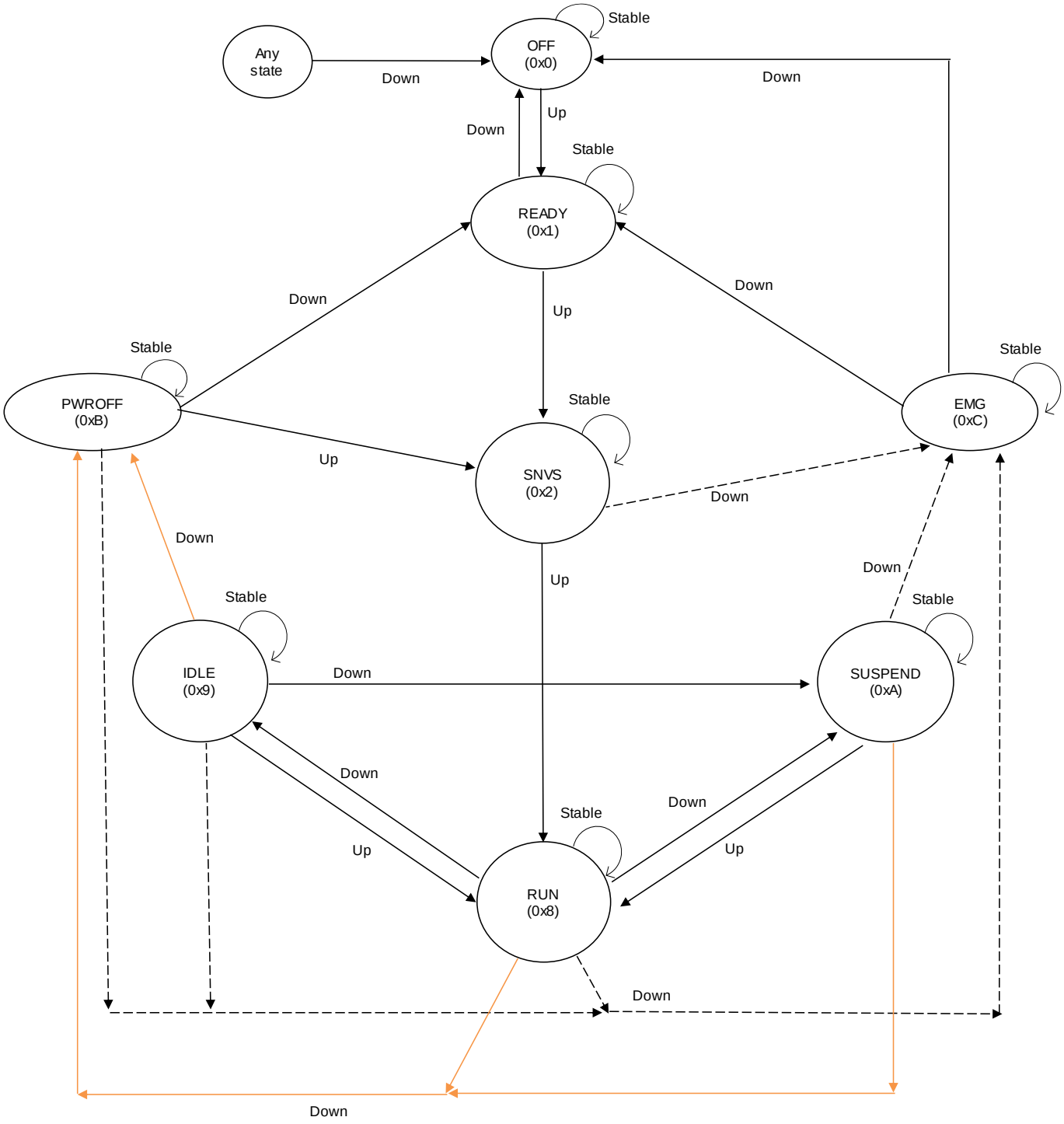


Figure 3-3. Power Sub State Definition

3.2.3. Power State Definition

(a) OFF state

BD71850MWV is in OFF state when INTLDO1P5_UVLO is detected. If INTLDO1P5_UVLO is 0, the data in all registers are reset to their default values.
To exit this state, VSYS voltage must exceed 3.0 V (VSYS_UVLO = 1)

(b) READY state

In this state, VSYS voltage is over 3.0V. When power state transitions from OFF state to READY state, OTP data will only be loaded to registers with "Yes" in "OTP" column of Register Map (Table 1-4). When power state transitions from PWROFF or EMG state to READY state, OTP data will only be loaded to registers with reset condition during READY state and "Yes" condition in "OTP" column. This OTP loading can be skipped depending on the value of RELOAD_REG in PWRCTRL0 register.

(c) SNVS state

If READY_TO_SNVS condition is satisfied, the power state changes to SNVS state. In this state, LDO1(NVCC_SNVS) and LDO2(VDD_SNVS) are turned on as shown in Table 3-8.

(d) RUN state

If SNVS_TO_RUN condition is satisfied, the power state changes to RUN state. In this state, the VR's shown in Table 3-8 are turned ON.
The voltage of BUCK1(VDD_SOC, VDDA_0V8, PHY_0V8) depends on BUCK1_VOLT_RUN register.
The voltage of BUCK2(VDD_ARM) depends on BUCK2_VOLT_RUN register.

(e) IDLE state

If IDLE_MODE in PWRCTRL1 register is set to 1, the power state changes to IDLE state. The voltage of BUCK1(VDD_SOC, VDDA_0V8, PHY_0V8) depends on BUCK1_VOLT_IDLE register. The voltage of BUCK2(VDD_ARM) depends on BUCK2_VOLT_IDLE register.

(f) SUSPEND state

If PMIC_STBY_REQ is set to 1, the power state changes to SUSPEND state. The voltage of BUCK1(VDD_SOC, VDDA_0V8, PHY_0V8) depends on BUCK1_VOLT_SUSP register.

(g) EMG state

If Emergency Shutdown Condition is satisfied, the power state changes to EMG state. In this state, all VR's are OFF.

(h) PWROFF state

If COLD_RESET Condition is satisfied or PMIC_ON_REQ is reset to 0, the power state changes to PWROFF state. In this state, all VR's except LDO1(NVCC_SNVS) and LDO2(VDD_SNVS) are OFF. The next state of PWROFF is either READY or SNVS. TRANS_COND1[3:0] values decide which power state to go.

3.2.3. Power State Definition – continued

Table 3-8. Voltage Rails ON/OFF for Respective Power State

VR No.	Function	Rail Name	Power State							
			OFF	READY	SNVS(Note)	SUSPEND(Note)	IDLE(Note)	RUN(Note)	PWROFF	EMG
VR1	NVCC_SNVS	LDO1	OFF	OFF	ON	ON	ON	ON	ON/OFF	OFF
VR2	VDD_SNVS	LDO2	OFF	OFF	ON	ON	ON	ON	ON/OFF	OFF
VR3	VDD_SOC, VDDA_0V8, PHY_0V8, VDD_DRAM, VDD_GPU	BUCK1	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR4	VDD_ARM	BUCK2	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
VR5	-	-	-	-	-	-	-	-	-	-
VR6	-	-	-	-	-	-	-	-	-	-
VR7	-	BUCK5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
VR8	VDDA_1V8, VDDA_DRAM	LDO3	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR9	-	LDO4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
VR10	NVCC_3V3	BUCK6	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR11	NVCC_1V8	BUCK7	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR12	NVCC_DRAM	BUCK8	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR13	-	LDO5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
VR14	VDD_PHY_1V2	LDO6	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
VR15	-	-	-	-	-	-	-	-	-	-
VR16	NVCC_SD2	MUXSW	OFF	OFF	OFF	ON	ON	ON	OFF	OFF

(Note) ON/OFF setting of each VR at SNVS/SUSPEND/IDLE/RUN state can be configured by OTP.

3.2.4. Power State Control Events

3.2.4.1. Reset Event

BD71850MWV has Cold and Warm resets.

Cold reset initiates POR_B asserted to L and power rails are turned off. Then, the power state changes to either READY state or SNVS state. Next, the power state returns to RUN state automatically.

Warm reset initiates POR_B asserted to L for 1 ms. It does not affect the on/off status of all power rails. Warm reset does not initiate the power state transition.

BD71850MWV has three reset sources as follows.
- PWRON_B terminal is set H to L. (PWRON_B Long Push reset)
- WDOG_B terminal is set H to L. (WDOG_B reset)
- SWRESET in SWRESET register is set 0 to 1 (Software reset)

The cold or warm reset selection setting is shown in Table 3-9.
The details of the two registers related to the setting are shown in Table 3-10 and Table 3-11.

3.2.4.1. Reset Event – continued

Table 3-9. Setting of Cold or Warm Reset Selection

Reset Source	Register Name	Register Bit Name	Value	Cold/Warm Reset or No Reset
PWRON_B Long Push	PWRCTRL0	DEBUG_STATE[1:0]	10 (default)	Cold reset
			11	Warm reset
			00 or 01	No reset action
WDOG_B	PWRCTRL0	WDOGB_SEL[1:0]	10 (default)	Cold reset
			11	Warm reset
			00 or 01	No reset action
Software	SWRESET	SWRESET_SEL[1:0]	10 (default)	Cold reset
			11	Warm reset
			00 or 01	No reset action

Table 3-10. SWRESET - Software Reset Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
SWRESET	R/W	-	-	-	-	-	SWRESET_SEL[1:0]		SWRESET	0x04	0x01

Bit	Name	Function	Initial
D[2:1]	SWRESET_SEL[1:0]	Select Cold reset, Warm reset or No reset action when SWRESET bit (D[0]) is set to 1. 00 = No reset action 01 = No reset action 10 = Cold reset 11 = Warm reset	10
D[0]	SWRESET	0 – No action 1 – Initiates Cold Reset or Warm Reset in accordance with SWRESET_SEL bit. Writing 1 to SWRESET bit, then SWRESET bit is automatically cleared to 0 when Cold Reset or Warm Reset operation is completed. Writing 1 to SWRESET bit can be done when Power State = RUN, IDLE and SUSPEND.	0

Table 3-11. PWRCTRL0 - Power Control 0 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRCTRL0	R/W	DEBUG_STATE[1:0]		RELOAD_ REG	-	-	-	WDOGB_SEL[1:0]		0xA2	0x03

Bit	Name	Function	Initial
D[7:6]	DEBUG_STATE[1:0]	Select Cold reset, Warm reset or No reset action when PWRON_B long push is detected. 00 = No reset action 01 = No reset action 10 = Cold reset 11 = Warm reset	10
D[5]	RELOAD_REG	Select OTP configurable registers initialization when the power state goes through READY state. 0 = No initialization 1= Reload OTP registers and set to initial value	1
D[1:0]	WDOGB_SEL[1:0]	Select Cold reset, Warm reset or No reset action when WDOG_B is asserted to 0. 00 = No reset action 01 = No reset action 10 = Cold reset 11 = Warm reset	10

3.2.4.2. Emergency Shutdown Event

There are four Emergency Shutdown Events as follows:

• Thermal Shutdown (Thermal Protection)

If the die temperature surpasses 150ºC, the thermal protection circuit will shut down all VR's to avoid damage. This detection is not valid at OFF, READY and SNVS state.

• OCP

If the OCP is triggered in any VR's, all VR's are turned off.

• VR Fault

If the voltage of VR is not within the regular range, all VR's are turned off.

• VSYS_UVLO = 0

If the VSYS_UVLO = 0, Emergency Shutdown sequence is initiated.

3.2.5. Power State Transitions

3.2.5.1. OFF to READY

Table 3-12 shows the conditions for exiting OFF state. "VSYS_UVLO = 1" is necessary.

Table 3-12. Conditions from OFF to READY state

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) VSYS Voltage Up from 0 V or 2.7 V	VSYS_UVLO = 1 (VSYS > 3.0 V)	READY	VSYS Insertion or VSYS recovery from 2.7 V

3.2.5.2. READY to SNVS

There are six event triggers for shifting from READY to SNVS as shown in Table 3-13. The event trigger of VSYS_UVLO, PMIC_ON_REQ, PWRON_B Short Push, and PWRON_B Long Push are configurable to be valid or invalid by TRANS_COND0 registers. VSYS_UVLO condition is valid with default setting.

Table 3-13. Conditions from READY to SNVS

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) VSYS_UVLO	VSYS_UVLO = 1	SNVS	No other event is necessary. Valid with default setting
2) PMIC_ON_REQ	VSYS_UVLO = 1 and PMIC_ON_REQ = 1	SNVS	Invalid with default setting
3) PWRON_B Short Push	VSYS_UVLO = 1 and PWRON_B = 0 ==> Short Push Detection	SNVS	Invalid with default setting
4) PWRON_B Long Push	VSYS_UVLO = 1 and PWRON_B = 0 ==> Long Push Detection	SNVS	Invalid with default setting
5) Cold Reset Sequence	VSYS_UVLO = 1 and Cold_Reset_flag = 1	SNVS	On the way back to RUN state in Cold Reset sequence
6) VR Fault Recovery Attempt	VSYS_UVLO = 1 and VR Fault Recovery	SNVS	

1) VSYS_UVLO

The power state shifts to SNVS if VSYS_UVLO = 1 as shown in Figure 3-4. No other conditions are necessary.

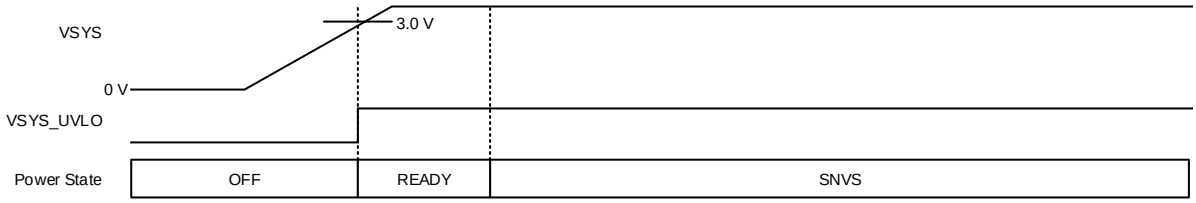


Figure 3-4. VSYS Condition for moving to SNVS

2) PMIC_ON_REQ

The power state shifts to SNVS if PMIC_ON_REQ = 1 as shown in Figure 3-5.

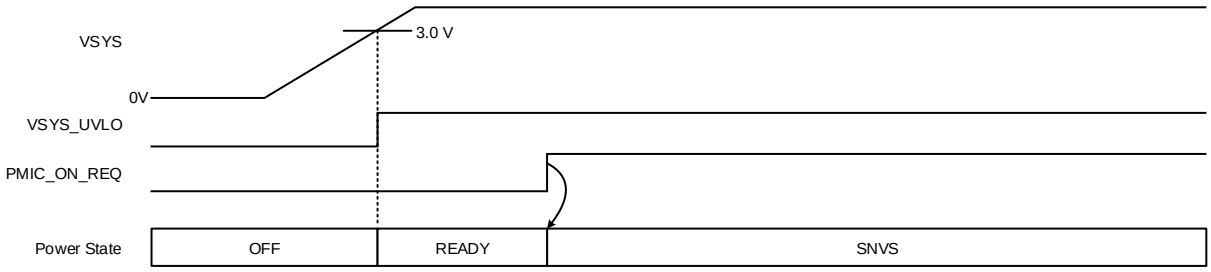


Figure 3-5. PMIC_ON_REQ Condition for moving to SNVS

3.2.5.2. READY to SNVS – continued

3) PWRON_B Short Push

The power state shifts to SNVS if PWRON_B Short Push is detected as shown in Figure 3-6.

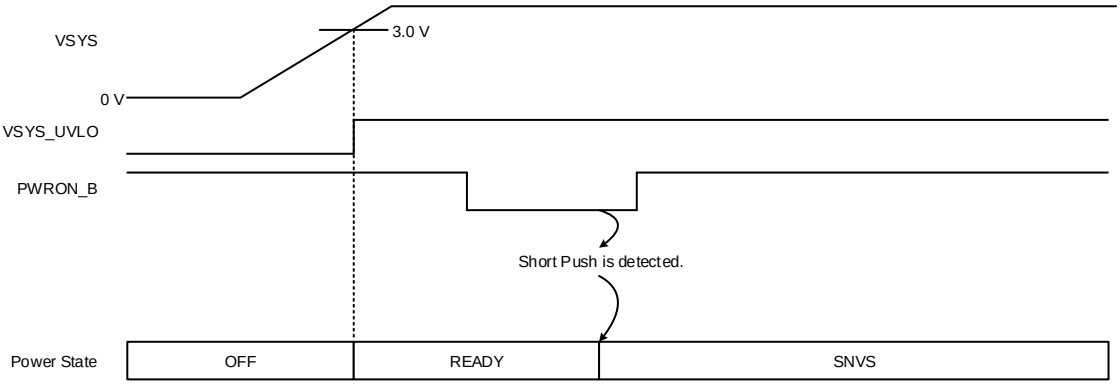


Figure 3-6. PWRON_B Short Push Condition for moving to SNVS

4) PWRON_B Long Push

The power state shifts to SNVS if PWRON_B Long Push is detected as shown in Figure 3-7.

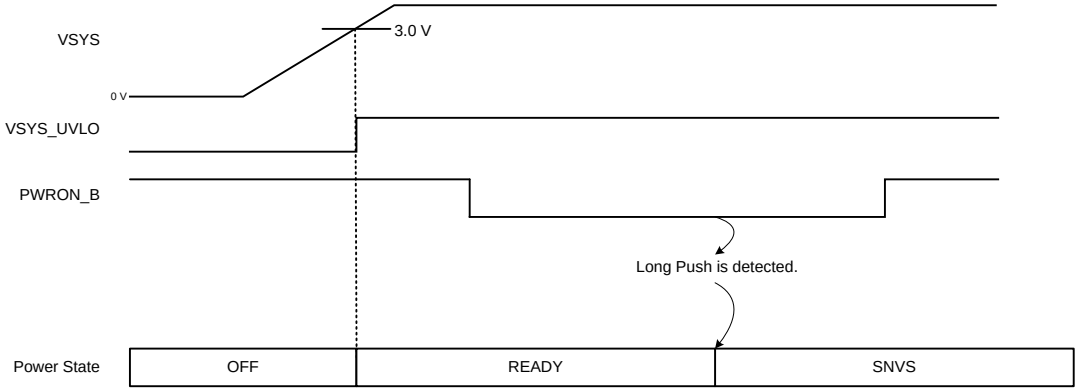


Figure 3-7. PWRON_B Long Push Condition for moving to SNVS

5) Cold Reset

The power state shifts to SNVS if Cold_Reset_flag = 1 as shown in Figure 3-8.

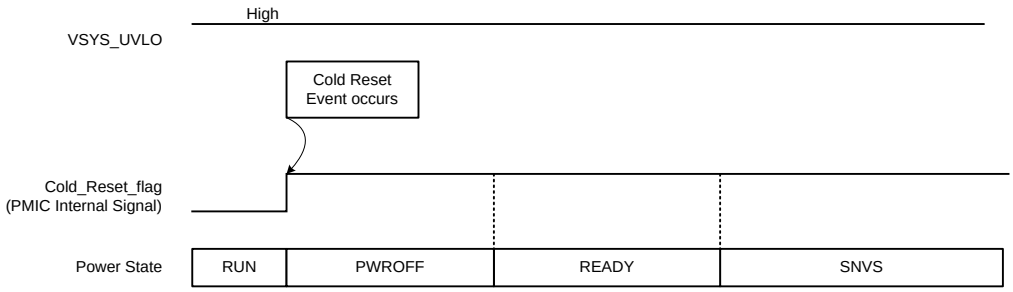


Figure 3-8. Cold Reset Condition for moving to SNVS

3.2.5.2. READY to SNVS – continued

6) VR Fault Recovery Attempt
Please see 3.2.5.10.

It is possible to use each four event triggers such as:
VSYS_UVLO,
PMIC_ON_REQ,
PWRON_B Short Push and
PWRON_B Long Push
These triggers are configurable to use them respectively by D[3:0] in TRANS_COND0 register as shown in Table 3-14.

Table 3-14. TRANS_COND0 - Transition Condition Select 0 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
TRANS_COND0	R/W	C1_ VSYS_3P0_ ONLY_EN	C1_ PMIC_ON_ REQ_EN	C1_ SHORT_ PUSH_EN	C1_ LONG_ PUSH_EN	C0_ VSYS_3P0_ ONLY_EN	C0_ PMIC_ON_ REQ_EN	C0_ SHORT_ PUSH_EN	C0_ LONG_ PUSH_EN	0x48	0x1F

Bit	Name	Function	Initial
D[7]	C1_VSYS_3P0_ONLY_EN	Select only VSYS_UVLO = 1 as SNVS ==> RUN transition condition or not 0 = VSYS_UVLO = 1 is not used as the condition 1 = VSYS_UVLO = 1 is used as the condition	0
D[6]	C1_PMIC_ON_REQ_EN	Select PMIC_ON_REQ as SNVS ==> RUN transition condition or not 0 = PMIC_ON_REQ is not used as the condition 1 = PMIC_ON_REQ is used as the condition	1
D[5]	C1_SHORT_PUSH_EN	Select PWRON_B Short Push as SNVS ==> RUN transition condition or not 0 = PWRON_B Short Push is not used as the condition 1 = PWRON_B Short Push is used as the condition	0
D[4]	C1_LONG_PUSH_EN	Select PWRON_B Long Push as SNVS ==> RUN transition condition or not 0 = PWRON_B Long Push is not used as the condition 1 = PWRON_B Long Push is used as the condition	0
D[3]	C0_VSYS_3P0_ONLY_EN	Select only VSYS_UVLO = 1 as READY ==> SNVS transition condition or not 0 = VSYS_UVLO = 1 is not used as the condition 1 = VSYS_UVLO = 1 is used as the condition	1
D[2]	C0_PMIC_ON_REQ_EN	Select PMIC_ON_REQ as READY ==> SNVS transition condition or not 0 = PMIC_ON_REQ is not used as the condition 1 = PMIC_ON_REQ is used as the condition	0
D[1]	C0_SHORT_PUSH_EN	Select PWRON_B Short Push as READY ==> SNVS transition condition or not 0 = PWRON_B Short Push is not used as the condition 1 = PWRON_B Short Push is used as the condition	0
D[0]	C0_LONG_PUSH_EN	Select PWRON_B Long Push as READY ==> SNVS transition condition or not 0 = PWRON_B Long Push is not used as the condition 1 = PWRON_B Long Push is used as the condition	0

3.2.5.3. SNVS to RUN

There are six event triggers for shifting from SNVS to RUN as shown in Table 3-15. The event trigger of VSYS_UVLO=1 PMIC_ON_REQ, PWRON_B Short Push, and PWRON_B Long Push are configurable to be valid or invalid by TRANS_COND0 registers. PMIC_ON_REQ condition is valid with default setting.

Table 3-15. Conditions from SNVS to RUN

Event Trigger	Conditions *(Note)* (All must be satisfied per Event Trigger)	Next State	Notes
1) VSYS_UVLO	VSYS_UVLO = 1	RUN	No other event is necessary. Invalid with default setting
2) PMIC_ON_REQ	VSYS_UVLO = 1 and PMIC_ON_REQ = 1	RUN	Valid with default setting
3) PWRON_B Short Push	VSYS_UVLO = 1 and PWRON_B = 0 ==> Short Push Detection	RUN	Invalid with default setting
4) PWRON_B Long Push	VSYS_UVLO = 1 and PWRON_B = 0 ==> Long Push Detection	RUN	Invalid with default setting
5) Cold Reset Sequence	VSYS_UVLO = 1 and Cold_Reset_flag = 1	RUN	On the way back to RUN state in Cold Reset sequence
6) VR Fault Recovery Attempt	VSYS_UVLO = 1 and VR Fault Recovery	RUN	

(Note) Die Temperature must be less than 150 ºC.

1) VSYS_UVLO

The power state shifts to RUN if VSYS_UVLO = 1 as shown in Figure 3-9. No other condition is required.

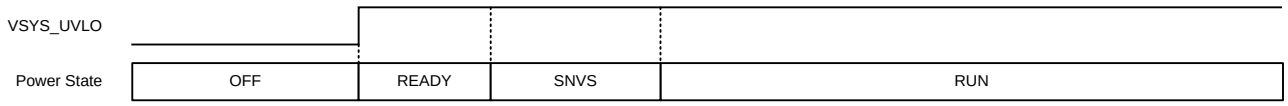


Figure 3-9. VSYS Condition for moving to RUN

2) PMIC_ON_REQ

The power state shifts to RUN if PMIC_ON_REQ = 1 as shown in Figure 3-10.

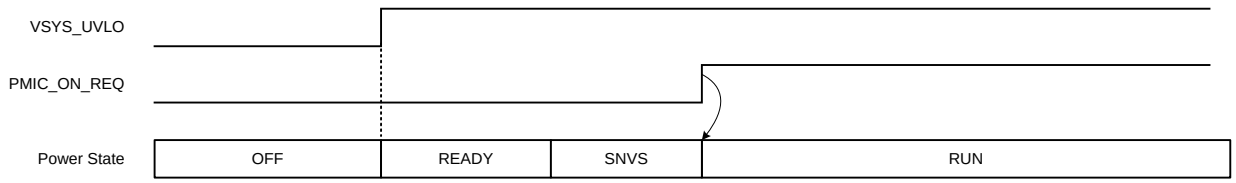


Figure 3-10. PMIC_ON_REQ Condition for moving to RUN

3.2.5.3. SNVS to RUN – continued

3) PWRON_B Short Push

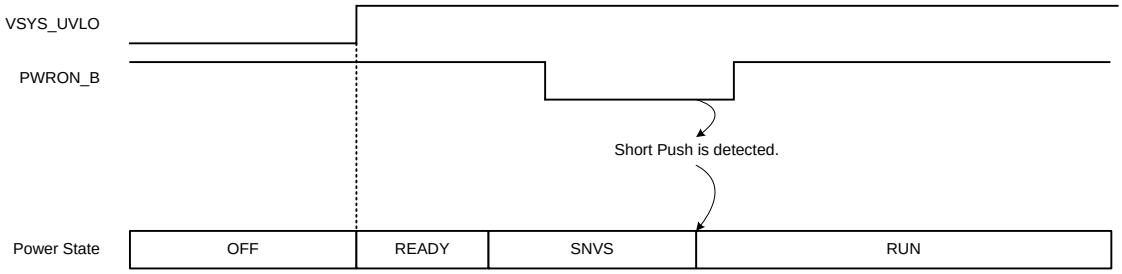


Figure 3-11. PWRON_B Short Push Condition for moving to RUN

4) PWRON_B Long Push

The power state shifts to RUN if PWRON_B Long Push is detected as shown in Figure 3-12.

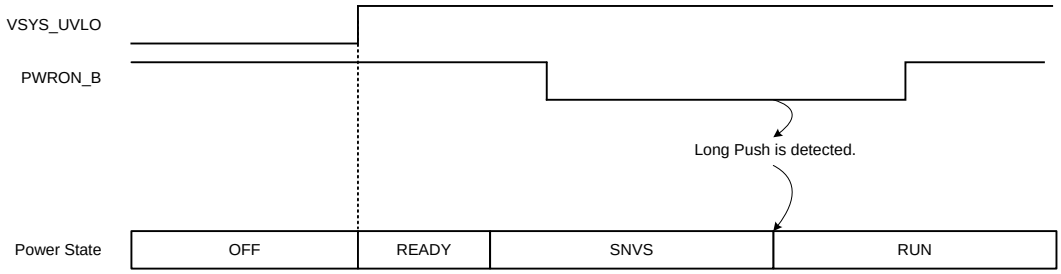


Figure 3-12. PWRON_B Long Push Condition for moving to RUN

5) Cold Reset

The power state shifts to RUN if Cold_Reset_flag = 1 as shown in Figure 3-13.

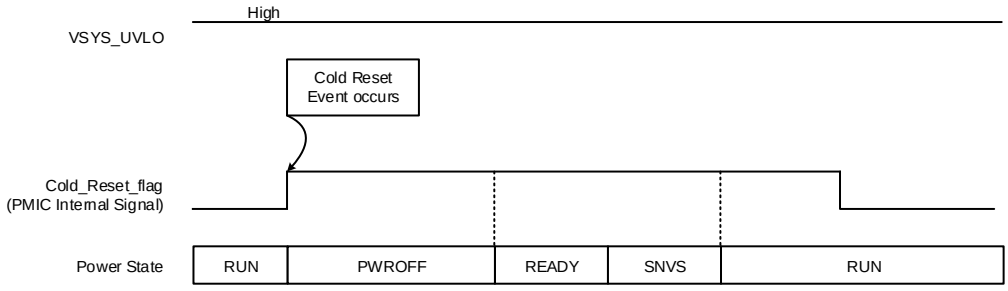


Figure 3-13. Cold Reset Condition for moving to RUN

6) VR Fault Recovery Attempt

Please see 3.2.5.10.

It is possible to use each four event triggers such as:
VSYS_UVLO,
PMIC_ON_REQ,
PWRON_B Short Push and
PWRON_B Long Push
These triggers are configurable to use them respectively by D[7:4] in TRANS_COND0 register as shown in Table 3-14.

3.2.5.4. RUN to IDLE

Table 3-16 shows the conditions for shifting from RUN to IDLE. The details of PWRCTRL1 register were described in Table 3-17.

Table 3-16. Conditions from RUN to IDLE

Event Trigger	Conditions *(Note)* (All must be satisfied)	Next State	Notes
Set IDLE_MODE (PWRCTRL1 register) = 1	PMIC_STBY_REQ = 0	IDLE	Register Write Operation
	PMIC_ON_REQ = 1		
	Set (reg) IDLE_MODE = 1		

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

Table 3-17. PWRCTRL1 - Power Control 1 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRCTRL1	R/W	-	-	-	-	-	-	-	IDLE_ MODE	0x00	0x04

Bit	Name	Function	Initial
D[0]	IDLE_MODE	Control power state transition between RUN and IDLE 0 = Exit IDLE and back to RUN, or indicates power state = except IDLE 1 = Enter IDLE from RUN, or indicates power state = IDLE Note : this bit automatically returns to 0 when power state enters PWROFF, EMG and SUSPEND.	0

3.2.5.5. IDLE to RUN

Table 3-18 shows the conditions for shifting from IDLE to RUN.

Table 3-18. Conditions from IDLE to RUN

Event Trigger	Conditions *(Note)* (All must be satisfied)	Next State	Notes
Set IDLE_MODE (PWRCTRL1 register) = 0	PMIC_STBY_REQ = 0	RUN	Register Write Operation
	PMIC_ON_REQ = 1		
	Set (reg) IDLE_MODE = 0		

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

3.2.5.6. RUN to SUSPEND

Table 3-19 shows the conditions for shifting from RUN to SUSPEND.

Table 3-19. Conditions from RUN to SUSPEND

Event Trigger	Conditions *(Note)* (All must be satisfied)	Next State	Notes
PMIC_STBY_REQ	PMIC_STBY_REQ = 1	SUSPEND	
	PMIC_ON_REQ = 1		

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

3.2.5.7. SUSPEND to RUN

Table 3-20 shows the conditions for shifting from SUSPEND to RUN.

Table 3-20. Conditions from SUSPEND to RUN

Event Trigger	Conditions *(Note)* (All must be satisfied)	Next State	Notes
PMIC_STBY_REQ	PMIC_STBY_REQ = 0	RUN	
	PMIC_ON_REQ = 1		

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

3.2.5.8. IDLE to SUSPEND

Table 3-21 shows the conditions for shifting from IDLE to SUSPEND. IDLE_MODE in PWRCTRL1 register automatically returns to 0.

Table 3-21. Conditions from IDLE to SUSPEND

Event Trigger	Conditions(Note) (All must be satisfied)	Next State	Notes
PMIC_STBY_REQ	PMIC_STBY_REQ = 1 PMIC_ON_REQ = 1	SUSPEND	

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

3.2.5.9. Emergency Shutdown

There are four Emergency Shutdown events which are:
Thermal Shutdown (Thermal Protection)
OCP
VR Fault
VSYS_UVLO = 0 as shown in Table 3-22.

Table 3-22. Conditions from SNVS, RUN, IDLE, SUSPEND, PWROFF to EMG

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) Thermal Shutdown	Die Temperature > 150 ºC	EMG	Thermal Protection This protection is invalid at OFF, READY, and SNVS state
2) OCP	Any VR's OCP	EMG	
3) VR Fault	Any VR's out of the target voltage	EMG	
4) VSYS_UVLO = 0	VSYS_UVLO = 0	EMG	

The detail of VR Fault is described in 3.2.5.10.

3.2.5.10. VR Fault

BD71850MWV has VR fault detection function which monitors all relevant VR's of the system. The system is shut down when a monitored voltage rail goes out of the target voltage. Once the system has shut down, the system tries to boot up several times which is determined by RCVLMT[3:0] in RCVCFG register.
Table 3-23 shows the VR fault threshold and monitoring conditions. Even if one of output rails which are described "Y" in Table 3-23 are not used, output inductors and capacitors are needed. If they are not connected, PMIC would be shut down because of VR fault detection.

Table 3-23. VR FAULT threshold and monitoring condition

VR No.	Function	Rail Name	SNVS		SUSPEND		IDLE		RUN	
			Monitor Y/N	Voltage Target Range	Monitor Y/N	Voltage Target Range	Monitor Y/N	Voltage Target Range	Monitor Y/N	Voltage Target Range
VR1	NVCC_SNVS	LDO1	Y	80% < LDO1	Y	80% < LDO1	Y	80% < LDO1	Y	80% < LDO1
VR2	VDD_SNVS	LDO2	Y	80% < LDO2	Y	80% < LDO2	Y	80% < LDO2	Y	80% < LDO2
VR3	VDD_SOC, VDDA_0V8, PHY_0V8	BUCK1	N	-	Y	80% < BUCK1 < 130%	Y	80% < BUCK1 < 130%	Y	80% < BUCK1 < 130%
VR4	VDD_ARM	BUCK2	N	-	N	-	Y	80% < BUCK2 < 130%	Y	80% < BUCK2 < 130%
VR5	-	-	-	-	-	-	-	-	-	-
VR6	-	-	-	-	-	-	-	-	-	-
VR7	-	BUCK5	N	-	N	-	N	-	N	-
VR8	VDDA_1V8, VDDA_DRAM	LDO3	N	-	Y	80% < LDO3	Y	80% < LDO3	Y	80% < LDO3
VR9	-	LDO4	N	-	N	-	N	-	N	-
VR10	NVCC_3V3	BUCK6	N	-	Y	80% < BUCK6 < 130%	Y	80% < BUCK6 < 130%	Y	80% < BUCK6 < 130%
VR11	NVCC_1V8	BUCK7	N	-	Y	80% < BUCK7 < 130%	Y	80% < BUCK7 < 130%	Y	80% < BUCK7 < 130%
VR12	NVCC_DRAM	BUCK8	N	-	Y	80% < BUCK8 < 130%	Y	80% < BUCK8 < 130%	Y	80% < BUCK8 < 130%
VR13	-	LDO5	N	-	N	-	N	-	N	-
VR14	VDD_PHY_1V2	LDO6	N	-	Y	80% < LDO6	Y	80% < LDO6	Y	80% < LDO6
VR15	-	-	-	-	-	-	-	-	-	-
VR16	NVCC_SD	MUXSW	Not available	-	Not available	-	Not available	-	Not available	-

Y: VR output is monitored to trigger VR Fault Emergency Shutdown sequence.

N: Not monitored at default (If the VR is turned ON by changing the register setting, its output is monitored for the VR Fault event trigger)

3.2.5.10. VR Fault – continued

BD71850MWV monitors each rail. If a monitored VR goes out of the target voltage in a certain time, the system will shut down. When the system cannot shift to RUN state after Power ON sequence several times which is defined by RCVLMT[3:0] in RCVCFG register, the system stays at EMG state until INTLDO1P5_UVLO = 0.

If a VR is turned OFF by VR control registers (BUCK1, BUCK2, BUCK5 to BUCK8 and LDO1 to LDO6), VR fault of that VR is masked.

BD71850MWV has VR individual masking registers as shown in Table 3-25, Table 3-26 and Table 3-27. This masking function is used for mainly debugging in development phase.

Table 3-24. VRFAULTEN - VR FAULT ON/OFF Register: Debugging Purpose

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VRFAULTEN	R/W	-	-	-	-	-	-	-	VRFLTEN	0x01	0x21

Bit	Name	Function	Initial
D[0]	VRFLTEN	VR Fault enable bit 0 = VR Fault is disabled. 1 = VR Fault is enabled. This bit is used for debugging purpose.Please do not set 0x00 in normal operation.	1

Table 3-25. MVRFLTMASK0 - VR FAULT Mask 0 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MVRFLTMASK0	R/W	MBUCK8_ VOUTOKH	MBUCK8_ VOUTOKL	MBUCK7_ VOUTOKH	MBUCK7_ VOUTOKL	MBUCK6_ VOUTOKH	MBUCK6_ VOUTOKL	MBUCK5_ VOUTOKH	MBUCK5_ VOUTOKL	0x00	0x22

Bit	Name	Function	Initial
D[7]	MBUCK8_VOUTOKH	Masking bit of BUCK8 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[6]	MBUCK8_VOUTOKL	Masking bit of BUCK8 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[5]	MBUCK7_VOUTOKH	Masking bit of BUCK7 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[4]	MBUCK7_VOUTOKL	Masking bit of BUCK7 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[3]	MBUCK6_VOUTOKH	Masking bit of BUCK6 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[2]	MBUCK6_VOUTOKL	Masking bit of BUCK6 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[1]	MBUCK5_VOUTOKH	Masking bit of BUCK5 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[0]	MBUCK5_VOUTOKL	Masking bit of BUCK5 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0

3.2.5.10. VR Fault – continued

Table 3-26. MVRFLTMASK1 - VR FAULT Mask 1 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MVRFLTMASK1	R/W	-	-	-	-	MBUCK2_ VOUTOKH	MBUCK2_ VOUTOKL	MBUCK1_ VOUTOKH	MBUCK1_ VOUTOKL	0x00	0x23

Bit	Name	Function	Initial
D[3]	MBUCK2_VOUTOKH	Masking bit of BUCK2 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[2]	MBUCK2_VOUTOKL	Masking bit of BUCK2 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[1]	MBUCK1_VOUTOKH	Masking bit of BUCK1 130% threshold for target voltage 0 = monitoring 130% threshold 1 = masked 130% threshold	0
D[0]	MBUCK1_VOUTOKL	Masking bit of BUCK1 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0

Table 3-27. MVRFLTMASK2 - VR FAULT Mask 2 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MVRFLTMASK2	R/W	-	-	MLDO6_ VOUTOKL	MLDO5_ VOUTOKL	MLDO4_ VOUTOKL	MLDO3_ VOUTOKL	MLDO2_ VOUTOKL	MLDO1_ VOUTOKL	0x00	0x24

Bit	Name	Function	Initial
D[5]	MLDO6_VOUTOKL	Masking bit of LDO6 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[4]	MLDO5_VOUTOKL	Masking bit of LDO5 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[3]	MLDO4_VOUTOKL	Masking bit of LDO4 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[2]	MLDO3_VOUTOKL	Masking bit of LDO3 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[1]	MLDO2_VOUTOKL	Masking bit of LDO2 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0
D[0]	MLDO1_VOUTOKL	Masking bit of LDO1 80% threshold for target voltage 0 = monitoring 80% threshold 1 = masked 80% threshold	0

Following a VR Fault and an Emergency Shutdown sequence, BD71850MWV stays in READY state for a programmed time which is specified by RCVDT[3:0] of RCVCFG register. Power ON sequence is then initiated once RCVDT[3:0] time has elapsed.

To prevent an infinite loop of VR Fault induced power cycles, BD71850MWV limits the number of attempts to recover the system by RCVLMT[3:0] of RCVCFG register when these failures occur. Once BD71850MWV has attempted to recover from a VR Fault for a number of times which is specified by RCVLMT[3:0], the next VR Fault results in BD71850MWV staying in EMG state until INTLDO1P5_UVLO = 0.

The ability to reset RCVNUM register which tracks the number of VR Fault recovery attempts via I2C is supported. This will allow the SoC to reset this count value when needed.

3.2.5.10. VR Fault – continued

Table 3-28. RCVCFG - Recovery Configuration Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
RCVCFG	R/W	RCVLMT[3:0]				RCVDT[3:0]				0x4C	0x25

Bit	Name	Function	Initial
D[7:4]	RCVLMT[3:0]	The limit number of attempts to recover the system after a VR Fault occurred. 0000 = No recovery. BD71850MWV stays in EMG state until VSYS is triggered again. 0001 = 1 time 0010 = 2 times 0011 = 3 times 0100 = 4 times : 1110 = 14 times 1111 = No limit of attempts to recover	0100
D[3:0]	RCVDT[3:0]	The duration time during which BD71850MWV stays in READY state after a VR Fault event. BD71850MWV remains in READY state for the duration programmed here then BD71850MWV performs a Power ON sequence, if RCVLMT[3:0] is not 0x0 or 0xF and RCVLMT[3:0] is not equal to RCVNUM[3:0] of RCVNUM register. 0000 = 5 ms 0001 = 10 ms 0010 = 15 ms 0011 = 20 ms 0100 = 25 ms 0101 = 30 ms 0110 = 35 ms 0111 = 40 ms 1000 = 45 ms 1001 = 50 ms 1010 = 75 ms 1011 = 100 ms 1100 = 250 ms 1101 = 500 ms 1110 = 750 ms 1111 = 1500 ms	1100

Table 3-29. RCVNUM - Recovery Number Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
RCVNUM	R/W	-	-	-	-	RCVNUM[3:0]				0x00	0x26

Bit	Name	Function	Initial
D[3:0]	RCVNUM[3:0]	The number of attempts to recover the system after a VR Fault occurred. Once BD71850MWV has attempted to recover from a power failure times which is indicated in RCVLMT[3:0] in RCVCFG register, the next failure shall result in BD71850MWV staying in EMG state until VSYS is triggered again. When SoC writes RCVNUM register via I2C, then RCVNUM[3:0] is cleared to 0000. As a result, the tracking number of power failure recovery attempts is reset. Note : When RCVLMT[3:0] = 0xF (no limit of attempts to recover) and the number of attempt is over 0xF, RCVNUM[3:0] value is fixed to 0xF.	0000

3.2.5.10. VR Fault – continued

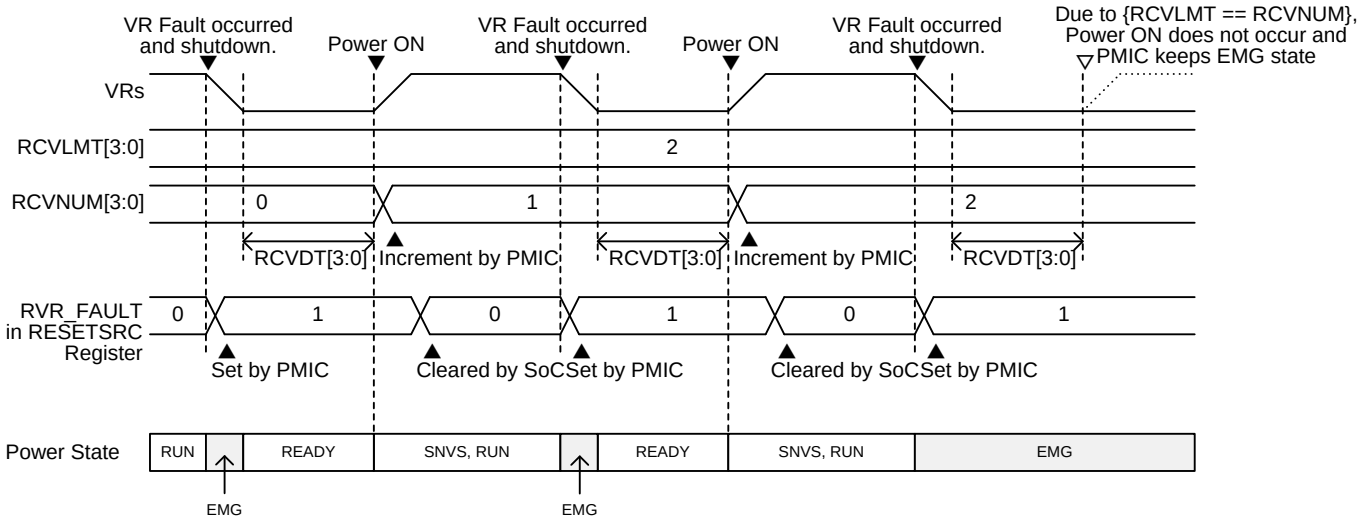


Figure 3-14. Example of VR Fault and Recovery Sequence (RCVLMT[3:0] = 2)

3.2.5.11. EMG to OFF

Table 3-30 shows the conditions for shifting from EMG to OFF. If INTLDO1P5_UVLO = 0 after entry to EMG, the power state immediately goes to OFF as shown in Figure 3-15.

Table 3-30. Conditions from EMG to OFF

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
VSYS Voltage Low	INTLDO1P5_UVLO = 0	OFF	

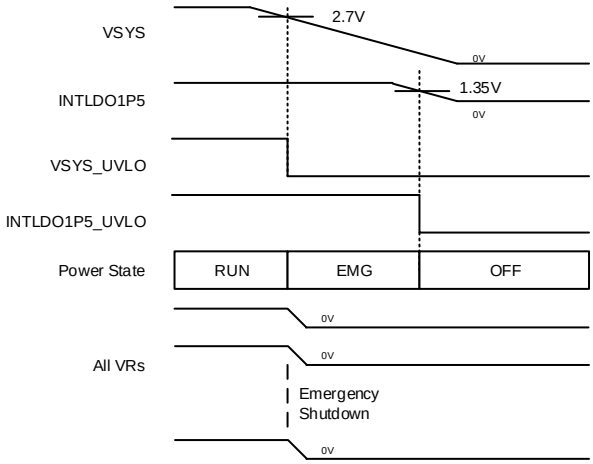


Figure 3-15. EMG to OFF Power State Transition

3.2.5.12. EMG to READY

Table 3-31 shows the conditions for shifting from EMG to READY. Basically, the power state can exit EMG when no emergency events are found as shown in Figure 3-14, Figure 3-16, and Figure 3-17.

Table 3-31. Conditions from EMG to READY

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) No Emergency Event	VSYS_UVLO = 1	READY	
	Die Temperature < 150 ºC		
	No OCP		
	No VR Fault		
2) VR Fault Recovery Attempt	VSYS_UVLO = 1	READY	
	Die Temperature < 150 ºC		
	During VR Fault Recovery Attempt		

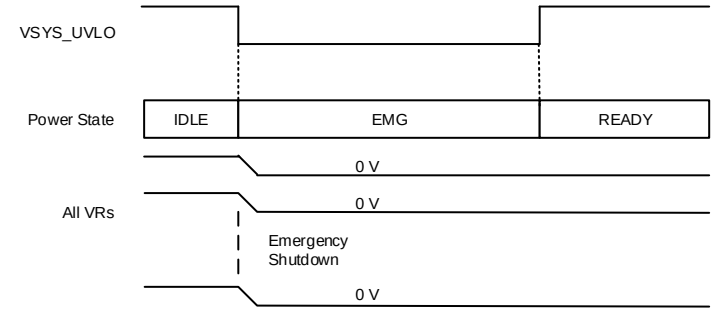


Figure 3-16. EMG to READY Power State Transition (VSYS_UVLO)

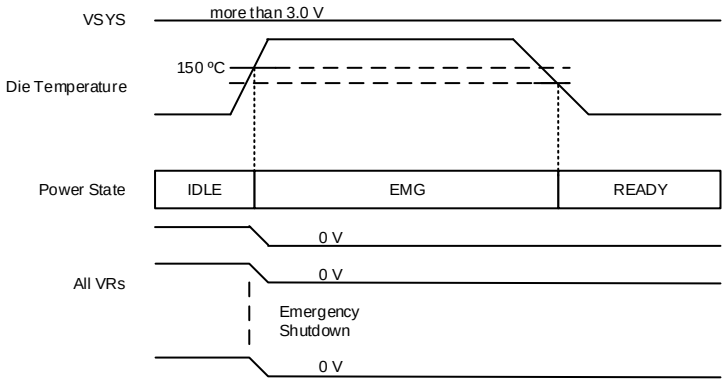


Figure 3-17. EMG to READY Power State Transition (Die Temperature)

3.2.5.13. EMG_STAY Condition

Table 3-32 shows the conditions for staying at EMG. Basically, the power state stays at EMG when emergency events are found as shown in Figure 3-14, Figure 3-16, and Figure 3-17.
Note: In case of 3) VR Fault Recovery Failure in Table 3-32; in order to exit EMG, VSYS voltage must be less than 2.7V and then the power state goes to OFF.

Table 3-32. Conditions for Stay at EMG

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) VSYS < 2.7 V	VSYS_UVLO = 0	EMG	
	INTLDO1P5_UVLO = 1		
2) Thermal Shutdown	Die Temperature > 150 ºC	EMG	Thermal Protection
	INTLDO1P5_UVLO = 1		
3) VR Fault Recovery Failure	VR Fault Recovery Attempt Failed	EMG	
	INTLDO1P5_UVLO = 1		

3.2.5.14. Warm Reset

Warm Reset is executed when the power state = RUN, IDLE and SUSPEND.
Warm Reset set POR_B = L for 1 ms as shown in Figure 3-18.
Please refer to the Table 3-9 for necessary register setting.

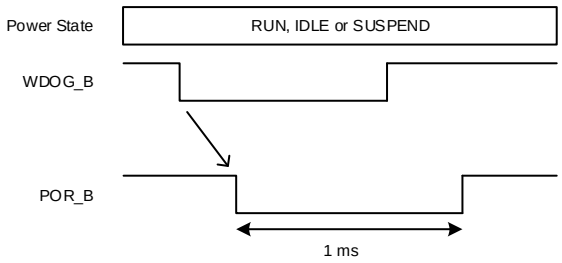


Figure 3-18. Warm Reset by WDOG_B

3.2.5.15. PWROFF

Table 3-33 shows the conditions for shifting from RUN, IDLE, SUSPEND to PWROFF.
When the power state is PWROFF, BD71850MWV runs Power OFF sequence and VR's are turned OFF in a defined sequential order.
In the end of the sequence, the on-off state of C32K_OUT, RTC_RESET_B, LDO2 and LDO1 depends on the setting of TRANS_COND1 register as shown in Table 3-34. The summary is shown in Table 3-35.

Table 3-33. Conditions from RUN, IDLE, SUSPEND to PWROFF

Event Trigger	Conditions (All must be satisfied per Event Trigger)	Next State	Notes
1) PWRON_B Long Push	PWRON_B = 0 ==> Long Push Detection	PWROFF	COLD_RESET event
2) WDOG_B	WDOG_B = 0	PWROFF	COLD_RESET event
3) Software Reset	Write 1 to SWRESET in SWRESET register	PWROFF	COLD_RESET event
4) PMIC_ON_REQ	PMIC_ON_REQ = 0	PWROFF	

(Note) Die Temperature must be less than 150 ºC. VSYS_UVLO = 1.

Table 3-34. TRANS_COND1 - Transition Condition Select 1 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
TRANS_COND1	R/W	PONT[3:0]				PWRON_ POFF_TO_ READY	WDOG_ POFF_TO_ READY	SWRST_ POFF_TO_ READY	ON_REQ_ POFF_TO_ READY	0xC0	0x20

Bit	Name	Function	Initial
D[7:4]	PONT[3:0]	COLD RESET duration during which the BD71850MWV stays in READY or SNVS in a COLD RESET event. The BD71850MWV remains in READY or SNVS for the duration programmed here then BD71850MWV performs a Power ON sequence. 0000 = 5 ms 0001 = 10 ms 0010 = 15 ms 0011 = 20 ms 0100 = 25 ms 0101 = 30 ms 0110 = 35 ms 0111 = 40 ms 1000 = 45 ms 1001 = 50 ms 1010 = 75 ms 1011 = 100 ms 1100 = 250 ms 1101 = 500 ms 1110 = 750 ms 1111 = 1500 ms	1100
D[3]	PWRON_ POFF_TO_READY	Set which power state to go after PWROFF triggered by PWRON_B Long Push 0 = to SNVS 1 = to READY	0
D[2]	WDOG_ POFF_TO_READY	Set which power state to go after PWROFF triggered by WDOG_B = 0 0 = to SNVS 1 = to READY	0
D[1]	SWRST_ POFF_TO_READY	Set which power state to go after PWROFF triggered by Software Reset 0 = to SNVS 1 = to READY	0
D[0]	ON_REQ_ POFF_TO_READY	Set which power state to go after PWROFF triggered by PMIC_ON_REQ = 0 0 = to SNVS 1 = to READY	0

3.2.5.15. PWROFF – continued

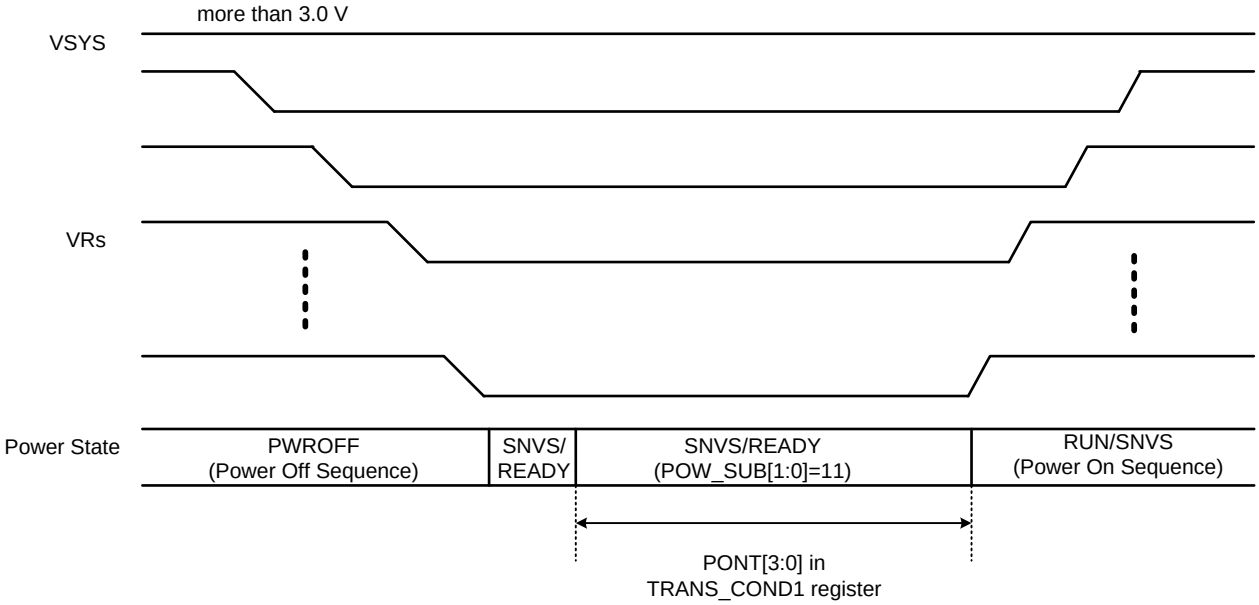


Figure 3-19. Cold Reset Duration Time set by PONT[3:0]

Table 3-35. VR Summary After Power OFF Sequence

PWROFF trigger	PWRON_ POFF_TO_ READY	WDOG_ POFF_TO_ READY	SWRST_ POFF_TO_ READY	ON_REQ_ POFF_TO_ READY	C32K_ OUT	RTC_ RESET_B	LDO2	LDO1
PWRON_B Long Push	0	-	-	-	On	High	On	On
	1	-	-	-	Off	Low	Off	Off
WDOG_B = 0	-	0	-	-	On	High	On	On
	-	1	-	-	Off	Low	Off	Off
Software Reset	-	-	0	-	On	High	On	On
	-	-	1	-	Off	Low	Off	Off
PMIC_ON_REQ = 0	-	-	-	0	On	High	On	On
	-	-	-	1	Off	Low	Off	Off

3.2.5.16. PWROFF to READY

After the completion of Power OFF sequence, the power state goes READY if the POFF_TO_READY = 1. This is in accordance with PWROFF trigger event in the TRANS_COND1 register.

3.2.5.17. PWROFF to SNVS

After the completion of Power OFF sequence, the power state goes SNVS if the POFF_TO_READY = 0. This is in accordance with PWROFF trigger event in the TRANS_COND1 register.

3.2.5.18. PWRON_B Functionality

The system has a button that can be used for triggering the system to power on or off. PWRON_B is an active-low input to BD71850MWV. Timer circuitry measures the length of time the button is pressed. Then the timer detects short push and long push events.

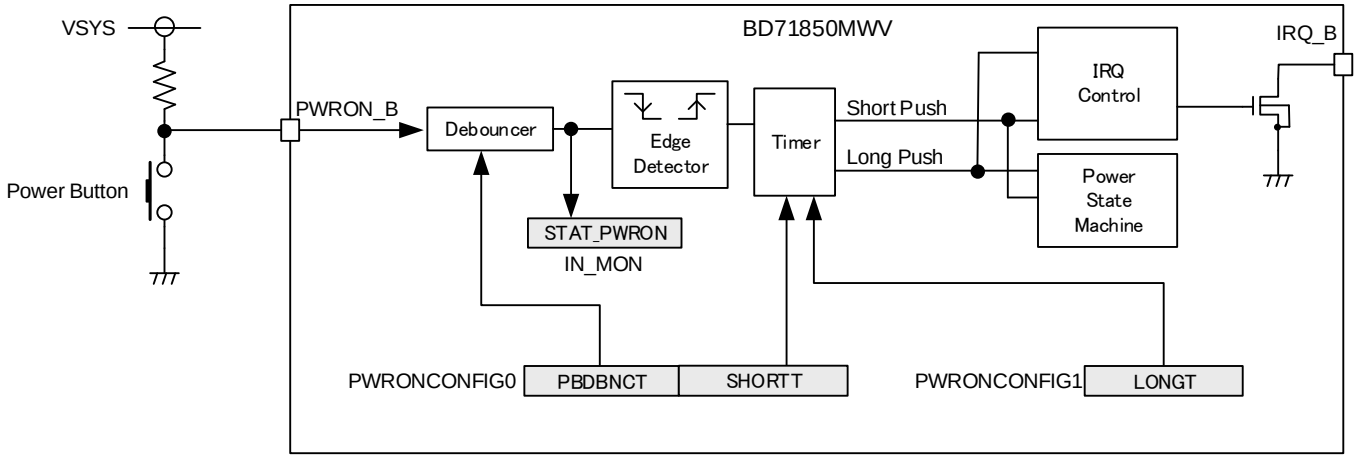


Figure 3-20. Power Button Block Diagram

Table 3-36. PWRONCONFIG0 - PWRON_B Configuration 0 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRONCONFIG0	R/W	-	-	PBDBNCT[1:0]		SHORTT[3:0]				0x16	0x27

Bit	Name	Function	Initial
D[5:4]	PBDBNCT[1:0]	PWRON_B Input Pin Debounce Time 00 = 10 ms 01 = 30 ms(default) 10 = 60 ms 11 = 100 ms	01
D[3:0]	SHORTT[3:0]	Short Push Timer : 0000 = 10 ms 0001 = 0.5 s 0010 = 1.0 s 0011 = 1.5 s 0100 = 2.0 s 0101 = 2.5 s 0110 = 3.0 s (default) 0111 = 3.5 s 1000 = 4.0 s 1001 = 4.5 s 1010 = 5.0 s 1011 = 5.5 s 1100 = 6.0 s 1101 = 6.5 s 1110 = 7.0 s 1111 = 7.5 s	0110

3.2.5.18. PWRON_B Functionality – continued

Table 3-37. PWRONCONFIG1 - PWRON_B Configuration 1 Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRONCONFIG1	R/W	-	-	-	-	LONGT[3:0]				0x00	0x28

Bit	Name	Function	Initial
D[3:0]	LONGT[3:0]	Long Push Timer : 0000 = 10 ms (default) 0001 = 1 s 0010 = 2 s 0011 = 3 s 0100 = 4 s 0101 = 5 s 0110 = 6 s 0111 = 7 s 1000 = 8 s 1001 = 9 s 1010 = 10 s 1011 = 11 s 1100 = 12 s 1101 = 13 s 1110 = 14 s 1111 = 15 s	0000

3.3. Power Sequence

3.3.1. Power ON Sequence

Figure 3-21 shows an example when TRANS_COND0 = 0x48, which are:

READY to SNVS condition: VSYS_UVLO = 1

SNVS to RUN condition: PMIC_ON_REQ

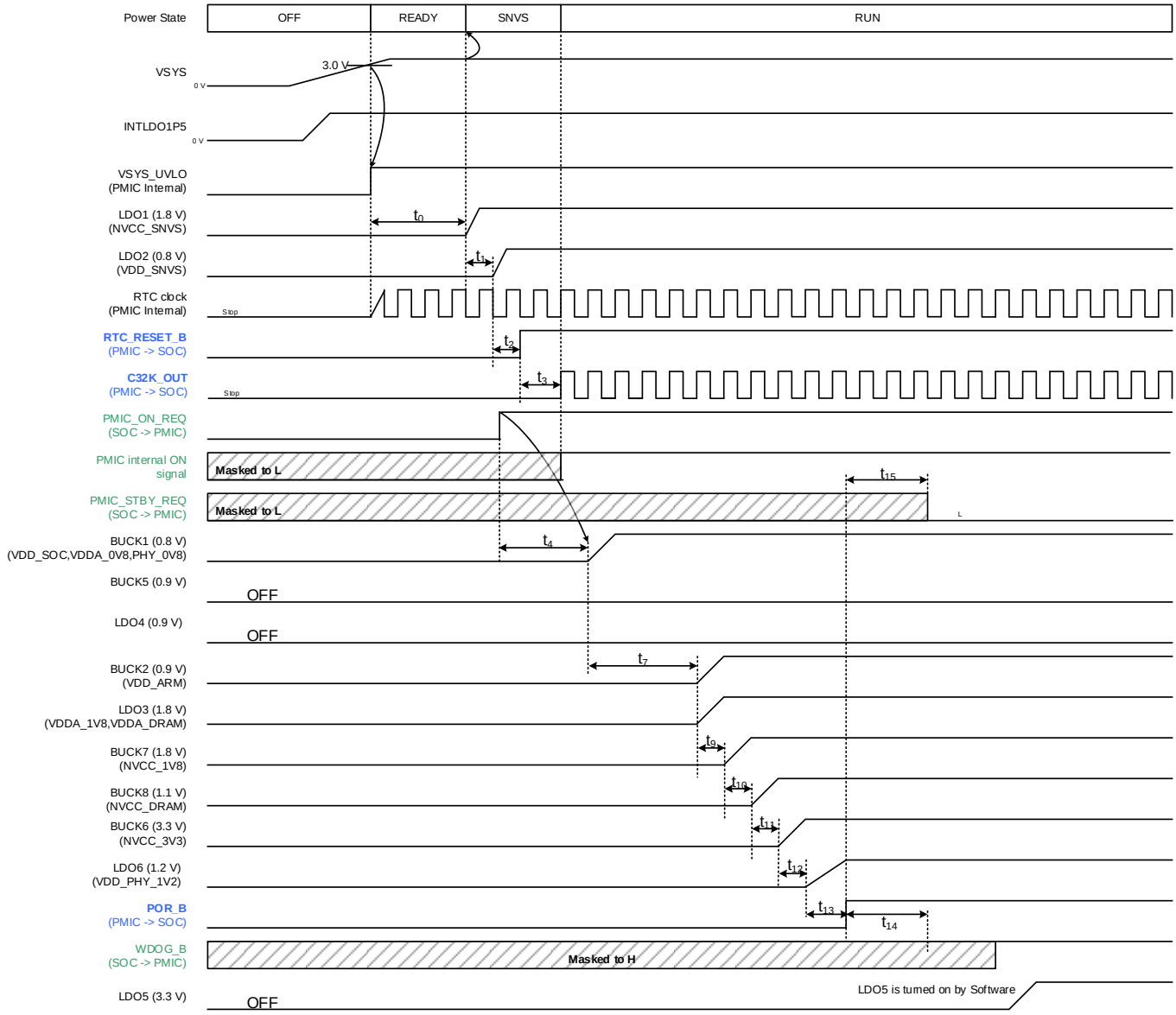


Figure 3-21. Power ON Sequence

3.3.1. Power ON Sequence – continued

Table 3-38. Power ON Sequence Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	VSYS = 3.0 V to LDO1 Assert Delay	0	20	22	ms
t_1	LDO1 Assert to LDO2 Assert Delay	0	2.0	2.4	ms
t_2	LDO2 Assert to RTC_RESET_B De-assert Delay	0	10	12	ms
t_3	RTC_RESET_B De-assert to C32K_OUT Output Delay	0	40	90	µs
t_4	PMIC_ON_REQ Assert to BUCK1 Assert Delay	0	0.20	12.49	ms
t_7	BUCK1 Assert to BUCK2 Assert Delay	0	4.0	4.8	ms
	BUCK1 Assert to LDO3 Assert Delay				
t_9	LDO3 Assert to BUCK7 Assert Delay	0	2.0	2.4	ms
t_{10}	BUCK7 Assert to BUCK8 Assert Delay	0	2.0	2.4	ms
t_{11}	BUCK8 Assert to BUCK6 Assert Delay	0	2.0	2.4	ms
t_{12}	BUCK6 Assert to LDO6 Assert Delay	0	2.0	2.4	ms
t_{13}	LDO6 Assert to POR_B De-assert Delay	0	20	22	ms
t_{14}	POR_B De-assert to WDOG_B Internal Mask Disabled	0	10	12	ms
t_{15}	POR_B De-assert to PMIC_STBY_REQ Internal Mask Disabled	0	10	12	ms

3.3.2. Power OFF Sequence

Figure 3-22 shows an example when triggered by PMIC_ON_REQ when ON_REQ_POFF_TO_READY = 0 in TRANS_COND1 register.

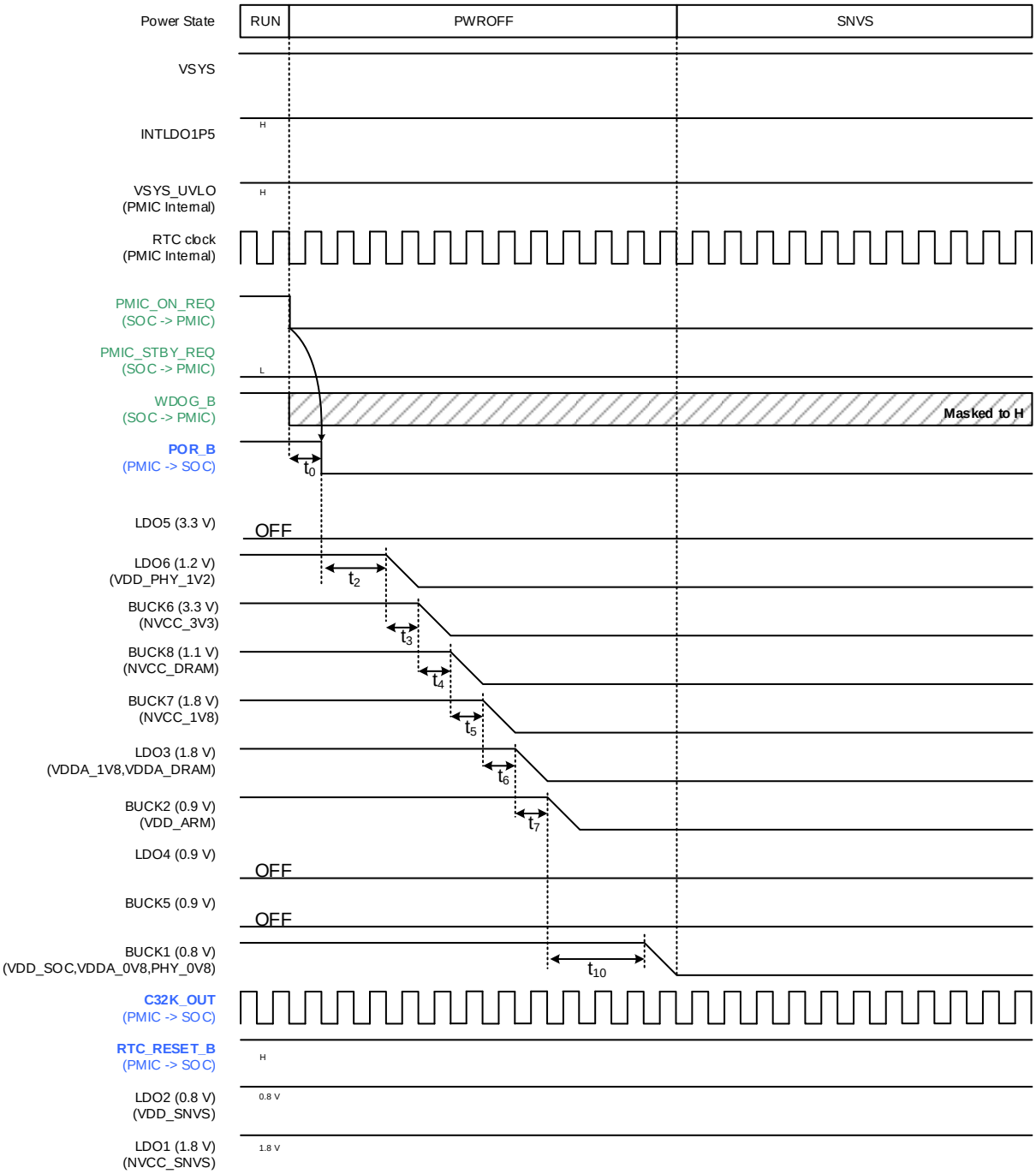


Figure 3-22. Power OFF Sequence (To SNVS)

3.3.2. Power OFF Sequence – continued

Table 3-39. Power OFF Sequence Timing Specification (To SNVS)

Symbol	Description	Min	Typ	Max	Unit
t_0	PMIC_ON_REQ De-assert to POR_B Assert Delay	0	120	200	µs
t_2	POR_B De-assert to LDO6 De-assert Delay	0	40	48	ms
t_3	LDO6 De-assert to BUCK6 De-assert Delay	0	10	12	ms
t_4	BUCK6 De-assert to BUCK8 De-assert Delay	0	10	12	ms
t_5	BUCK8 De-assert to BUCK7 De-assert Delay	0	10	12	ms
t_6	BUCK7 De-assert to LDO3 De-assert Delay	0	10	12	ms
t_7	LDO3 De-assert to BUCK2 De-assert Delay	0	10	12	ms
t_{10}	BUCK2 De-assert to BUCK1 De-assert Delay	0	30	36	ms

3.3.2. Power OFF Sequence – continued

Figure 3-23 shows an example when triggered by PMIC_ON_REQ when ON_REQ_POFF_TO_READY = 1 in TRANS_COND1 register.

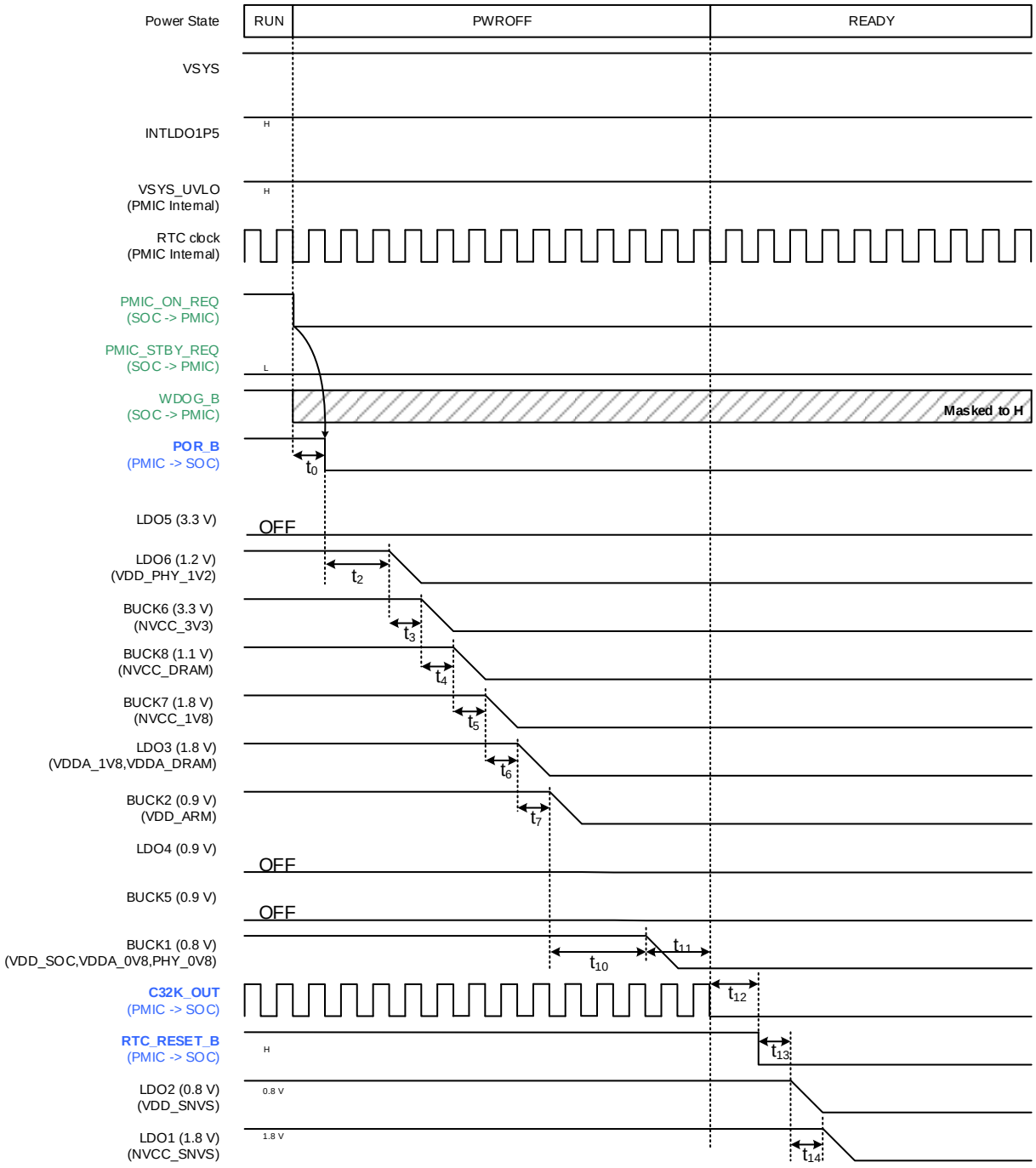


Figure 3-23. Power OFF Sequence (To READY)

3.3.2. Power OFF Sequence – continued

Table 3-40. Power OFF Sequence Timing Specification (To READY)

Symbol	Description	Min	Typ	Max	Unit
t_0	PMIC_ON_REQ De-assert to POR_B Assert Delay	0	120	200	µs
t_2	POR_B De-assert to LDO6 De-assert Delay	0	40	48	ms
t_3	LDO6 De-assert to BUCK6 De-assert Delay	0	10	12	ms
t_4	BUCK6 De-assert to BUCK8 De-assert Delay	0	10	12	ms
t_5	BUCK8 De-assert to BUCK7 De-assert Delay	0	10	12	ms
t_6	BUCK7 De-assert to LDO3 De-assert Delay	0	10	12	ms
t_7	LDO3 De-assert to BUCK2 De-assert Delay	0	10	12	ms
t_{10}	BUCK2 De-assert to BUCK1 De-assert Delay	0	30	36	ms
t_{11}	BUCK1 De-assert to C32K_OUT Output Stop Delay	0	10	12	ms
t_{12}	C32K_OUT Output Stop to RTC_RESET_B Assert Delay	0	10	12	ms
t_{13}	RTC_RESET_B Assert to LDO2 De-assert Delay	0	10	12	ms
t_{14}	LDO2 De-assert to LDO1 De-assert Delay	0	10	12	ms

3.3.3. RUN to IDLE

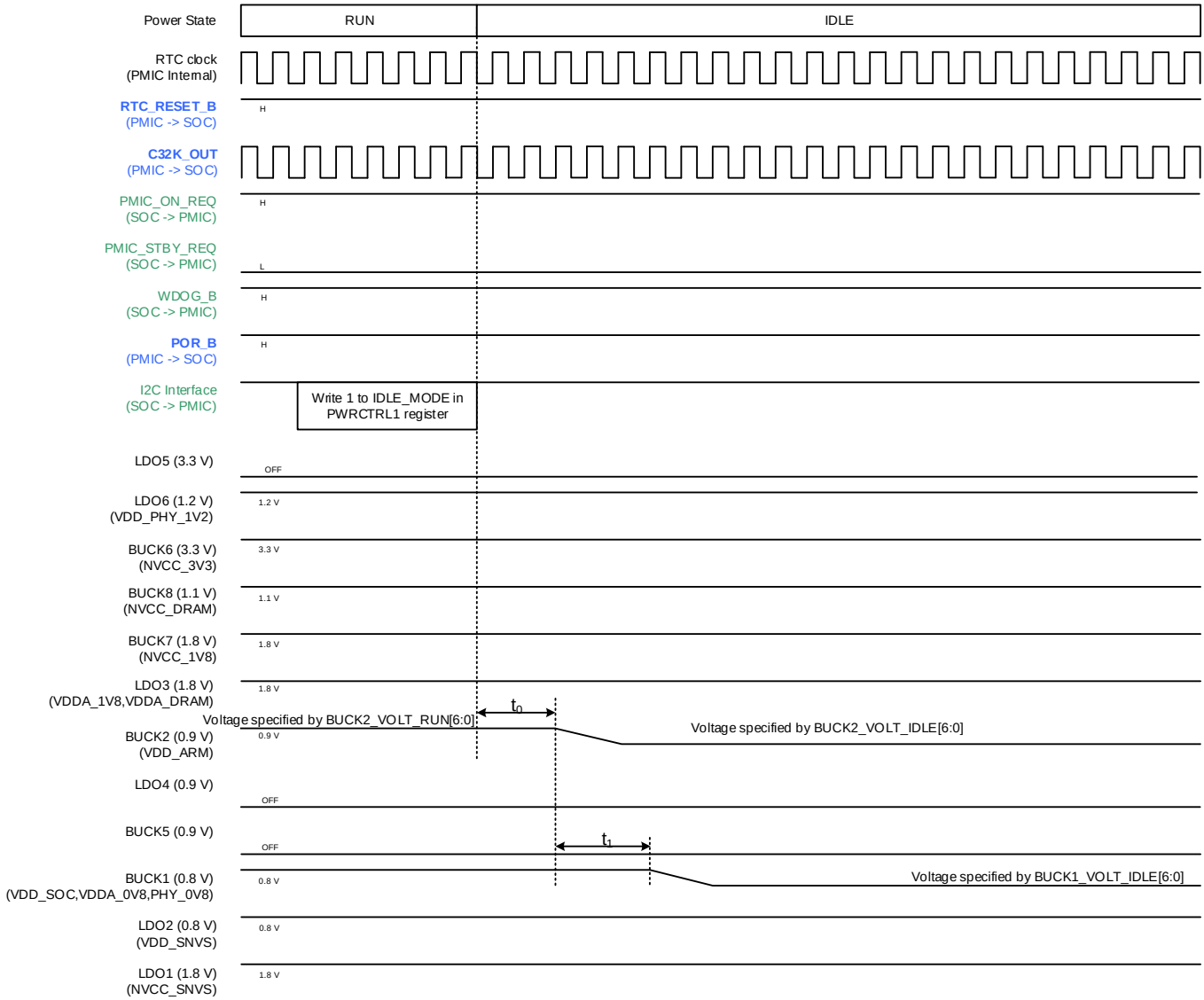


Figure 3-24. RUN to IDLE

Table 3-41. RUN to IDLE Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	End of I2C Access to BUCK2 Voltage Change Start	0	120	200	µs
t_1	BUCK2 to BUCK1 Voltage Change Delay	0	120	200	µs

3.3.4. IDLE to RUN

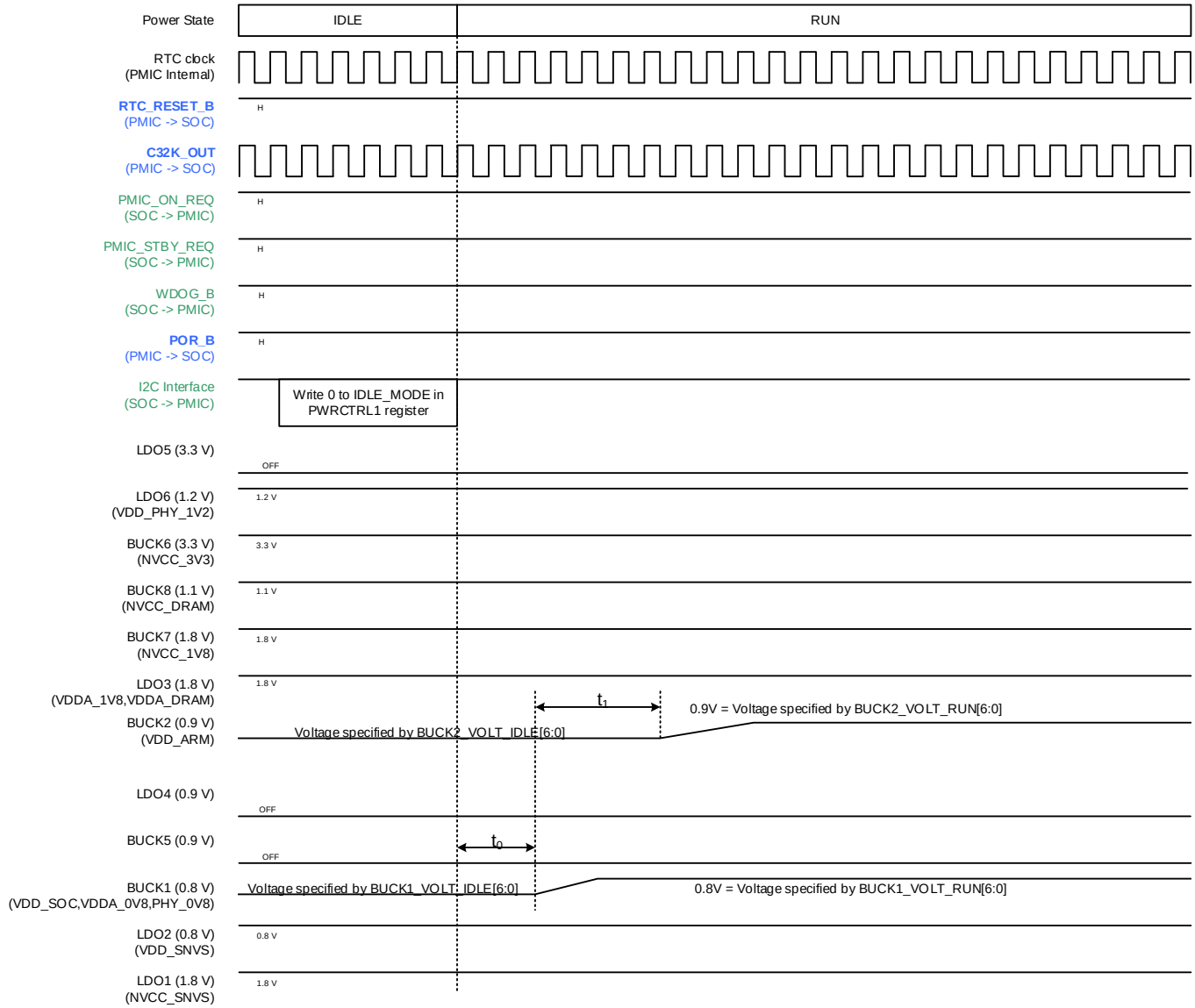


Figure 3-25. IDLE to RUN

Table 3-42. IDLE to RUN Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	End of I2C Access to BUCK1 Voltage Change Start	0	120	200	µs
t_1	BUCK1 to BUCK2 Voltage Change Delay	0	120	200	µs

3.3.5. RUN to SUSPEND

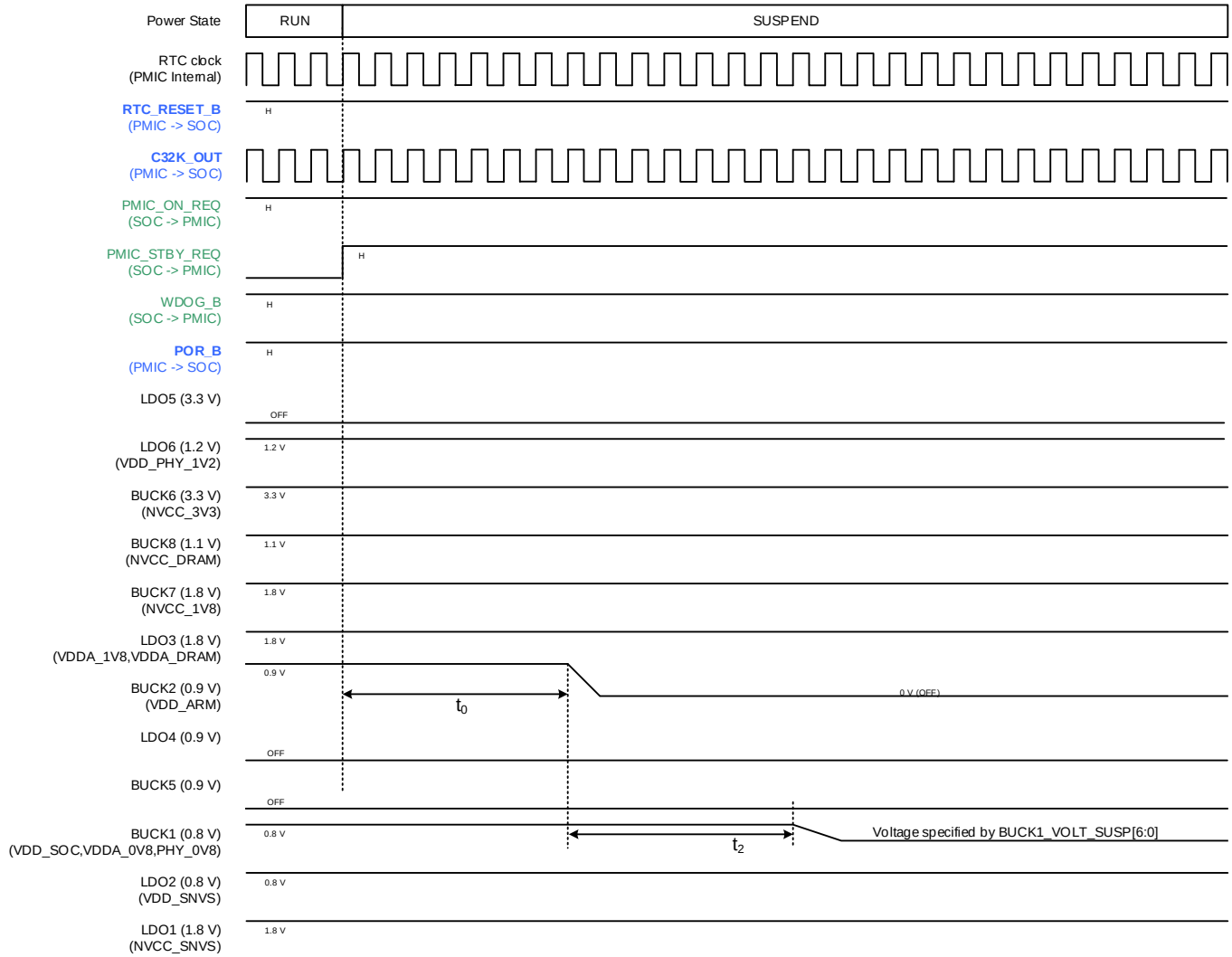


Figure 3-26. RUN to SUSPEND

Table 3-43. RUN to SUSPEND Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	PMIC_STBY_REQ High to BUCK2 De-assert Delay	0	120	200	µs
t_2	BUCK2 to BUCK1 Voltage Change Delay	0	20	24	ms

3.3.6. SUSPEND to RUN

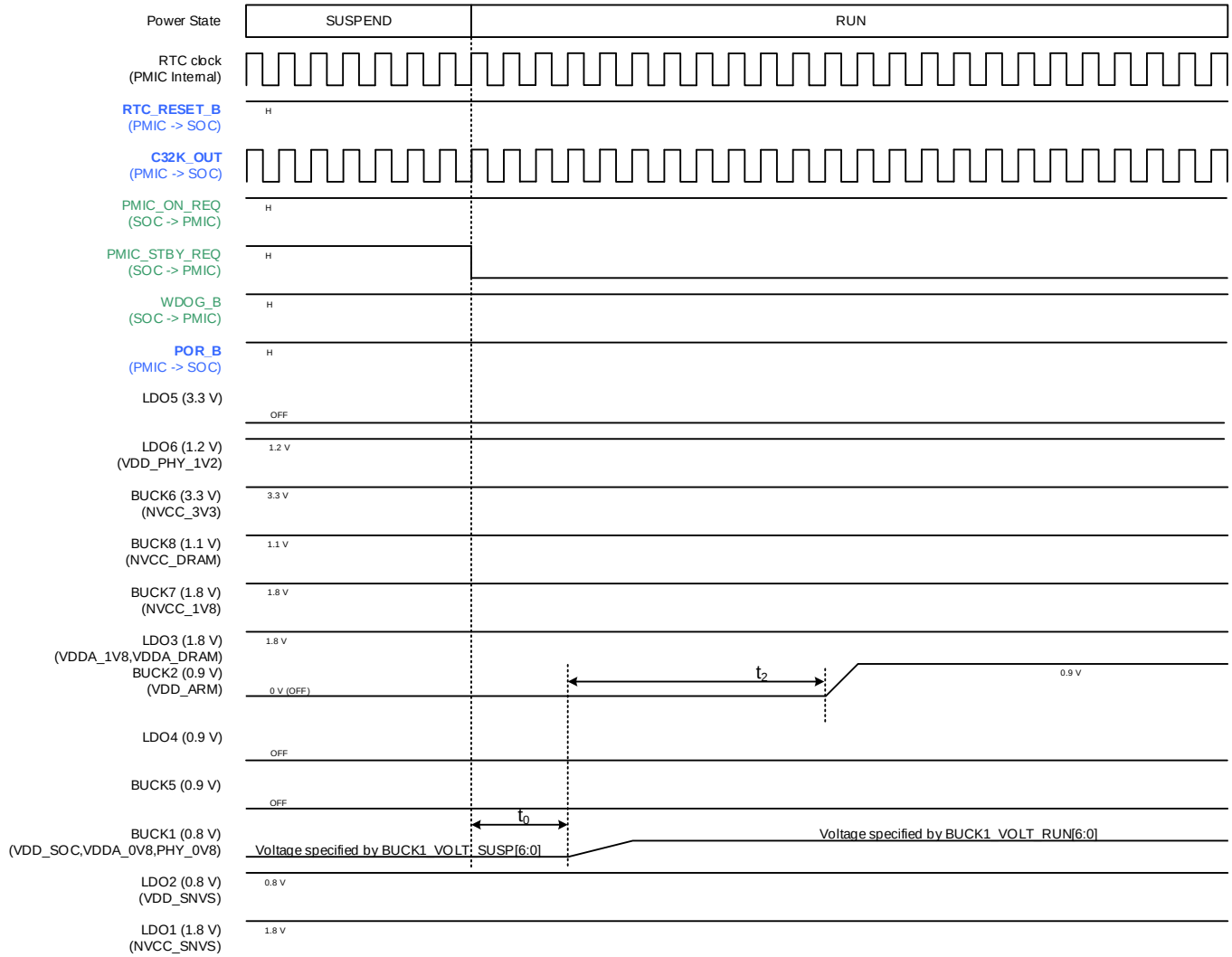


Figure 3-27. SUSPEND to RUN

Table 3-44. SUSPEND to RUN Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	PMIC_STBY_REQ Low to BUCK1 Voltage Change Start	0	120	200	µs
t_2	BUCK1 to BUCK2 Voltage Change Delay	0	2.0	2.4	ms

3.3.7. IDLE to SUSPEND

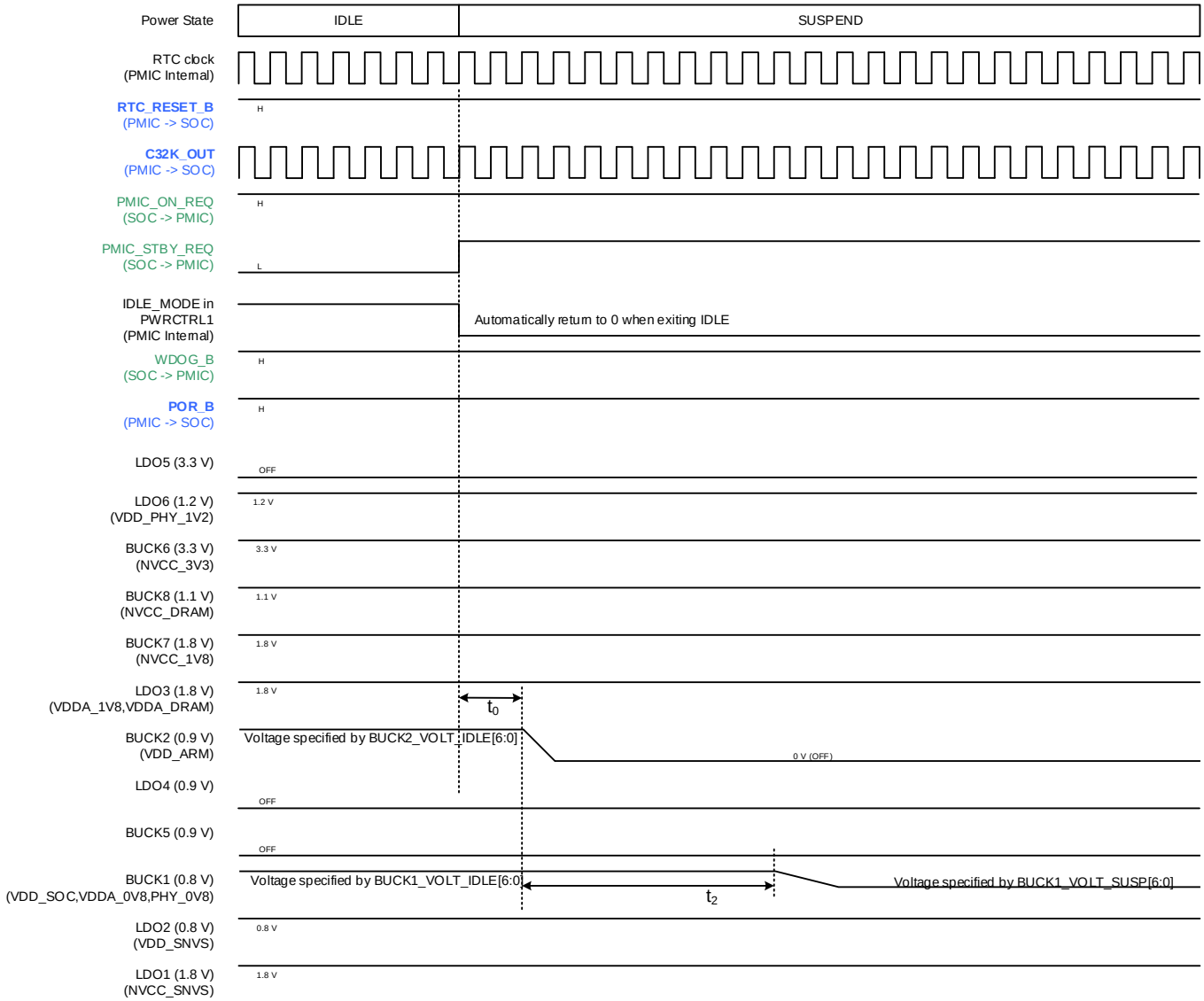


Figure 3-28. IDLE to SUSPEND

Table 3-45. IDLE to SUSPEND Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	PMIC_STBY_REQ High to BUCK2 De-assert Delay	0	120	200	µs
t_2	BUCK2 to BUCK1 Voltage Change Delay	0	20	24	ms

3.3.8. Emergency Shutdown

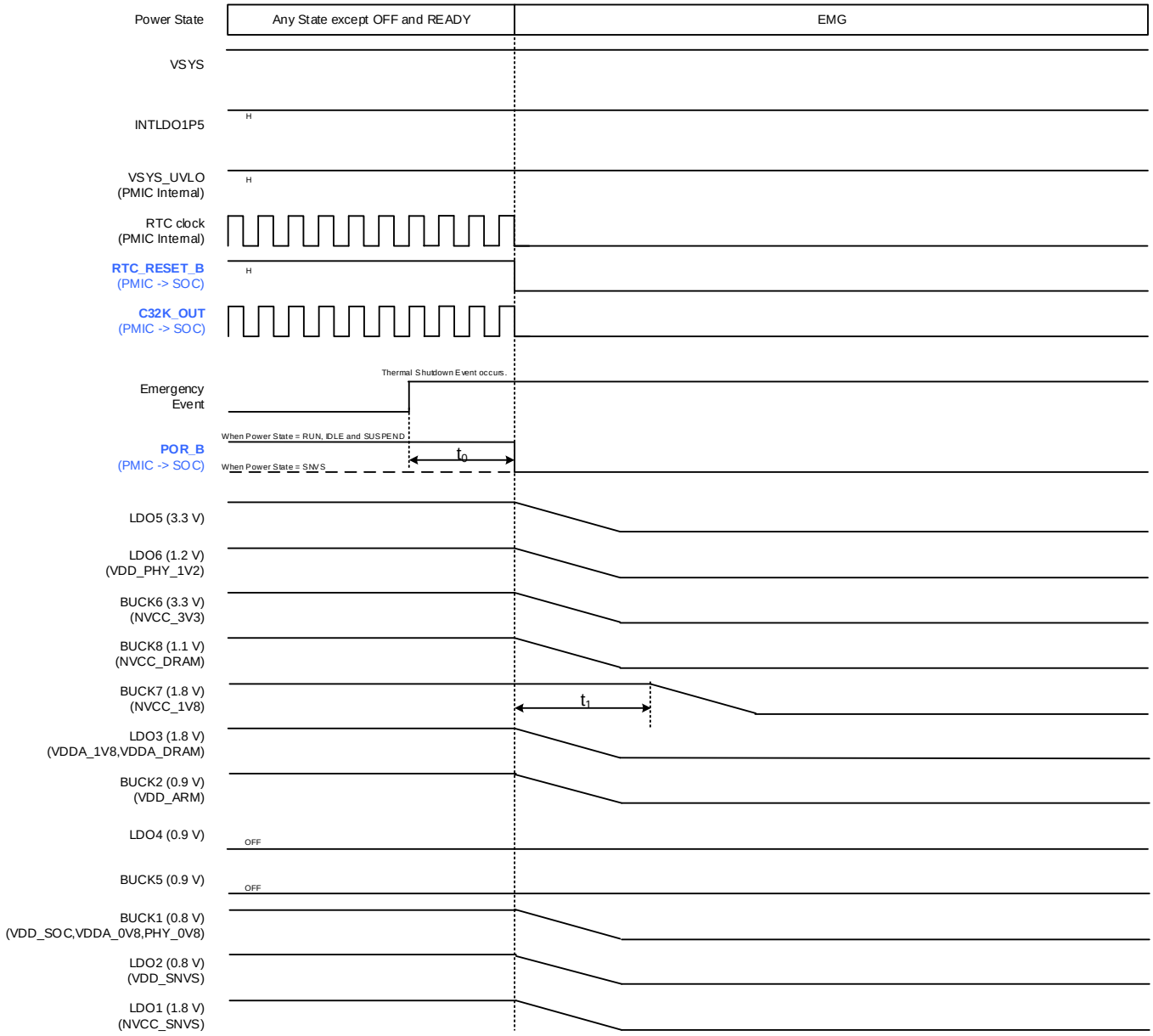


Figure 3-29. Emergency Shutdown

Table 3-46. Emergency Shutdown Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	Emergency Event to POR_B Assert and All VRs Except BUCK7 De-assert Delay	0	120	200	µs
t_1	POR_B Assert to BUCK7 De-assert Delay	0	30	35	ms

3.3.9. Warm Reset

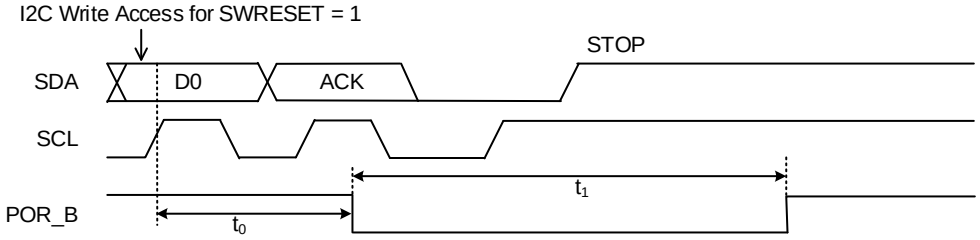


Figure 3-30. Warm Reset (SWRESET)

Table 3-47. Warm Reset (SWRESET) Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	SCL rising to POR_B assert delay	-	-	1.0	µs
t_1	POR_B assert duration time	0.95	1.00	1.05	ms

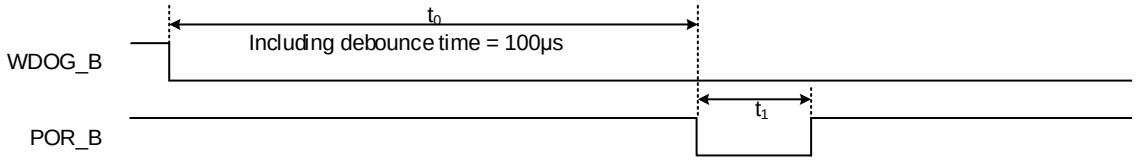


Figure 3-31. Warm Reset (WDOG_B)

Table 3-48. Warm Reset (WDOG_B) Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	WDOG_B falling to POR_B assert delay	100	110	120	µs
t_1	POR_B assert duration time	0.95	1.00	1.05	ms

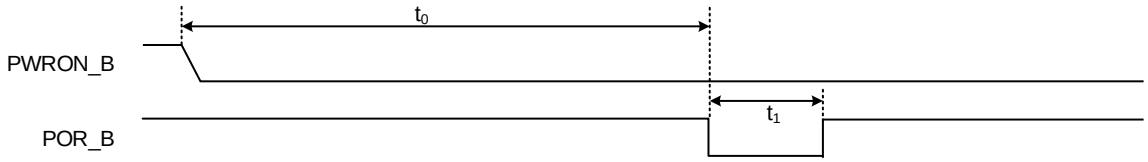


Figure 3-32. Warm Reset (PWRON_B Long Push)

Table 3-49. Warm Reset (PWRON_B Long Push) Timing Specification

Symbol	Description	Min	Typ	Max	Unit
t_0	PWRON_B falling to POR_B assert delay	PBDBNCT[1:0] in PWRONCONFIG0 + LONGT[3:0] in PWRONCONFIG1 -50	PBDBNCT[1:0] in PWRONCONFIG0 + LONGT[3:0] in PWRONCONFIG1	PBDBNCT[1:0] in PWRONCONFIG0 + LONGT[3:0] in PWRONCONFIG1 +50	ms
t_1	POR_B assert duration time	0.95	1.00	1.05	ms

3.3.10.Reset Source Indicators

The BD71850MWV has RESETSRC register which is intended to store the cause of a shutdown or reset, the firmware reads this data on the next startup. Depending on the cause of a shutdown or reset, the only bit of RESETSRC register is 1.

Table 3-50. RESETSRC - Reset Source Indicator Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
RESETSRC	R/W	RPWRON	RWDOG	RSWRST	RPMIC_ON_REQ	RVSYS_2P7	RTEMP	ROCP	RVR_FAULT	0x00	0x29

Bit	Name	Function	Initial
D[7]	RPWRON	0 = Default 1 = Previous shutdown was due to the PWRON_B Long Push Cold Reset (Write-1-clear bit)	0
D[6]	RWDOG	0 = Default 1 = Previous shutdown was due to the WDOG_B Cold Reset (Write-1-clear bit)	0
D[5]	RSWRST	0 = Default 1 = Previous shutdown was due to the Software Cold Reset (Write-1-clear bit)	0
D[4]	RPMIC_ON_REQ	0 = Default 1 = Previous shutdown was due to the PMIC_ON_REQ = 0 (Write-1-clear bit)	0
D[3]	RVSYS_2P7	0 = Default 1 = Previous shutdown was due to the Emergency VSYS < 2.7V (Write-1-clear bit)	0
D[2]	RTEMP	0 = Default 1 = Previous shutdown was due to the Emergency Thermal Shutdown (Write-1-clear bit)	0
D[1]	ROCP	0 = Default 1 = Previous shutdown was due to the Emergency OCP (Write-1-clear bit)	0
D[0]	RVR_FAULT	0 = Default 1 = Previous shutdown was due to the Emergency VR Fault (Write-1-clear bit)	0

4. I2C and Interrupt

4.1. I2C Bus Interface

4.1.1. I2C Bus Interface Overview

I2C access is not permitted when the power state = READY.

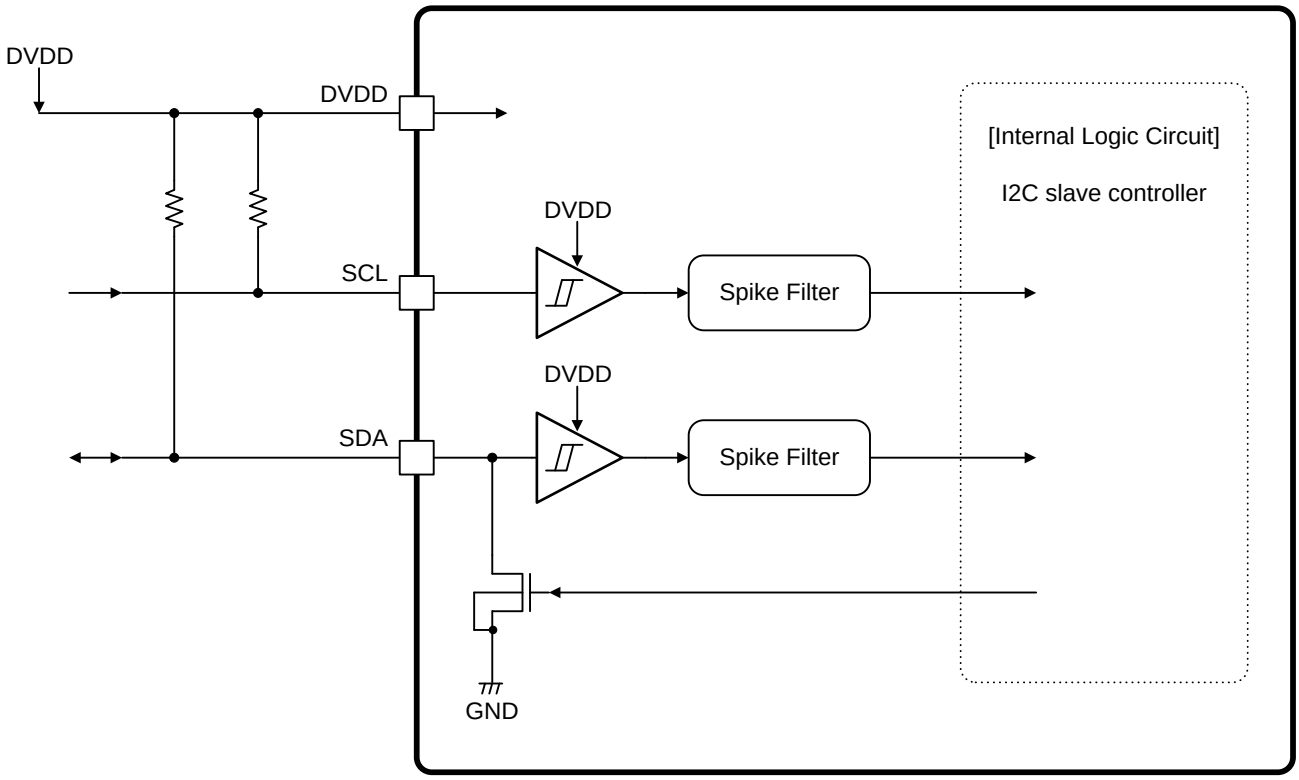


Figure 4-1. I2C (Slave) Block Diagram

4.1.2. I2C Bus Interface Electrical Characteristics

Table 4-1. I2C Bus Interface DC Electrical Characteristics

(Unless otherwise specified, Ta=+25°C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Digital pin characteristics – Input (SCL)						
SCL Input "H" Level	V_{IH_SCL}	DVDD x 0.7	-	DVDD + 0.3	V	
SCL Input "L" Level	V_{IL_SCL}	-0.3	-	DVDD x 0.3	V	
SCL Input Hysteresis	V_{IHYS_SCL}	0.1	-	-	V	
SCL Input Leak Current(Input=0 V)	I_{OFF1_SCL}	-1	-	+1	µA	
SCL Input Leak Current(Input=5.5 V)	I_{OFF2_SCL}	-1	-	+1	µA	
Digital pin characteristics – Input (SDA)						
SDA Input "H" Level	V_{IH_SDA}	DVDD x 0.7	-	DVDD + 0.3	V	
SDA Input "L" Level	V_{IL_SDA}	-0.3	-	DVDD x 0.3	V	
SDA Input Hysteresis	V_{IHYS_SDA}	0.1	-	-	V	
SDA Input Leak Current(Input=0 V)	I_{OFF1_SDA}	-1	-	+1	µA	
SDA Input Leak Current(Input=5.5 V)	I_{OFF2_SDA}	-1	-	+1	µA	
Digital pin characteristics - Output (SDA)						
SDA Output "L" Level Voltage	V_{OL_SDA}	-	-	0.4	V	I_{OL}=6mA
Output Off Leak Current(Input=0 V)	I_{OFF3_SDA}	-1	-	+1	µA	
Output Off Leak Current(Input=5.5 V)	I_{OFF4_SDA}	-1	-	+1	µA	

4.1.2. I2C Bus Interface Electrical Characteristics – continued

Table 4-2. I2C Bus Interface AC Timing - Fast Mode

(Unless otherwise specified, Ta=+25°C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Fast mode			Fast mode plus			Unit
		Min	Typ	Max	Min	Typ	Max	
I2C_CLK Clock Frequency	f_{SCL}	0	-	400	0	-	1000	kHz
Hold Time START Condition	t_{HD_STA}	0.60	-	-	0.26	-	-	µs
LOW Period of I2C_CLK Clock	t_{LOW}	1.3	-	-	0.5	-	-	µs
HIGH Period of I2C_CLK Clock	t_{HIGH}	0.60	-	-	0.26	-	-	µs
Set-up Time for a Repeated START Condition	t_{SU_STA}	0.60	-	-	0.26	-	-	µs
Data Hold Time	t_{HD_DAT}	0	-	-	0	-	-	ns
Data Set-up Time	t_{SU_DAT}	100	-	-	50	-	-	ns
Set-up Time for STOP Condition	t_{SU_STO}	0.60	-	-	0.26	-	-	µs
Fall Time of I2C_DATA Signal	t_F	20		300	-	-	120	ns
Capacitive Load for Each Bus Line	C_B	-	-	400	-	-	550	pF
Pulse Width of Spikes that are Suppressed by the Input Filter	t_{SP}	0	-	50	0	-	50	ns
Bus Free Time	t_{BUF}	1.3	-	-	0.5	-	-	µs
Data Valid Time	t_{VD_DAT}	-	-	0.90	-	-	0.45	µs
Data Valid Acknowledge Time	t_{VD_ACK}	-	-	0.90	-	-	0.45	µs

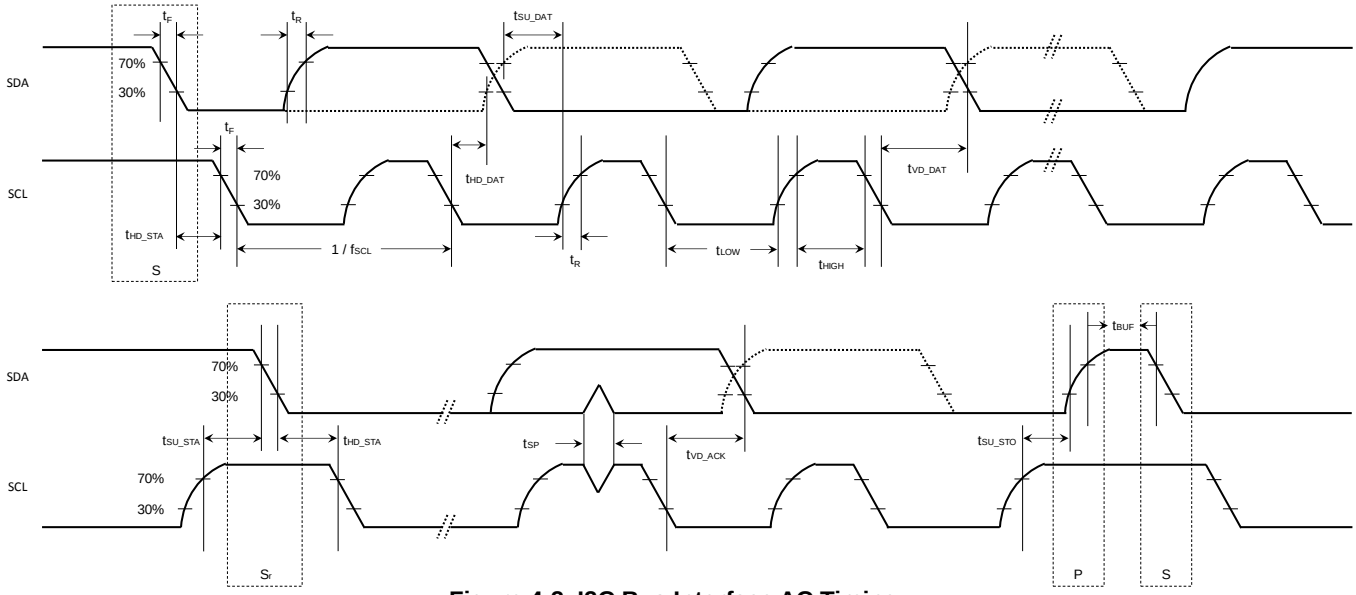


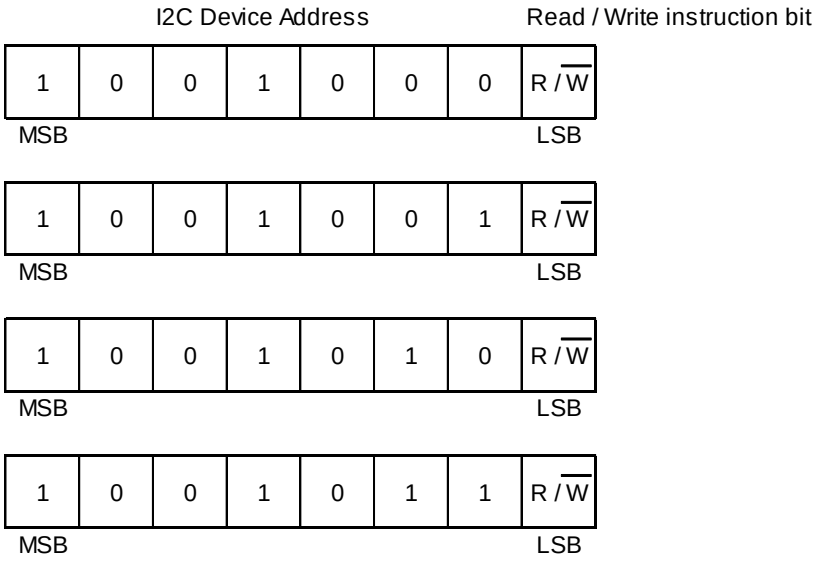
Figure 4-2. I2C Bus Interface AC Timing

4.1.3. Device Addressing

Table 4-3. I2C_DEV - I2C Device Address Indicator Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
I2C_DEV	R	-	-	-	-	-	-	I2C_DEV_ADRS[1:0]		0x03	0x02

Bit	Name	Function	Initial
D[1:0]	I2C_DEV_ADRS[1:0]	00 = I2C 7 bit Device Address = 0x48 01 = I2C 7 bit Device Address = 0x49 10 = I2C 7 bit Device Address = 0x4A 11 = I2C 7 bit Device Address = 0x4B	11



I2C Device Address is decided by OTP setting.

Figure 4-3. I2C Device Addressing

4.1.4. Write / Read Operation

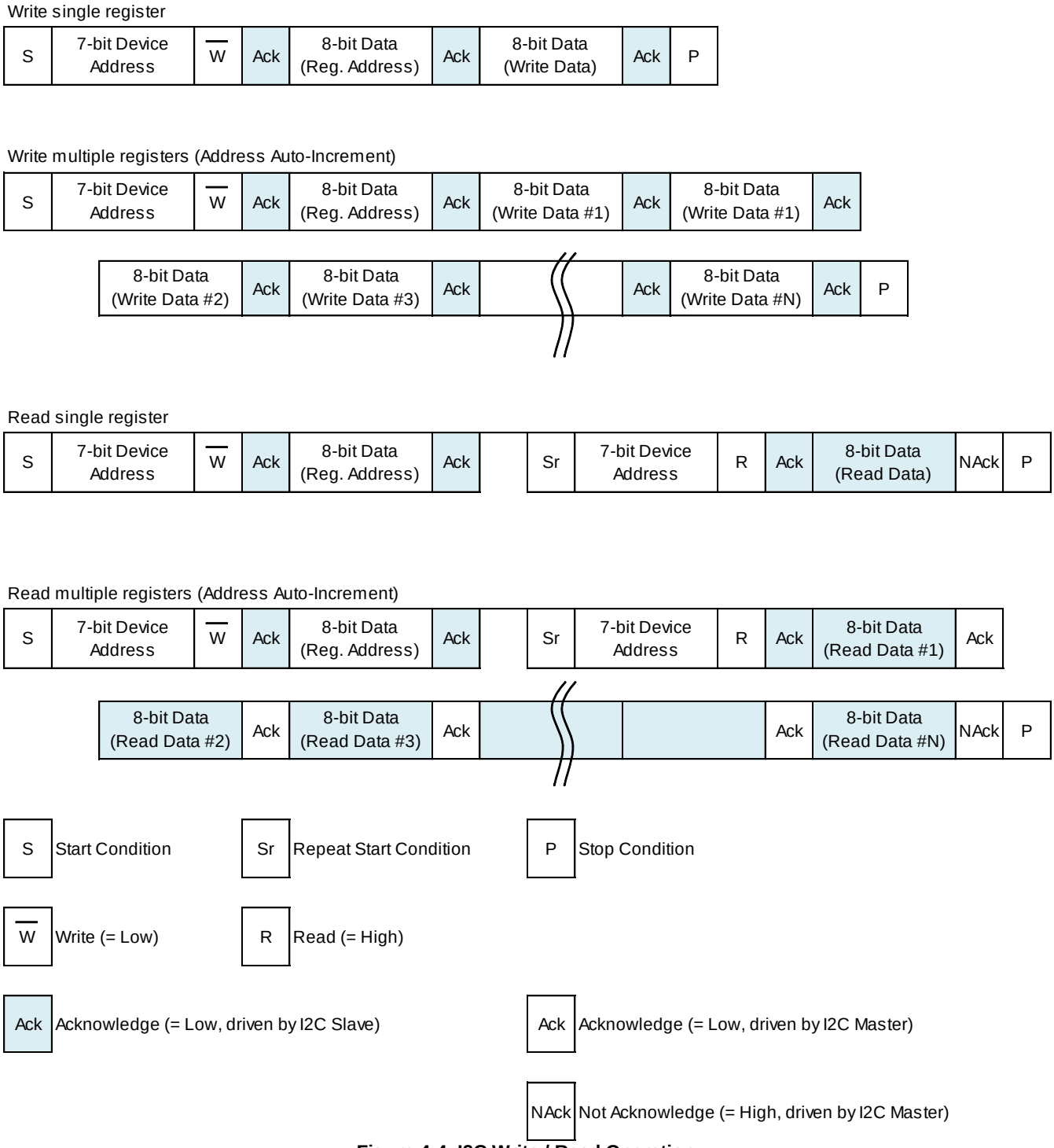


Figure 4-4. I2C Write / Read Operation

4.2. Interrupt

4.2.1. Interrupt Overview

Table 4-4. Interrupt Event

IRQ Event	Definition
PWRON	PWRON_B Pin Level Changed
PWRON_S	PWRON_B Short Push Detection
PWRON_L	PWRON_B Long Push Detection
WDOG	WDOG_B Pin Level Changed
SWRST	Written 1 to SWRESET in SWRESET Register
ON_REQ	PMIC_ON_REQ Pin Level Changed
STBY_REQ	PMIC_STBY_REQ Pin Level Changed

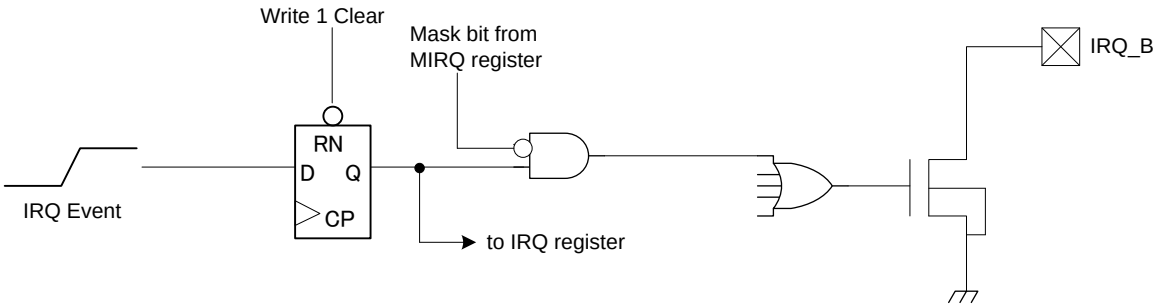


Figure 4-5. IRQ_B Architecture Block Diagram

Table 4-5. IRQ_B Electrical Characteristics

(Unless otherwise specified, Ta=+25°C, VSYS=5.0 V, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output "L" Level Voltage	V_{OL_IRQB}	-	-	DVDD x 0.2	V	I_{OL}=3 mA Sink
Output Off Leak Current	I_{OLK_IRQB}	-1	-	+1	µA	

4.2.1. Interrupt Overview – continued

Table 4-6. IRQ - Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
IRQ	R/W	-	SWRST	PWRON_S	PWRON_L	PWRON	WDOG	ON_REQ	STBY_REQ	0x00	0x2B

Bit	Name	Function	Initial
D[6]	SWRST	0 = SWRESET in SWRESET register is not written 1 1 = SWRESET in SWRESET register is written 1 This bit is a write-1-to-clear bit.	0
D[5]	PWRON_S	0 = PWRON_B Short Push not detected 1 = PWRON_B Short Push detected This bit is a write-1-to-clear bit.	0
D[4]	PWRON_L	0 = PWRON_B Long Push not detected 1 = PWRON_B Long Push detected This bit is a write-1-to-clear bit.	0
D[3]	PWRON	0 = PWRON_B level change not generated 1 = PWRON_B level change generated This bit is a write-1-to-clear bit.	0
D[2]	WDOG	0 = WDOG_B level change not generated 1 = WDOG_B level change generated This bit is a write-1-to-clear bit.	0
D[1]	ON_REQ	0 = PMIC_ON_REQ level change not generated 1 = PMIC_ON_REQ level change generated This bit is a write-1-to-clear bit.	0
D[0]	STBY_REQ	0 = PMIC_STBY_REQ level change not generated 1 = PMIC_STBY_REQ level change generated This bit is a write-1-to-clear bit.	0

Table 4-7. MIRQ – IRQ Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MIRQ	R/W	-	MSWRST	MPWRON_S	MPWRON_L	MPWRON	MWDOG	MON_REQ	MSTBY_REQ	0x7F	0x2A

Bit	Name	Function	Initial
D[6]	MSWRST	0 = No Mask 1 = Mask Interrupt	1
D[5]	MPWRON_S	0 = No Mask 1 = Mask Interrupt	1
D[4]	MPWRON_L	0 = No Mask 1 = Mask Interrupt	1
D[3]	MPWRON	0 = No Mask 1 = Mask Interrupt	1
D[2]	MWDOG	0 = No Mask 1 = Mask Interrupt	1
D[1]	MON_REQ	0 = No Mask 1 = Mask Interrupt	1
D[0]	MSTBY_REQ	0 = No Mask 1 = Mask Interrupt	1

4.2.1. Interrupt Overview – continued

Table 4-8. IN_MON - Input Port Monitor Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
IN_MON	R	-	-	-	-	STAT_ PWRON	STAT_ WDOG	STAT_ ON_REQ	STAT_ STBY_REQ	0x00	0x2C

Bit	Name	Function	Initial
D[3]	STAT_PWRON	0 = PWRON_B level is 0 1 = PWRON_B level is 1	0
D[2]	STAT_WDOG	0 = WDOG_B level is 0 1 = WDOG_B level is 1	0
D[1]	STAT_ON_REQ	0 = PMIC_ON_REQ level is 0 1 = PMIC_ON_REQ level is 1	0
D[0]	STAT_STBY_REQ	0 = PMIC_STBY_REQ level is 0 1 = PMIC_STBY_REQ level is 1	0

5. Power Rails

5.1. Output Voltage Range

Table 5-1. Output Voltage Range1

Data [Hex]	BUCK1	BUCK2	-	-	BUCK5	BUCK6	BUCK7	BUCK8	LDO1	LDO2	LDO3	LDO4	LDO5	LDO6	-
00	0.70	0.70			0.70	3.00	1.605	0.80	3.00	0.90	1.80 *(Note 1)*	0.90 *(Note 1)*	1.80	0.90	
01	0.71	0.71			0.80	3.10	1.695	0.81	3.10		1.90	1.00	1.90	1.00	
02	0.72	0.72			0.90 *(Note 1)*	3.20	1.755	0.82	3.20		2.00	1.10	2.00	1.10	
03	0.73	0.73			1.00	3.30 *(Note 1)*	1.800 *(Note 1)*	0.83	3.30		2.10	1.20	2.10	1.20 *(Note 1)*	
04	0.74	0.74			1.05		1.845	0.84			2.20	1.30	2.20	1.30	
05	0.75	0.75			1.10		1.905	0.85			2.30	1.40	2.30	1.40	
06	0.76	0.76			1.20		1.950	0.86			2.40	1.50	2.40	1.50	
07	0.77	0.77			1.35		1.995	0.87			2.50	1.60	2.50	1.60	
08	0.78	0.78						0.88			2.60	1.70	2.60	1.70	
09	0.79	0.79						0.89			2.70	1.80	2.70	1.80	
0A	0.80 *(Note 1)*	0.80						0.90			2.80		2.80		
0B	0.81	0.81						0.91			2.90		2.90		
0C	0.82	0.82						0.92			3.00		3.00		
0D	0.83	0.83						0.93			3.10		3.10		
0E	0.84	0.84						0.94			3.20		3.20		
0F	0.85	0.85						0.95			3.30		3.30 (Note 1)		
10	0.86	0.86						0.96							
11	0.87	0.87						0.97							
12	0.88	0.88						0.98							
13	0.89	0.89						0.99							
14	0.90	0.90 *(Note 1)*						1.00							
15	0.91	0.91						1.01							
16	0.92	0.92						1.02							
17	0.93	0.93						1.03							
18	0.94	0.94						1.04							
19	0.95	0.95						1.05							
1A	0.96	0.96						1.06							
1B	0.97	0.97						1.07							
1C	0.98	0.98						1.08							
1D	0.99	0.99						1.09							
1E	1.00	1.00						1.10 *(Note 1)*							
1F	1.01	1.01						1.11							

(Note 1) initial voltage(run mode)

5.1. Output Voltage Range – continued

Table 5-2. Output Voltage Range2

Data [Hex]	BUCK1	BUCK2	-	-	BUCK5	BUCK6	BUCK7	BUCK8	LDO1	LDO2	LDO3	LDO4	LDO5	LDO6	-
20	1.02	1.02						1.12	1.60	0.80 *(Note 1)*					
21	1.03	1.03						1.13	1.70						
22	1.04	1.04						1.14	1.80 *(Note 1)*						
23	1.05	1.05						1.15	1.90						
24	1.06	1.06						1.16							
25	1.07	1.07						1.17							
26	1.08	1.08						1.18							
27	1.09	1.09						1.19							
28	1.10	1.10						1.20							
29	1.11	1.11						1.21							
2A	1.12	1.12						1.22							
2B	1.13	1.13						1.23							
2C	1.14	1.14						1.24							
2D	1.15	1.15						1.25							
2E	1.16	1.16						1.26							
2F	1.17	1.17						1.27							
30	1.18	1.18						1.28							
31	1.19	1.19						1.29							
32	1.20	1.20						1.30							
33	1.21	1.21						1.31							
34	1.22	1.22						1.32							
35	1.23	1.23						1.33							
36	1.24	1.24						1.34							
37	1.25	1.25						1.35							
38	1.26	1.26						1.36							
39	1.27	1.27						1.37							
3A	1.28	1.28						1.38							
3B	1.29	1.29						1.39							
3C	1.30	1.30						1.40							
3D															
3E															
3F															

(Note 1) initial voltage(run mode)

5.2. Details of Buck

5.2.1. BUCK1

5.2.1.1. BUCK1 Block Diagram

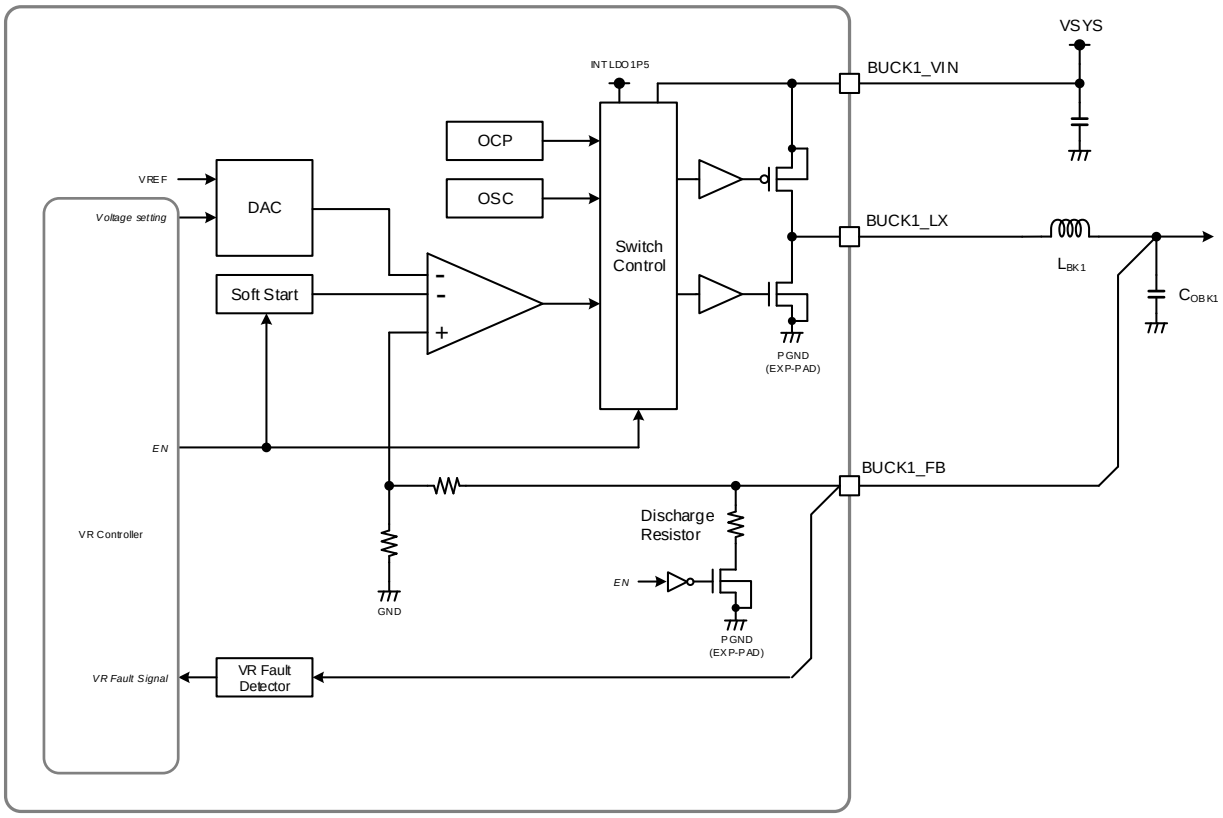


Figure 5-1. BUCK1 Block Diagram

5.2.1.2. BUCK1 Electrical Characteristics

Table 5-3. BUCK1 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK1}	0.791	0.800	0.809	V	Vo = 0.8 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK1}	0.7	-	1.3	V	10 mV step
Quiescent Current	I_{Q_BK1}	-	15	-	µA	Vo = 0.8 V Io = 0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK1}	3000	-	-	mA	
Over Current Protection	I_{OCP_BK1}	4500	-	-	mA	Peak current of inductor *(Note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK1}	-1	0	+1	%	Io = 1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK1_1mA}	-	80	-	%	Io = 1 mA, Vo = 0.8 V
	η_{BK1_500mA}	-	84	-	%	Io = 500 mA, Vo = 0.8 V
	η_{BK1_max}	-	70	-	%	Io = Iomax, Vo = 0.8 V
Oscillating Frequency	f_{SW_BK1}	-	2	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK1}	-	144	500	µs	During EN to 90 % of nominal Voltage, BUCK1_RAMPRATE_RUN[1:0] = 01
Discharge Resistance	R_{D_BK1}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK1_L}	-	80	-	%	Vo = 0.8 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK1_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK1_H}	-	130	-	%	Vo = 0.8 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK1_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK1}	-	0.47	-	µH	*(Note 2)*
Output Capacitance	C_{OBK1}	22	44	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias Max value is limited by ramp rate. <Output Max Capacitance> ramp rate 1.25 mV, 2.5 mV, 5 mV : 100 µF ramp rate 10 mV : 50 µF

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

5.2.1.3. BUCK1 Control

Table 5-4. BUCK1_CTRL - BUCK1 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK1_CTRL	R/W	BUCK1_RAMPRATE [1:0]		-	-	BUCK1_ PWM_FIX	-	BUCK1_SEL	BUCK1_EN	0x40	0x05

Bit	Name	Function	Initial
D[7:6]	BUCK1_RAMPRATE[1:0]	BUCK1 DVS ramp rate 00 = 10 mV/µs 01 = 5 mV/µs 10 = 2.5 mV/µs 11 = 1.25 mV/µs Note : When BUCK1 voltage starts up from 0V, the ramp rate is fixed 5mV/µs, regardless of the value of BUCK1_RAMPRATE[1:0].	01
D[3]	BUCK1_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK1_SEL	BUCK1 control select bit 0 = BUCK1 ON/OFF is controlled by state machine. 1 = BUCK1 ON/OFF is controlled by D[0] on this register.	0
D[0]	BUCK1_EN	BUCK1 control bit with condition of D[1] 0 = BUCK1 OFF 1 = BUCK1 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown. When system is in SNVS, BUCK1_SEL = 1 and BUCK1_EN = 1, BUCK1 voltage is specified by BUCK1_VOLT_SUSP register.	0

Table 5-5. BUCK1_VOLT_RUN - BUCK1 Voltage (RUN) Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK1_VOLT_RUN	R/W	-	BUCK1_VOLT_RUN[6:0]							0x0A	0x0D

Bit	Name	Function	Initial
D[6:0]	BUCK1_VOLT_RUN[6:0]	BUCK1 voltage when Power State = RUN 0x00 = 0.70 V 0x01 = 0.71 V 0x02 = 0.72 V 0x03 = 0.73 V 0x04 = 0.74 V 0x05 = 0.75 V 0x06 = 0.76 V 0x07 = 0.77 V 0x08 = 0.78 V 0x09 = 0.79 V 0x0A = 0.80V(initial) 0x0B = 0.81 V 0x0C = 0.82 V 0x0D = 0.83 V 0x0E = 0.84 V 0x0F = 0.85 V 0x10 = 0.86 V 0x11 = 0.87 V 0x12 = 0.88 V 0x13 = 0.89 V 0x14 = 0.90 V 0x15 = 0.91 V 0x16 = 0.92 V 0x17 = 0.93 V 0x18 = 0.94 V 0x19 = 0.95 V 0x1A = 0.96 V 0x1B = 0.97 V 0x1C = 0.98 V 0x1D = 0.99 V 0x1E = 1.00 V 0x1F = 1.01 V 0x20 = 1.02 V 0x21 = 1.03 V 0x22 = 1.04 V 0x23 = 1.05 V 0x24 = 1.06 V 0x25 = 1.07 V 0x26 = 1.08 V 0x27 = 1.09 V 0x28 = 1.10 V 0x29 = 1.11 V 0x2A = 1.12 V 0x2B = 1.13 V 0x2C = 1.14 V 0x2D = 1.15 V 0x2E = 1.16 V 0x2F = 1.17 V 0x30 = 1.18 V 0x31 = 1.19 V 0x32 = 1.20 V 0x33 = 1.21 V 0x34 = 1.22 V 0x35 = 1.23 V 0x36 = 1.24 V 0x37 = 1.25 V 0x38 = 1.26 V 0x39 = 1.27 V 0x3A = 1.28 V 0x3B = 1.29 V 0x3C = 1.30 V 0x3D-0x7F = reserved	0001010

5.2.1.3. BUCK1 Control – continued

Table 5-6. BUCK1_VOLT_IDLE - BUCK1 Voltage (IDLE) Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK1_VOLT_IDLE	R/W	-	BUCK1_VOLT_IDLE[6:0]							0x0A	0x0E

Bit	Name	Function	Initial
D[6:0]	BUCK1_VOLT_IDLE[6:0]	BUCK1 voltage when Power State = IDLE 0x00 = 0.70 V 0x01 = 0.71 V 0x02 = 0.72 V 0x03 = 0.73 V 0x04 = 0.74 V 0x05 = 0.75 V 0x06 = 0.76 V 0x07 = 0.77 V 0x08 = 0.78 V 0x09 = 0.79 V 0x0A = 0.80 V(initial) 0x0B = 0.81 V 0x0C = 0.82 V 0x0D = 0.83 V 0x0E = 0.84 V 0x0F = 0.85 V 0x10 = 0.86 V 0x11 = 0.87 V 0x12 = 0.88 V 0x13 = 0.89 V 0x14 = 0.90 V 0x15 = 0.91 V 0x16 = 0.92 V 0x17 = 0.93 V 0x18 = 0.94 V 0x19 = 0.95 V 0x1A = 0.96 V 0x1B = 0.97 V 0x1C = 0.98 V 0x1D = 0.99 V 0x1E = 1.00 V 0x1F = 1.01 V 0x20 = 1.02 V 0x21 = 1.03 V 0x22 = 1.04 V 0x23 = 1.05 V 0x24 = 1.06 V 0x25 = 1.07 V 0x26 = 1.08 V 0x27 = 1.09 V 0x28 = 1.10 V 0x29 = 1.11 V 0x2A = 1.12 V 0x2B = 1.13 V 0x2C = 1.14 V 0x2D = 1.15 V 0x2E = 1.16 V 0x2F = 1.17 V 0x30 = 1.18 V 0x31 = 1.19 V 0x32 = 1.20 V 0x33 = 1.21 V 0x34 = 1.22 V 0x35 = 1.23 V 0x36 = 1.24 V 0x37 = 1.25 V 0x38 = 1.26 V 0x39 = 1.27 V 0x3A = 1.28 V 0x3B = 1.29 V 0x3C = 1.30 V 0x3D-0x7F = reserved	0001010

Table 5-7. BUCK1_VOLT_SUSP - BUCK1 Voltage (SUSPEND) Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK1_VOLT_SUSP	R/W	-	BUCK1_VOLT_SUSP[6:0]							0x0A	0x0F

Bit	Name	Function	Initial
D[6:0]	BUCK1_VOLT_SUSP[6:0]	BUCK1 voltage when Power State = SUSPEND 0x00 = 0.70 V 0x01 = 0.71 V 0x02 = 0.72 V 0x03 = 0.73 V 0x04 = 0.74 V 0x05 = 0.75 V 0x06 = 0.76 V 0x07 = 0.77 V 0x08 = 0.78 V 0x09 = 0.79 V 0x0A = 0.80V(initial) 0x0B = 0.81 V 0x0C = 0.82 V 0x0D = 0.83 V 0x0E = 0.84 V 0x0F = 0.85 V 0x10 = 0.86 V 0x11 = 0.87 V 0x12 = 0.88 V 0x13 = 0.89 V 0x14 = 0.90 V 0x15 = 0.91 V 0x16 = 0.92 V 0x17 = 0.93 V 0x18 = 0.94 V 0x19 = 0.95 V 0x1A = 0.96 V 0x1B = 0.97 V 0x1C = 0.98 V 0x1D = 0.99 V 0x1E = 1.00 V 0x1F = 1.01 V 0x20 = 1.02 V 0x21 = 1.03 V 0x22 = 1.04 V 0x23 = 1.05 V 0x24 = 1.06 V 0x25 = 1.07 V 0x26 = 1.08 V 0x27 = 1.09 V 0x28 = 1.10 V 0x29 = 1.11 V 0x2A = 1.12 V 0x2B = 1.13 V 0x2C = 1.14 V 0x2D = 1.15 V 0x2E = 1.16 V 0x2F = 1.17 V 0x30 = 1.18 V 0x31 = 1.19 V 0x32 = 1.20 V 0x33 = 1.21 V 0x34 = 1.22 V 0x35 = 1.23 V 0x36 = 1.24 V 0x37 = 1.25 V 0x38 = 1.26 V 0x39 = 1.27 V 0x3A = 1.28 V 0x3B = 1.29 V 0x3C = 1.30 V 0x3D-0x7F = reserved	0001010

5.2.2. BUCK2

5.2.2.1. BUCK2 Block Diagram

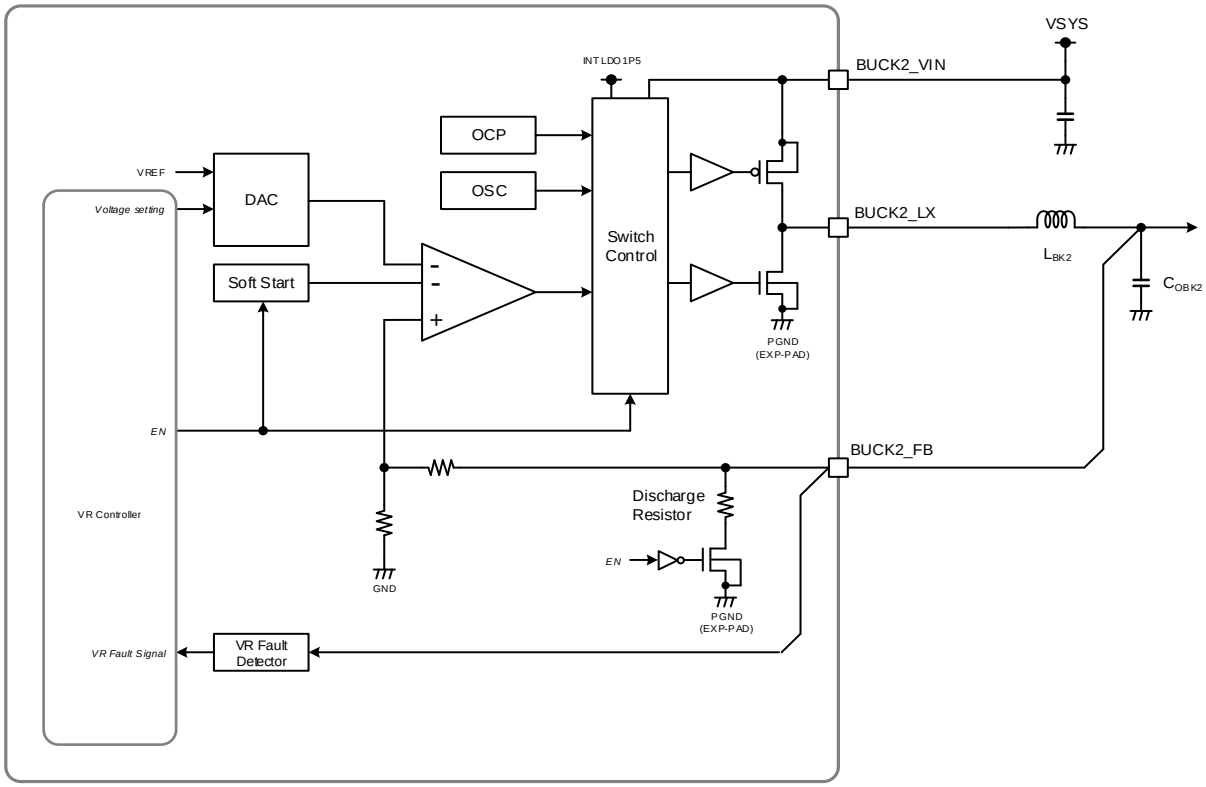


Figure 5-2. BUCK2 Block Diagram

5.2.2.2. BUCK2 Electrical Characteristics

Table 5-8. BUCK2 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK2}	0.89	0.90	0.91	V	Vo = 0.9 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK2}	0.7	-	1.3	V	10 mV step
Quiescent Current	I_{Q_BK2}	-	15	-	µA	Vo = 0.9 V Io = 0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK2}	3000	-	-	mA	
Over Current Protection	I_{OCP_BK2}	4500	-	-	mA	Peak current of inductor *(Note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK2}	-1	0	+1	%	Io = 1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK2_1mA}	-	79	-	%	Io = 1 mA, Vo = 0.9 V
	η_{BK2_500mA}	-	84	-	%	Io = 500 mA, Vo = 0.9 V
	η_{BK2_max}	-	71	-	%	Io = Iomax, Vo = 0.9 V
Oscillating Frequency	f_{SW_BK2}	-	2	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK2}	-	162	500	µs	During EN to 90 % of nominal Voltage, BUCK2_RAMPRATE_RUN[1:0] = 01
Discharge Resistance	R_{D_BK2}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK2_L}	-	80	-	%	Vo = 0.9 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK2_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK2_H}	-	130	-	%	Vo = 0.9 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK2_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK2}	-	0.47	-	µH	*(Note 2)*
Output Capacitance	C_{OBK2}	22	44	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias Max value is limited by ramp rate. <Output Max Capacitance> ramp rate 1.25 mV, 2.5 mV, 5 mV : 100 µF ramp rate 10 mV : 50 µF

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

5.2.2.3. BUCK2 Control

Table 5-9. BUCK2_CTRL - BUCK2 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK2_CTRL	R/W	BUCK2_RAMPRATE[1:0]		-	-	BUCK2_PWM_FIX	-	BUCK2_SEL	BUCK2_EN	0x40	0x06

Bit	Name	Function	Initial
D[7:6]	BUCK2_RAMPRATE[1:0]	BUCK2 DVS ramp rate 00 = 10 mV/µs 01 = 5 mV/µs 10 = 2.5 mV/µs 11 = 1.25 mV/µs Note : When BUCK2 voltage starts up from 0V, the ramp rate is fixed 5mV/µs, regardless of the value of BUCK2_RAMPRATE[1:0].	01
D[3]	BUCK2_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK2_SEL	BUCK2 control select bit 0 = BUCK2 ON/OFF is controlled by state machine. 1 = BUCK2 ON/OFF is controlled by D[0] on this register.	0
D[0]	BUCK2_EN	BUCK2 control bit with condition of D[1] 0 = BUCK2 OFF 1 = BUCK2 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown. When system is in SNVS or SUSPEND, BUCK2_SEL = 1 and BUCK2_EN = 1, BUCK2 voltage is specified by BUCK2_VOLT_IDLE register.	0

Table 5-10. BUCK2_VOLT_RUN - BUCK2 Voltage (RUN) Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK2_VOLT_RUN	R/W	-	BUCK2_VOLT_RUN[6:0]							0x14	0x10

Bit	Name	Function	Initial
D[6:0]	BUCK2_VOLT_RUN[6:0]	BUCK2 voltage when Power State = RUN 0x00 = 0.70 V 0x01 = 0.71 V 0x02 = 0.72 V 0x03 = 0.73 V 0x04 = 0.74 V 0x05 = 0.75 V 0x06 = 0.76 V 0x07 = 0.77 V 0x08 = 0.78 V 0x09 = 0.79 V 0x0A = 0.80 V 0x0B = 0.81 V 0x0C = 0.82 V 0x0D = 0.83 V 0x0E = 0.84 V 0x0F = 0.85 V 0x10 = 0.86 V 0x11 = 0.87 V 0x12 = 0.88 V 0x13 = 0.89 V 0x14 = 0.90 V (initial) 0x15 = 0.91 V 0x16 = 0.92 V 0x17 = 0.93 V 0x18 = 0.94 V 0x19 = 0.95 V 0x1A = 0.96 V 0x1B = 0.97 V 0x1C = 0.98 V 0x1D = 0.99 V 0x1E = 1.00 V 0x1F = 1.01 V 0x20 = 1.02 V 0x21 = 1.03 V 0x22 = 1.04 V 0x23 = 1.05 V 0x24 = 1.06 V 0x25 = 1.07 V 0x26 = 1.08 V 0x27 = 1.09 V 0x28 = 1.10 V 0x29 = 1.11 V 0x2A = 1.12 V 0x2B = 1.13 V 0x2C = 1.14 V 0x2D = 1.15 V 0x2E = 1.16 V 0x2F = 1.17 V 0x30 = 1.18 V 0x31 = 1.19 V 0x32 = 1.20 V 0x33 = 1.21 V 0x34 = 1.22 V 0x35 = 1.23 V 0x36 = 1.24 V 0x37 = 1.25 V 0x38 = 1.26 V 0x39 = 1.27 V 0x3A = 1.28 V 0x3B = 1.29 V 0x3C = 1.30 V 0x3D-0x7F = reserved	0010100

5.2.2.3. BUCK2 Control – continued

Table 5-11. BUCK2_VOLT_IDLE - BUCK2 Voltage (IDLE) Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK2_VOLT_IDLE	R/W	-	BUCK2_VOLT_IDLE[6:0]							0x0A	0x11

Bit	Name	Function	Initial
D[6:0]	BUCK2_VOLT_IDLE[6:0]	BUCK2 voltage when Power State = IDLE 0x00 = 0.70 V 0x01 = 0.71 V 0x02 = 0.72 V 0x03 = 0.73 V 0x04 = 0.74 V 0x05 = 0.75 V 0x06 = 0.76 V 0x07 = 0.77 V 0x08 = 0.78 V 0x09 = 0.79 V 0x0A = 0.80V(initial) 0x0B = 0.81 V 0x0C = 0.82 V 0x0D = 0.83 V 0x0E = 0.84 V 0x0F = 0.85 V 0x10 = 0.86 V 0x11 = 0.87 V 0x12 = 0.88 V 0x13 = 0.89 V 0x14 = 0.90 V 0x15 = 0.91 V 0x16 = 0.92 V 0x17 = 0.93 V 0x18 = 0.94 V 0x19 = 0.95 V 0x1A = 0.96 V 0x1B = 0.97 V 0x1C = 0.98 V 0x1D = 0.99 V 0x1E = 1.00 V 0x1F = 1.01 V 0x20 = 1.02 V 0x21 = 1.03 V 0x22 = 1.04 V 0x23 = 1.05 V 0x24 = 1.06 V 0x25 = 1.07 V 0x26 = 1.08 V 0x27 = 1.09 V 0x28 = 1.10 V 0x29 = 1.11 V 0x2A = 1.12 V 0x2B = 1.13 V 0x2C = 1.14 V 0x2D = 1.15 V 0x2E = 1.16 V 0x2F = 1.17 V 0x30 = 1.18 V 0x31 = 1.19 V 0x32 = 1.20 V 0x33 = 1.21 V 0x34 = 1.22 V 0x35 = 1.23 V 0x36 = 1.24 V 0x37 = 1.25 V 0x38 = 1.26 V 0x39 = 1.27 V 0x3A = 1.28 V 0x3B = 1.29 V 0x3C = 1.30 V 0x3D-0x7F = reserved	0001010

5.2.3. BUCK5

5.2.3.1. BUCK5 Block Diagram

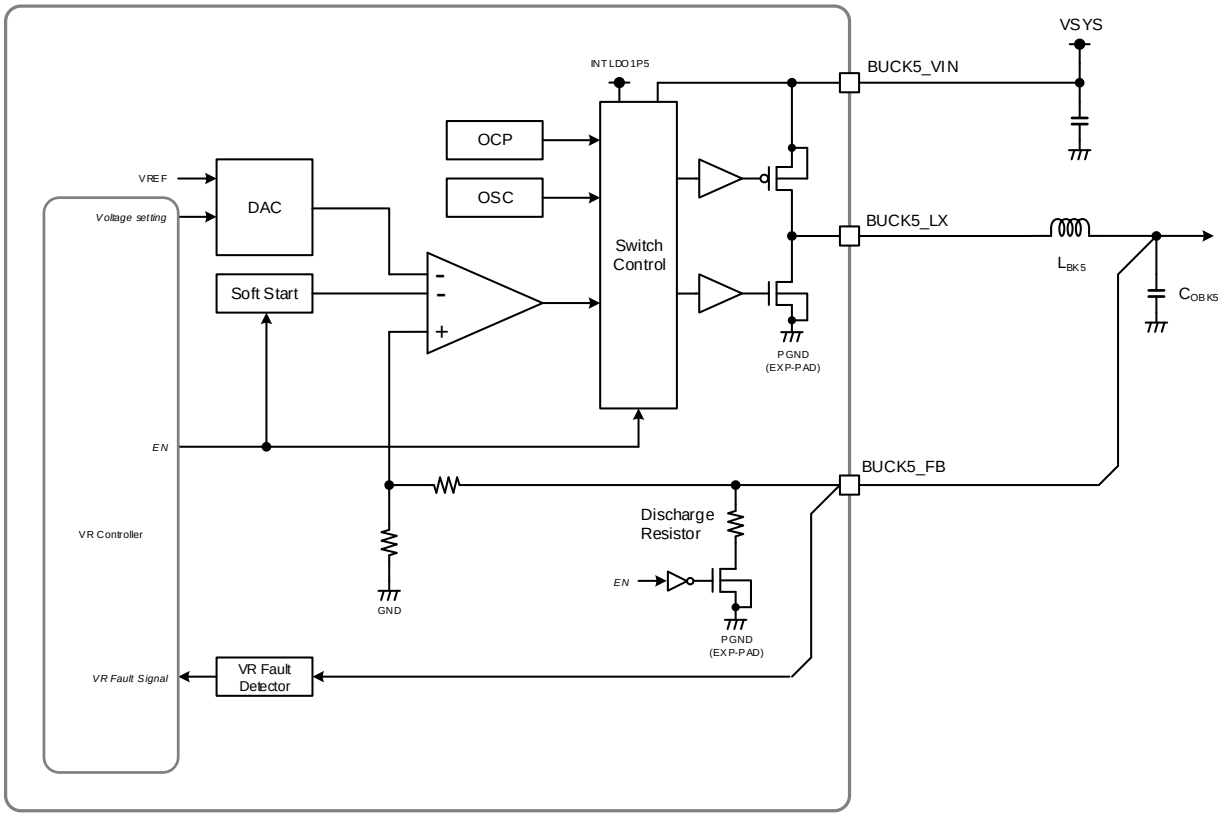


Figure 5-3. BUCK5 Block Diagram

5.2.3.2. BUCK5 Electrical Characteristics

Table 5-12. BUCK5 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK5}	0.89	0.90	0.91	V	Vo = 0.9 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK5}	0.70	-	1.35	V	0.70 V, 0.80 V, 0.90 V, 1.00 V, 1.05 V, 1.10 V, 1.20 V, 1.35 V
Quiescent Current	I_{Q_BK5}	-	15	-	µA	Vo = 0.9 V Io = 0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK5}	3000	-	-	mA	
Over Current Protection	I_{OCP_BK5}	4500	-	-	mA	Peak current of inductor *(Note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK5}	-1	0	+1	%	Io = 1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK5_1mA}	-	79	-	%	Io = 1 mA, Vo = 0.9 V
	η_{BK5_500mA}	-	84	-	%	Io = 500 mA, Vo = 0.9 V
	η_{BK5_max}	-	71	-	%	Io = Iomax, Vo = 0.9 V
Oscillating Frequency	f_{SW_BK5}	-	2	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK5}	-	162	500	µs	During EN to 90 % of nominal Voltage
Discharge Resistance	R_{D_BK5}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK5_L}	-	80	-	%	Vo = 0.9 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK5_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK5_H}	-	130	-	%	Vo = 0.9 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK5_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK5}	-	0.47	-	µH	*(Note 2)*
Output Capacitance	C_{OBK5}	22	44	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

5.2.3.3. BUCK5 Control

Table 5-13. BUCK5_CTRL - BUCK5 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK5_CTRL	R/W	-	-	-	-	BUCK5_PWM_FIX	-	BUCK5_SEL	BUCK5_EN	0x02	0x09

Bit	Name	Function	Initial
D[3]	BUCK5_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK5_SEL	BUCK5 control select bit 0 = BUCK5 ON/OFF is controlled by state machine. 1 = BUCK5 ON/OFF is controlled by D[0] on this register.	1
D[0]	BUCK5_EN	BUCK5 control bit with condition of D[1] 0 = BUCK5 OFF 1 = BUCK5 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0

Table 5-14. BUCK5_VOLT - BUCK5 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK5_VOLT	R/W	BUCK5_VOLT_SEL[1:0]		-	-	-	BUCK5_VOLT[2:0]			0x02	0x14

Bit	Name	Function	Initial
D[7:6]	BUCK5_VOLT_SEL[1:0]	Select the BUCK5 voltage range set by D[2:0]. 00 = 0.70 V to 1.35 V 01 = 0.55 V to 0.90 V 10 = 0.675 V to 1.325 V 11 = reserved	00
D[2:0]	BUCK5_VOLT[2:0]	BUCK5 voltage If D[7:6]=00 000 = 0.70 V 001 = 0.80 V 010 = 0.90 V (Initial) 011 = 1.00 V 100 = 1.05 V 101 = 1.10 V 110 = 1.20 V 111 = 1.35 V If D[7:6]=01 000 = 0.55 V 001 = 0.60 V 010 = 0.65 V 011 = 0.70 V 100 = 0.75 V 101 = 0.80 V 110 = 0.85 V 111 = 0.90 V If D[7:6]=10 000 = 0.675 V 001 = 0.775 V 010 = 0.875 V 011 = 0.975 V 100 = 1.025 V 101 = 1.075 V 110 = 1.175 V 111 = 1.325 V	010

5.2.4. BUCK6

5.2.4.1. BUCK6 Block Diagram

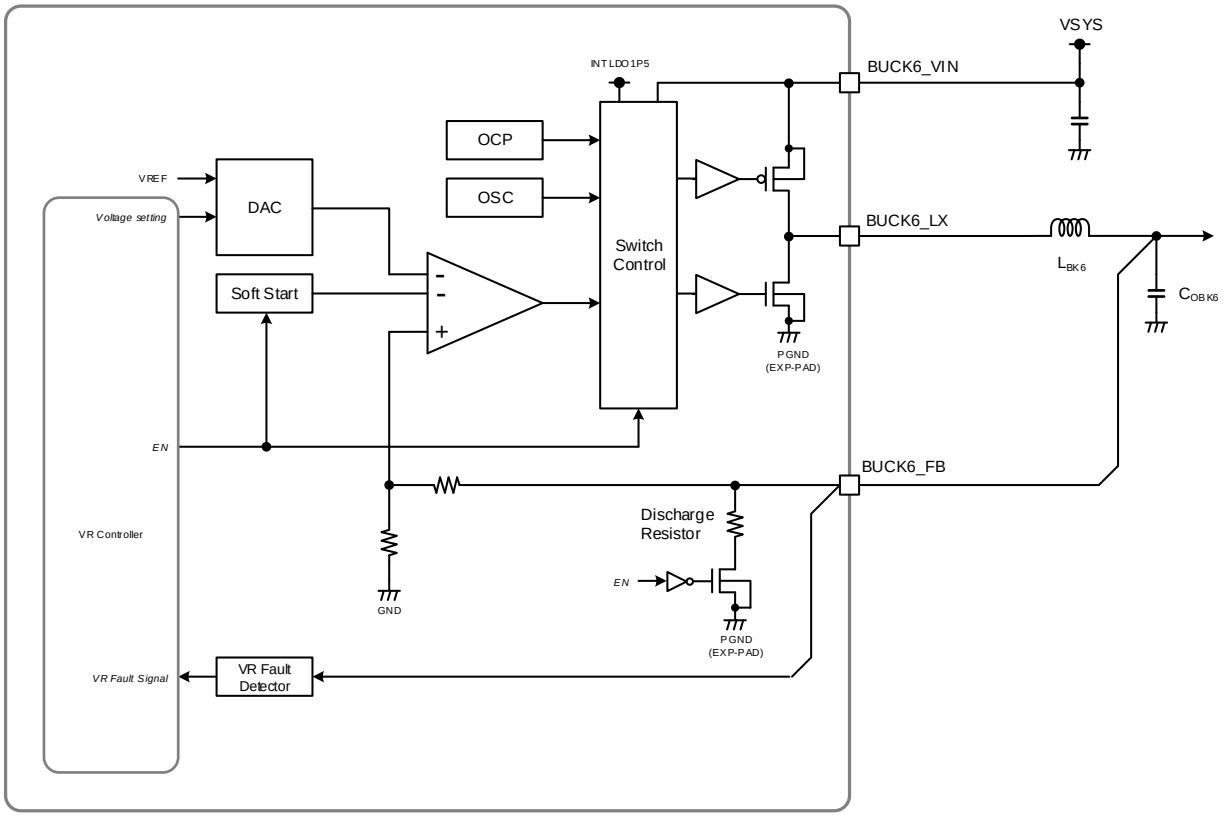


Figure 5-4. BUCK6 Block Diagram

5.2.4.2. BUCK6 Electrical Characteristics

Table 5-15. BUCK6 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK6}	3.267	3.300	3.333	V	Vo=3.3 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK6}	2.6	-	3.3	V	100 mV step
Quiescent Current	I_{Q_BK6}	-	9	-	µA	Vo=3.3 V Io=0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK6}	3000	-	-	mA	
Over Current Protection	I_{OCP_BK6}	4500	-	-	mA	Peak current of inductor *(Note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK6}	-1	0	+1	%	Io=1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK6_1mA}	-	93	-	%	Io = 1 mA, Vo=3.3 V
	η_{BK6_500mA}	-	95	-	%	Io = 500 mA, Vo=3.3 V
	η_{BK6_max}	-	88	-	%	Io = Iomax, Vo=3.3 V
Oscillating Frequency	f_{SW_BK6}	-	1.5	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK6}	-	240	500	µs	During EN to 90% of nominal Voltage
Discharge Resistance	R_{D_BK6}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK6_L}	-	80	-	%	Vo = 3.3 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK6_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK6_H}	-	130	-	%	Vo = 3.3 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK6_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK6}	-	1	-	µH	*(Note 2)*
Output Capacitance	C_{OBK6}	15.4	44	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

Headroom for BUCK6

BUCK6 can't maintain output voltage when the input voltage close to output voltage. The headroom voltage is determined by output current and the impedance from VSYS to BUCK6 output including the inductor parasitic impedance (DCR). The PMIC internal impedance from BUCK6_VIN to BUCK6_LX is 121 mΩ at the worst case. Please calculate total impedance using this value, and secure enough headroom for VSYS according to the output current and voltage.

(Example – ROHM Evaluation Board case)

Vo = 3.3V setting: V_O
VSYS to BUCK6_VIN impedance of the EVB = 3 mΩ: R_{VIN}
BUCK6_LX to inductor impedance of the EVB = 6 mΩ: R_{LX}
Inductor parasitic impedance (DCR) = 45 mΩ: R_{IND}
PMIC internal impedance from BUCK6_VIN to BUCK6_LX = 121 mΩ: R_{PMIC}
Total impedance = 175 mΩ: $R_{TOTAL}=R_{VIN}+R_{LX}+R_{IND}+R_{PMIC}$
Headroom = R_{TOTAL} x Output Current

Output current	Required minimum VSYS voltage
1.0 A	3.475 V
2.0 A	3.650 V
3.0 A	3.825 V

5.2.4.3. BUCK6 Control

Table 5-16. BUCK6_CTRL - BUCK6 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK6_CTRL	R/W	-	-	-	-	BUCK6_PWM_FIX	-	BUCK6_SEL	BUCK6_EN	0x00	0x0A

Bit	Name	Function	Initial
D[3]	BUCK6_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK6_SEL	BUCK6 control select bit 0 = BUCK6 ON/OFF is controlled by state machine. 1 = BUCK6 ON/OFF is controlled by D[0] on this register.	0
D[0]	BUCK6_EN	BUCK6 control bit with condition of D[1] 0 = BUCK6 OFF 1 = BUCK6 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0

Table 5-17. BUCK6_VOLT - BUCK6 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK6_VOLT	R/W	-	BUCK6_VOLT_SEL	-	-	-	-	BUCK6_VOLT[1:0]		0x03	0x15

Bit	Name	Function	Initial
D[6]	BUCK6_VOLT_SEL	Select the BUCK6 voltage range set by D[6]. 0 =3.0 V to 3.3 V 1 = 2.6 V to 2.9 V Note: Changing BUCK6 voltage value is not allowed when BUCK6 is still ON. In the case where this register value is changed, BUCK6 should be turned OFF.	0
D[1:0]	BUCK6_VOLT[1:0]	BUCK6 voltage If D[6]=0 00 = 3.0 V 01 = 3.1 V 10 = 3.2 V 11 = 3.3 V(Initial) If D[6]=1 00 = 2.6 V 01 = 2.7 V 10 = 2.8 V 11 = 2.9 V Note: Changing BUCK6 voltage value is not allowed when BUCK6 is still ON. In the case where this register value is changed, BUCK6 should be turned OFF.	11

5.2.5. BUCK7

5.2.5.1. BUCK7 Block Diagram

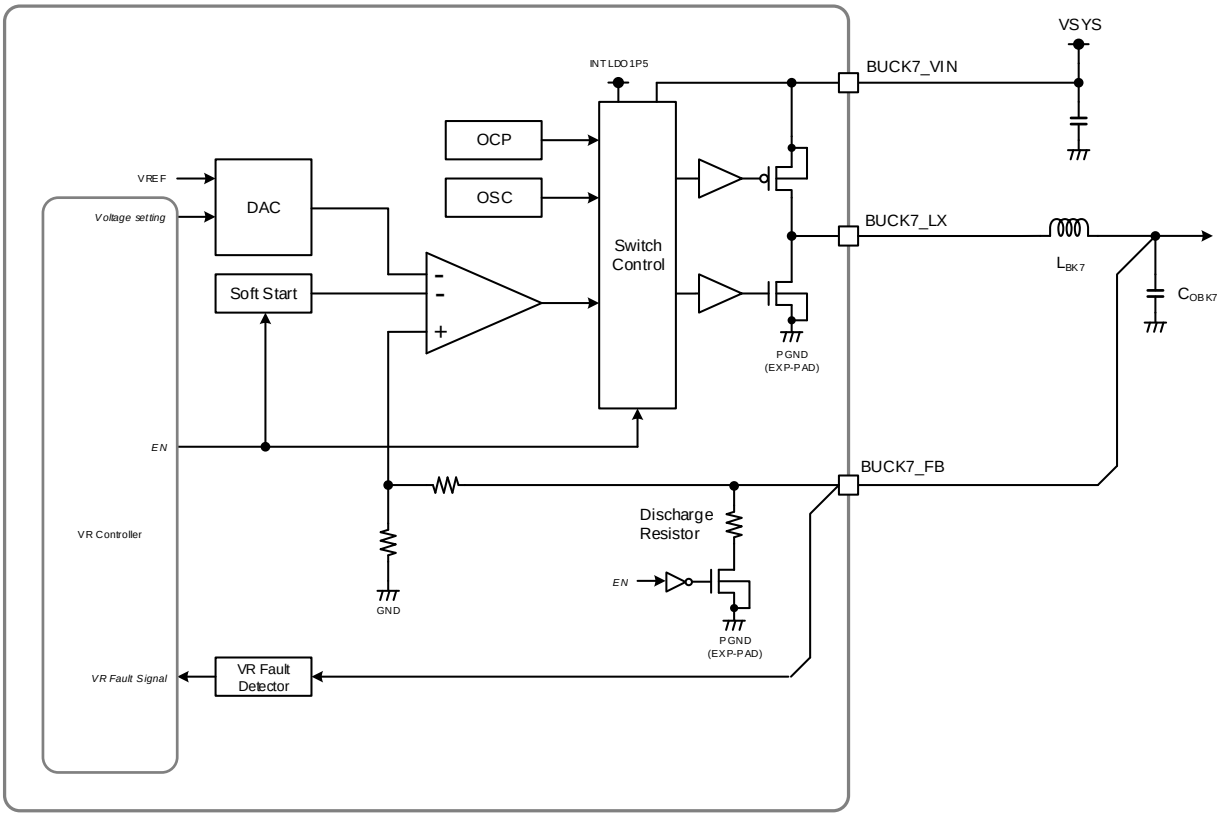


Figure 5-5. BUCK7 Block Diagram

5.2.5.2. BUCK7 Electrical Characteristics

Table 5-18. BUCK7 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK7}	1.782	1.800	1.818	V	Vo = 1.8 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK7}	1.605	-	1.995	V	1.605 V, 1.695 V, 1.755 V, 1.800 V, 1.845 V, 1.905 V, 1.950 V, 1.995 V
Quiescent Current	I_{Q_BK7}	-	15	-	µA	Vo = 1.8 V Io = 0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK7}	1500	-	-	mA	
Over Current Protection	I_{OCP_BK7}	3000	-	-	mA	Peak current of inductor *(Note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK7}	-1	0	+1	%	Io = 1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK7_1mA}	-	85	-	%	Io = 1 mA, Vo=1.8 V
	η_{BK7_500mA}	-	89	-	%	Io = 500 mA, Vo=1.8 V
	η_{BK7_max}	-	85	-	%	Io = Iomax, Vo=1.8 V
Oscillating Frequency	f_{SW_BK7}	-	2	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK7}	-	220	500	µs	During EN to 90 % of nominal Voltage
Discharge Resistance	R_{D_BK7}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK7_L}	-	80	-	%	Vo = 1.8 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK7_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK7_H}	-	130	-	%	Vo = 1.8 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK7_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK7}	-	0.47	-	µH	*(Note 2)*
Output Capacitance	C_{OBK7}	11	22	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

5.2.5.3. BUCK7 Control

Table 5-19. BUCK7_CTRL - BUCK7 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK7_CTRL	R/W	-	-	-	-	BUCK7_PWM_FIX	-	BUCK7_SEL	BUCK7_EN	0x00	0x0B

Bit	Name	Function	Initial
D[3]	BUCK7_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK7_SEL	BUCK7 control select bit 0 = BUCK7 ON/OFF is controlled by state machine. 1 = BUCK7 ON/OFF is controlled by D[0] on this register.	0
D[0]	BUCK7_EN	BUCK7 control bit with condition of D[1] 0 = BUCK7 OFF 1 = BUCK7 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0

Table 5-20. BUCK7_VOLT - BUCK7 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK7_VOLT	R/W	-	-	-	-	-	BUCK7_VOLT[2:0]			0x03	0x16

Bit	Name	Function	Initial
D[2:0]	BUCK7_VOLT[2:0]	BUCK7 voltage 000 = 1.605 V 001 = 1.695 V 010 = 1.755 V 011 = 1.800 V (Initial) 100 = 1.845 V 101 = 1.905 V 110 = 1.950 V 111 = 1.995 V Note: Changing BUCK7 voltage value is not allowed when BUCK7 is still ON. In the case where this register value is changed, BUCK7 should be turned OFF.	011

5.2.6. BUCK8

5.2.6.1. BUCK8 Block Diagram

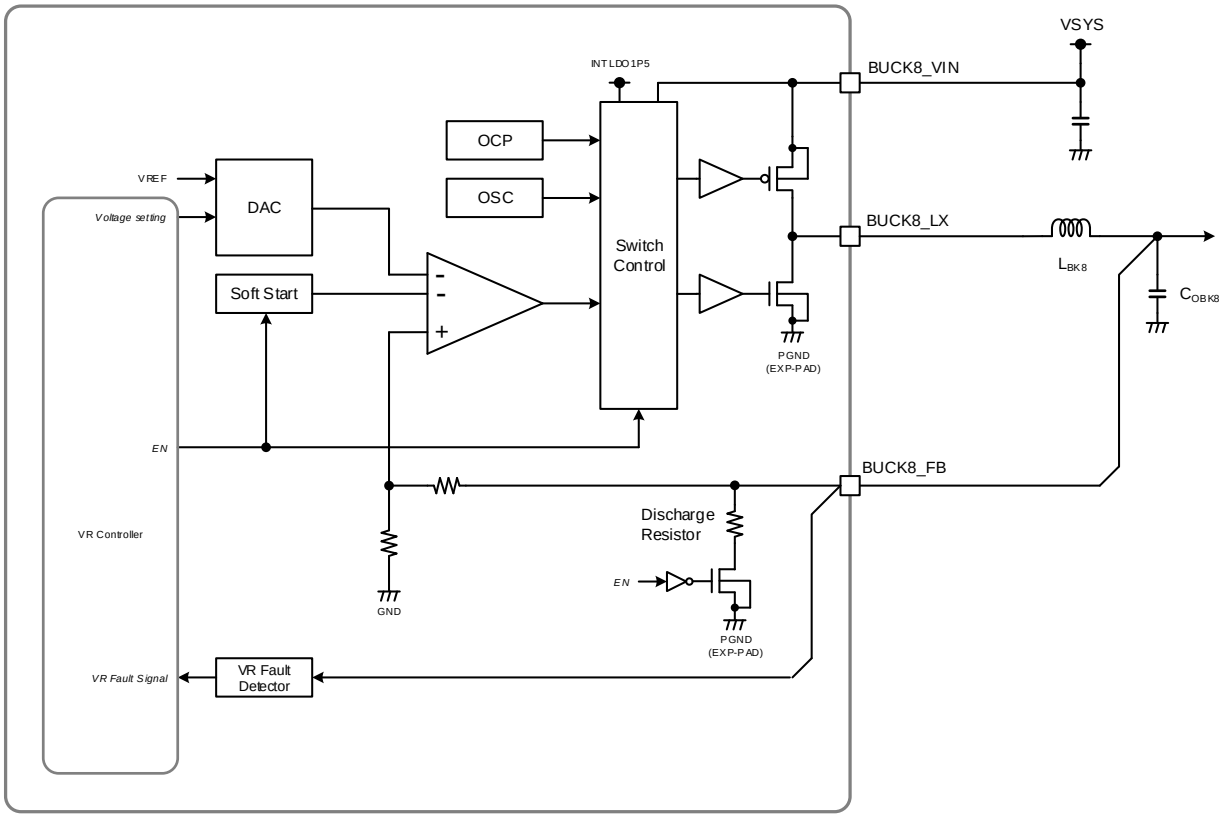


Figure 5-6. BUCK8 Block Diagram

5.2.6.2. BUCK8 Electrical Characteristics

Table 5-21. BUCK8 Electrical Characteristics

(Unless otherwise specified, Ta=+25 °C, VSYS=5.0 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_BK8}	1.089	1.100	1.111	V	Vo = 1.1 V Io = 200 mA, PWM fix Mode
Programmable Output Voltage Range	V_{ORG_BK8}	0.8	-	1.4	V	10 mV step
Quiescent Current	I_{Q_BK8}	-	15	-	µA	Vo = 1.1 V Io = 0 mA, Auto mode
Maximum Output Current	I_{OMAX_BK8}	3000	-	-	mA	
Over Current Protection	I_{OCP_BK8}	4500	-	-	mA	Peak current of inductor *(note 1)*
DC Output Voltage Load Regulation	ΔV_{LDR_BK8}	-1	0	+1	%	Io = 1 mA to Iomax, PWM fix Mode
Efficiency	η_{BK8_1mA}	-	82	-	%	Io = 1 mA, Vo=1.1 V
	η_{BK8_500mA}	-	86	-	%	Io = 500 mA, Vo=1.1 V
	η_{BK8_max}	-	75	-	%	Io = Iomax, Vo=1.1 V
Oscillating Frequency	f_{SW_BK8}	-	2	-	MHz	PWM fix mode, Io = 0 mA
Start up Time	t_{ST_BK8}	-	200	500	µs	During EN to 90 % of nominal Voltage
Discharge Resistance	R_{D_BK8}	-	100	-	Ω	
Low Side VR Fault Detect Level	D_{VRFBK8_L}	-	80	-	%	Vo = 1.1 V (FB = Sweep down) VR fault detect level / Vo x 100
Low Side VR Fault Detect Hysteresis	D_{VRFBK8_LHYS}	-	10	-	%	(VR fault release level - detect level) / Vo x 100
High Side VR Fault Detect Level	D_{VRBK8_H}	-	130	-	%	Vo = 1.1 V (FB = Sweep up) Power good detect level / Vo x 100
High Side VR Fault Detect Hysteresis	D_{VRFBK8_HHYS}	-	20	-	%	(VR fault detect level - release level) / Vo x 100
Output Inductance	L_{BK8}	-	0.47	-	µH	*(Note 2)*
Output Capacitance	C_{OBK8}	22	44	100	µF	*(Note 2)* Effective capacitance with BUCK's DC bias

(Note 1) For Buck- DCDC converters, (minimum Over Current Protection Current – ½ inductor ripple current) is the maximum output current.

(Note 2) This part value range need to be guaranteed over the operating surrounding temperature.

5.2.6.3. BUCK8 Control

Table 5-22. BUCK8_CTRL - BUCK8 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK8_CTRL	R/W	-	-	-	-	BUCK8_PWM_FIX	-	BUCK8_SEL	BUCK8_EN	0x00	0x0C

Bit	Name	Function	Initial
D[3]	BUCK8_PWM_FIX	0 – AUTO PWM/PFM mode VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0
D[1]	BUCK8_SEL	BUCK8 control select bit 0 = BUCK8 ON/OFF is controlled by state machine. 1 = BUCK8 ON/OFF is controlled by D[0] on this register.	0
D[0]	BUCK8_EN	BUCK8 control bit with condition of D[1] 0 = BUCK8 OFF 1 = BUCK8 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0

Table 5-23. BUCK8_VOLT - BUCK8 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK8_VOLT	R/W	-	BUCK8_VOLT[6:0]							0x1E	0x17

Bit	Name	Function	Initial
D[6:0]	BUCK8_VOLT[6:0]	BUCK8 voltage 0x00 = 0.80 V 0x01 = 0.81 V 0x02 = 0.82 V 0x03 = 0.83 V 0x04 = 0.84 V 0x05 = 0.85 V 0x06 = 0.86 V 0x07 = 0.87 V 0x08 = 0.88 V 0x09 = 0.89 V 0x0A = 0.90 V 0x0B = 0.91 V 0x0C = 0.92 V 0x0D = 0.93 V 0x0E = 0.94 V 0x0F = 0.95 V 0x10 = 0.96 V 0x11 = 0.97 V 0x12 = 0.98 V 0x13 = 0.99 V 0x14 = 1.00 V 0x15 = 1.01 V 0x16 = 1.02 V 0x17 = 1.03 V 0x18 = 1.04 V 0x19 = 1.05 V 0x1A = 1.06 V 0x1B = 1.07 V 0x1C = 1.08 V 0x1D = 1.09 V 0x1E = 1.10 V (initial) 0x1F = 1.11 V 0x20 = 1.12 V 0x21 = 1.13 V 0x22 = 1.14 V 0x23 = 1.15 V 0x24 = 1.16 V 0x25 = 1.17 V 0x26 = 1.18 V 0x27 = 1.19 V 0x28 = 1.20 V 0x29 = 1.21 V 0x2A = 1.22 V 0x2B = 1.23 V 0x2C = 1.24 V 0x2D = 1.25 V 0x2E = 1.26 V 0x2F = 1.27 V 0x30 = 1.28 V 0x31 = 1.29 V 0x32 = 1.30 V 0x33 = 1.31 V 0x34 = 1.32 V 0x35 = 1.33 V 0x36 = 1.34 V 0x37 = 1.35 V 0x38 = 1.36 V 0x39 = 1.37 V 0x3A = 1.38 V 0x3B = 1.39 V 0x3C = 1.40 V 0x3D-0x7F = reserved	0011110

5.3. Details of LDO

5.3.1. LDO1

5.3.1.1. LDO1 Block Diagram

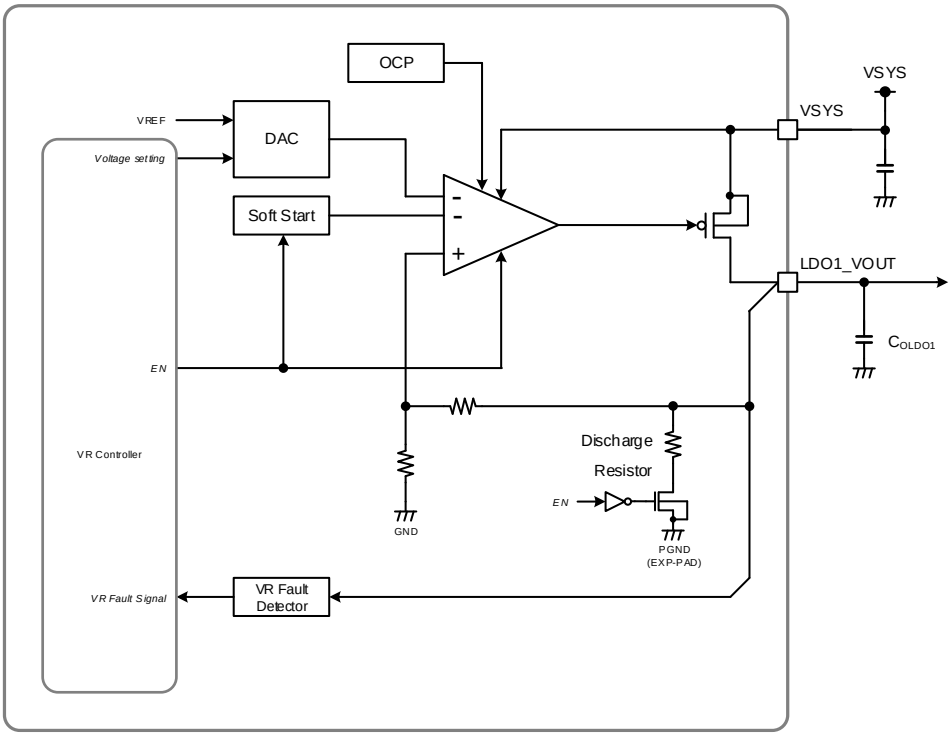


Figure 5-7. LDO1 Block Diagram

5.3.1.2. LDO1 Electrical Characteristics

Table 5-24. LDO1 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 1.8 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO1}	1.782	1.800	1.818	V	V_O=1.8 V setting Io=1 mA
Output Voltage Range 1	$V_{ORG\_LDO1\_1}$	1.600	-	1.900	V	100 mV step
Output Voltage Range 2	$V_{ORG\_LDO1\_2}$	3.000	-	3.300	V	100 mV step
Maximum Output Current	I_{OMAX_LDO1}	10	-	-	mA	
Over Current Protection	I_{OCP_LDO1}	20	-	-	mA	
Quiescent Current	I_{Q_LDO1}	-	6	-	µA	Io=0 mA
Dropout Voltage	ΔV_{ODP_LDO1}	-	40	-	mV	Io = Iomax VSYS=3.2 V, V_O=3.3 V setting
Start up Time	t_{ST_LDO1}	-	440	1000	µs	Io=0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO1}	-	10	20	mV	Io=1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO1}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io=Iomax
Discharge Resistance	R_{DIS_LDO1}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO1}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO1\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO1}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO1}	0.5	1.0	5.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.1.3. LDO1 Control

Table 5-25. LDO1_VOLT - LDO1 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO1_VOLT	R/W	LDO1_SEL	LDO1_EN	LDO1_VOLT_SEL	-	-	-	LDO1_VOLT[1:0]		0x22	0x18

Bit	Name	Function	Initial
D[7]	LDO1_SEL	LDO1 control select bit 0 = LDO1 ON/OFF is controlled by state machine. 1 = LDO1 ON/OFF is controlled by D[6] on this register.	0
D[6]	LDO1_EN	LDO1 control bit with condition of D[7] 0 = LDO1 OFF 1 = LDO1 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[5]	LDO1_VOLT_SEL	Select the LDO1 voltage range set by D[1:0]. 0 = 3.0 V to 3.3 V 1 = 1.6 V to 1.9 V Note: Changing LDO1 voltage value is not allowed when LDO1 is still ON. In the case where this register value is changed, LDO1 should be turned OFF.	1
D[1:0]	LDO1_VOLT[1:0]	LDO1 voltage If D[5]=0, 00 = 3.0 V 01 = 3.1 V 10 = 3.2 V 11 = 3.3 V If D[5]=1, 00 = 1.6 V 01 = 1.7 V 10 = 1.8 V (Initial) 11 = 1.9 V Note: Changing LDO1 voltage value is not allowed when LDO1 is still ON. In the case where this register value is changed, LDO1 should be turned OFF.	10

5.3.2. LDO2

5.3.2.1. LDO2 Block Diagram

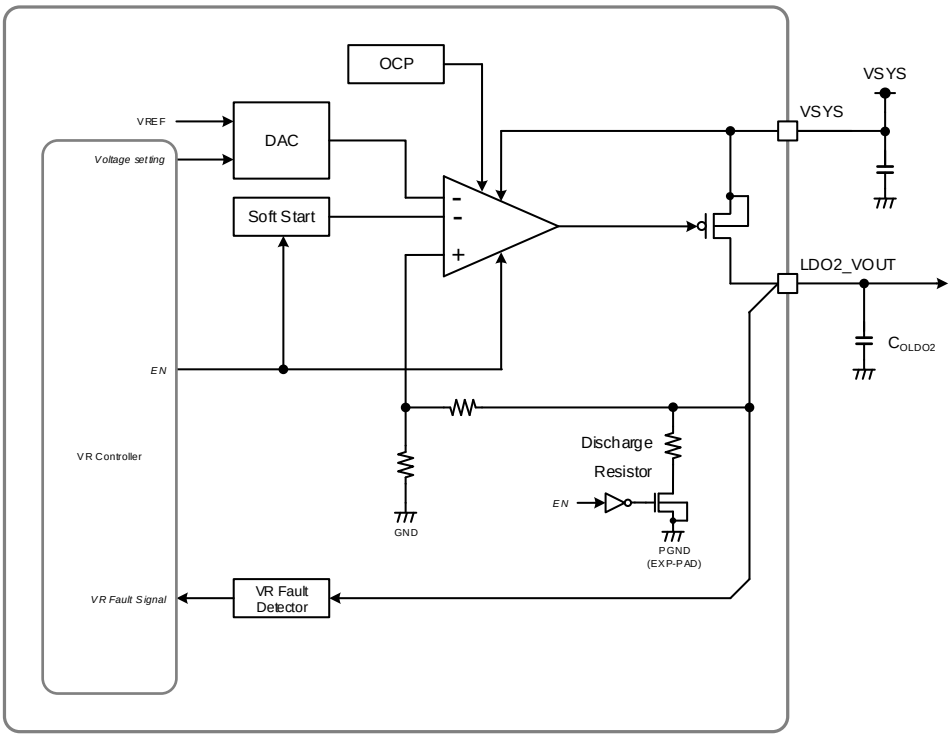


Figure 5-8. LDO2 Block Diagram

5.3.2.2. LDO2 Electrical Characteristics

Table 5-26. LDO2 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 0.8 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO2}	0.785	0.800	0.815	V	V_O=0.8 V setting Io=1 mA
Output Voltage Range	V_{ORG_LDO2}	0.800	-	0.900	V	100 mV step
Maximum Output Current	I_{OMAX_LDO2}	10	-	-	mA	
Over Current Protection	I_{OCP_LDO2}	20	-	-	mA	
Quiescent Current	I_{Q_LDO2}	-	6	-	µA	Io = 0 mA
Start up Time	t_{ST_LDO2}	-	370	1000	µs	Io = 0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO2}	-	10	20	mV	Io = 1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO2}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io = Iomax
Discharge Resistance	R_{DIS_LDO2}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO2}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO2\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO2}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO2}	0.5	1.0	5.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.2.3. LDO2 Control

Table 5-27. LDO2_VOLT - LDO2 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO2_VOLT	R/W	LDO2_SEL	LDO2_EN	LDO2_VOLT_SEL	-	-	-	-	-	0x20	0x19

Bit	Name	Function	Initial
D[7]	LDO2_SEL	LDO2 control select bit 0 = LDO2 ON/OFF is controlled by state machine. 1 = LDO2 ON/OFF is controlled by D[6] on this register.	0
D[6]	LDO2_EN	LDO2 control bit with condition of D[7] 0 = LDO2 OFF 1 = LDO2 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[5]	LDO2_VOLT_SEL	Select the LDO2 voltage. 0 = 0.9V 1 = 0.8V (initial) Note: Changing LDO2 voltage value is not allowed when LDO2 is still ON. In the case where this register value is changed, LDO2 should be turned OFF.	1

5.3.3. LDO3

5.3.3.1. LDO3 Block Diagram

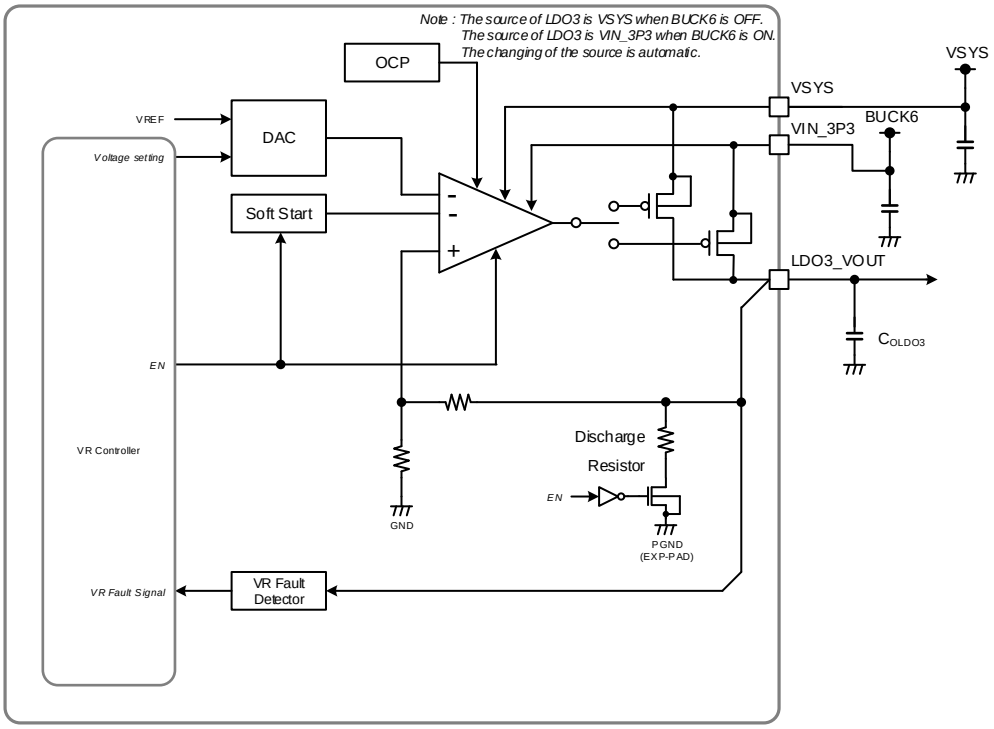


Figure 5-9. LDO3 Block Diagram

5.3.3.2. LDO3 Electrical Characteristics

Table 5-28. LDO3 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 1.8 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO3}	1.782	1.800	1.818	V	V_O=1.8 V setting Io=1 mA
Output Voltage Range	V_{ORG_LDO3}	1.800	-	3.300	V	100 mV step
Maximum Output Current	I_{OMAX_LDO3}	300	-	-	mA	
Over Current Protection	I_{OCP_LDO3}	390	-	-	mA	
Quiescent Current	I_{Q_LDO3}	-	9	-	µA	Io = 0 mA
Dropout Voltage	ΔV_{ODP_LDO3}	-	450	-	mV	Io = Iomax VIN_3P3 = 1.7 V, V_O = 1.8V setting
Start up Time	t_{ST_LDO3}	-	310	1000	µs	Io = 0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO3}	-	10	20	mV	Io = 1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO3}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io = 50 mA
Discharge Resistance	R_{DIS_LDO3}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO3}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO3\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO3}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO3}	1.1	2.2	22.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.3.3. LDO3 Control

Table 5-29. LDO3_VOLT - LDO3 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO3_VOLT	R/W	LDO3_SEL	LDO3_EN	-	-	LDO3_VOLT[3:0]				0x00	0x1A

Bit	Name	Function	Initial
D[7]	LDO3_SEL	LDO3 control select bit 0 = LDO3 ON/OFF is controlled by state machine. 1 = LDO3 ON/OFF is controlled by D[6] on this register.	0
D[6]	LDO3_EN	LDO3 control bit with condition of D[7] 0 = LDO3 OFF 1 = LDO3 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[3:0]	LDO3_VOLT[3:0]	LDO3 voltage 0x0 = 1.8 V (Initial) 0x1 = 1.9 V 0x2 = 2.0 V 0x3 = 2.1 V 0x4 = 2.2 V 0x5 = 2.3 V 0x6 = 2.4 V 0x7 = 2.5 V 0x8 = 2.6 V 0x9 = 2.7 V 0xA = 2.8 V 0xB = 2.9 V 0xC = 3.0 V 0xD = 3.1 V 0xE = 3.2 V 0xF = 3.3 V Note: Changing LDO3 voltage value is not allowed when LDO3 is still ON. In the case where this register value is changed, LDO3 should be turned OFF.	0000

It is recommended that the VIN_3P3 pin is connected to BUCK6. LDO3 power source is switched from the VSYS pin to the VIN_3P3 pin after BUCK6 is turned on. On the other hand, LDO3 power source is switched from the VIN_3P3 pin to the VSYS pin when BUCK6 is turned off. It takes 3 ms to complete this switching operation. Therefore, actual BUCK6 turn-off is delayed as shown in Figure 5-10.

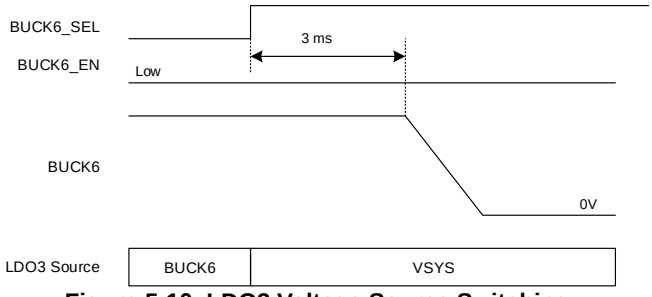


Figure 5-10. LDO3 Voltage Source Switching

5.3.4. LDO4

5.3.4.1. LDO4 Block Diagram

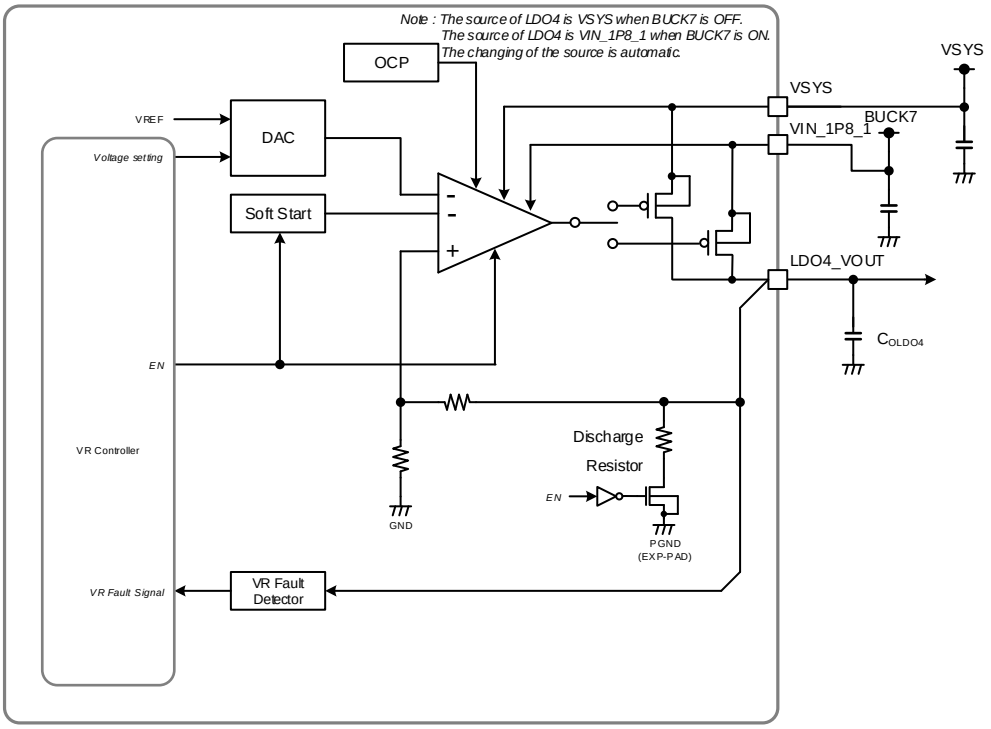


Figure 5-11. LDO4 Block Diagram

5.3.4.2. LDO4 Electrical Characteristics

Table 5-30. LDO4 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 0.9 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO4}	0.885	0.900	0.915	V	V_O=0.9 V setting Io=1 mA
Output Voltage Range	V_{ORG_LDO4}	0.900	-	1.800	V	100 mV step
Maximum Output Current	I_{OMAX_LDO4}	250	-	-	mA	
Over Current Protection	I_{OCP_LDO4}	325	-	-	mA	
Quiescent Current	I_{Q_LDO4}	-	9	-	µA	Io = 0 mA
Dropout Voltage	ΔV_{ODP_LDO4}	-	450	-	mV	Io = Iomax VIN_V1P8_1 = 1.7 V, V_O = 1.8 V setting
Start up Time	t_{ST_LDO4}	-	400	1000	µs	Io = 0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO4}	-	10	20	mV	Io = 1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO4}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io = 50 mA
Discharge Resistance	R_{DIS_LDO4}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO4}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO4\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO4}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO4}	1.1	2.2	22.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.4.3. LDO4 Control

Table 5-31. LDO4_VOLT - LDO4 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO4_VOLT	R/W	LDO4_SEL	LDO4_EN	-	-	LDO4_VOLT[3:0]				0x80	0x1B

Bit	Name	Function	Initial
D[7]	LDO4_SEL	LDO4 control select bit 0 = LDO4 ON/OFF is controlled by state machine. 1 = LDO4 ON/OFF is controlled by D[6] on this register.	1
D[6]	LDO4_EN	LDO4 control bit with condition of D[7] 0 = LDO4 OFF 1 = LDO4 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[3:0]	LDO4_VOLT[3:0]	LDO4 voltage 0x0 = 0.9 V (Initial) 0x1 = 1.0 V 0x2 = 1.1 V 0x3 = 1.2 V 0x4 = 1.3 V 0x5 = 1.4 V 0x6 = 1.5 V 0x7 = 1.6 V 0x8 = 1.7 V 0x9 = 1.8 V 0xA = 1.8 V 0xB = 1.8 V 0xC = 1.8 V 0xD= 1.8 V 0xE = 1.8 V 0xF = 1.8 V Note: Changing LDO4 voltage value is not allowed when LDO4 is still ON. In the case where this register value is changed, LDO4 should be turned OFF.	0000

It is recommended that the VIN_1P8_1 pin is connected to BUCK7. LDO4 power source is switched from the VSYS pin to the VIN_1P8_1 pin after BUCK7 is turned on. On the other hand, LDO4 power source is switched from the VIN_1P8_1 pin to the VSYS pin when BUCK7 is turned off. It takes 3 ms to complete this switching operation. Therefore, actual BUCK7 turn-off is delayed as shown in Figure 5-12.

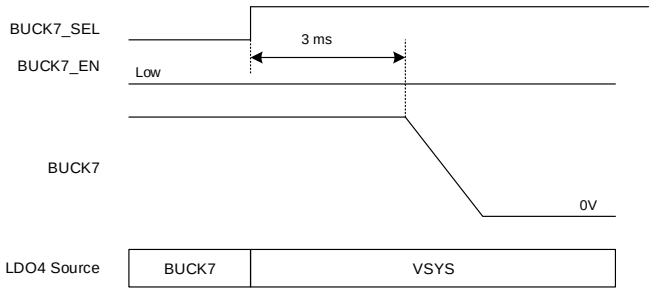


Figure 5-12. LDO4 Voltage Source Switching

5.3.5. LDO5

5.3.5.1. LDO5 Block Diagram

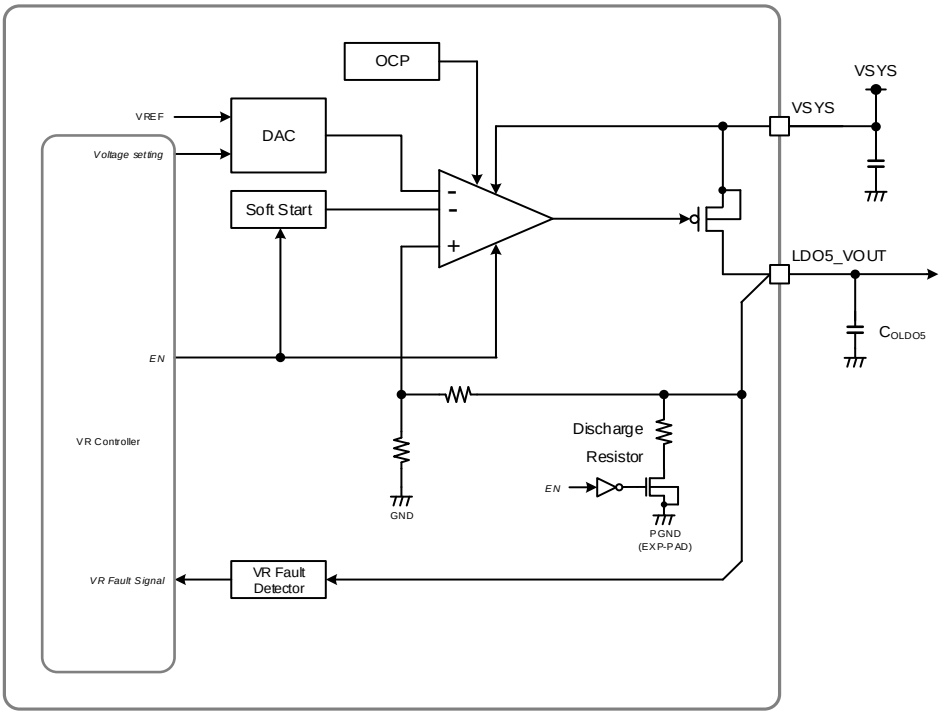


Figure 5-13. LDO5 Block Diagram

5.3.5.2. LDO5 Electrical Characteristics

Table 5-32. LDO5 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 3.3 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO5}	3.267	3.300	3.333	V	V_O=3.3 V setting Io=1 mA
Output Voltage Range	V_{ORG_LDO5}	0.800	-	3.300	V	100 mV step
Maximum Output Current	I_{OMAX_LDO5}	300	-	-	mA	
Over Current Protection	I_{OCP_LDO5}	340	-	-	mA	
Quiescent Current	I_{Q_LDO5}	-	9	-	µA	Io = 0 mA
Dropout Voltage	ΔV_{ODP_LDO5}	-	250	-	mV	Io = Iomax VSYS = 3.2 V, V_O = 3.3 V setting
Start up Time	t_{ST_LDO5}	-	530	1000	µs	Io = 0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO5}	-	10	20	mV	Io = 1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO5}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io = 50 mA
Discharge Resistance	R_{DIS_LDO5}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO5}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO5\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO5}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO5}	1.1	2.2	22.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.5.3. LDO5 Control

Table 5-33. LDO5_VOLT - LDO5 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO5_VOLT	R/W	LDO5_SEL	LDO5_EN	LDO5_VOLT_SEL	-	LDO5_VOLT[3:0]				0x8F	0x1C

Bit	Name	Function	Initial
D[7]	LDO5_SEL	LDO5 control select bit 0 = LDO5 ON/OFF is controlled by state machine. 1 = LDO5 ON/OFF is controlled by D[6] on this register.	1
D[6]	LDO5_EN	LDO5 control bit with condition of D[7] 0 = LDO5 OFF 1 = LDO5 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[5]	LDO5_VOLT_SEL	Select the LDO5 voltage range set by D[1:0]. 0 = 1.8 V to 3.3 V 1 = 0.8 V to 2.3 V Note: Changing LDO5 voltage value is not allowed when LDO5 is still ON. In the case where this register value is changed, LDO5 should be turned OFF.	0
D[3:0]	LDO5_VOLT[3:0]	LDO5 voltage if D[5]=0, 0x0 = 1.8 V 0x1 = 1.9 V 0x2 = 2.0 V 0x3 = 2.1 V 0x4 = 2.2 V 0x5 = 2.3 V 0x6 = 2.4 V 0x7 = 2.5 V 0x8 = 2.6 V 0x9 = 2.7 V 0xA = 2.8 V 0xB = 2.9 V 0xC = 3.0 V 0xD= 3.1 V 0xE = 3.2 V 0xF = 3.3 V(initial) if D[5]=1, 0x0 = 0.8 V 0x1 = 0.9 V 0x2 = 1.0 V 0x3 = 1.1 V 0x4 = 1.2 V 0x5 = 1.3 V 0x6 = 1.4 V 0x7 = 1.5 V 0x8 = 1.6 V 0x9 = 1.7 V 0xA = 1.8 V 0xB = 1.9 V 0xC = 2.0 V 0xD= 2.1 V 0xE = 2.2 V 0xF = 2.3 V Note: Changing LDO5 voltage value is not allowed when LDO5 is still ON. In the case where this register value is changed, LDO5 should be turned OFF.	1111

5.3.6. LDO6

5.3.6.1. LDO6 Block Diagram

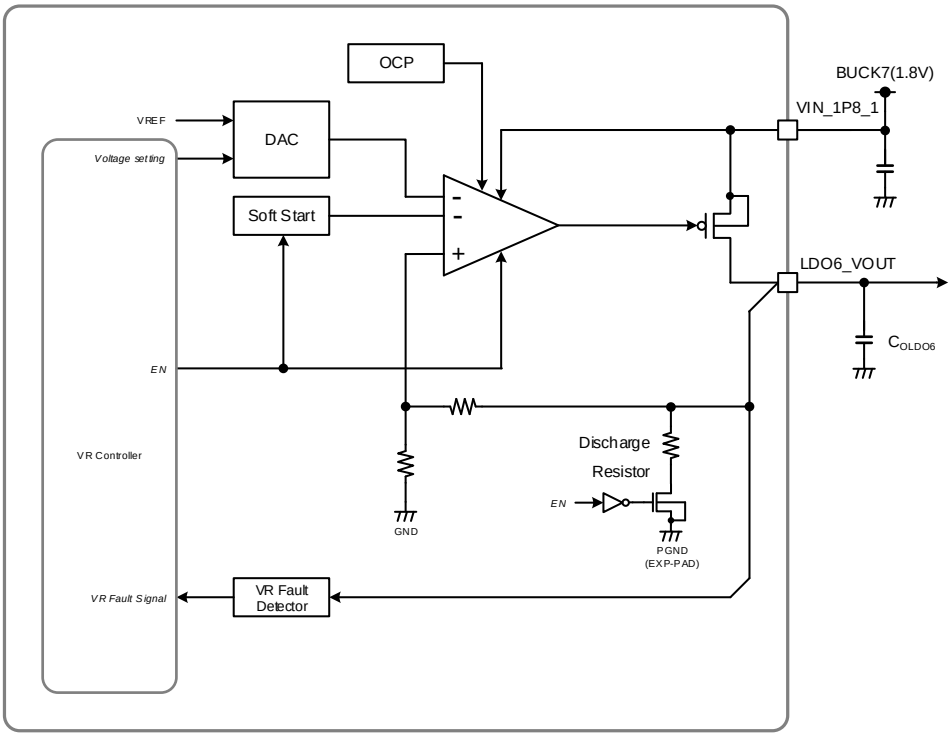


Figure 5-14. LDO6 Block Diagram

5.3.6.2. LDO6 Electrical Characteristics

Table 5-34. LDO6 Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_1 = 1.8 V, Vo = 1.2 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Voltage	V_{O_LDO6}	1.185	1.200	1.215	V	V_O=1.2 V setting Io=1 mA
Output Voltage Range	V_{ORG_LDO6}	0.900	-	1.800	V	100 mV step
Maximum Output Current	I_{OMAX_LDO6}	300	-	-	mA	
Over Current Protection	I_{OCP_LDO6}	340	-	-	mA	
Quiescent Current	I_{Q_LDO6}	-	9	-	µA	Io = 0 mA
Dropout Voltage	ΔV_{ODP_LDO6}	-	450	-	mV	Io = Iomax VIN_V1P8_1 = 1.7 V, V_O = 1.8 V setting
Start up Time	t_{ST_LDO6}	-	400	1000	µs	Io = 0 mA, During EN to 90 % of nominal Voltage
DC Output Voltage Load Regulation	ΔV_{LDR_LDO6}	-	10	20	mV	Io = 1 mA to Iomax
DC Output Voltage Line Regulation	ΔV_{LNR_LDO6}	-	2	5	mV	VSYS = 4.5 V to 5.5 V, Io = 50 mA
Discharge Resistance	R_{DIS_LDO6}	-	100	200	Ω	
VR Fault Detect Level	$D_{VRFLDO6}$	-	80	-	%	Output = Sweep down Power good detect level / Vo x 100
VR Fault Detect Hysteresis	$D_{VRFLDO6\_HYS}$	-	10	-	%	(VR fault release level - detect level) / Vo x 100
Ripple Rejection Ratio	RR_{LDO6}	-	60	-	dB	VSYS = 5.0 V, I_O=Iomax/2 V_R = -20 dBV, f_R=100 Hz BW=20 Hz to 20 kHz
Output Capacitance	C_{OLDO6}	1.1	2.2	22.0	µF	*(Note 1)* Effective capacitance with LDO's DC bias

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

5.3.6.3. LDO6 Control

Table 5-35. LDO6_VOLT - LDO6 Voltage Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LDO6_VOLT	R/W	LDO6_SEL	LDO6_EN	-	-	LDO6_VOLT[3:0]				0x03	0x1D

Bit	Name	Function	Initial
D[7]	LDO6_SEL	LDO6 control select bit 0 = LDO6 ON/OFF is controlled by state machine. 1 = LDO6 ON/OFF is controlled by D[6] on this register.	0
D[6]	LDO6_EN	LDO6 control bit with condition of D[7] 0 = LDO6 OFF 1 = LDO6 ON This bit returns to 0 at the beginning of PWROFF sequence or emergency shutdown.	0
D[3:0]	LDO6_VOLT[3:0]	LDO6 voltage 0x0 = 0.9 V 0x1 = 1.0 V 0x2 = 1.1 V 0x3 = 1.2 V (initial) 0x4 = 1.3 V 0x5 = 1.4 V 0x6 = 1.5 V 0x7 = 1.6 V 0x8 = 1.7 V 0x9 = 1.8 V 0xA = 1.8 V 0xB = 1.8 V 0xC = 1.8 V 0xD= 1.8 V 0xE = 1.8 V 0xF = 1.8 V Note: Changing LDO6 voltage value is not allowed when LDO6 is still ON. In the case where this register value is changed, LDO6 should be turned OFF.	0011

5.4. MUXSW

MUX Switch is for SD card power.

5.4.1. MUXSW Block Diagram

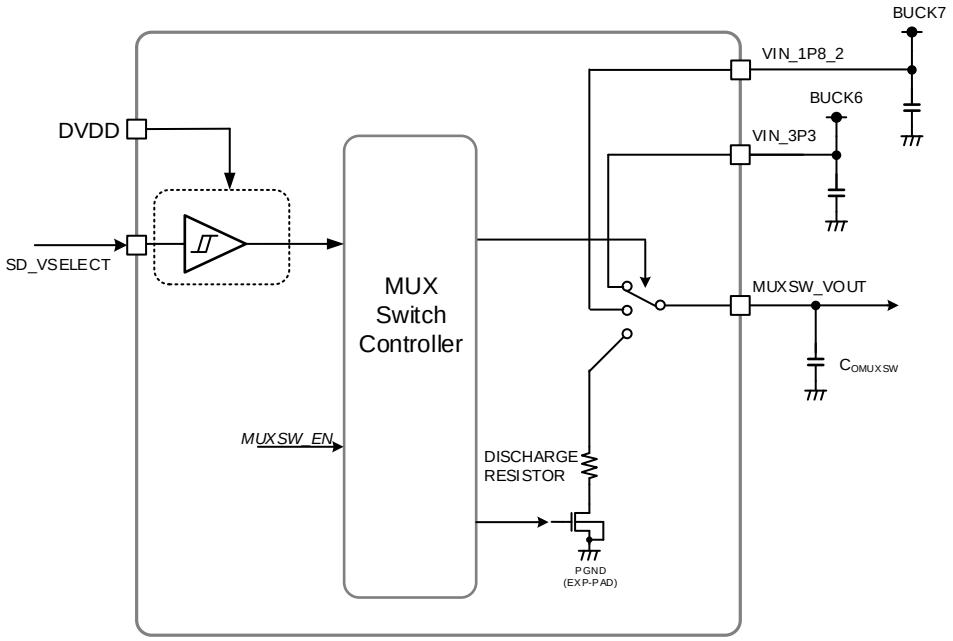


Figure 5-15. MUXSW Block Diagram

5.4.2. MUXSW Electrical Characteristics

Table 5-36. MUXSW Electrical Characteristics

(Unless otherwise specified, Ta = +25 °C, VSYS = 5.0 V, VIN_3P3 = 3.3 V, VIN_1P8_2 = 1.8 V, Vo = 3.3 V setting)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
VIN_3P3 Input Voltage	V_{IN_3P3}	-	3.300	-	V	
Switch ON Resistance(3.3 V mode)	R_{ON_3P3}	-	-	500	mΩ	SD_VSELECT=0 V, VIN_3P3>3.2 V
VIN_1P8_2 Input Voltage	V_{IN_1P8}	-	1.800	-	V	
Switch ON Resistance(1.8 V mode)	R_{ON_1P8}	-	-	500	mΩ	SD_VSELECT=DVDD, VIN_1P8_2>1.7 V
Maximum Output Current	I_{OMAX_MUX}	150	-	-	mA	
Discharge Resistance	R_{DIS_MUX}	-	30	50	Ω	VIN_1P8_2=0 V, VIN_3P3=0 V, I_O=-10 mA
Output Capacitance	C_{O_MUX}	11	22	33	µF	*(Note 1)* Effective capacitance with Output voltage

(Note 1) This part value range need to be guaranteed over the operating surrounding temperature.

Table 5-37. SD_VSELECT Electrical Characteristics

(Unless otherwise specified, Ta=25°C, DVDD=1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Input "H" Level	V_{IHSDV}	DVDD x0.75	-	-	V	
Input "L" Level	V_{ILSDV}	-	-	DVDD x0.25	V	

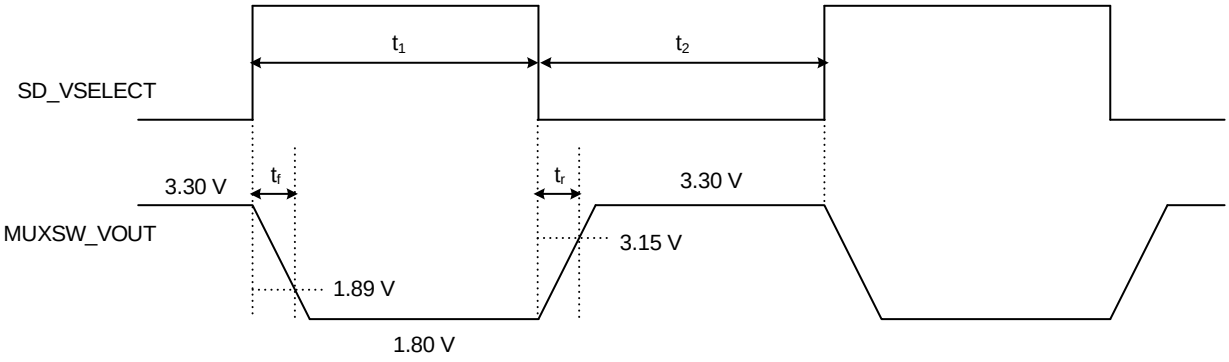


Figure 5-16. MUXSW Sequence

Table 5-38. MUXSW Sequence Timing

Symbol	Description	Min	Typ	Max	Unit
t_1	SD_VSELCT High Time *(Note 1)*	2	-	-	ms
t_2	SD_VSELCT Low Time *(Note 1)*	2	-	-	ms
t_f	Transition Time 3.3 V to 1.8 V	-	-	1	ms
t_r	Transition Time 1.8 V to 3.3 V	-	-	1	ms

(Note 1) t_1 and t_2 need over 2ms.

Table 5-39. MUXSW_EN - MUXSW Enable Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
MUXSW_EN	R/W	-	-	-	-	-	-	-	MUXSW_EN	0x01	0x30

Bit	Name	Function	Initial
D[0]	MUXSW_EN	MUXSW control bit 0 = MUXSW OFF 1 = MUXSW ON	1

6. 32.768 kHz Crystal Oscillator Driver

6.1. 32.768 kHz Crystal Oscillator Driver Block Diagram

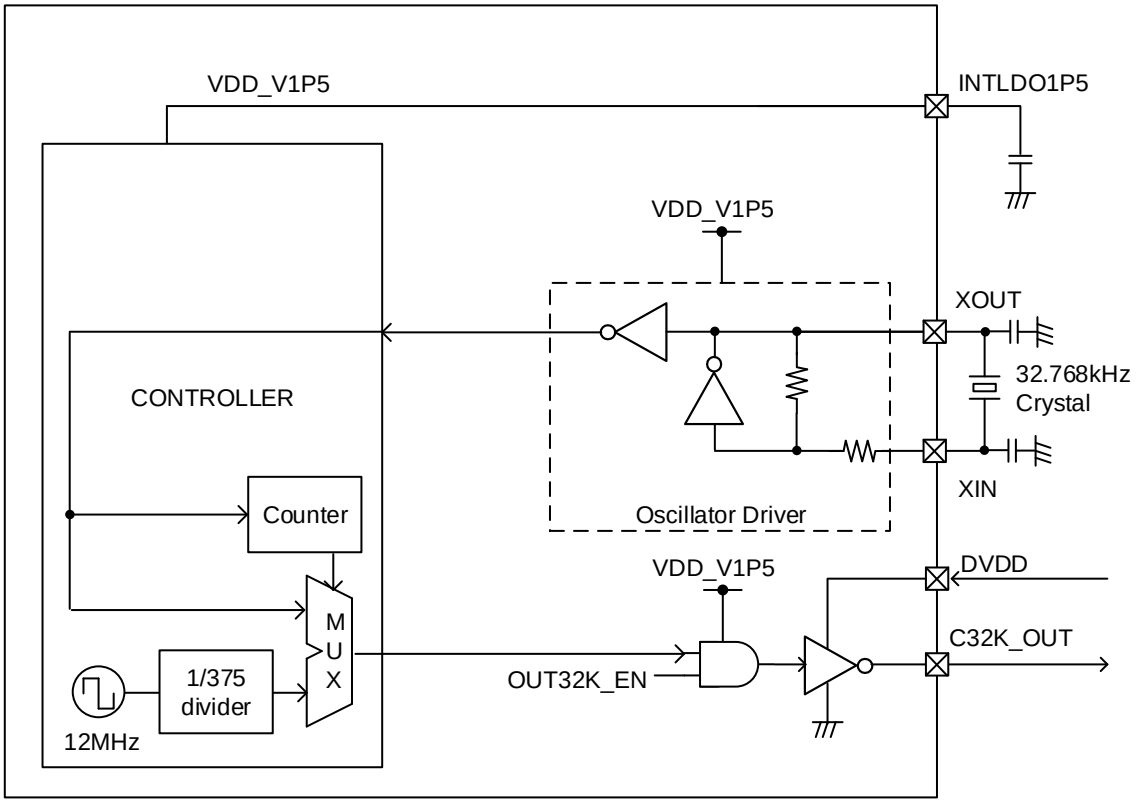


Figure 6-1. 32.768 kHz Crystal Oscillator Driver Block Diagram

Table 6-1. C32K_OUT Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT32K	R/W	-	-	-	-	-	-	-	OUT32K_EN	0x01	0x2E

Bit	Name	Function	Initial
D[0]	OUT32K_EN	0 = Disable (C32K_OUT is Low level) 1 = Enable	1

At the beginning of power-on, the C32K_OUT pin output clock is generated from the 12 MHz internal oscillator; the clock frequency is equal to 12 MHz / 375.
If an external 32.768 kHz crystal is present, the C32K_OUT pin output clock's clock source is switched from the internal oscillator to the crystal clock after 3000 crystal clock cycles, i.e., it is assumed that the crystal clock is stable by then.

6.2. 32.768 kHz Crystal Oscillator Driver Electrical Characteristics

Table 6-2. 32.768 kHz Crystal Oscillator Driver Electrical Characteristics

(Unless otherwise specified, Ta = +25°C, VSYS = 5.0 V, DVDD = 1.8 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output Frequency	f_{RTCLK}	-	32.768	-	kHz	With external crystal
Output Duty Cycle	D_{RTCLK}	40	50	60	%	
Output H Level Voltage	V_{OH32K}	DVDD x0.8	-	-	V	I_{OH} = -1 mA
Output L Level Voltage	V_{OL32K}	-	-	0.4	V	I_{OL} = 1 mA

(Note) The following 32.768 kHz crystal is recommended.
ST3215SB32768H5HPWAA (KYOCERA: C_L=12.5pF)

7. Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7. Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

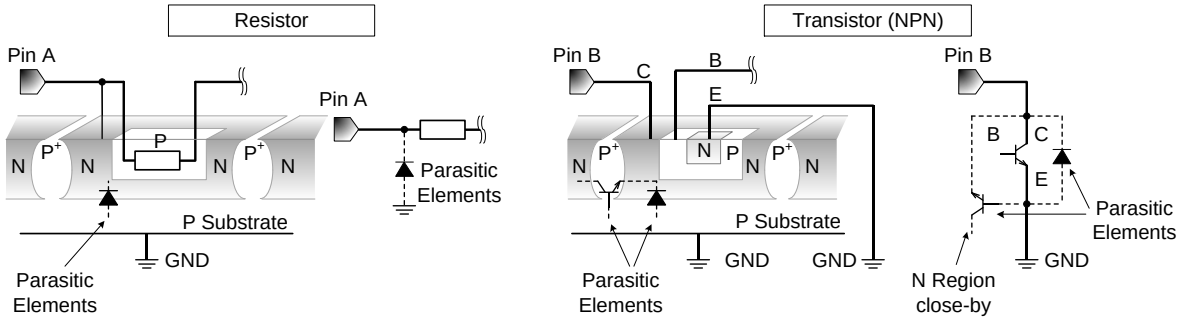


Figure 7-1. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

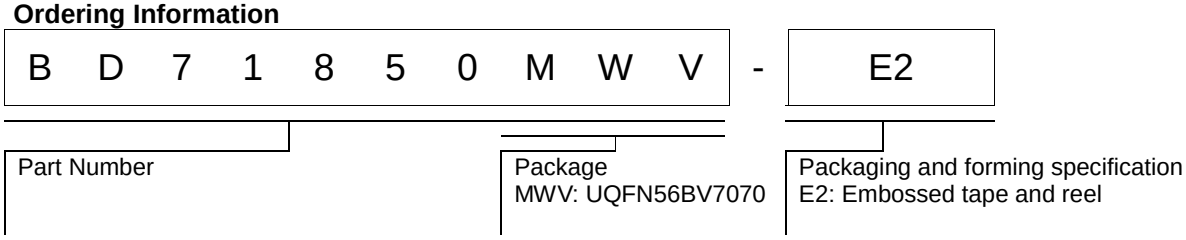
12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

8. Ordering Information



9. Marking Diagram

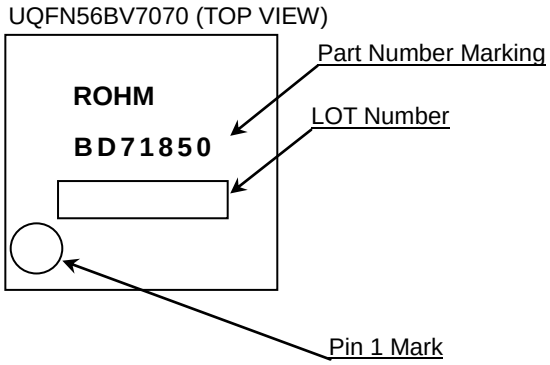
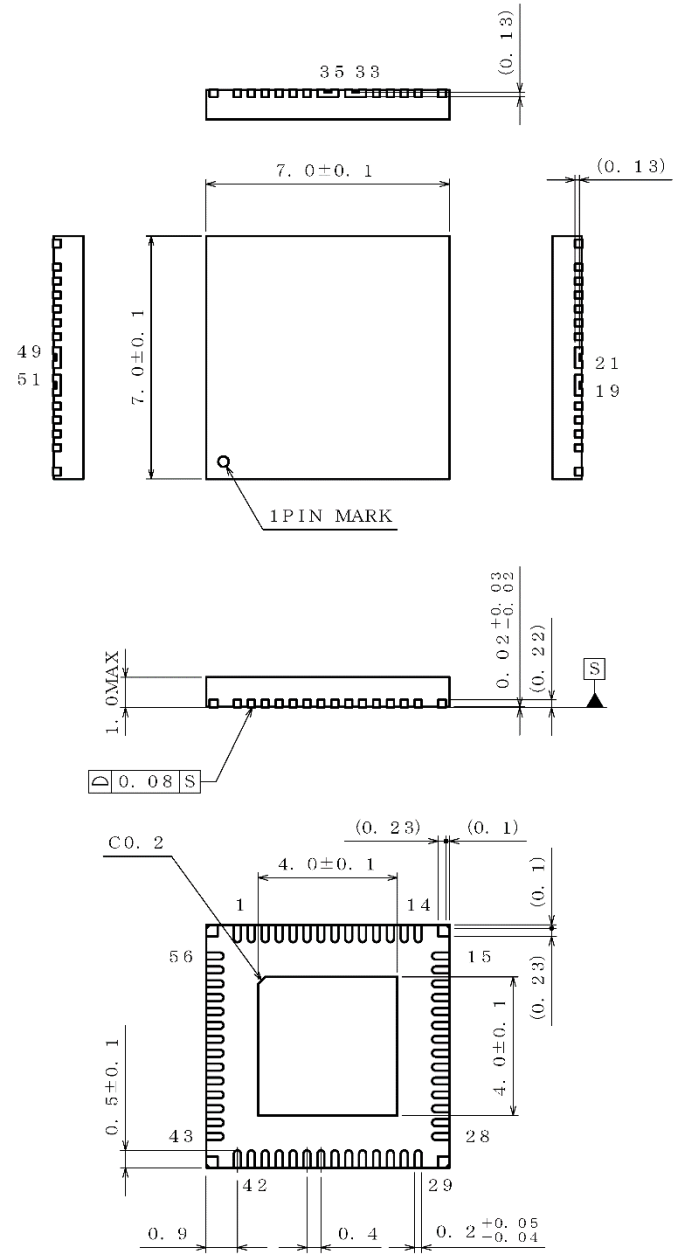


Figure 9-1. Marking Diagram

10. Physical Dimension and Packing Information

Package Name	UQFN56BV7070

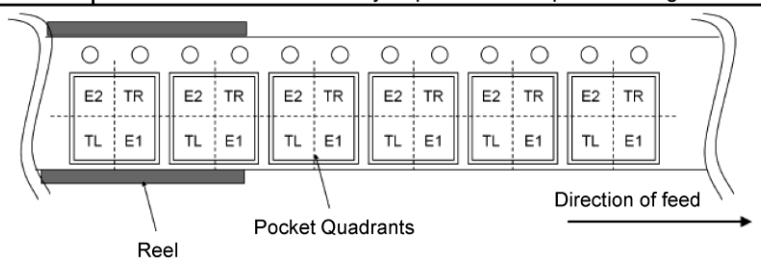


(UNIT : mm)

PKG : UQFN56BV7070
Drawing No. EX411−5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



11. Revision History

Date	Revision Number	Description
27.Sep.2019	001	First Release
16.Mar.2020	002	p.1,18 Changed maximum operating temperature to 105 °C. p.73,77,81,84,87,90,93,96,98,101,104,107,110 Deleted temperature condition of parts. Added note about parts temperature.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

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8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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