



**THE DATASHEET OF  
BD9D323QWZ-E2**



# 4.5V to 18V Input, 3.0A Integrated MOSFET 1ch Synchronous Buck DC/DC Converter

## BD9D323QWZ

### General Description

BD9D323QWZ is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. It is capable of providing current of up to 3 A. External phase compensation circuit is not necessary for it is a constant on-time control DC/DC converter with fast transient response.

### Features

- Synchronous Single DC/DC Converter
- Constant On-time Control
- Over Current Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Adjustable Soft Start
- UMMP008Z2020 Package (Backside Heat Dissipation)

### Applications

- Step-down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Set-top Box
- LCD TVs
- DVD / Blu-ray Player / Recorder
- POL Power Supply, etc.

### Key Specifications

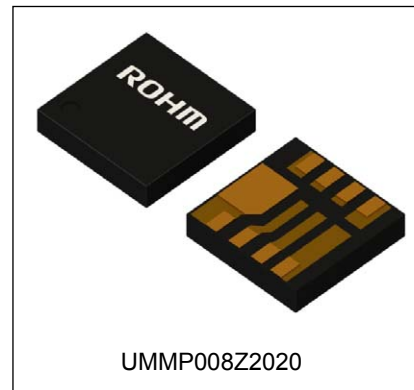
- Input Voltage Range: 4.5V to 18.0 V
- Output Voltage Setting Range: 0.765V to 7V  
( $V_{IN} \times 0.07$ )V to ( $V_{IN} \times 0.65$ )V
- Output Current: 3A (Max)
- Switching Frequency: 700kHz (Typ)
- High Side MOSFET On-Resistance: 80mΩ (Typ)
- Low Side MOSFET On-Resistance: 50mΩ (Typ)
- Standby Current: 2μA (Typ)

### Package

UMMP008Z2020

W(Typ) x D(Typ) x H(Max)

2.00mm x 2.00mm x 0.40mm



### Typical Application Circuit

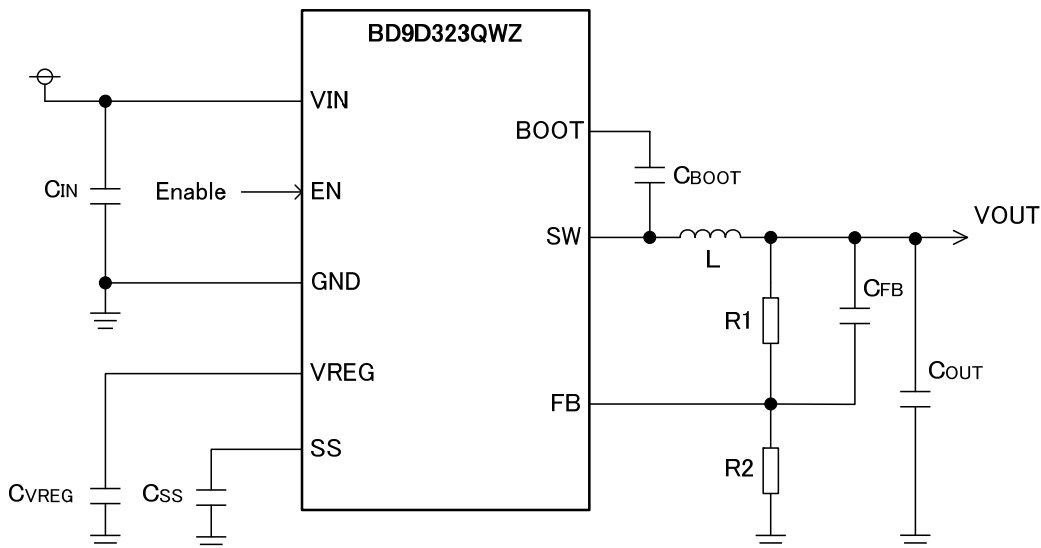


Figure 1. Typical Application Circuit

## Pin Configuration

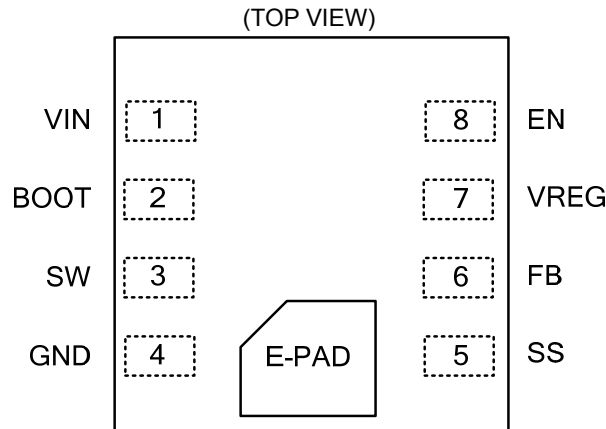


Figure 2. Pin Configuration

## Pin Descriptions

Terminal No.	Symbol	Function
1	VIN	Power supply terminal for the switching regulator. Connecting 10 $\mu$ F and 0.1 $\mu$ F ceramic capacitors to ground is recommended.
2	BOOT	Connect a bootstrap capacitor of 0.1 $\mu$ F between this terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
3	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1 $\mu$ F between this terminal and BOOT terminal. In addition, connect an inductor considering the direct current superimposition characteristic.
4	GND	Ground terminal for the output stage of the switching regulator and the control circuit.
5	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. Refer to page.28 for how to calculate the capacitance.
6	FB	An inverting input terminal of comparator which compares with reference voltage ( $V_{REF}$ ). Refer to page.27 for how to calculate the resistance of the output voltage setting.
7	VREG	Power supply voltage terminal inside IC. Voltage of 5.25V (Typ) is outputted with more than 2.2V is impressed to EN terminal. Connect 1 $\mu$ F ceramic capacitor to ground.
8	EN	Turning this terminal signal low level (0.3 V or lower) forces the device to enter the shutdown mode. Turning this terminal signal high level (2.2 V or higher) enables the device. This terminal must be terminated.
-	E-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple via provides excellent heat dissipation characteristics.

Block Diagram

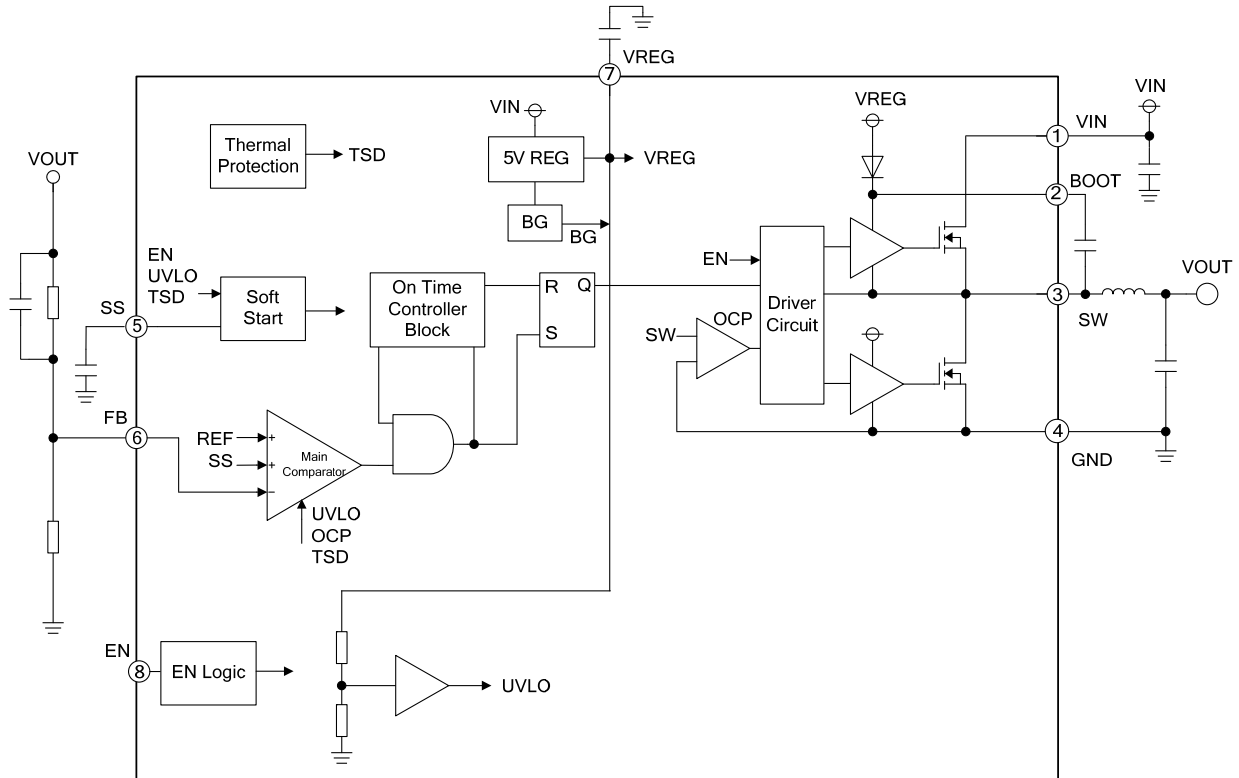


Figure 3. Block Diagram

## Description of Blocks

- EN Logic  
The EN Logic block is for control IC shutdown or starts up. It will shut down the IC when EN falls to 0.3V (Max) or lower. When VEN reaches 2.2 V(Min), the internal circuit is activated and the IC starts up.
- 5V REG  
Block creating internal power supply 5.25V (Typ).
- BG  
Block creating internal reference voltage.
- Main Comparator  
When FB terminal voltage becomes lower than REF, it outputs High and reports to the On Time block that the output voltage has dropped below control voltage.
- On Time Controller Block  
This is a block which creates On Time. Desired On Time is created when Main Comparator output becomes High. On Time is adjusted to restrict frequency change even with I/O voltage change.
- Soft Start  
The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current.
- Driver Circuit  
This block is a DC/DC driver. A signal from On Time Controller Block is applied to drive the MOSFETs.
- UVLO  
UVLO is a protection circuit that prevents low voltage malfunction. It prevents malfunction of the internal circuit from sudden rise and fall of power supply voltage. It monitors the  $V_{IN}$  power supply voltage and the internal regulator voltage. If  $V_{IN}$  is higher than the threshold voltage 3.8 V (Typ), the soft-start circuit will be restarted. This threshold voltage has a hysteresis of 300 mV (Typ). If  $V_{IN}$  is less than the threshold voltage 3.5 V (Typ), the POWER MOS FET output will turn OFF.
- TSD  
Thermal shutdown block. Usually IC operating in the allowable power dissipation, but when the IC power dissipation more than rating value,  $T_j$  will increase. When the chip temperature exceeds 175°C (Typ), the thermal shutdown circuit is intended for shutting down internal power devices. When  $T_j$  decreased to 25°C (Typ), IC will restart automatically. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.
- OCP  
Effective by controlling current which flows in low side MOSFET by 1 cycle each of switching period. With inductor current exceeding the source current restriction setting value  $I_{OCP}$  when low side MOSFET is ON, the high side MOSFET cannot turn ON even with FB voltage is lower than REF voltage and low side MOSFET continues to be ON until it is below  $I_{OCP}$ . High side MOSFET will turn ON when it goes below  $I_{OCP}$ . If low side MOSFET exceed sink current limited setting value when it is ON, low side MOSFET will turn OFF.

**Absolute Maximum Ratings (Ta = 25°C)**

Parameter	Symbol	Rating	Unit
Input Voltage	V <sub>IN</sub>	-0.3 ~ 20	V
BOOT-GND Voltage	V <sub>BOOT</sub>	-0.3 ~ 27	V
BOOT-SW Voltage	V <sub>BOOT-VSW</sub>	-0.3 ~ 7	V
FB Voltage	V <sub>FB</sub>	-0.3 ~ V <sub>REG</sub>	V
SW Voltage	V <sub>SW</sub>	-0.5 ~ V <sub>IN</sub> + 0.3	V
VREG Voltage	V <sub>REG</sub>	-0.3 ~ 7	V
SS Voltage	V <sub>SS</sub>	-0.3 ~ 7	V
EN Input Voltage	V <sub>EN</sub>	-0.3 ~ V <sub>IN</sub>	V
Maximum Junction Temperature	T <sub>jmax</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

**Thermal Resistance**<sup>(Note 1)</sup>

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
UMMP008Z2020				
Junction to Ambient	θ <sub>JA</sub>	-	58.3	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	-	11	°C/W

(Note 1)Based on JESD51-2A(Still-Air)

(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm
Top		
Copper Pattern	Thickness	
Footprints and Traces	70µm	

(Note 4)Using a PCB board based on JESD51-5, 7

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note 5)</sup>		
			Pitch	Diameter	
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mm	-	Φ0.30mm	
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage	V <sub>IN</sub>	4.5	12	18	V
Operating Temperature Range	T <sub>opr</sub>	-40	-	+85 (Note 1)	°C
Output Current	I <sub>OUT</sub>	0	-	3	A
Output Voltage Range	V <sub>RANGE</sub>	0.765 (Note 2)	-	7 (Note 3)	V

(Note 1) T<sub>j</sub> must be lower than 150°C under actual operating environment.

(Note 2) Please use under the condition of V<sub>OUT</sub> ≥ V<sub>IN</sub> × 0.07 [V].

(Note 3) Please use under the condition of V<sub>OUT</sub> ≤ V<sub>IN</sub> × 0.65 [V].

(Refer to the page 27 for how to calculate the output voltage setting.)

Electrical Characteristics (T<sub>a</sub> = 25°C, V<sub>IN</sub> = 12V, V<sub>EN</sub> = 3V unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Circuit Current	I <sub>STB</sub>	-	2	15	μA	V <sub>EN</sub> =GND
Operating Circuit Current	I <sub>VIN</sub>	-	1	2	mA	I <sub>OUT</sub> =0mA when no switching
EN Low Voltage	V <sub>ENL</sub>	GND	-	0.3	V	
EN High Voltage	V <sub>ENH</sub>	2.2	-	V <sub>IN</sub>	V	
EN Input Current	I <sub>EN</sub>	-	3	10	μA	V <sub>EN</sub> =3V
VREG Standby Voltage	V <sub>VREG_STB</sub>	-	-	0.1	V	V <sub>EN</sub> =GND
VREG Output Voltage	V <sub>VREG</sub>	5	5.25	5.5	V	
VREG Output Current	I <sub>VREG</sub>	-	10	-	mA	
UVLO Threshold Voltage	V <sub>VREG_UVLO</sub>	3.4	3.8	4.2	V	VREG: Sweep up
UVLO Hysteresis Voltage	dV <sub>VREG_UVLO</sub>	200	300	400	mV	VREG: Sweep down
Reference Voltage	V <sub>REF</sub>	0.753	0.765	0.777	V	V <sub>IN</sub> =12V, V <sub>OUT</sub> =1.8V
FB Input Current	I <sub>FB</sub>	-	-	1	μA	V <sub>FB</sub> =1V
SS Charge Current	I <sub>SSC</sub>	1.4	2.0	2.6	μA	
SS Discharge Current	I <sub>SSD</sub>	0.1	0.2	-	mA	V <sub>VREG</sub> =5.25V, V <sub>SS</sub> =0.5V
On Time	T <sub>on</sub>	-	215	-	ns	V <sub>IN</sub> =12V, V <sub>OUT</sub> =1.8V
Minimum Off Time	T <sub>offmin</sub>	100	200	-	ns	
High Side FET ON Resistance	R <sub>ONH</sub>	-	80	160	mΩ	
Low Side FET ON Resistance	R <sub>ONL</sub>	-	50	100	mΩ	
Over Current Protection Current Limit	I <sub>ocp</sub>	-	5 (Note 4)	-	A	

(Note 4) No tested on outgoing inspection.

Typical Performance Curves

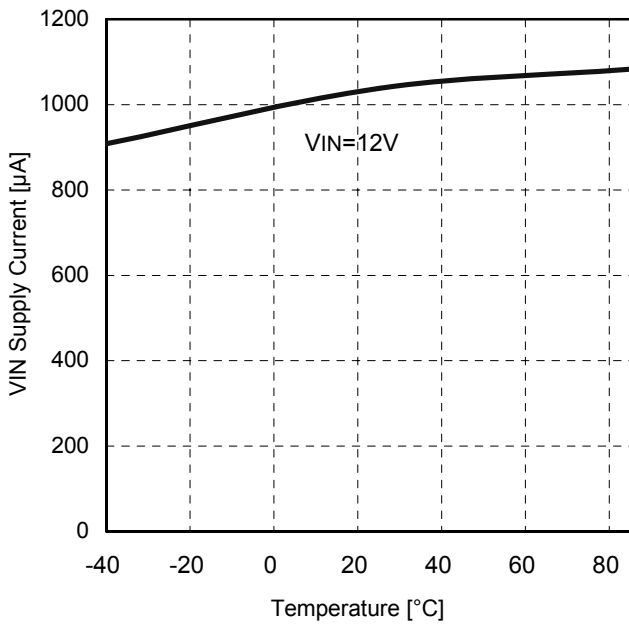


Figure 4. Operating Circuit Current vs Temperature

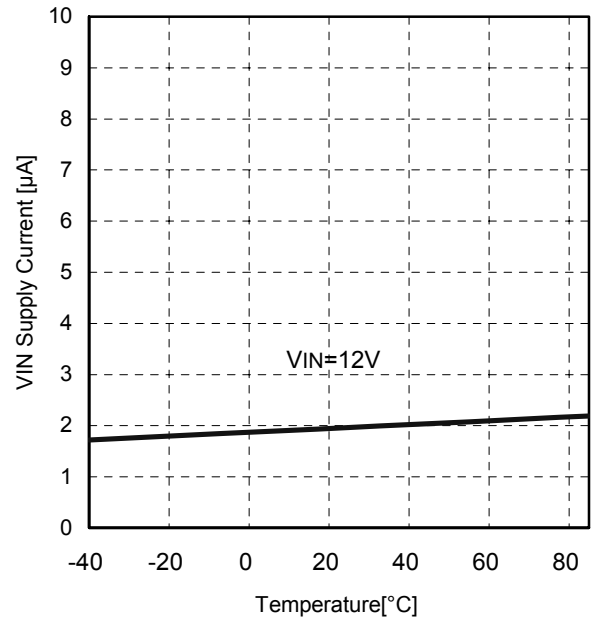


Figure 5. Standby Circuit Current vs Temperature

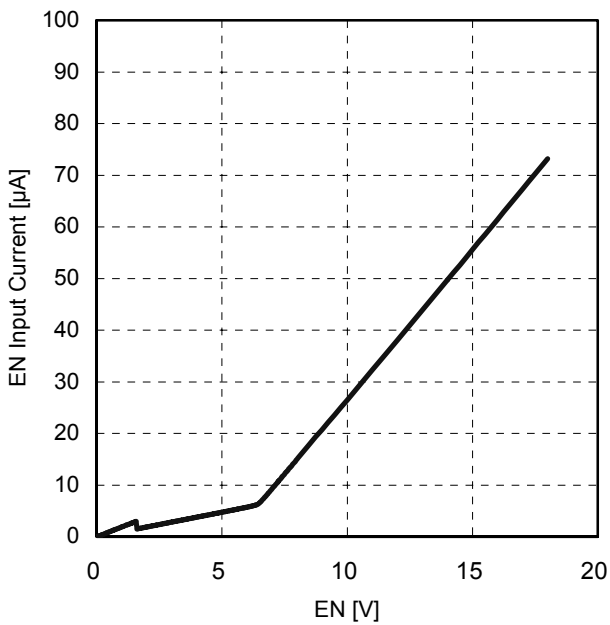


Figure 6. EN Input Current vs EN Voltage

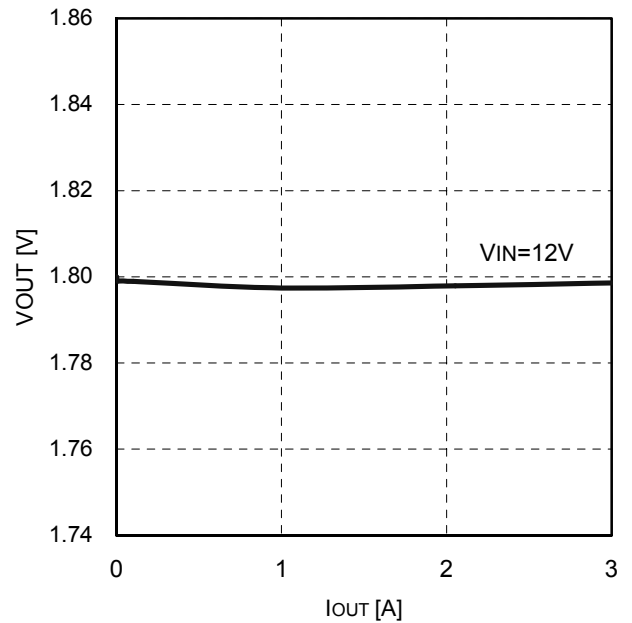


Figure 7. Output Voltage vs Output Current

Typical Performance Curves (Continued)

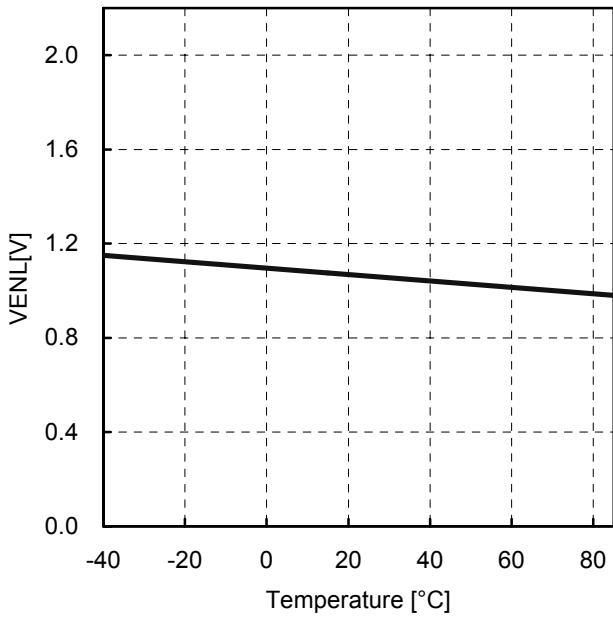


Figure 8. EN OFF Threshold Voltage vs Temperature

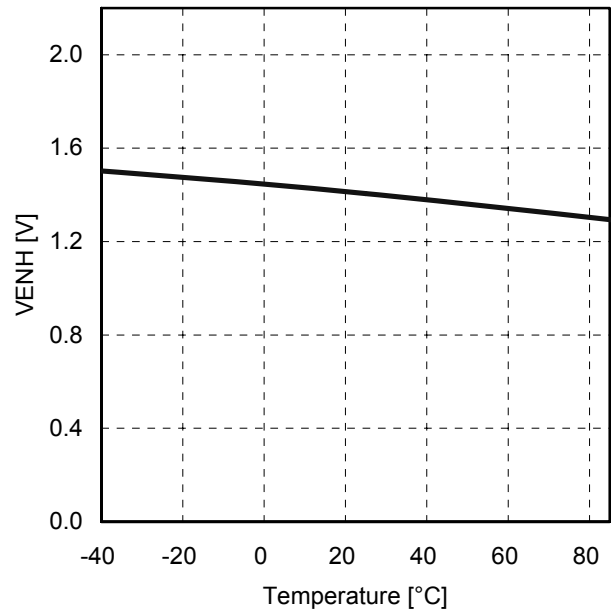


Figure 9. EN ON Threshold Voltage vs Temperature

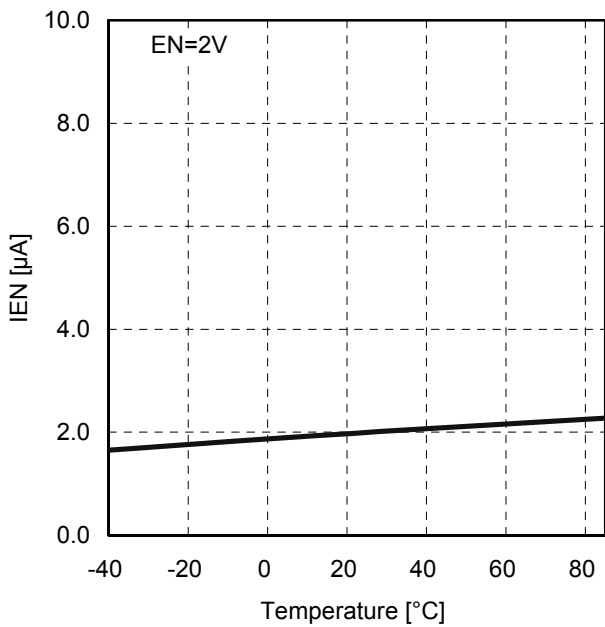


Figure 10. EN Input Current vs Temperature

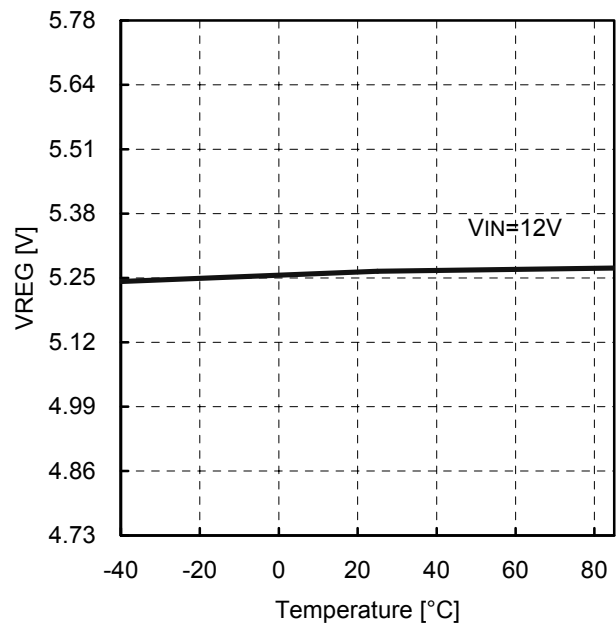


Figure 11. VREG Output Voltage vs Temperature

Typical Performance Curves (Continued)

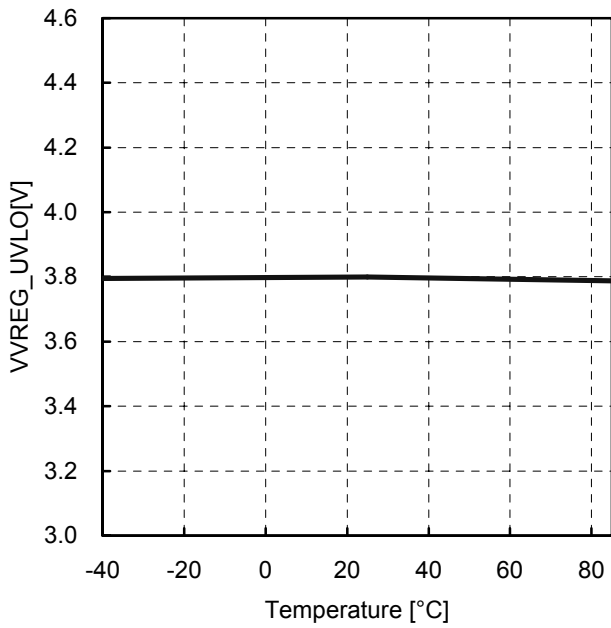


Figure 12. UVLO Threshold Voltage vs Temperature

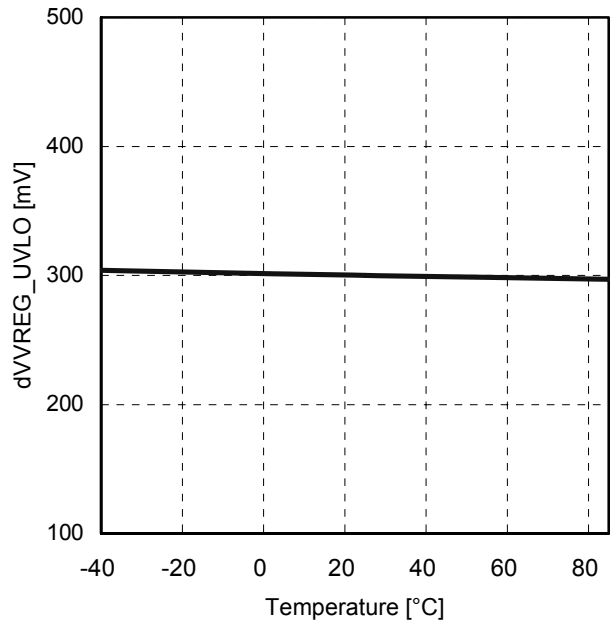


Figure 13. UVLO Hysteresis Voltage vs Temperature

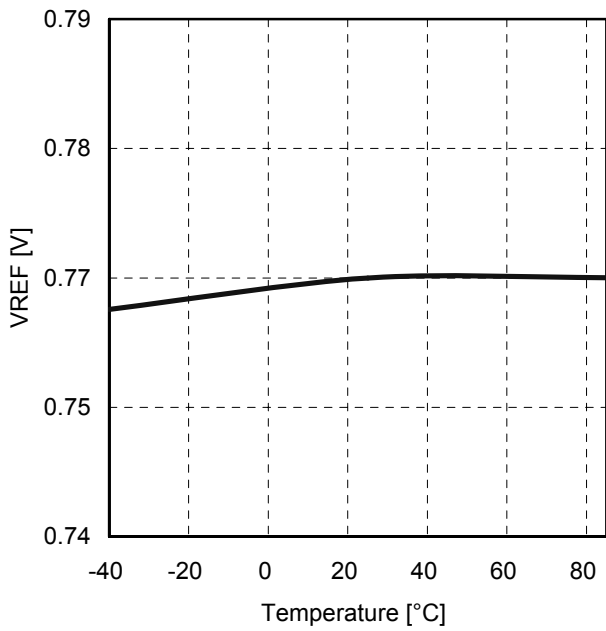


Figure 14. Reference Voltage vs Temperature

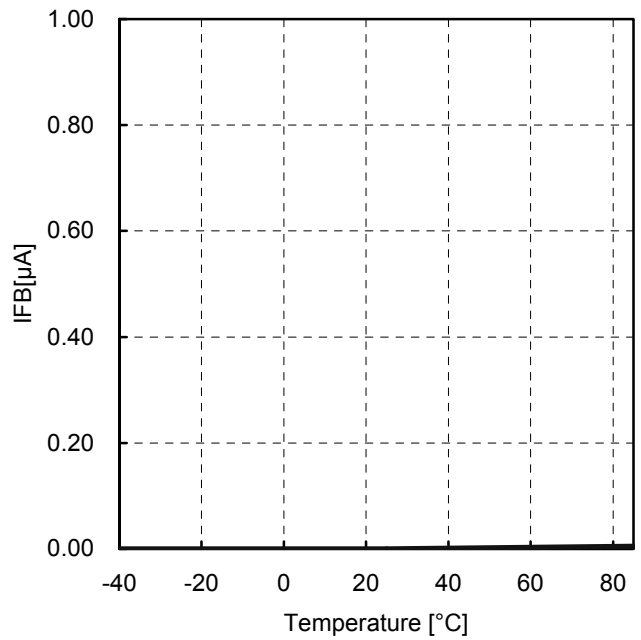


Figure 15. FB Input Current vs Temperature

Typical Performance Curves (Continued)

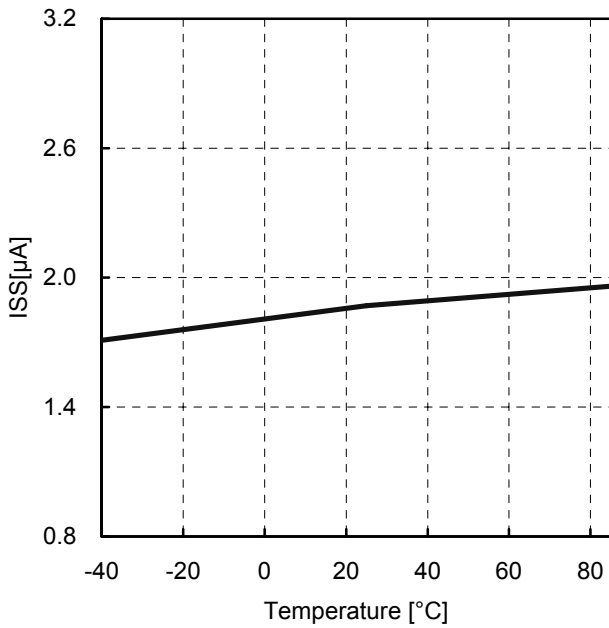


Figure 16. SS Charge Current vs Temperature

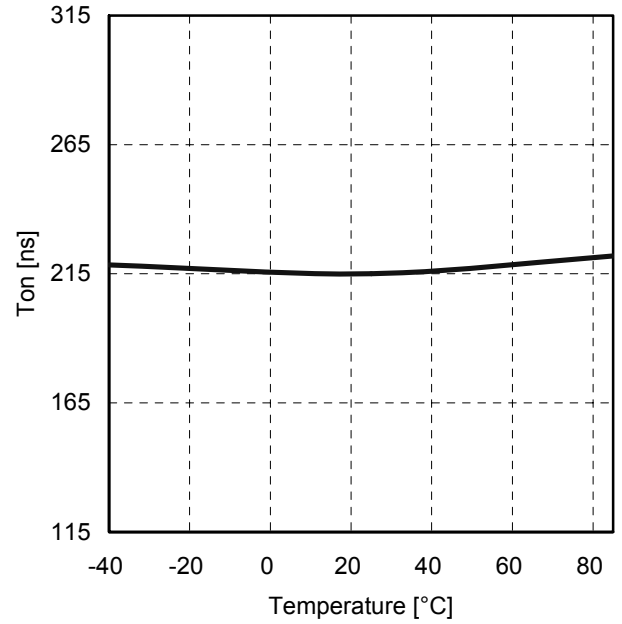


Figure 17. On Time vs Temperature

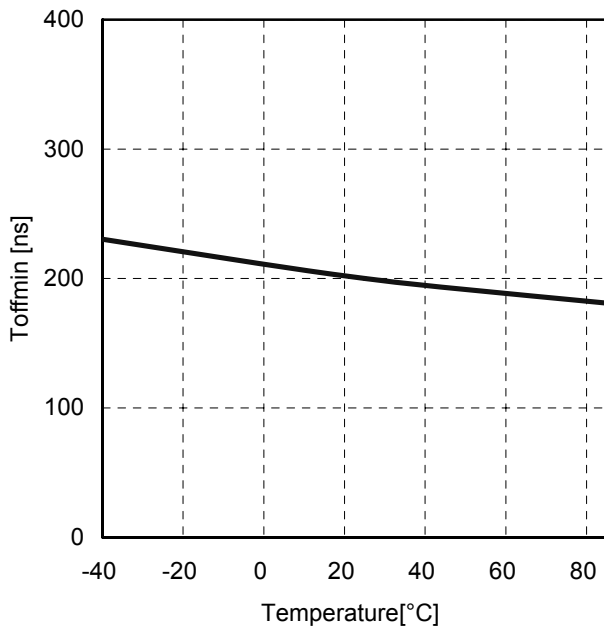


Figure 18. Minimum Off Time vs Temperature

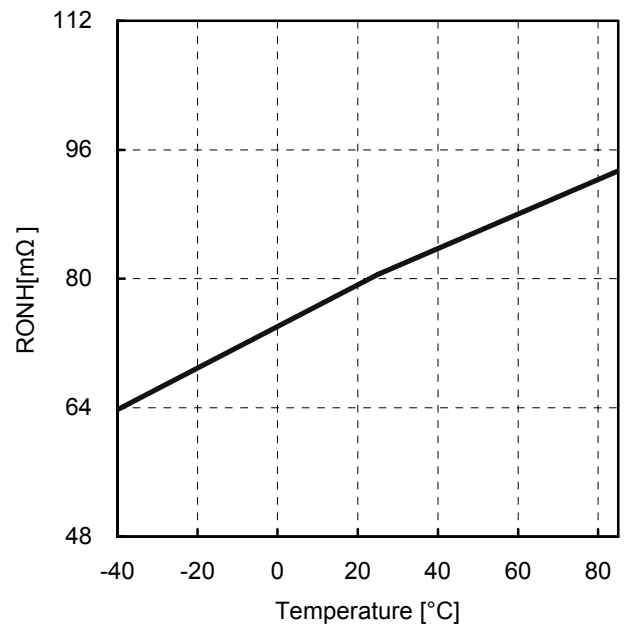


Figure 19. High Side MOSFET On-Resistance vs Temperature

Typical Performance Curves (Continued)

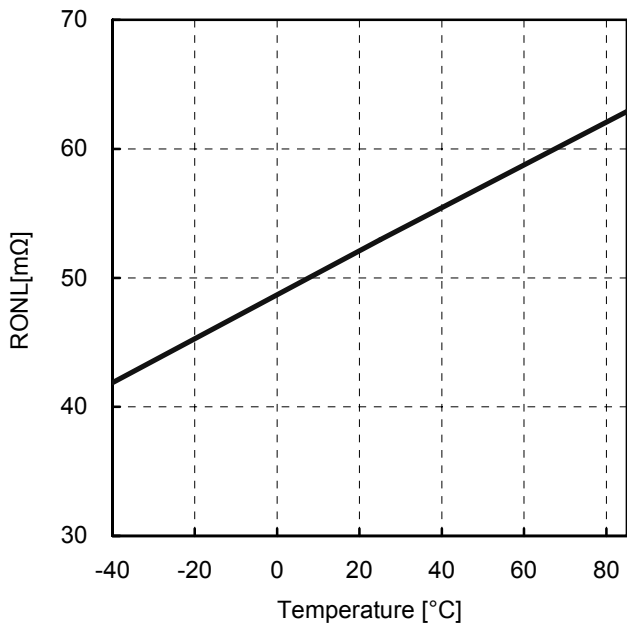


Figure 20. Low Side MOSFET On-Resistance vs Temperature

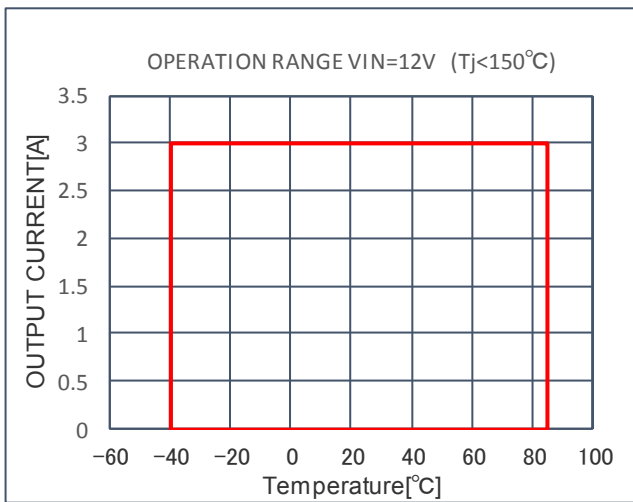


Figure 21. Output Current vs Temperature (VIN=12V, VOUT=1V, Measured ON FR-4 board 67.5 mm x 67.5 mm, Copper Thickness : Top and Bottom 70μm, 2 Internal Layers 35μm)

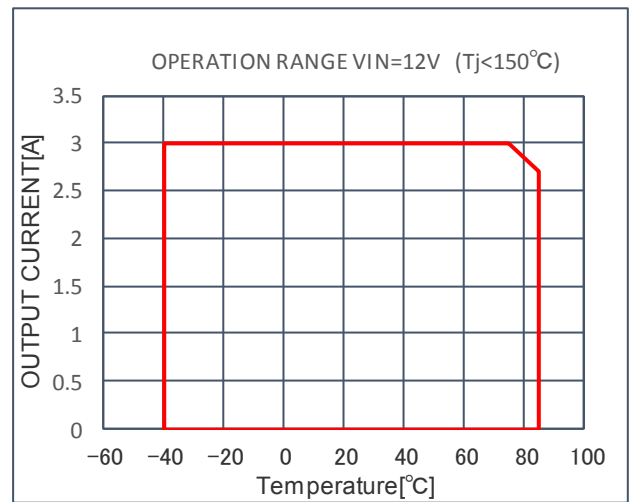


Figure 22. Output Current vs Temperature (VIN=12V, VOUT=5V, Measured ON FR-4 board 67.5 mm x 67.5 mm, Copper Thickness : Top and Bottom 70μm, 2 Internal Layers 35μm)

Typical Performance Curves (Continued)

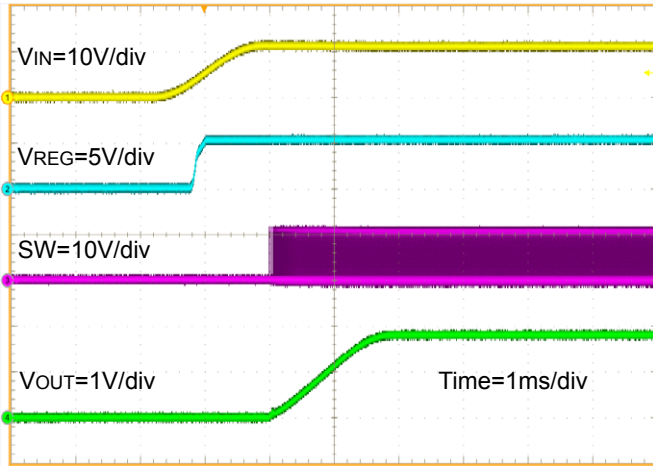


Figure 23. Power ON ( $V_{IN} = EN$ )  
 ( $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ ,  $C_{SS}=3300pF$ )

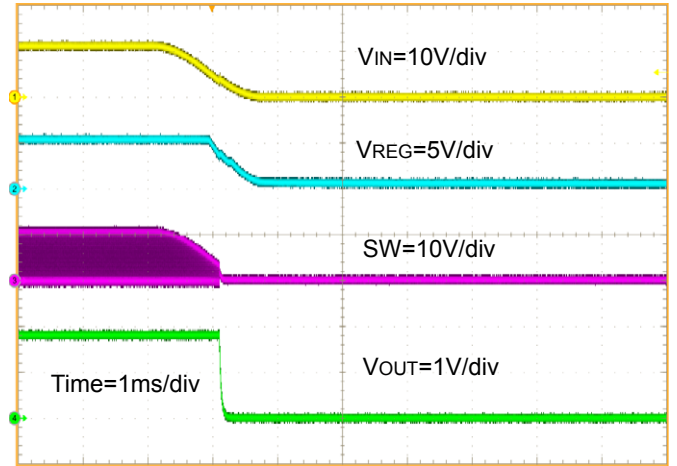


Figure 24. Power OFF ( $V_{IN} = EN$ )  
 ( $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ ,  $C_{SS}=3300pF$ )

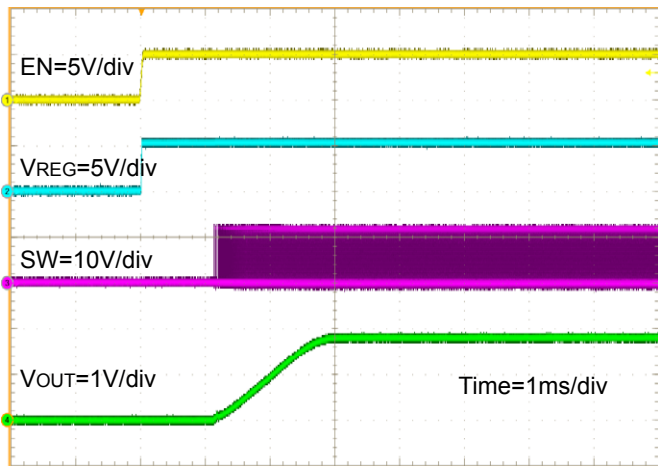


Figure 25. Power ON ( $EN = 0V \rightarrow 5V$ )  
 ( $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ ,  $C_{SS}=3300pF$ )

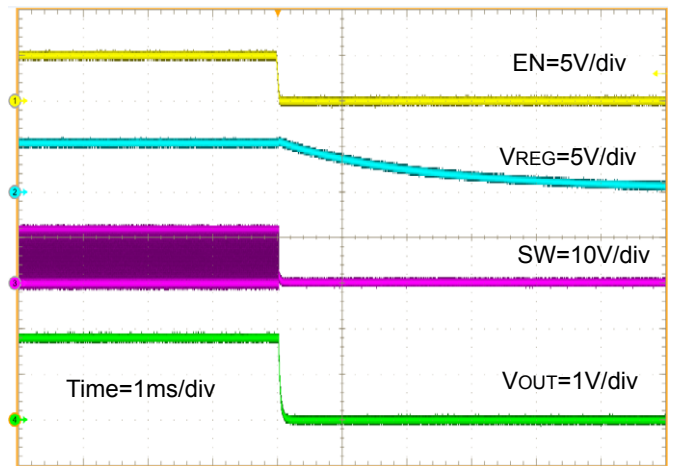


Figure 26. Power OFF ( $EN = 5V \rightarrow 0V$ )  
 ( $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=3A$ ,  $C_{SS}=3300pF$ )

Typical Performance Curves (Continued)

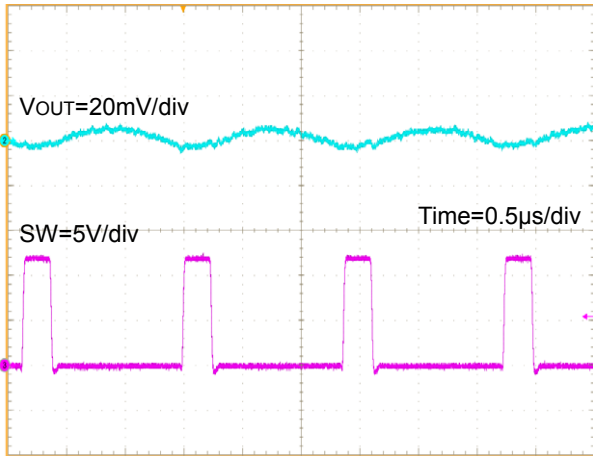


Figure 27. VOUT Ripple  
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, COUT=22µF x 2)

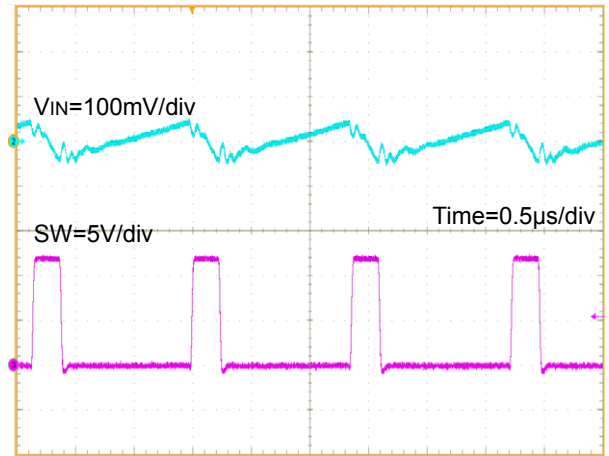


Figure 28. VIN Ripple  
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, COUT=22µF x 2)

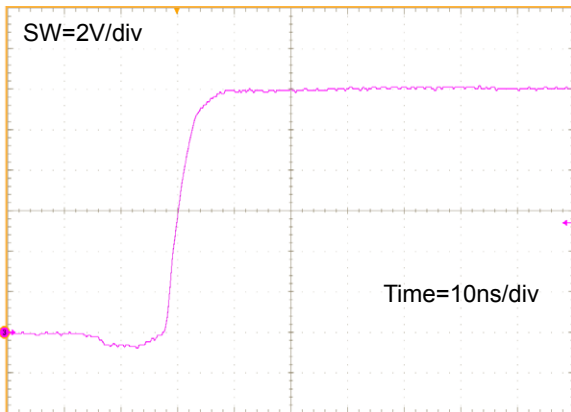


Figure 29. SW Turn ON  
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, COUT=22µF x 2)

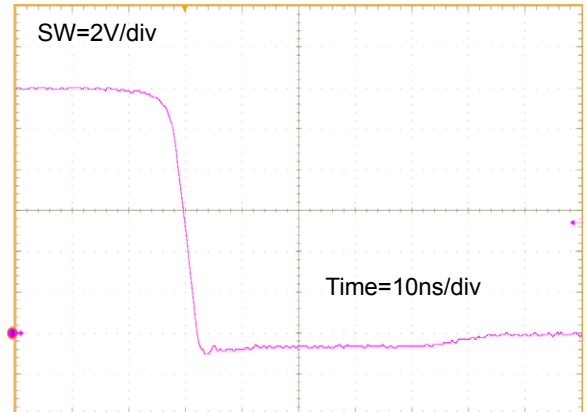


Figure 30. SW Turn OFF  
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, COUT=22µF x 2)

Typical Performance Curves (Continued)

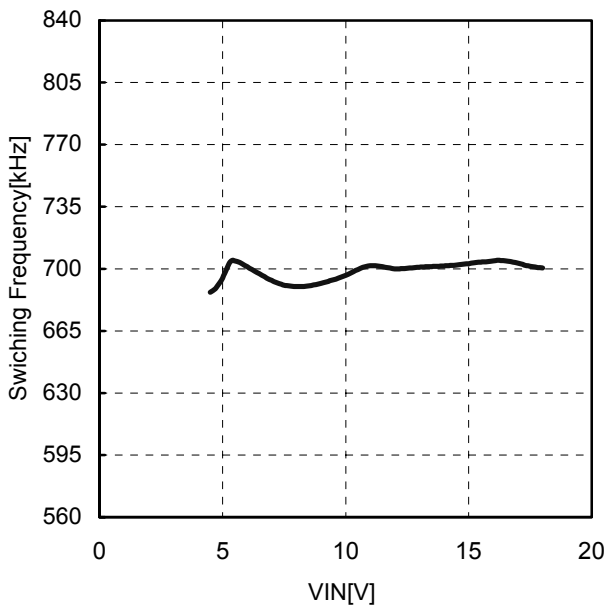


Figure 31. Switching Frequency vs Input Voltage (VOUT=1.8V, IOUT=3A, L=2.2μH, COUT=22μF x 2)

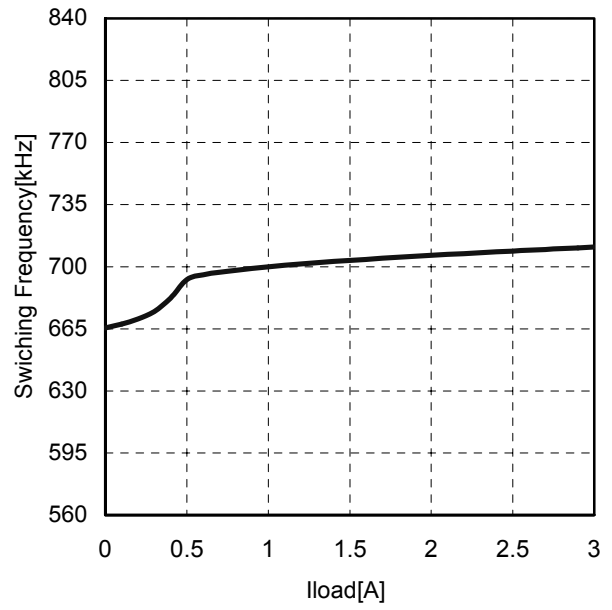


Figure 32. Switching Frequency vs Output Current (VIN=12V, VOUT=1.8V, L=2.2μH, COUT=22μF x 2)

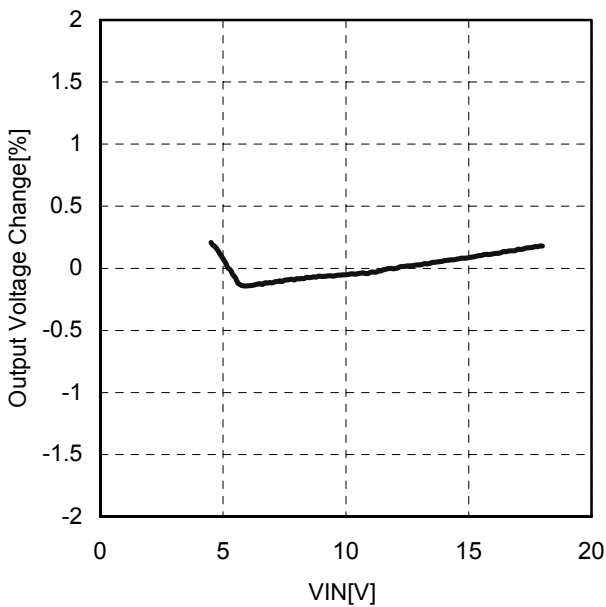


Figure 33. VOUT Line Regulation (VOUT=1.8V)

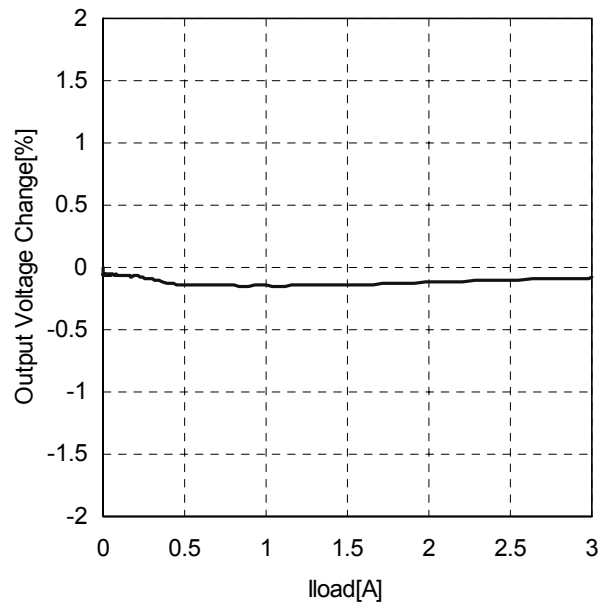


Figure 34. VOUT Load Regulation (VIN=12V, VOUT=1.8V)

Function Explanations

1 Basic Operation

1-1 Constant On Time Control

BD9D323QWZ is a single synchronous buck switching regulator employing a constant on-time control system. It controls the on-time by using the duty ratio of  $V_{OUT} / V_{IN}$  inside IC so that a switching frequency becomes 700 kHz(Typ). Therefore it runs with the frequency of 700kHz(Typ) under the constant on-time decided with  $V_{OUT} / V_{IN}$ .

1-2 Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When  $V_{EN}$  reaches 2.2 V (Min), the internal circuit is activated and the IC starts up.

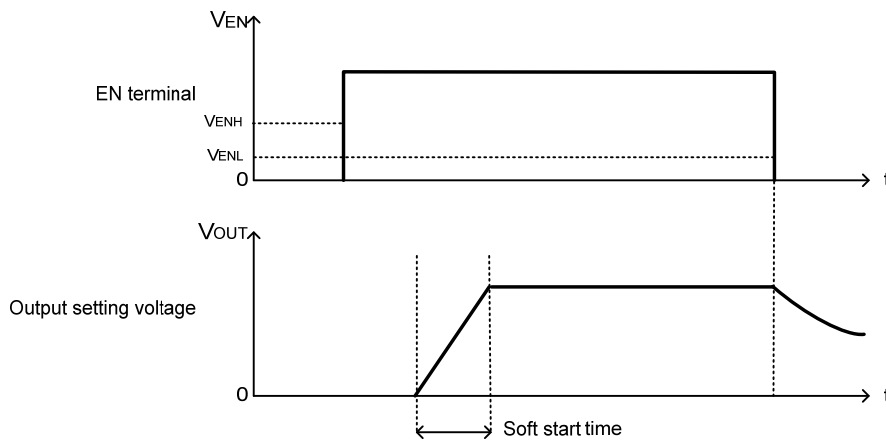


Figure35. Start-up with EN pin

1-3 Soft Start Function

By turning EN terminal to High, the soft start function operates and it gradually starts output voltage by controlling the current at start-up. Also soft start function prevents sudden current and over shoot of output voltage. Rising time can be set by connecting capacitor to SS terminal. For setting the rising time, please refer to page.28.

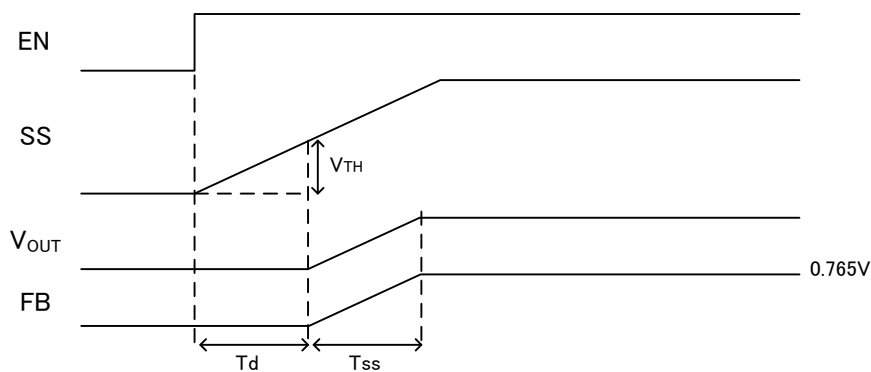


Figure 36. Soft Start Timing Chart

2 Protective Functions

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

2-1 Over Current Protection (OCP)

Over current protection function is effective by controlling current which flows in low side MOSFET by 1 cycle each of switching period. With inductor current exceeding the current restriction setting value  $I_{OCP}$  when LG is ON, the HG pulse cannot be hit even with FB voltage under REF voltage and LG continues to be ON until it is below  $I_{OCP}$ . It hits HG when it goes below  $I_{OCP}$ . As a result both frequency and duty fluctuates and output voltage may decrease. In a case where output is decreased because of OCP, output may rise after OCP is released due to the action at high speed load response. This is non-latch protection and after over current situation is released the output voltage will recover.

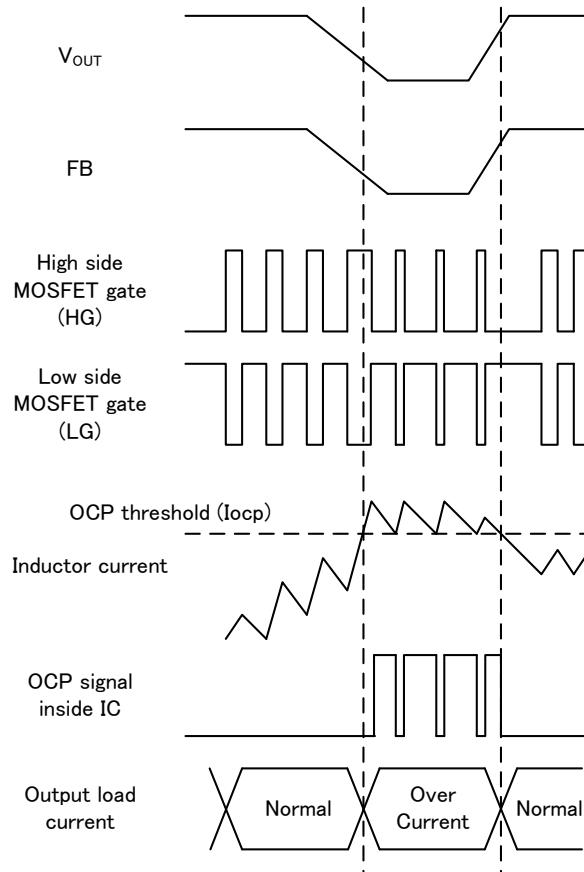


Figure 37. Over Current Protection Timing Chart

**2-2 Under Voltage Lockout Protection (UVLO)**

The Under Voltage Lockout Protection circuit monitors the VREG terminal voltage. The operation enters standby when the VREG terminal voltage is 3.5 V (Typ) or lower. The operation starts when the VREG terminal voltage is 3.8 V (Typ) or higher.

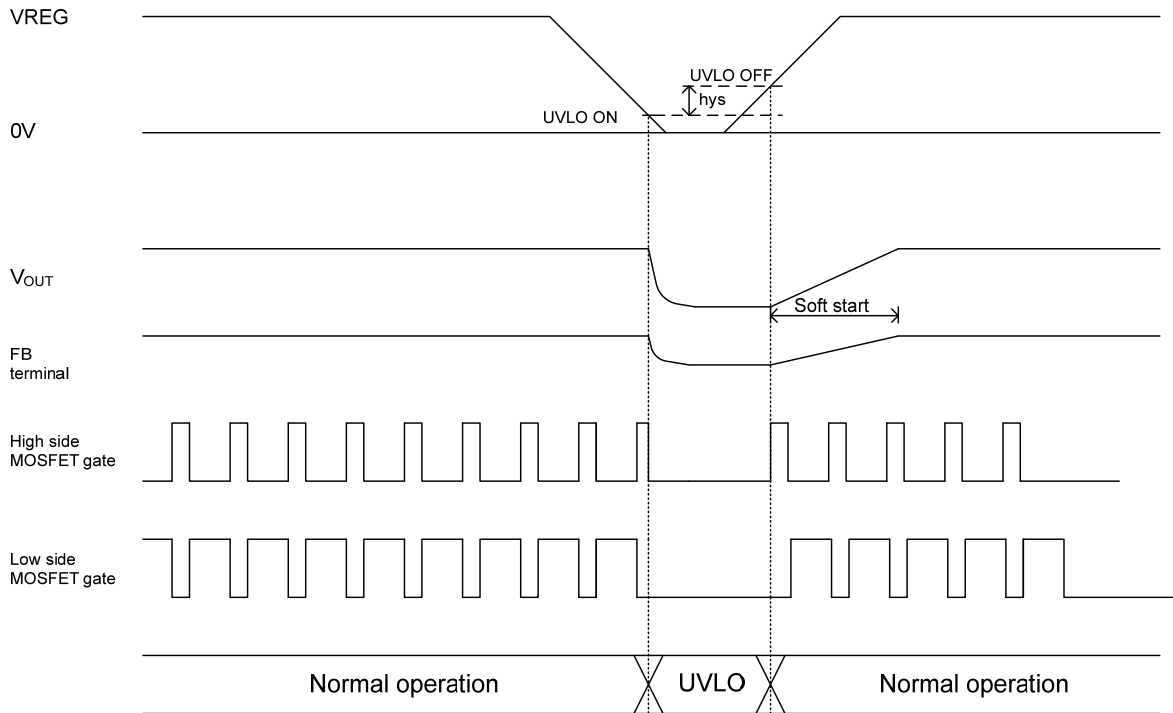


Figure 38. UVLO Timing Chart

※Load at Startup

Ensure that the respective output has light load at startup of this IC. Also, restrain the power supply line noise at start-up and voltage drop generated by operating current within the hysteresis width of UVLO. Noise exceeding the hysteresis noise width may cause the IC to malfunction.

**2-3 Thermal Shutdown Function**

When the chip temperature exceeds  $T_j = 175^\circ\text{C}$  (Typ), the DC/DC converter is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding  $T_{jmax} = 150^\circ\text{C}$ . Do not use this function for application protection design. This is non-latch protection.

Application Example

Parameter	Symbol	Specification Example
Input Voltage	$V_{IN}$	12 V
Output Voltage	$V_{OUT}$	5.0 V
Switching Frequency	$F_{OSC}$	700kHz(Typ)
Maximum Output Load	$I_{OMAX}$	3A
Operating Temperature Range	$T_{opr}$	-40 °C ~ +75 °C

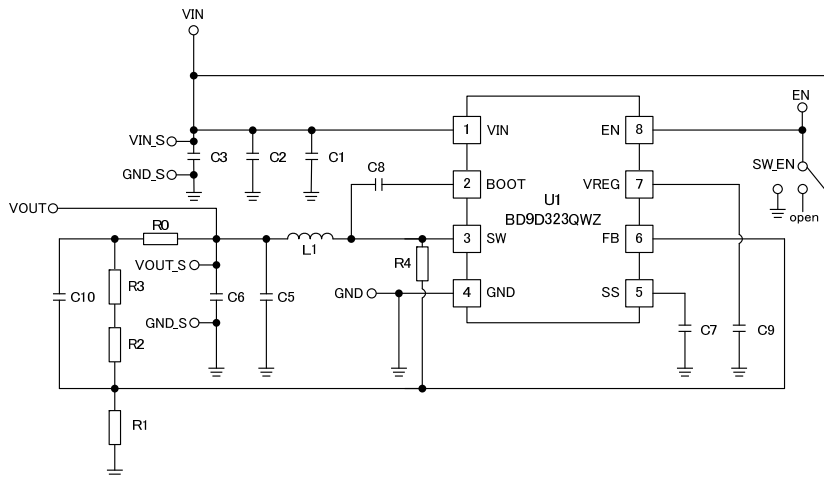


Figure 39. Application Circuit

Table 1. Recommendation Circuit constants

Part No	Value	Company	Part name
U1		ROHM	BD9D323QWZ
L1	3.3µH	TOKO	FSD0518-H-3R3M
C1(Note 1)	0.1µF	Murata	GRM188R71H104KA93D
C2(Note 2)	10µF	Murata	GRM32DB31E106KA75L
C3(Note 2)	10µF	Murata	GRM32DB31E106KA75L
C5(Note 3)	22µF	Murata	GRM32EB31E226ME15L
C6(Note 3)	22µF	Murata	GRM32EB31E226ME15L
C7	3300pF	Murata	GRM155B11H332KA01
C8	0.1µF	Murata	GRM188R71H104KA93D
C9	1µF	Murata	GRM188B11A105KA61D
C10	22pF	Murata	GRM1552C1E220JA01
R0	0Ω	ROHM	MCR01MZPJ000
R1	22kΩ	ROHM	MCR01MZPF2202
R2	120kΩ	ROHM	MCR01MZPF1203
R3	1.8kΩ	ROHM	MCR01MZPF1801
R4	OPEN	-	-

- (Note 1) In order to reduce the influence of high frequency noise, arrange the 0.1µF ceramic capacitor as close as possible to the VIN pin and GND pin.
- (Note 2) For capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 4.7µF. When VIN is lower than 7V at normal state, add capacitor same as C2 to C3.
- (Note 3) In case capacitance value fluctuates due to temperature characteristics, DC bias characteristics, etc. of output capacitor, Loop Response may fluctuate. Please confirm on actual equipment. When selecting a capacitor, confirm the characteristics of the capacitor in its datasheet, Please use capacitors such as ceramic type are recommended for output capacitor.

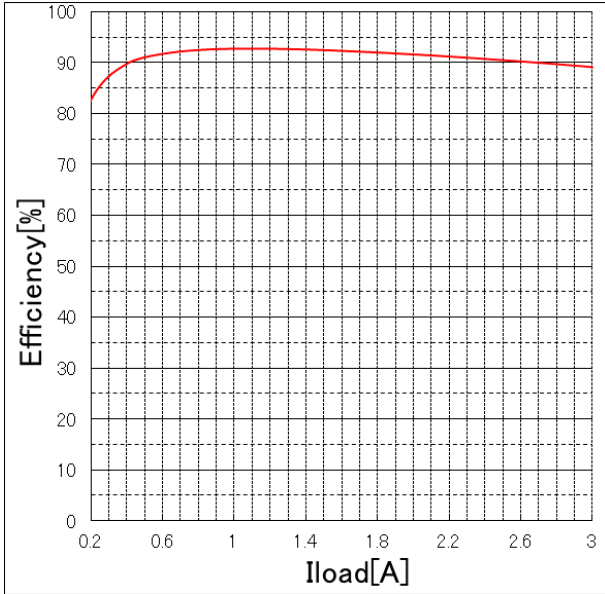


Figure 40. Efficiency vs Output Current  
(VIN=12V, VOUT = 5V)

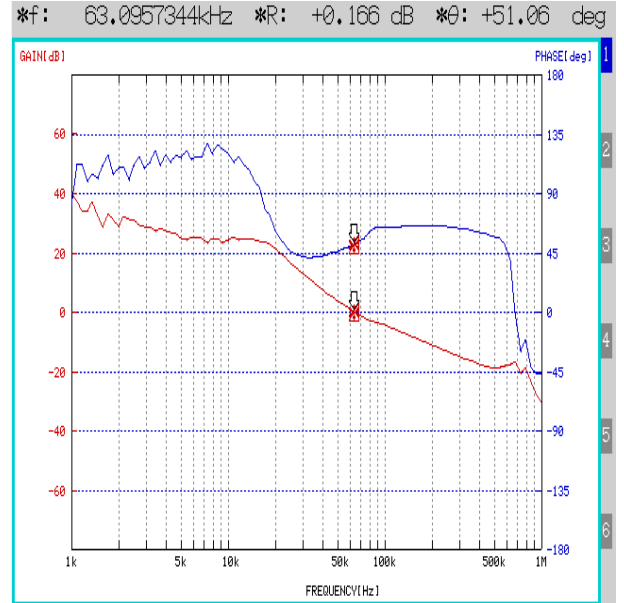


Figure 41. Loop Response IOUT=3A  
(VIN=12V, VOUT=5V)

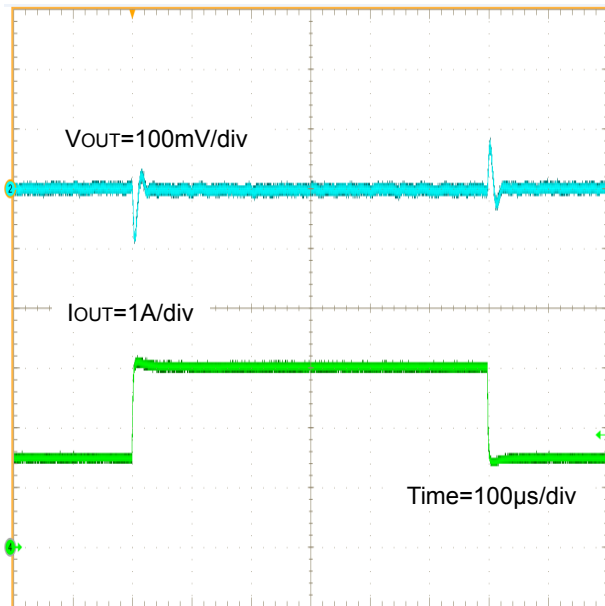


Figure 42. Load Transient Response IOUT=1.5A - 3A  
(VIN=12V, VOUT=5V)

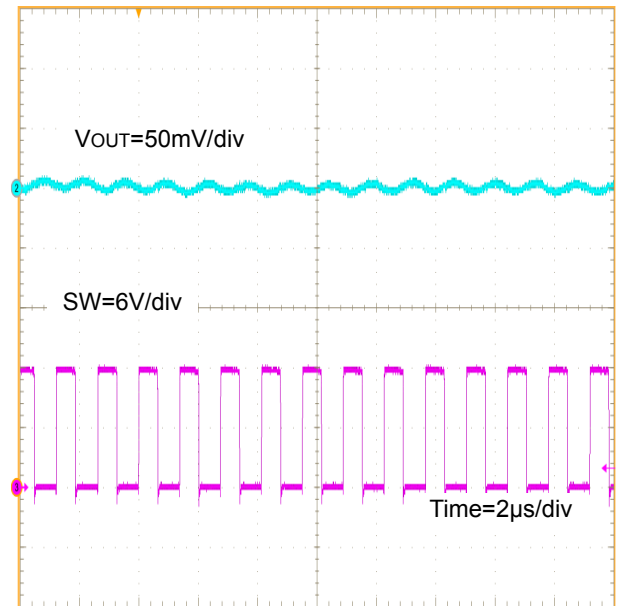


Figure 43. VOUT Ripple IOUT=3A  
(VIN = 12V, VOUT = 5V)



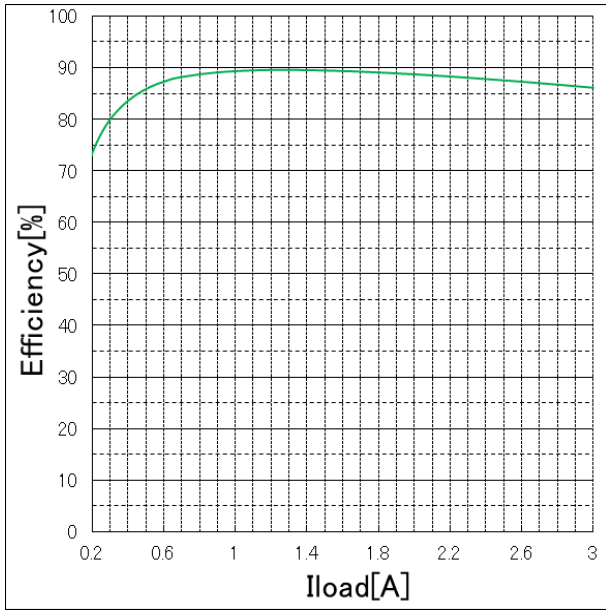


Figure 45. Efficiency vs Output Current  
(VIN=12V, VOUT = 3.3V)

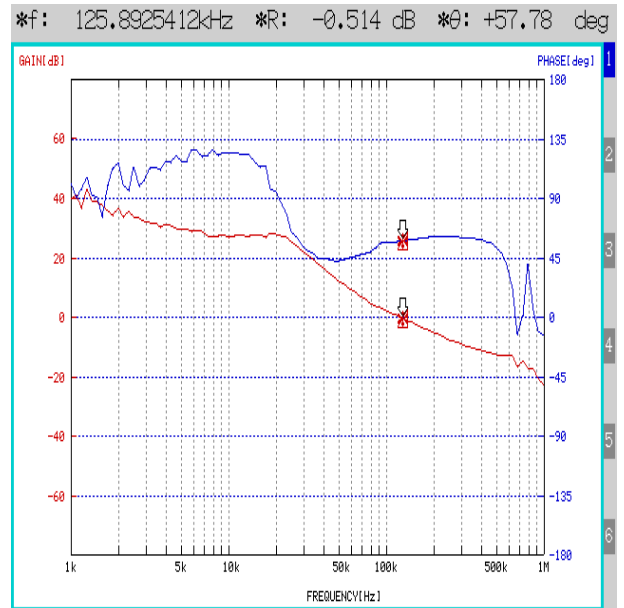


Figure 46. Loop Response IOUT=3A  
(VIN=12V, VOUT=3.3V)

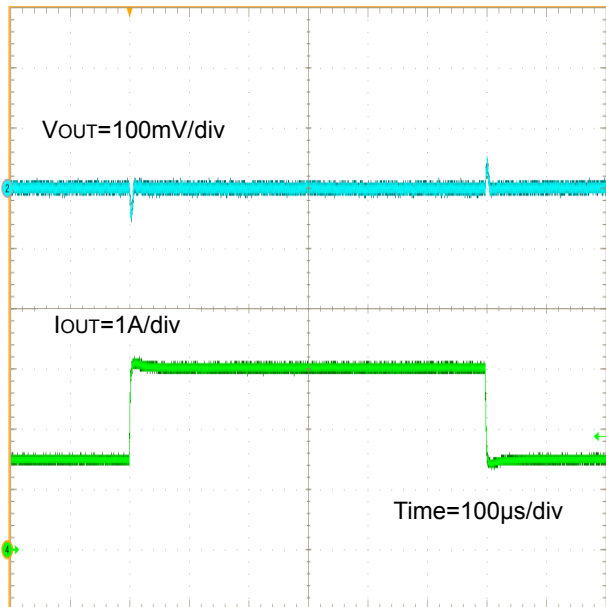


Figure 47. Load Transient Response IOUT=1.5A - 3A  
(VIN=12V, VOUT=3.3V)

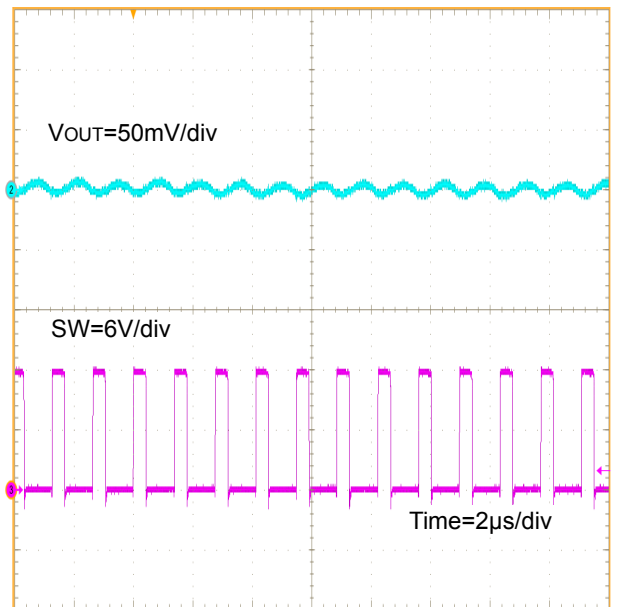


Figure 48. VOUT Ripple IOUT=3A  
(VIN = 12V, VOUT = 3.3V)

Application Example

Parameter	Symbol	Specification Example
Input Voltage	$V_{IN}$	12 V
Output Voltage	$V_{OUT}$	1.8 V
Switching Frequency	$F_{OSC}$	700kHz(Typ)
Maximum Output Load	$I_{OMAX}$	3A
Operating Temperature Range	$T_{opr}$	-40 °C ~ +85°C

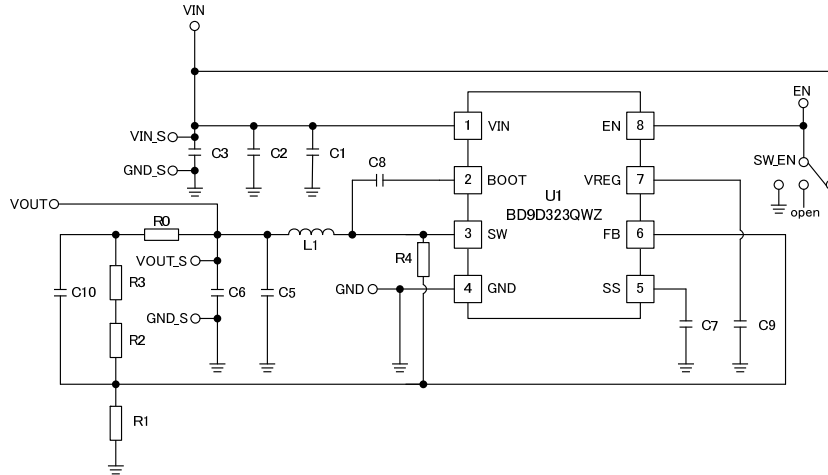


Figure 49. Application Circuit

Table 3. Recommendation Circuit constants

Part No	Value	Company	Part name
U1		ROHM	BD9D323QWZ
L1	2.2 $\mu$ H	TOKO	FSD0518-H-2R2M
C1(Note 1)	0.1 $\mu$ F	Murata	GRM188R71H104KA93D
C2(Note 2)	10 $\mu$ F	Murata	GRM32DB31E106KA75L
C3(Note 2)	10 $\mu$ F	Murata	GRM32DB31E106KA75L
C5(Note 3)	22 $\mu$ F	Murata	GRM21BB30J226ME38L
C6(Note 3)	22 $\mu$ F	Murata	GRM21BB30J226ME38L
C7	3300pF	Murata	GRM155B11H332KA01
C8	0.1 $\mu$ F	Murata	GRM188R71H104KA93D
C9	1 $\mu$ F	Murata	GRM188B11A105KA61D
C10	47pF	Murata	GRM1552C1E470JA01
R0	0 $\Omega$	ROHM	MCR01MZPJ000
R1	22k $\Omega$	ROHM	MCR01MZPF2202
R2	30k $\Omega$	ROHM	MCR01MZPF3002
R3	0 $\Omega$	ROHM	MCR01MZPJ000
R4	OPEN	-	-

- (Note 1) In order to reduce the influence of high frequency noise, arrange the 0.1 $\mu$ F ceramic capacitor as close as possible to the  $V_{IN}$  pin and GND pin.
- (Note 2) For capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 4.7 $\mu$ F. When  $V_{IN}$  is lower than 7V at normal state, add capacitor same as C2 to C3.
- (Note 3) In case capacitance value fluctuates due to temperature characteristics, DC bias characteristics, etc. of output capacitor, Loop Response may fluctuate. Please confirm on actual equipment. When selecting a capacitor, confirm the characteristics of the capacitor in its datasheet, Please use capacitors such as ceramic type are recommended for output capacitor.

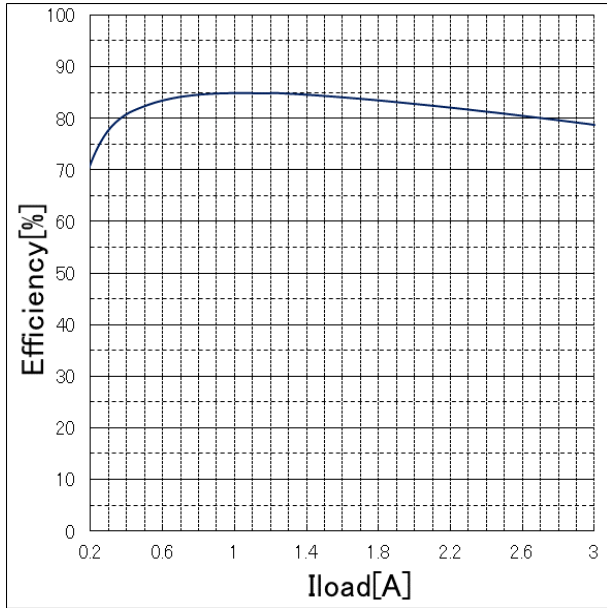


Figure 50. Efficiency vs Output Current  
(VIN=12V, VOUT = 1.8V)

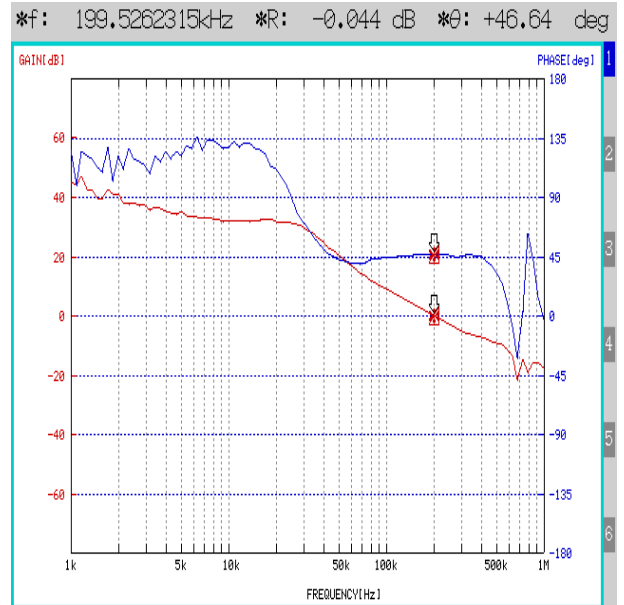


Figure 51. Loop Response IOUT=3A  
(VIN=12V, VOUT=1.8V)

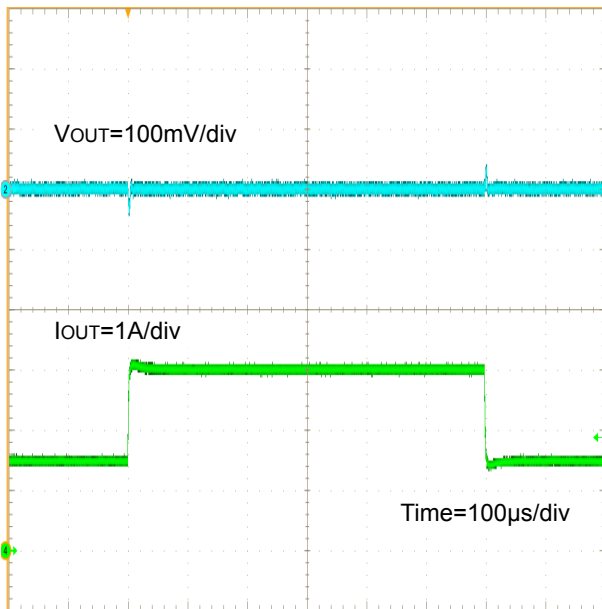


Figure 52. Load Transient Response IOUT=1.5A - 3A  
(VIN=12V, VOUT=1.8V)

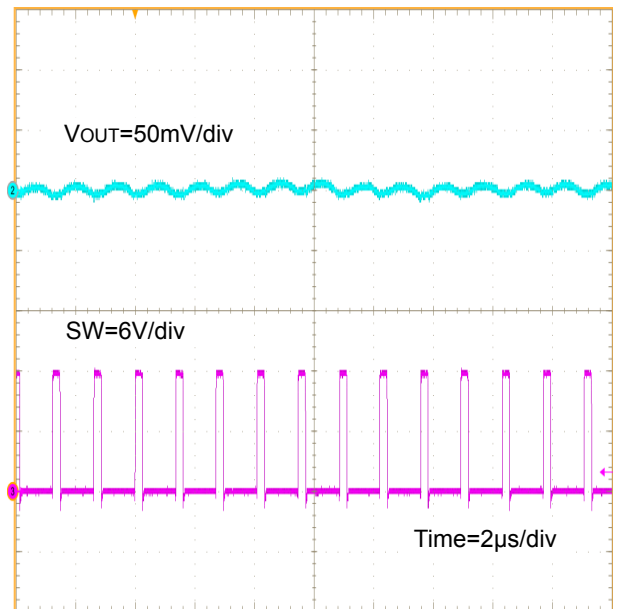


Figure 53. VOUT Ripple IOUT=3A  
(VIN = 12V, VOUT = 1.8V)

Application Example

Parameter	Symbol	Specification Example
Input Voltage	$V_{IN}$	12 V
Output Voltage	$V_{OUT}$	1.2 V
Switching Frequency	$F_{osc}$	700kHz(Typ)
Maximum Output Load	$I_{OMAX}$	3A
Operating Temperature Range	$T_{opr}$	-40 °C ~ +85°C

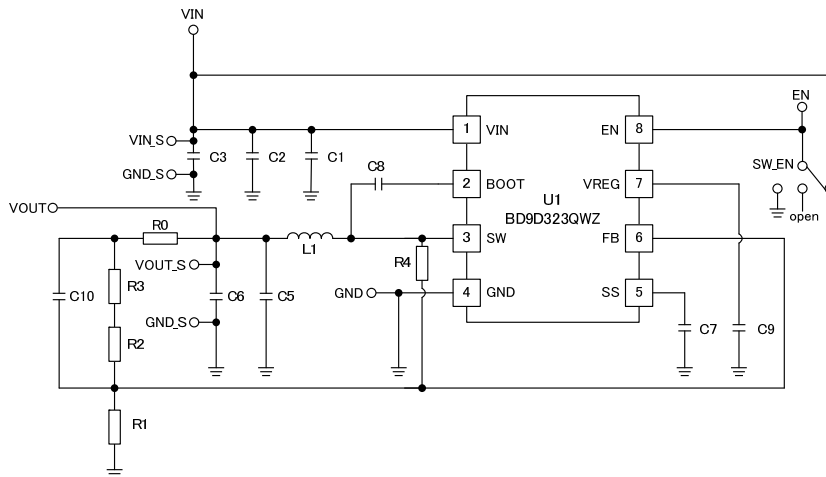


Figure 54. Application Circuit

Table 4. Recommendation Circuit constants

Part No	Value	Company	Part name
U1		ROHM	BD9D323QWZ
L1	1.5μH	TOKO	FSDS0518-H-1R5M
C1(Note 1)	0.1μF	Murata	GRM188R71H104KA93D
C2(Note 2)	10μF	Murata	GRM32DB31E106KA75L
C3(Note 2)	10μF	Murata	GRM32DB31E106KA75L
C5(Note 3)	22μF	Murata	GRM31CB31A226ME19L
C6(Note 3)	22μF	Murata	GRM31CB31A226ME19L
C7	3300pF	Murata	GRM155B11H332KA01
C8	0.1μF	Murata	GRM188R71H104KA93D
C9	1μF	Murata	GRM188B11A105KA61D
C10	220pF	Murata	GRM155B11H221KA01
R0	0Ω	ROHM	MCR01MZPJ000
R1	10kΩ	ROHM	MCR01MZPF1002
R2	4.7kΩ	ROHM	MCR01MZPF4701
R3	1kΩ	ROHM	MCR01MZPF1001
R4	300kΩ	ROHM	MCR01MZPF3003

- (Note 1) In order to reduce the influence of high frequency noise, arrange the 0.1μF ceramic capacitor as close as possible to the  $V_{IN}$  pin and GND pin.
- (Note 2) For capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 4.7μF. When  $V_{IN}$  is lower than 7V at normal state, add capacitor same as C2 to C3.
- (Note 3) In case capacitance value fluctuates due to temperature characteristics, DC bias characteristics, etc. of output capacitor, Loop Response may fluctuate. Please confirm on actual equipment. When selecting a capacitor, confirm the characteristics of the capacitor in its datasheet, Please use capacitors such as ceramic type are recommended for output capacitor.

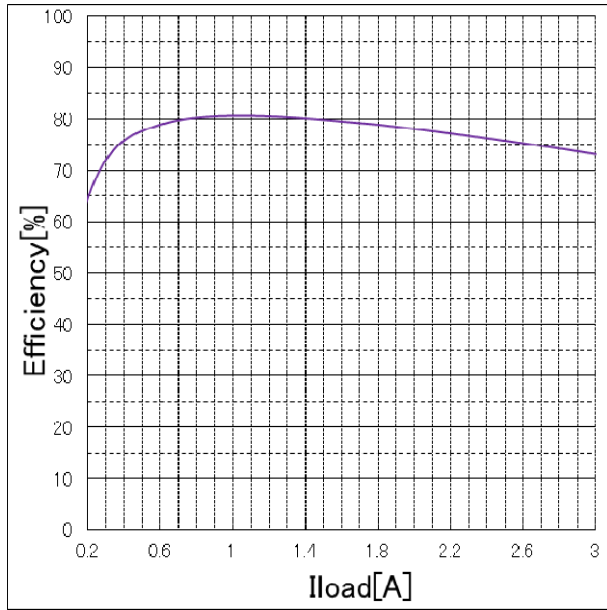


Figure 55. Efficiency vs Output Current  
(VIN=12V, VOUT = 1.2V)

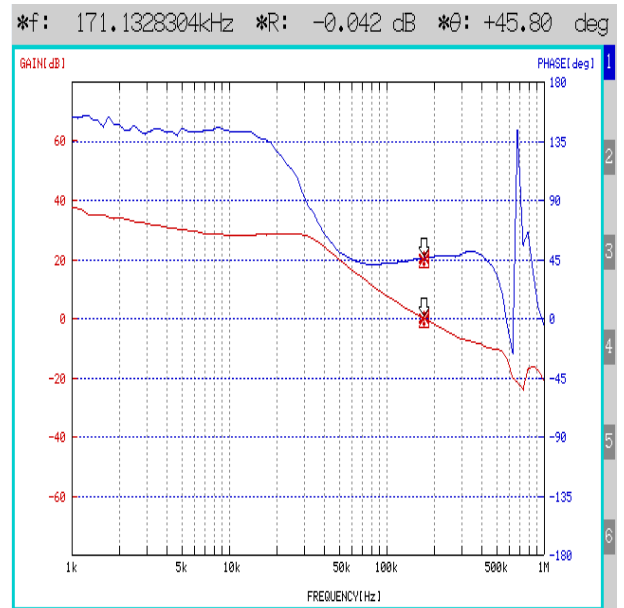


Figure 56. Loop Response IOUT=3A  
(VIN=12V, VOUT=1.2V)

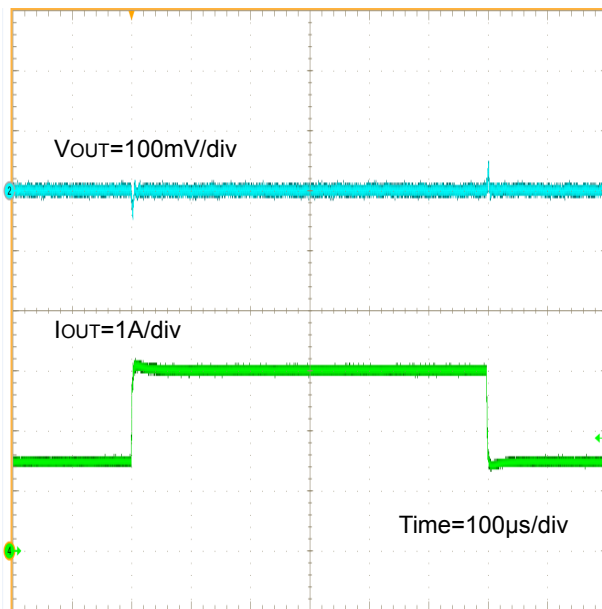


Figure 57. Load Transient Response IOUT=1.5A - 3A  
(VIN=12V, VOUT=1.2V)

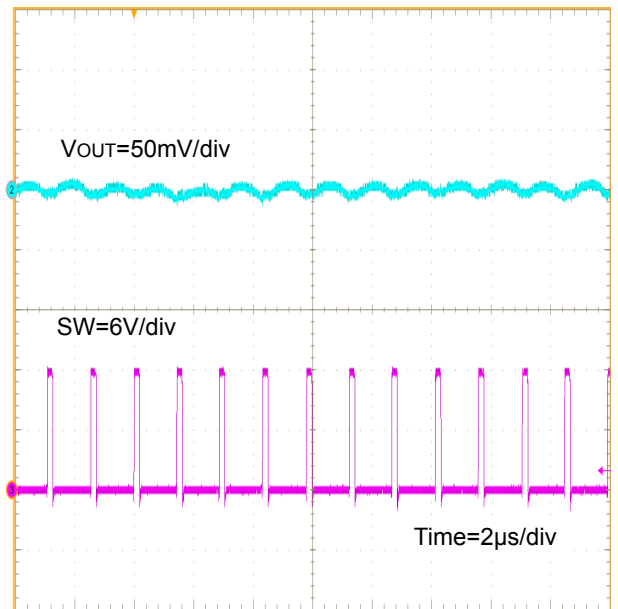


Figure 58. VOUT Ripple IOUT=3A  
(VIN = 12V, VOUT = 1.2V)

Selection of Components Externally Connected

About the application except the recommendation, please contact us.

(1) Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current  $\Delta I_L$  that flows into the inductor to be small. However, decreasing the ripple voltage generated in the output is not advantageous in terms of the load transient response characteristic. An inductor with a small inductance improves the load transient response characteristic but causes the inductor ripple current to be large which increases the ripple voltage in the output voltage, showing a trade-off relationship. Please use recommended inductor values.

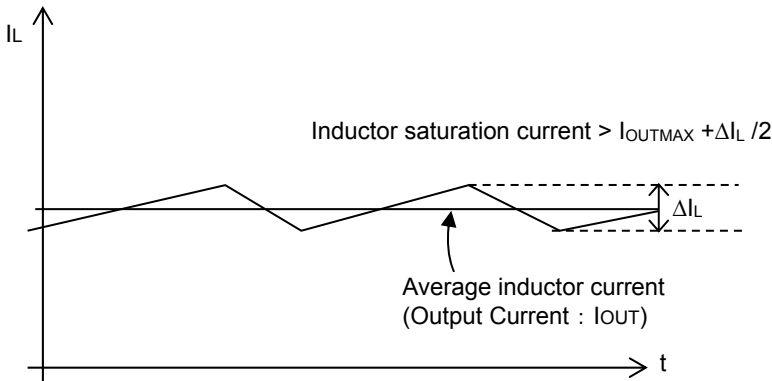


Figure 59. Waveform of current through inductor

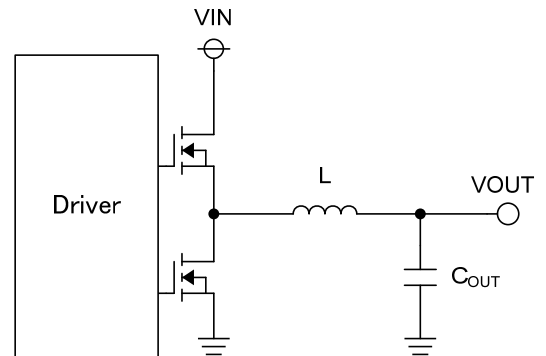


Figure 60. Output LC filter circuit

Here, select an inductance so that the size of the ripple current component of the inductor will be 20% to 50% of the Max output current (3A).  
 Now calculating with  $V_{IN} = 12V$ ,  $V_{OUT} = 1.8V$ , switching frequency  $F_{OSC} = 700kHz$ ,  $\Delta I_L$  is 1.0A, inductance value, that can be used is calculated as follows:

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 2.19 \div 2.2 [\mu H]$$

Also for saturation current of inductor, select the one with larger current than maximum output current added by 1/2 of inductor ripple current  $\Delta I_L$ .

Output capacitor  $C_{OUT}$  affects output ripple voltage characteristics. Select output capacitor  $C_{OUT}$  so that necessary ripple voltage characteristics are satisfied.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) [mV]$$

$R_{ESR}$  is the Equivalent Series Resistance (ESR) of the output capacitor.  
 With  $C_{OUT} = 44\mu F$ ,  $R_{ESR} = 10m\Omega$  the output ripple voltage is calculated as follows:

$$\Delta V_{RPL} = 1.0 \times (10m + \frac{1}{8 \times 44\mu \times 700k}) = 14.06 [mV]$$

※The capacitor rating must allow a sufficient margin with respect to the output voltage.  
 The output ripple voltage is decreased with a smaller ESR capacitor.  
 Considering temperature and DC bias characteristics, please use ceramic capacitor with 22 μF to 100 μF capacity.

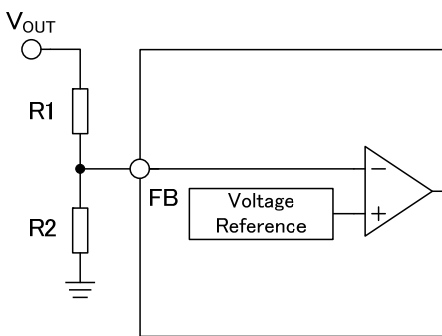
※Pay attention to total capacitance value, when additional capacitor C<sub>LOAD</sub> is connected in addition to output capacitor C<sub>OUT</sub>. Then, please determine C<sub>LOAD</sub> and soft start time T<sub>SS</sub> (Refer to (4) Soft Start Setting) as satisfying the following equation.

$$C_{OUT} + C_{LOAD} \leq \frac{(I_{OCP} - I_{OUT}) \times T_{SS}}{V_{OUT}} \text{ [F]}$$

I<sub>OCP</sub> is Over Current Protection Current limit value.

**(2) Output Voltage Setting**

The output voltage value is set by the feedback resistance ratio.



$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 0.765 \text{ [V]}$$

BD9D323QWZ operates under the condition which satisfies the following equation.

$$0.07 \leq \frac{V_{OUT}}{V_{IN}} \leq 0.65$$

Figure 61. Feedback Resistor Circuit

**(3) Input capacitor configuration**

For input capacitor, use a ceramic capacitor. It is more effective, the closer it is to the V<sub>IN</sub> pin and GND pin. Please consider temperature and DC bias characteristics when usage. For normal setting, 10μF is recommended, but with larger value, input ripple voltage can be further reduced. Also, considering temperature and DC bias characteristics, do not use capacity less than 4.7μF. In order to reduce the influence of high frequency noise, place 0.1μF ceramic capacitor close to V<sub>IN</sub> pin and GND pin as much as possible. When V<sub>IN</sub> is lower than 7V at normal state, double the value of input capacitor.

**(4) Soft Start Setting**

Turning the EN terminal signal High activates the soft start function. This makes output voltage to rise gradually while controlling current at start-up. This prevents output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$T_d = \frac{C_{SS} \times V_{TH}}{I_{SS}} \quad [\text{s}]$$

$$T_{SS} = \frac{C_{SS} \times V_{FB} \times 1.15}{I_{SS}} \quad [\text{s}]$$

T<sub>d</sub> : Soft Start Delay Time

T<sub>SS</sub> : Soft Start Time

C<sub>SS</sub> : Capacitor connected to Soft Start Time Terminal

V<sub>FB</sub> : FB Terminal Voltage (0.765V Typ)

V<sub>TH</sub> : Internal MOS threshold voltage (0.7V Typ)

I<sub>SS</sub> : Soft Start Terminal Source Current (2.0μA Typ)

With C<sub>SS</sub> = 3300pF,

$$T_d = (3300 \text{ pF} \times 0.7 \text{ V}) / 2.0 \text{ } \mu\text{A}$$

$$= 1.16\text{ms}$$

$$T_{SS} = (3300 \text{ pF} \times 0.765 \text{ V} \times 1.15) / 2.0 \text{ } \mu\text{A}$$

$$= 1.45\text{ms}$$

**(5) Bootstrap capacitor**

Connect 0.1μF ceramic capacitor between SW pin and BOOT pin.

**(6) VREG capacitor**

Connect 1μF ceramic capacitor to ground.

PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the high side FET is turned ON. The flow starts from the input capacitor  $C_{IN}$ , runs through the FET, inductor L and output capacitor  $C_{OUT}$  and back to ground of  $C_{IN}$  via ground of  $C_{OUT}$ . The second loop is the one into which the current flows when the low side FET is turned on. The flow starts from the low side FET, runs through the inductor L and output capacitor  $C_{OUT}$  and back to ground of the low side FET via ground of  $C_{OUT}$ . Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

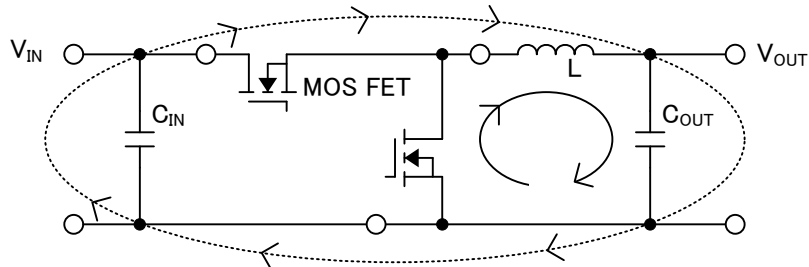
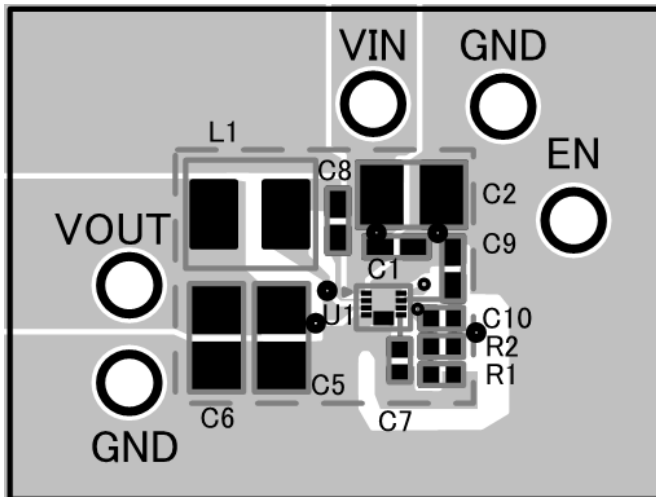


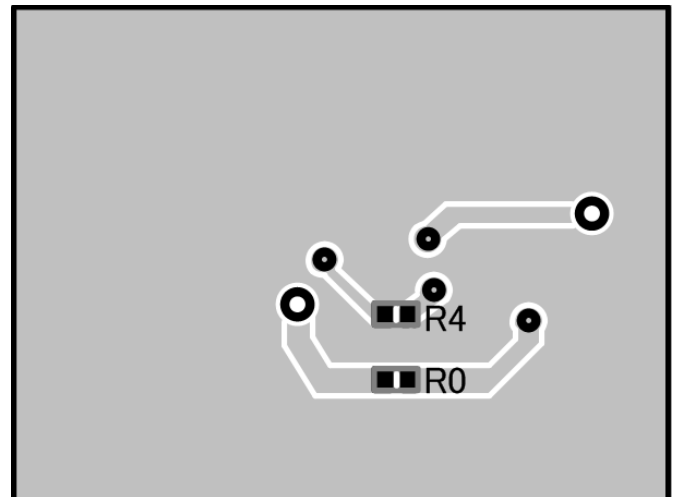
Figure 62. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC  $V_{IN}$  terminal and GND terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and SS far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



TOP Layer



Bottom Layer

Figure 63. Example of PCB layout

I/O Equivalent Circuit

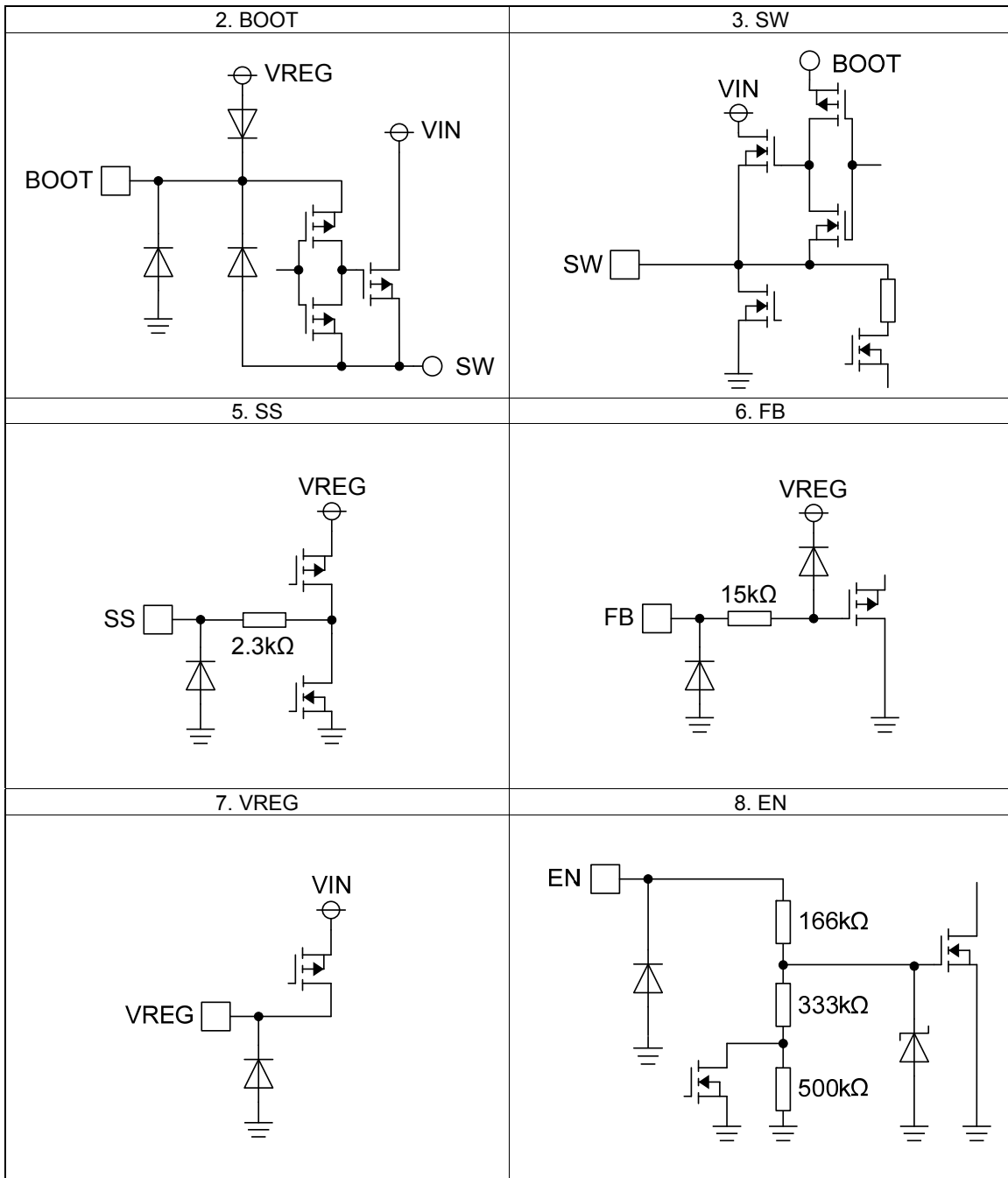


Figure 64. I/O equivalence circuit

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

## Operational Notes – continued

**8. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

**9. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**11. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

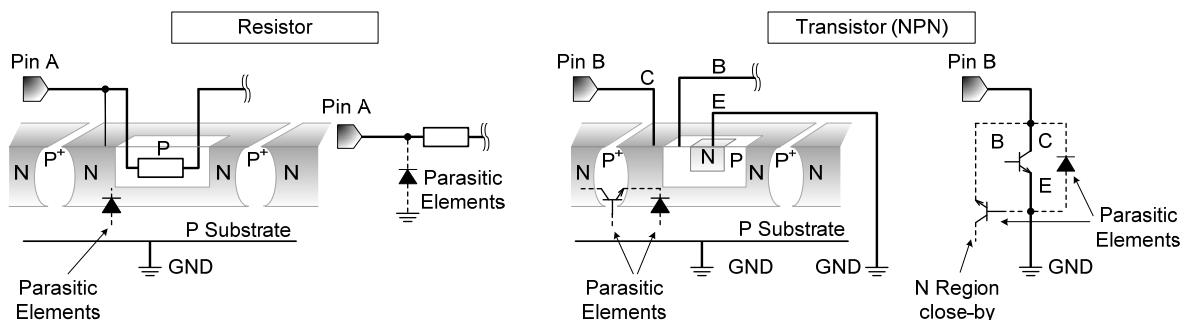


Figure 65. Example of monolithic IC structure

**12. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**13. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

**Operational Notes – continued****14. Thermal Shutdown Circuit(TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

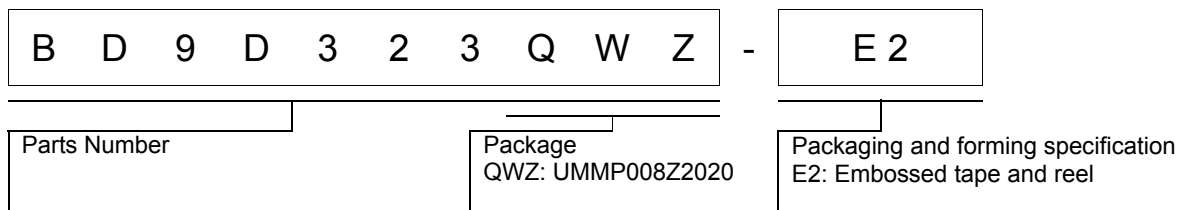
**15. Over Current Protection Circuit (OCP)**

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

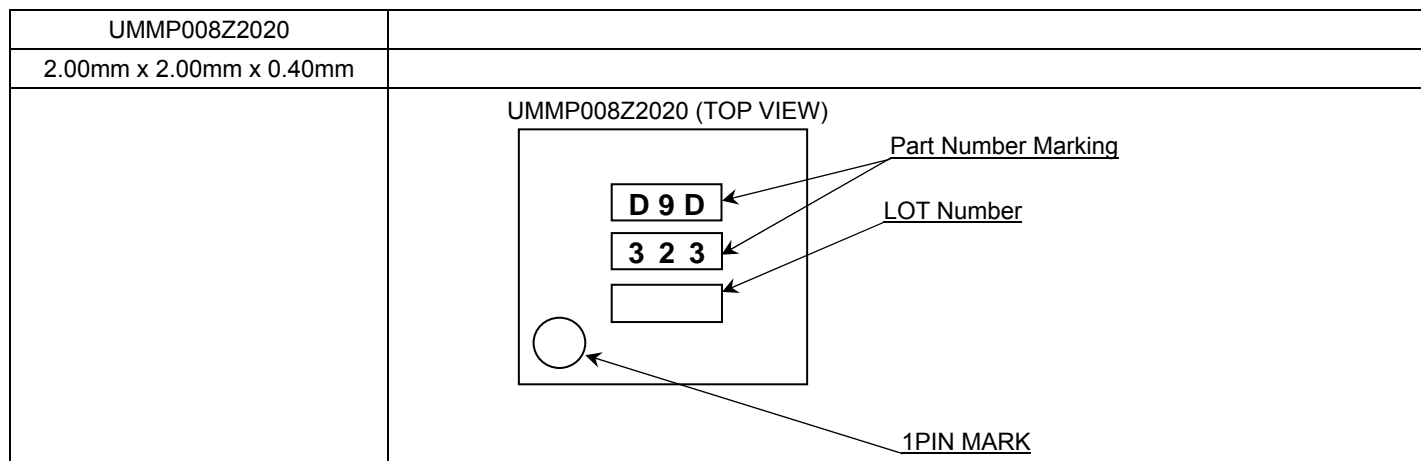
**16. Disturbance light**

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

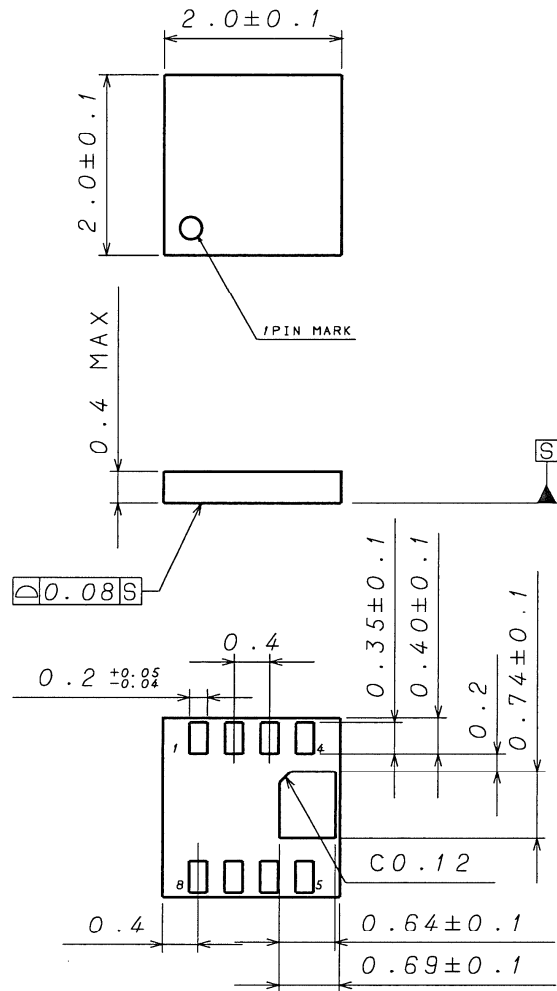


Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	UMMP008Z2020
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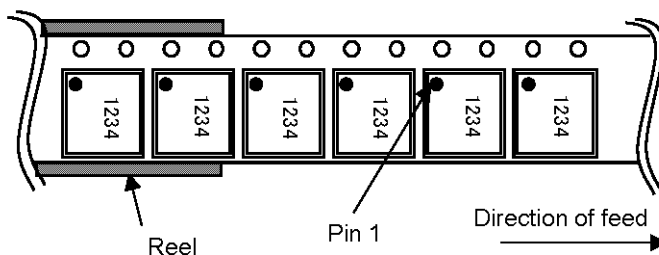


(UNIT : mm)

PKG : UMMP008Z2020

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



## Revision History

Date	Revision	Changes
-	001	Not Release
09.Dec.2016	002	New
06.Feb.2017	003	Added note in Recommended Operating Conditions.

# Notice

## Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment <sup>(Note 1)</sup>, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

### Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

### Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

### Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

### Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

### Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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