



**THE DATASHEET OF
BLS7G3135LS-200U**



BLS7G3135LS-200

LDMOS S-band radar power transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for S-band radar applications in the frequency range from 3100 MHz to 3500 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$; $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\%$; $I_{Dq} = 100\text{ mA}$; in a class-AB production test circuit.

Test signal	f (GHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	t _r (ns)	t _f (ns)
pulsed RF	3.1	32	200	12	48	8	6
	3.3	32	200	12	46	8	6
	3.5	32	200	12	43	8	6

1.2 Features and benefits

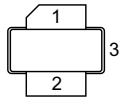
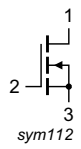
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use (input and output)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequency range 3100 MHz to 3500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS7G3135LS-200	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	65	V
V_{GS}	gate-source voltage	-0.5	+13	V
T_{stg}	storage temperature	-65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	$T_{case} = 85\text{ °C}; P_L = 200\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.147	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.162	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.186	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.7\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	4.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	51	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	420	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 2.7\text{ A}$	-	2.34	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	0.06	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\%$; RF performance at $V_{DS} = 32\text{ V}$; $I_{DQ} = 100\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 200\text{ W}$	8.8	12	-	dB
RL_{in}	input return loss	$P_L = 200\text{ W}$	-	-8	-4	dB
η_D	drain efficiency	$P_L = 200\text{ W}$	38	43	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 200\text{ W}$	-	0.1	0.25	dB
t_r	rise time	$P_L = 200\text{ W}$	-	8	50	ns
t_f	fall time	$P_L = 200\text{ W}$	-	6	50	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLS7G3135LS-200 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 32\text{ V}$; $I_{DQ} = 100\text{ mA}$; $P_L = 200\text{ W}$; $f = 3100\text{ MHz}$; $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\%$.

7.2 Impedance information

Table 8. Typical impedance

Measured load pull data; $V_{DS} = 32\text{ V}$; $I_{DQ} = 100\text{ mA}$; typical values unless otherwise specified.

f (MHz)	Z_S (Ω)	Z_L (Ω)
3100	0.9 – j4.3	5.3 – j1.6
3200	1.3 – j4.9	4.8 – j1.5
3300	1.7 – j5.5	4.6 – j1.9
3400	2.4 – j6.4	4.0 – j2.1
3500	4.1 – j6.9	4.0 – j2.1

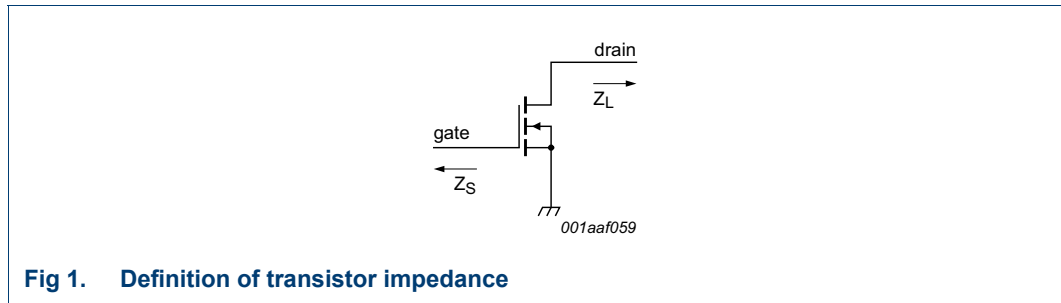
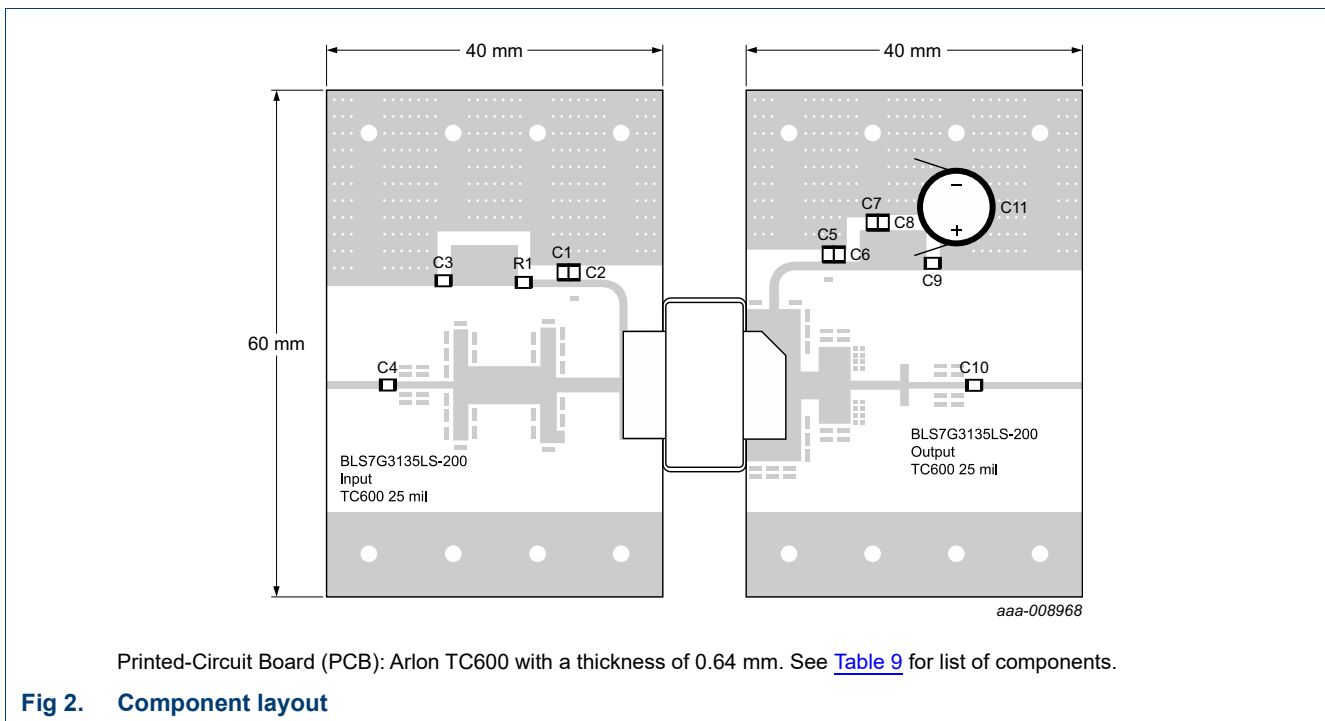


Fig 1. Definition of transistor impedance

7.3 Test circuit information



Printed-Circuit Board (PCB): Arlon TC600 with a thickness of 0.64 mm. See [Table 9](#) for list of components.

Fig 2. Component layout

Table 9. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C4, C4, C10	multilayer ceramic chip capacitor	15 pF	[1] ATC600F
C2, C5	multilayer ceramic chip capacitor	10 pF	[1] ATC600F
C3, C9	multilayer ceramic chip capacitor	0.1 μ F	[2] TDK
C7	multilayer ceramic chip capacitor	1 μ F	[3] Murata
C8	multilayer ceramic chip capacitor	10 μ F	[3] Murata
C11	electrolytic capacitor	2200 μ F, 63 V	
R1	chip resistor	9.1 Ω	[4] SMD 0805

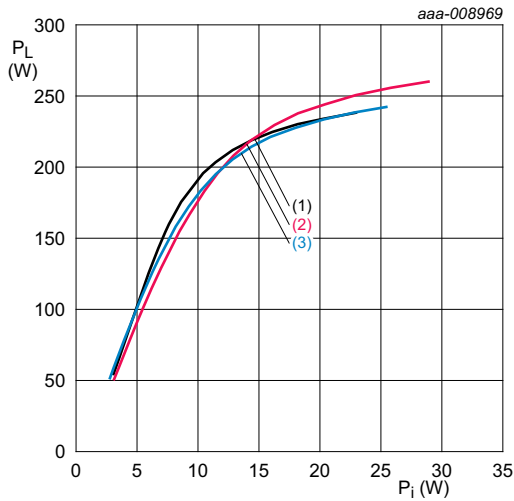
[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] Murata or capacitor of same quality.

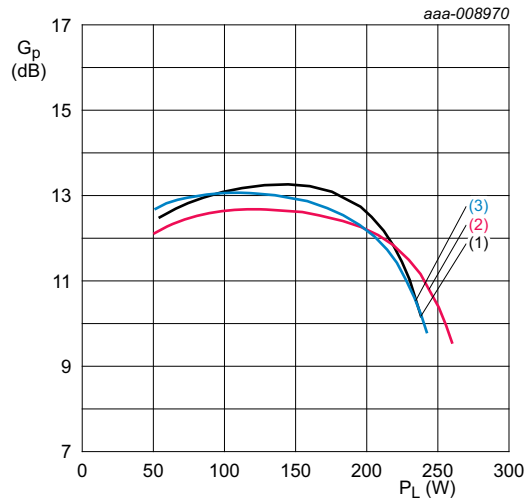
[4] Vishay Dale or resistor of same quality.

7.4 Graphical data



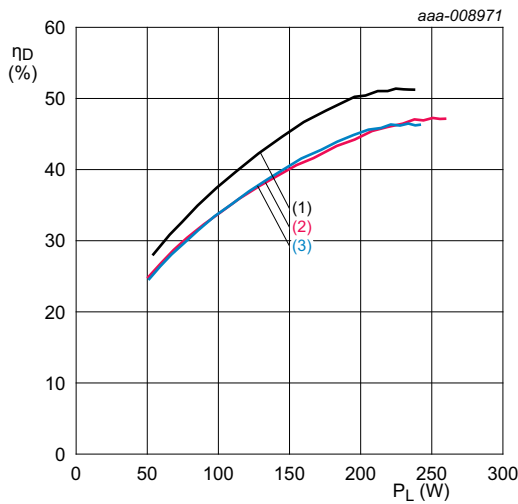
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; \delta = 10\%; t_p = 300\ \mu\text{s}.$
 (1) $f = 3100\text{ MHz}$
 (2) $f = 3300\text{ MHz}$
 (3) $f = 3500\text{ MHz}$

Fig 3. Output power as a function of input power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; \delta = 10\%; t_p = 300\ \mu\text{s}.$
 (1) $f = 3100\text{ MHz}$
 (2) $f = 3300\text{ MHz}$
 (3) $f = 3500\text{ MHz}$

Fig 4. Power gain as a function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; \delta = 10\%; t_p = 300\ \mu\text{s}.$
 (1) $f = 3100\text{ MHz}$
 (2) $f = 3300\text{ MHz}$
 (3) $f = 3500\text{ MHz}$

Fig 5. Drain efficiency as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads

SOT502B

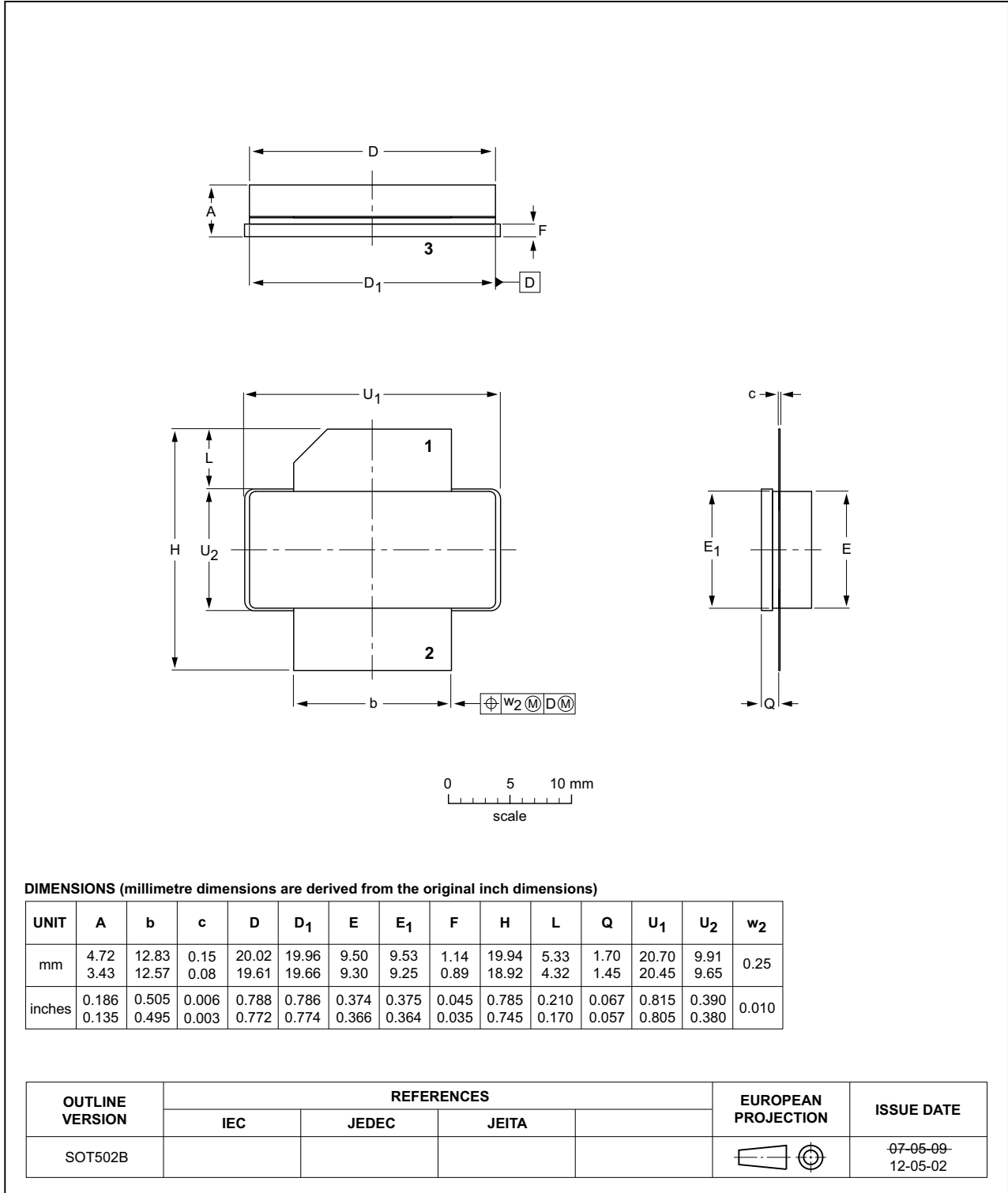


Fig 6. Package outline SOT502B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
S-band	Short wave band
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS7G3135LS-200#3	20150901	Product data sheet		BLS7G3135LS-200 v.2
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLS7G3135LS-200 v.2	20130923	Product data sheet	-	BLS7G3135LS-200 v.1
BLS7G3135LS-200 v.1	20121009	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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