



**THE DATASHEET OF  
BSH205,215**



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Kind regards,

Team Nexperia

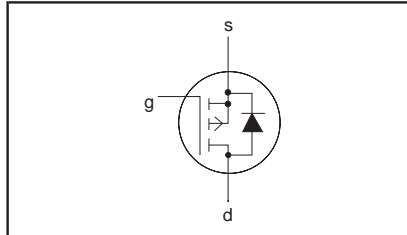
## P-channel enhancement mode MOS transistor

BSH205

### FEATURES

- Very low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

### SYMBOL



### QUICK REFERENCE DATA

$$V_{DS} = -12 \text{ V}$$

$$I_D = -0.75 \text{ A}$$

$$R_{DS(ON)} \leq 0.5 \Omega \quad (V_{GS} = -2.5 \text{ V})$$

$$V_{GS(TO)} \geq 0.4 \text{ V}$$

### GENERAL DESCRIPTION

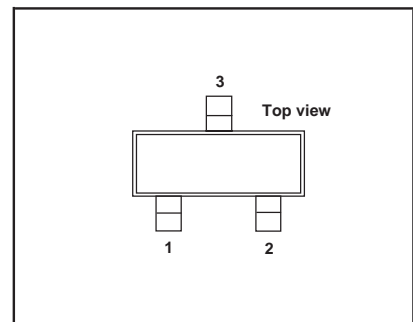
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH205 is supplied in the SOT23 subminiature surface mounting package.

### PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

### SOT23



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage		-	-12	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	-12	V
$V_{GS}$	Gate-source voltage		-	$\pm 8$	V
$I_D$	Drain current (DC)	$T_a = 25 \text{ }^\circ\text{C}$	-	-0.75	A
		$T_a = 100 \text{ }^\circ\text{C}$	-	-0.47	A
$I_{DM}$	Drain current (pulse peak value)	$T_a = 25 \text{ }^\circ\text{C}$	-	-3	A
$P_{tot}$	Total power dissipation	$T_a = 25 \text{ }^\circ\text{C}$	-	0.417	W
		$T_a = 100 \text{ }^\circ\text{C}$	-	0.17	W
$T_{stg}, T_j$	Storage & operating temperature		-55	150	$^\circ\text{C}$

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

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**ELECTRICAL CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

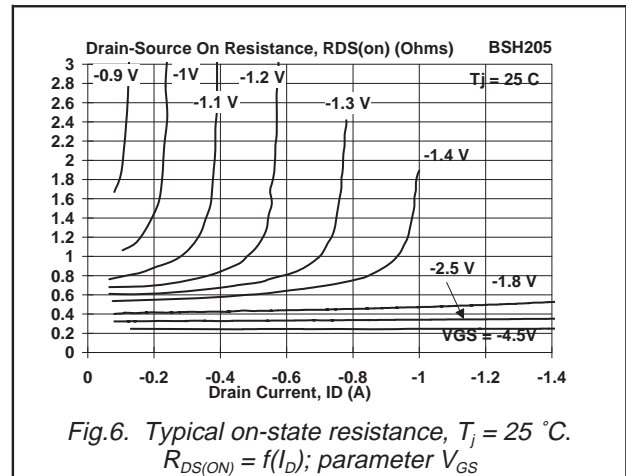
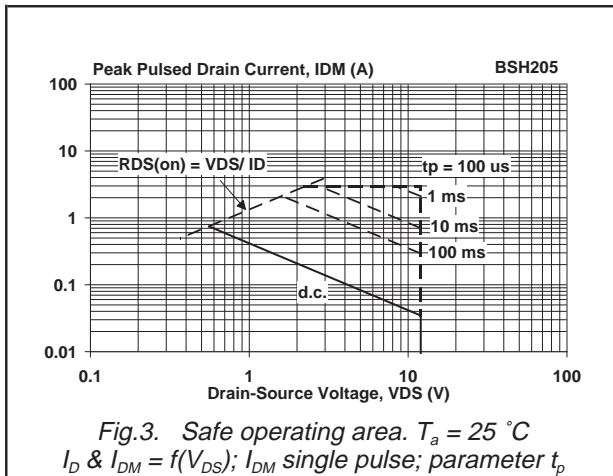
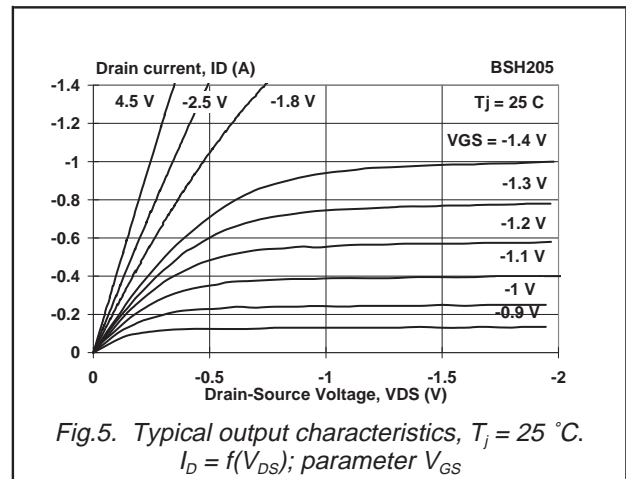
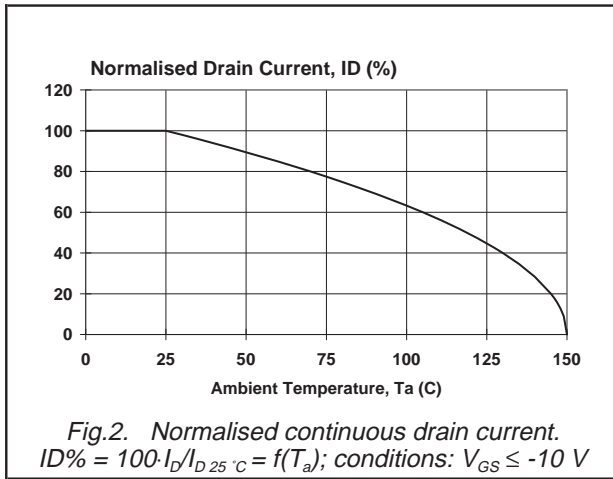
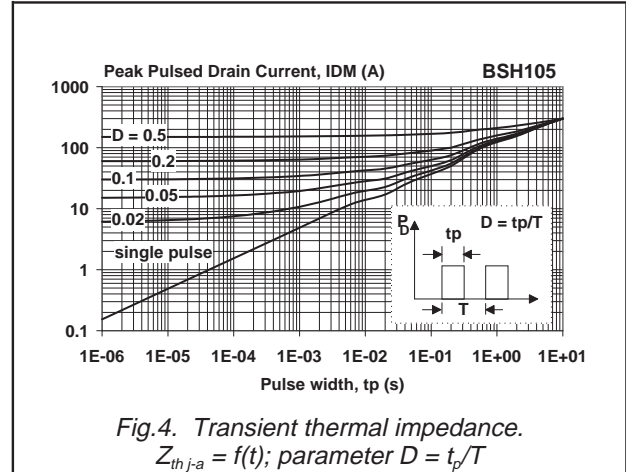
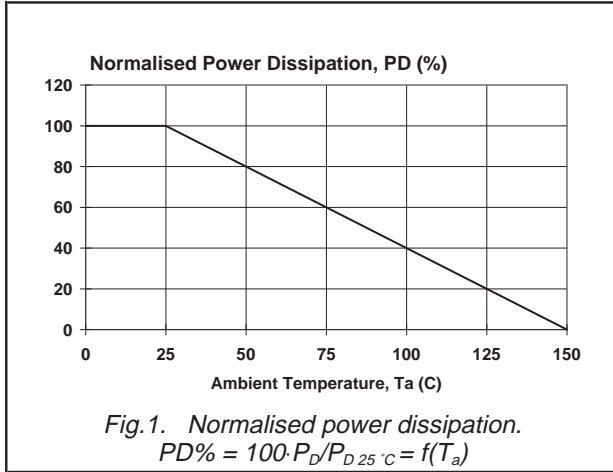
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = -10\ \mu\text{A}$	-12	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = -1\ \text{mA}$ $T_j = 150^\circ\text{C}$	-0.4 -0.1	-0.68 -	- -	V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}; I_D = -430\ \text{mA}$ $V_{GS} = -2.5\ \text{V}; I_D = -430\ \text{mA}$ $V_{GS} = -1.8\ \text{V}; I_D = -210\ \text{mA}$ $V_{GS} = -2.5\ \text{V}; I_D = -430\ \text{mA}; T_j = 150^\circ\text{C}$	- - - -	0.18 0.32 0.42 0.48	0.4 0.5 0.6 0.75	$\Omega$ $\Omega$ $\Omega$ $\Omega$
$g_{fs}$	Forward transconductance	$V_{DS} = -9.6\ \text{V}; I_D = -430\ \text{mA}$	0.5	1.6	-	S
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 8\ \text{V}; V_{DS} = 0\ \text{V}$	-	$\pm 10$	$\pm 100$	nA
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = -9.6\ \text{V}; V_{GS} = 0\ \text{V};$ $T_j = 150^\circ\text{C}$	-	-50 -11	-100 -100	nA $\mu\text{A}$
$Q_{g(\text{tot})}$	Total gate charge	$I_D = -0.5\ \text{A}; V_{DD} = -10\ \text{V}; V_{GS} = -4.5\ \text{V}$	-	3.8	-	nC
$Q_{gs}$	Gate-source charge		-	0.4	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	1.0	-	nC
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = -10\ \text{V}; I_D = -0.5\ \text{A};$	-	2	-	ns
$t_r$	Turn-on rise time	$V_{GS} = -8\ \text{V}; R_G = 6\ \Omega$	-	4.5	-	ns
$t_{d\text{ off}}$	Turn-off delay time	Resistive load	-	45	-	ns
$t_f$	Turn-off fall time		-	20	-	ns
$C_{iss}$	Input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = -9.6\ \text{V}; f = 1\ \text{MHz}$	-	200	-	pF
$C_{oss}$	Output capacitance		-	95	-	pF
$C_{rss}$	Feedback capacitance		-	41	-	pF

**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	$T_a = 25^\circ\text{C}$	-	-	-0.75	A
$I_{DRM}$	Pulsed reverse drain current		-	-	-3	A
$V_{SD}$	Diode forward voltage	$I_F = -0.38\ \text{A}; V_{GS} = 0\ \text{V}$	-	-0.72	-1.3	V
$t_{rr}$	Reverse recovery time	$I_F = -0.5\ \text{A}; -di_F/dt = 100\ \text{A}/\mu\text{s};$	-	75	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0\ \text{V}; V_R = -9.6\ \text{V}$	-	69	-	nC

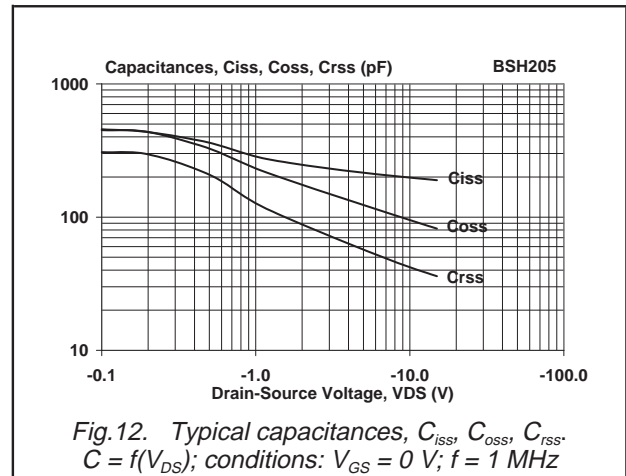
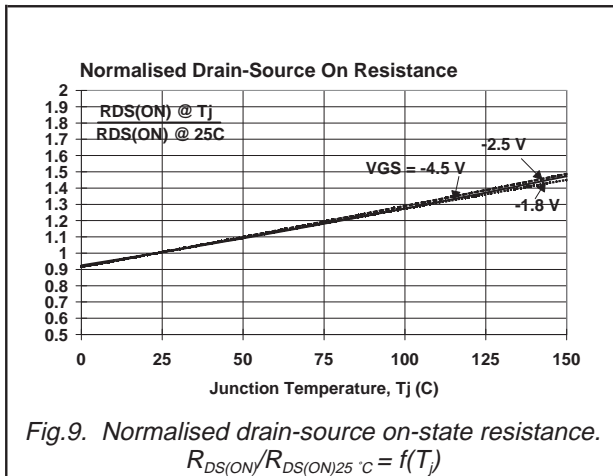
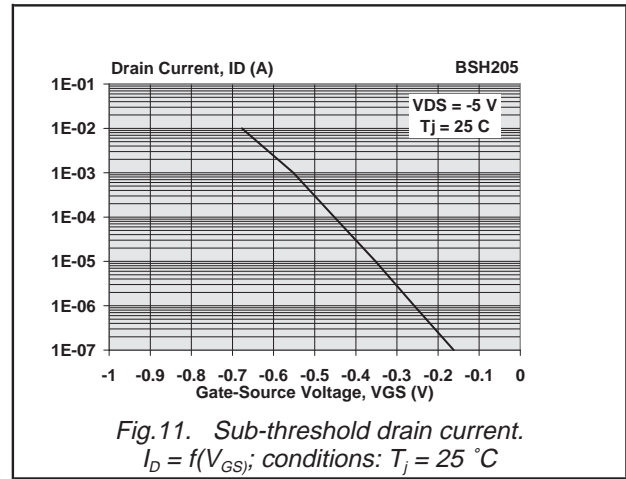
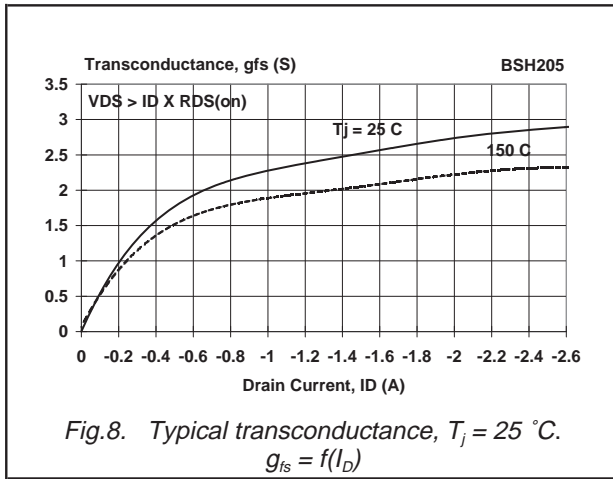
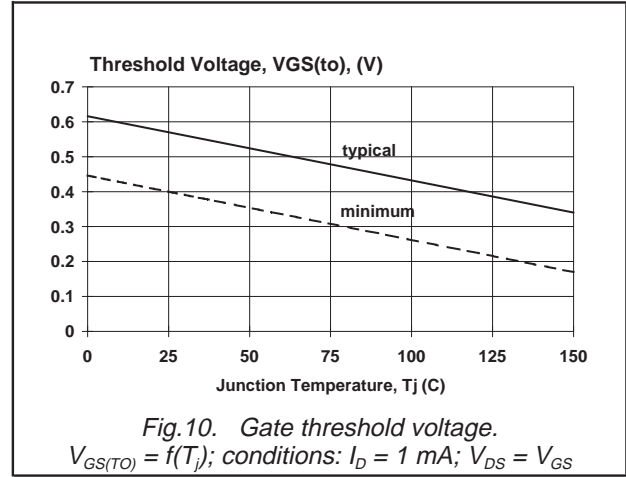
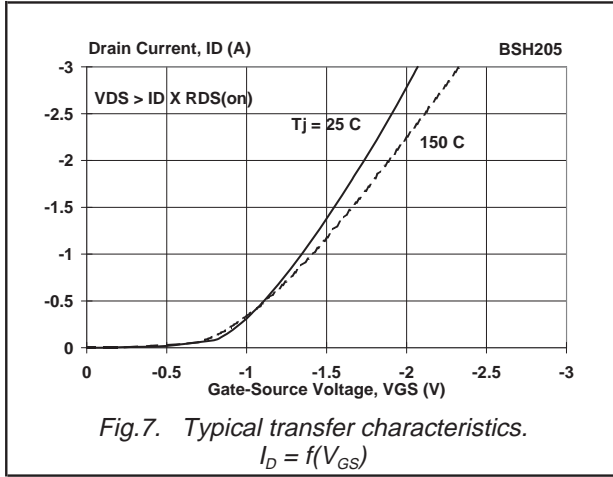
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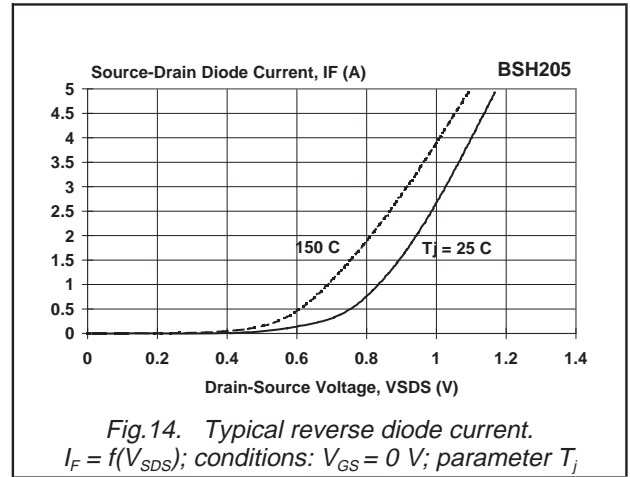
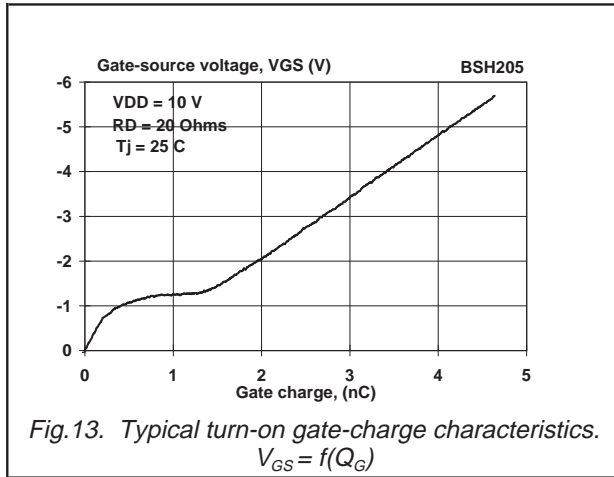
P-channel enhancement mode  
MOS transistor

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MECHANICAL DATA

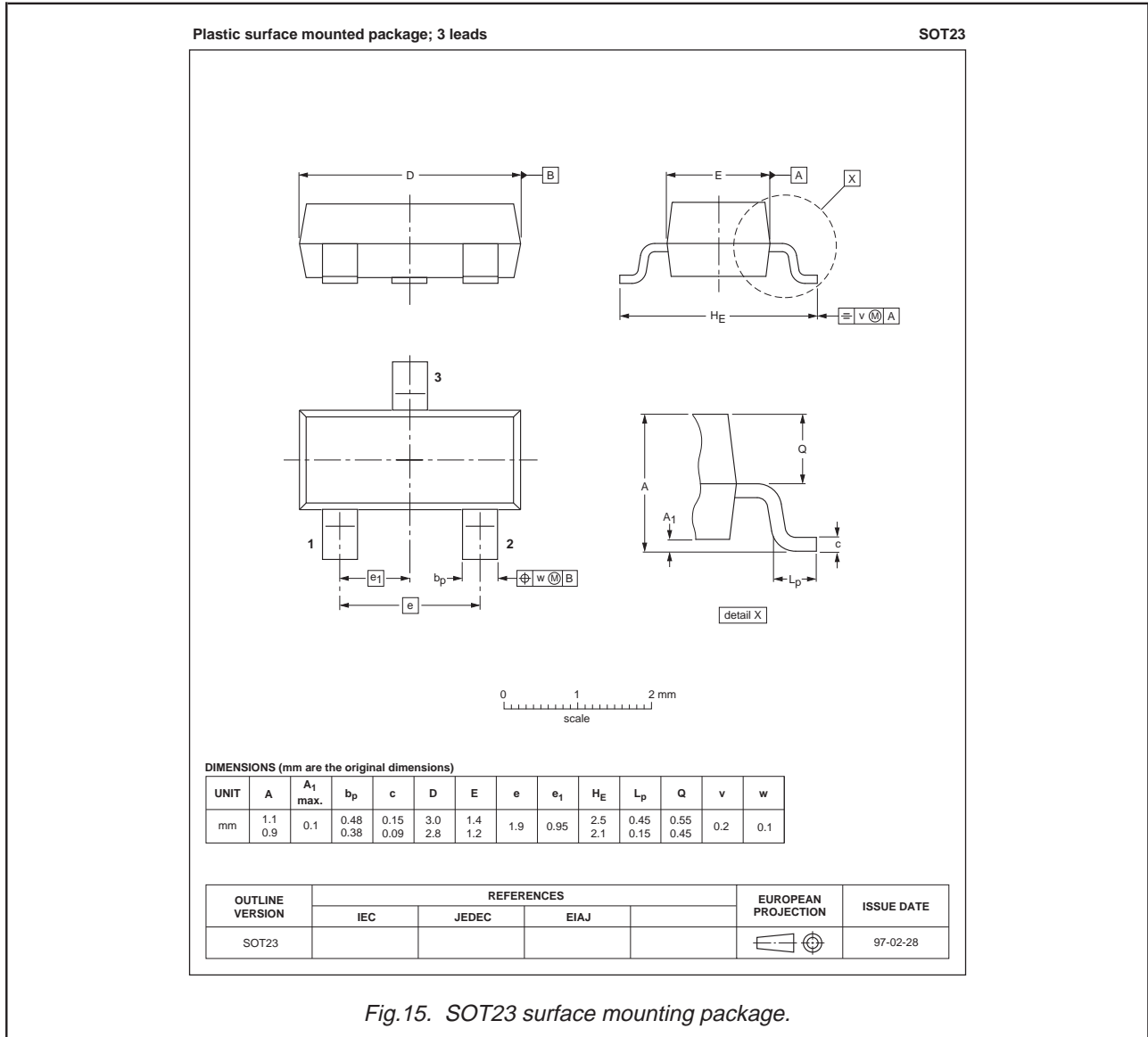


Fig.15. SOT23 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

## Looking for pricing, stock, or lifecycle information?

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