



**THE DATASHEET OF  
BSP225/S911115**



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Team Nexperia

# DATA SHEET

## **BSP225**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# P-channel enhancement mode vertical D-MOS transistor

**BSP225**

## FEATURES

- Low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

## DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

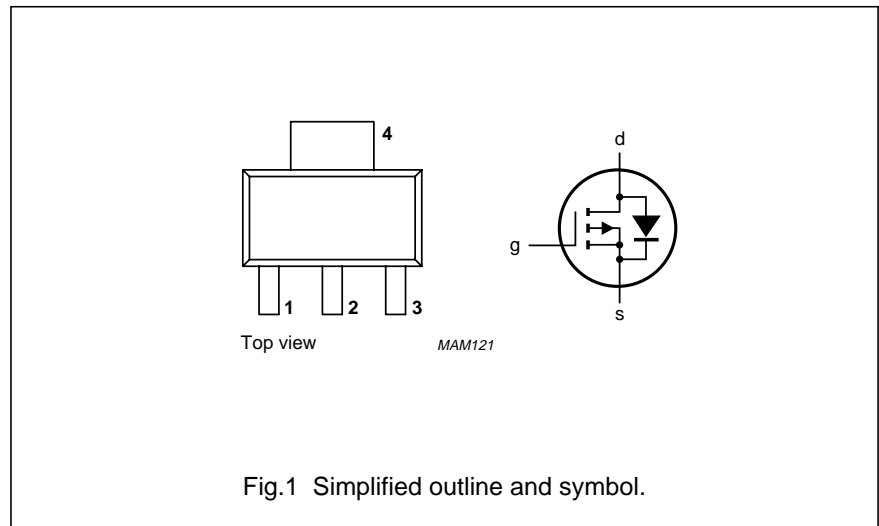
## PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200 \text{ mA}$ $-V_{GS} = 10 \text{ V}$	15	$\Omega$
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1 \text{ mA}$ $V_{GS} = V_{DS}$	2.8	V

## PIN CONFIGURATION



## P-channel enhancement mode vertical D-MOS transistor

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### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ °C}$ (note 1)	–	1.5	W
$T_{stg}$	storage temperature range		–65	150	°C
$T_j$	junction temperature		–	150	°C

#### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

### THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3	K/W

#### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

# P-channel enhancement mode vertical D-MOS transistor

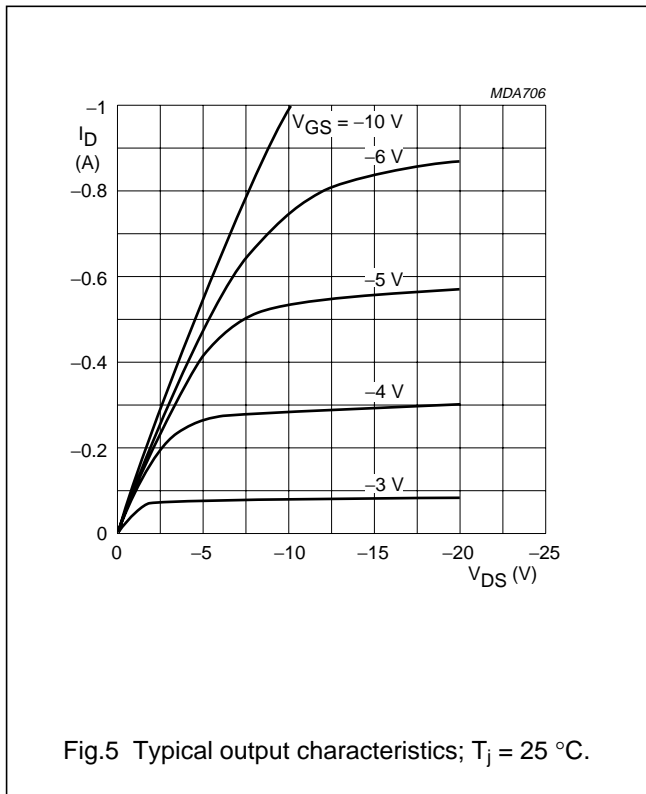
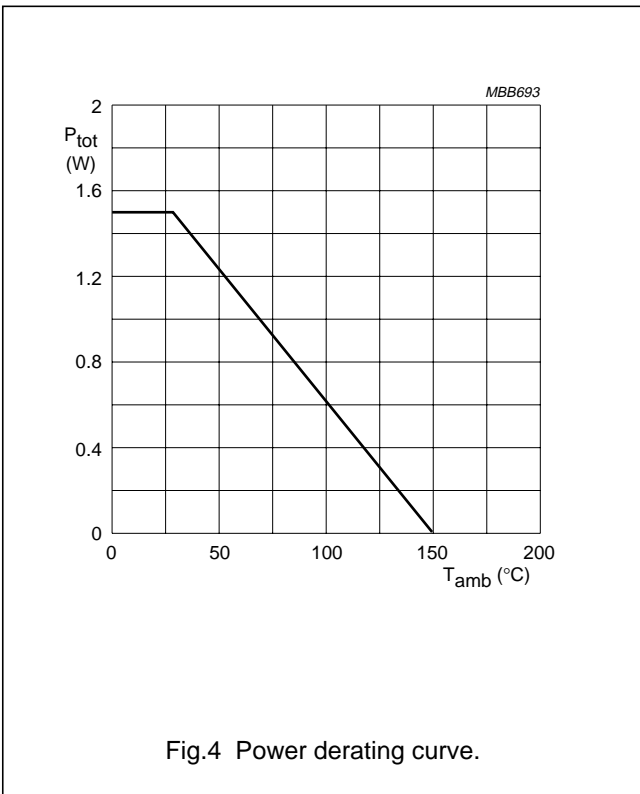
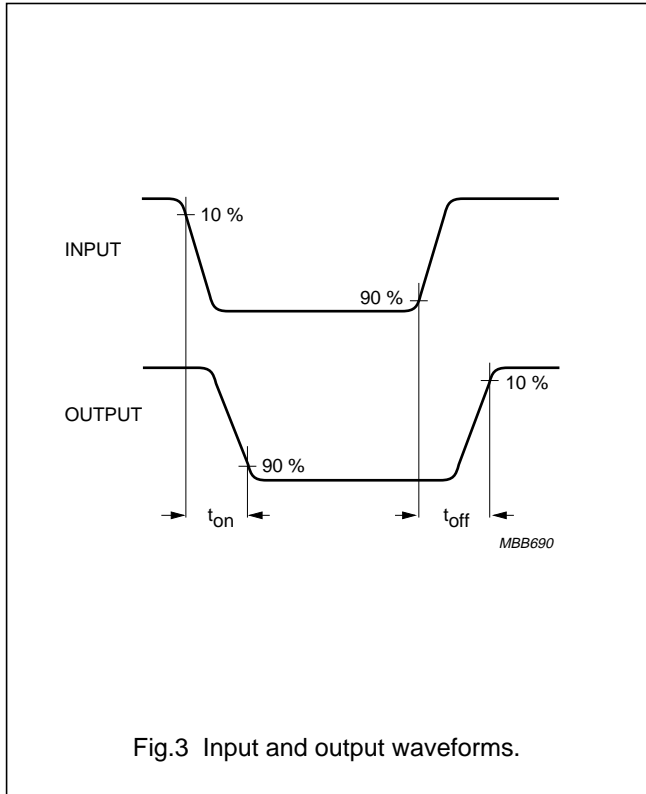
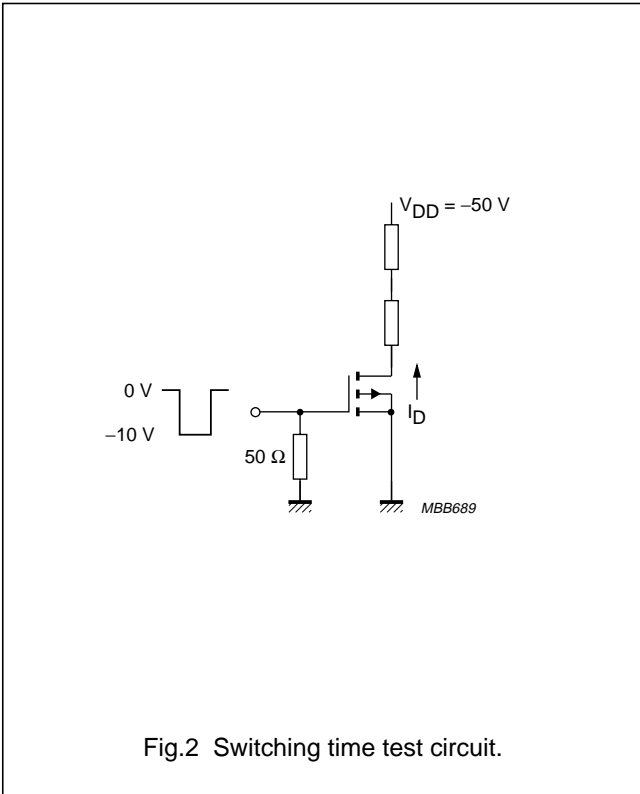
BSP225

**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 200\ \text{V}$ $V_{GS} = 0$	–	–	1	$\mu\text{A}$
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20\ \text{V}$	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200\ \text{mA}$ $-V_{GS} = 10\ \text{V}$	–	10	15	$\Omega$
$ Y_{fs} $	transfer admittance	$-I_D = 200\ \text{mA}$ $-V_{DS} = 25\ \text{V}$	100	200	–	mS
$C_{iss}$	input capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	65	90	pF
$C_{oss}$	output capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	20	30	pF
$C_{rss}$	feedback capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	6	15	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$-I_D = 250\ \text{mA}$ $-V_{DD} = 50\ \text{V}$ $-V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	5	10	ns
$t_{off}$	turn-off time	$-I_D = 250\ \text{mA}$ $-V_{DD} = 50\ \text{V}$ $-V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	20	30	ns

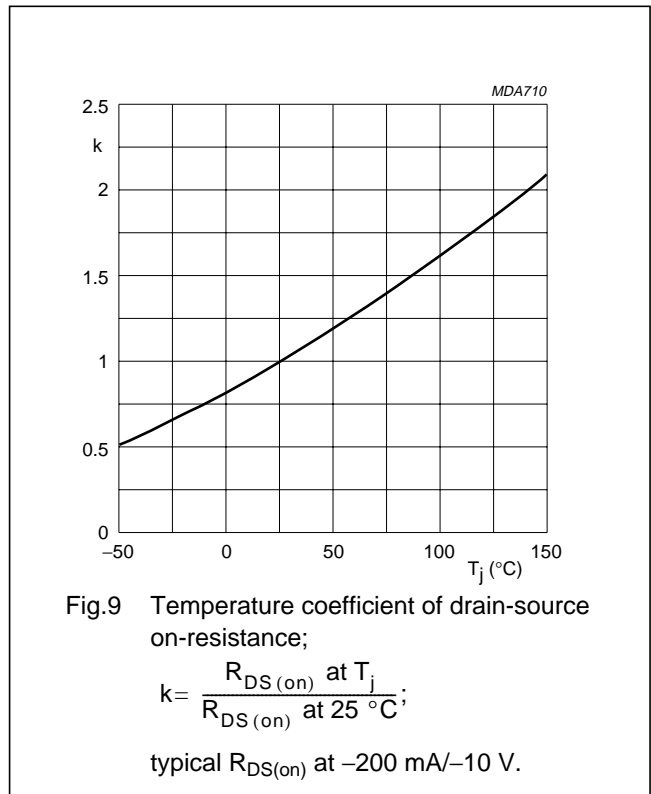
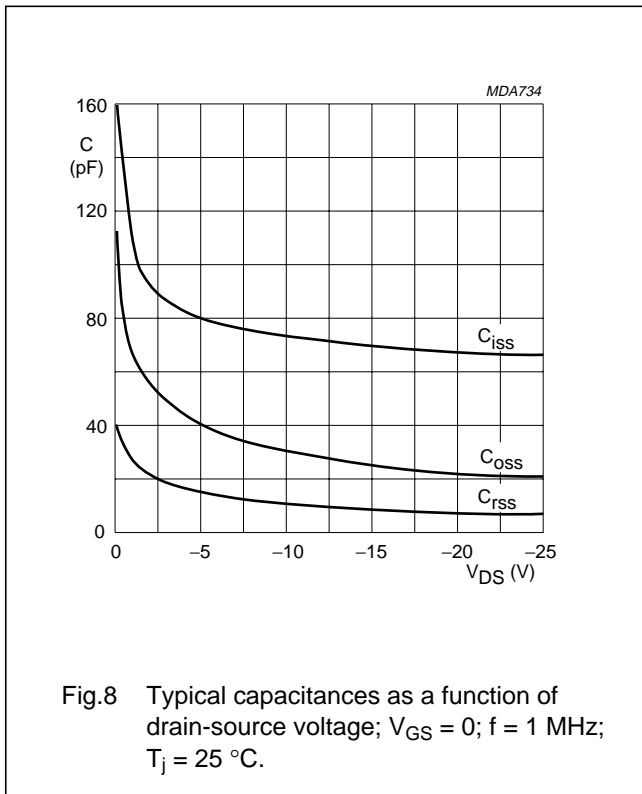
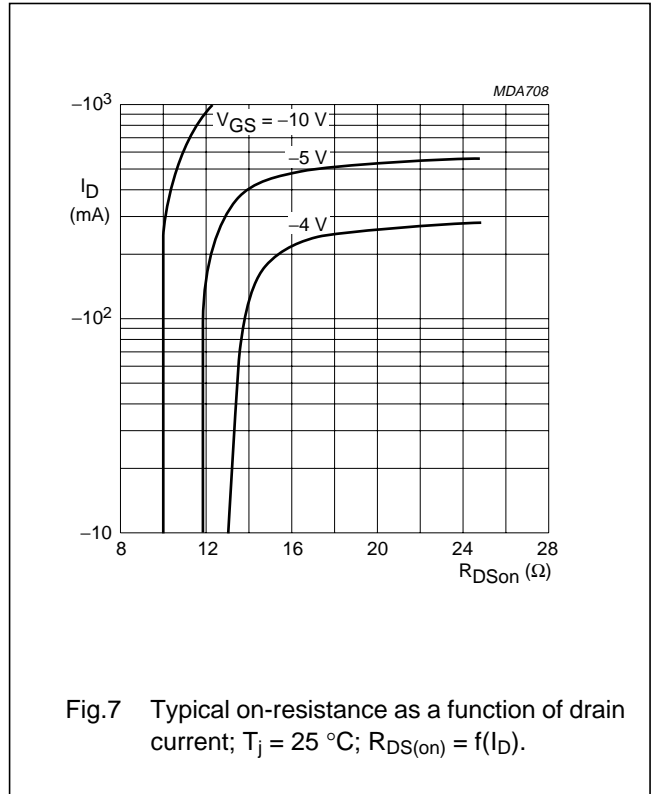
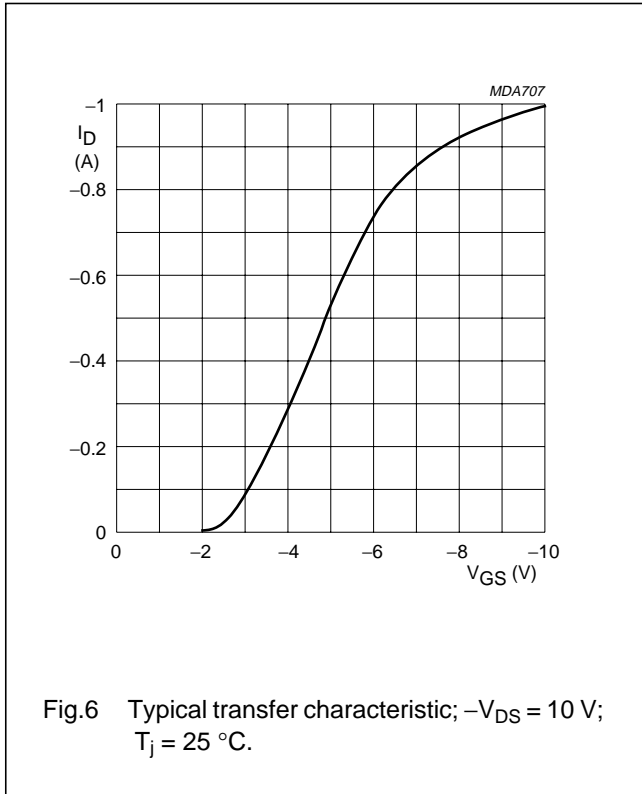
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P-channel enhancement mode vertical  
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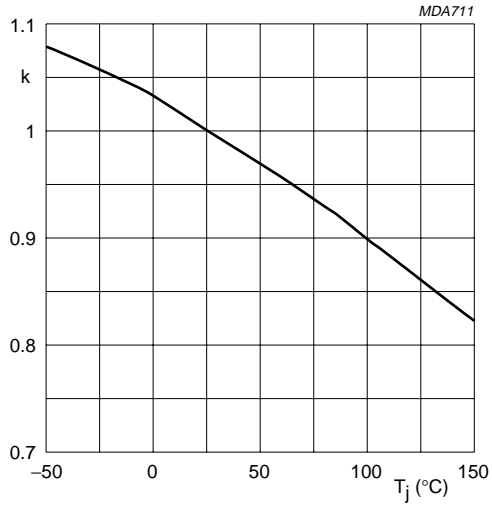


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25^\circ\text{C}};$$

typical  $V_{GS(th)}$  at -1 mA.

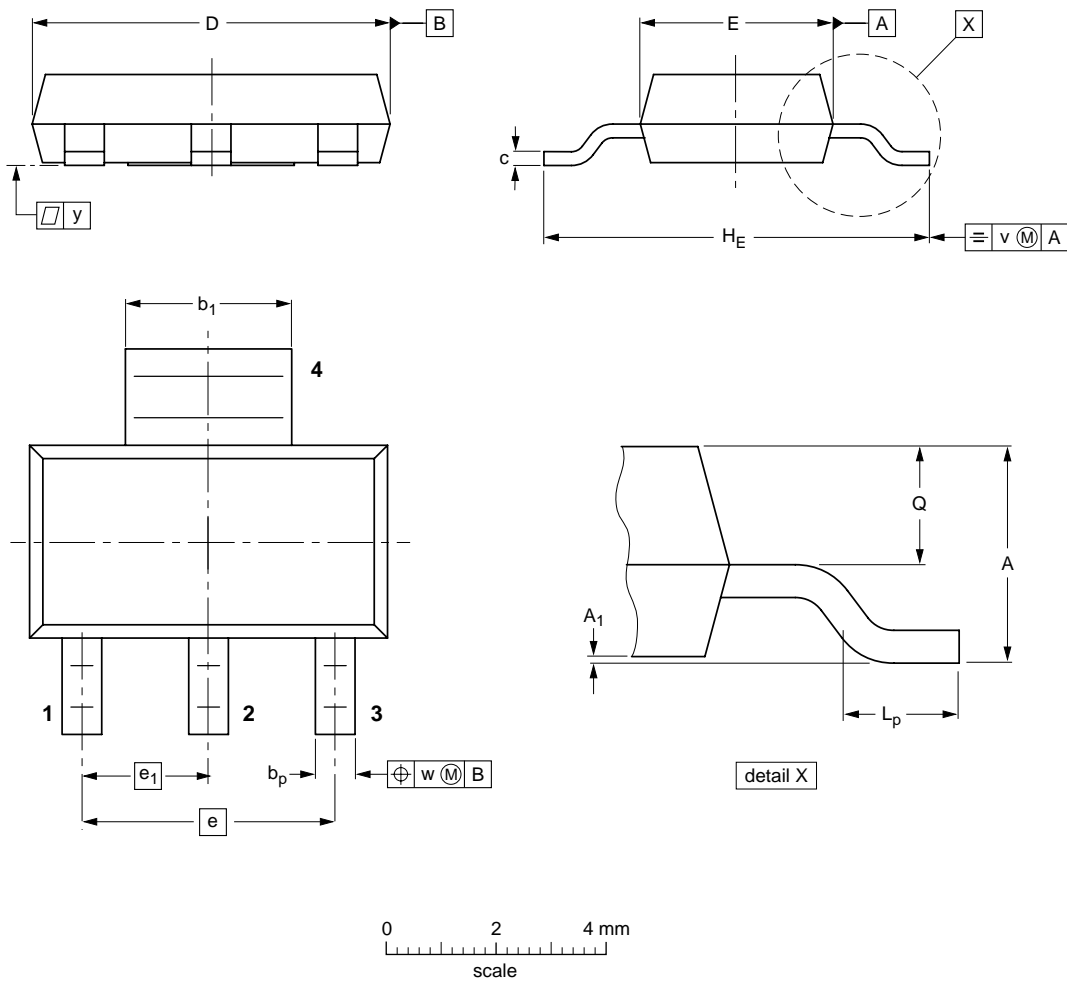
P-channel enhancement mode vertical  
D-MOS transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

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**P-channel enhancement mode vertical  
D-MOS transistor**

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**BSP225****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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P-channel enhancement mode vertical  
D-MOS transistor

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**NOTES**

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P-channel enhancement mode vertical  
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**NOTES**

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
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**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Colombia:** see South America

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**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
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**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
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**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
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**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
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**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
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**Indonesia:** see Singapore

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Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
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**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
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Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
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Printed in The Netherlands

137107/00/01/pp12

Date of release: April 1995

Document order number: 9397 750 02483

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