



**THE DATASHEET OF
SIHF9Z24STRR-GE3**



Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	- 60
$R_{DS(on)}$ (Ω)	$V_{GS} = -10\text{ V}$ 0.28
Q_g max. (nC)	19
Q_{gs} (nC)	5.4
Q_{gd} (nC)	11
Configuration	Single

FEATURES

- Advanced process technology
- Surface mount (IRF9Z24S, SiHF9Z24S)
- 175 °C operating temperature
- Fast switching
- P-channel
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

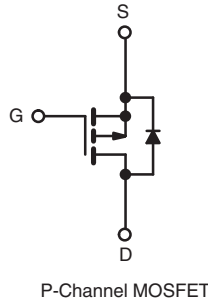
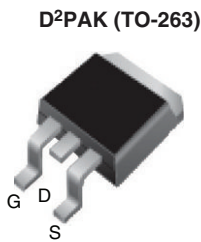
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.



ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9Z24S-GE3	SiHF9Z24STRL-GE3 ^a	SiHF9Z24STRR-GE3 ^a
Lead (Pb)-free	IRF9Z24SPbF	IRF9Z24STRLPbF ^a	IRF9Z24STRRPbF ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^e	V_{GS} at -10 V	$T_C = 25\text{ }^\circ\text{C}$	-11
		$T_C = 100\text{ }^\circ\text{C}$	-7.7
Pulsed Drain Current ^{a, e}		I_{DM}	-44
Linear Derating Factor			0.40
Single Pulse Avalanche Energy ^{b, e}		E_{AS}	240
Repetitive Avalanche Current ^a		I_{AR}	-11
Repetitive Avalanche Energy ^a		E_{AR}	6.0
Maximum Power Dissipation		$T_A = 25\text{ }^\circ\text{C}$	3.7
		$T_C = 25\text{ }^\circ\text{C}$	60
Peak Diode Recovery dV/dt ^{c, e}		dV/dt	-4.5
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175
Soldering Recommendations (Peak temperature) ^d		for 10 s	300

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 2.3\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -11\text{ A}$ (see fig. 12).
- $I_{SD} \leq -11\text{ A}$, $dI/dt \leq 140\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Uses IRF9Z24, SiHF9Z24 data and test conditions.



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient (PCB mount) ^a	R _{thJA}	-	-	40	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	-	2.5		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA ^c		-	-0.056	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -6.6 A ^b	-	-	0.28	Ω
Forward Transconductance	g _{fs}	V _{DS} = -25 V, I _D = -6.6 A ^c		1.4	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5 ^c		-	570	-	pF
Output Capacitance	C _{oss}			-	360	-	
Reverse Transfer Capacitance	C _{rss}			-	65	-	
Total Gate Charge	Q _g	V _{GS} = -10 V	I _D = -11 A, V _{DS} = -48 V, see fig. 6 and 13 ^{b, c}	-	-	19	nC
Gate-Source Charge	Q _{gs}			-	-	5.4	
Gate-Drain Charge	Q _{gd}			-	-	11	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, I _D = -11 A, R _g = 18 Ω, R _D = 2.5 Ω, see fig. 10 ^b		-	13	-	ns
Rise Time	t _r			-	68	-	
Turn-Off Delay Time	t _{d(off)}			-	15	-	
Fall Time	t _f			-	29	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-11	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	-44	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -11 A, V _{GS} = 0 V ^b		-	-	-6.3	V
Drain-Source Body Diode Characteristics							
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -11 A, dI/dt = 100 A/μs ^{b, c}		-	100	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	320	640	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. Uses IRF9Z24, SiHF9Z24 data and test conditions.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

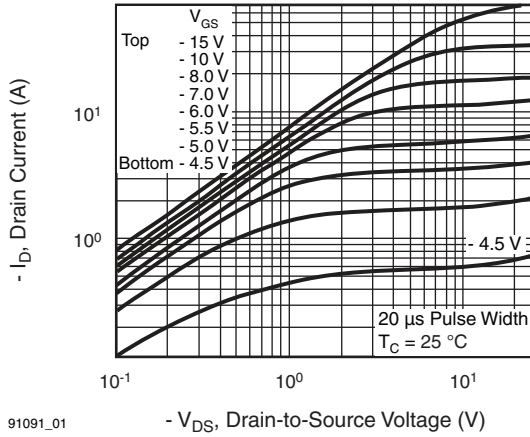


Fig. 1 - Typical Output Characteristics

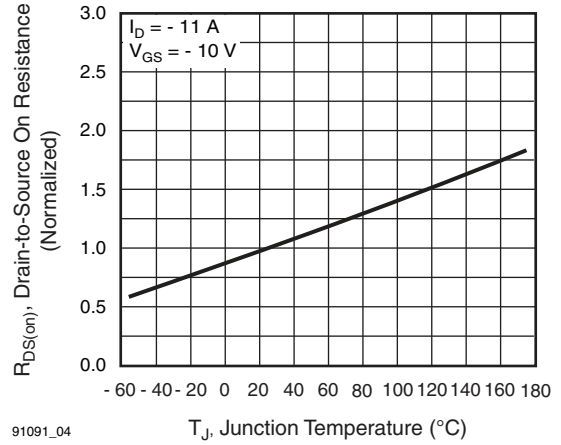


Fig. 4 - Normalized On-Resistance vs. Temperature

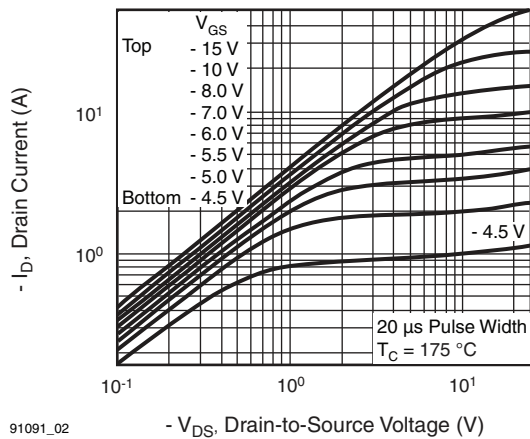


Fig. 2 - Typical Output Characteristics

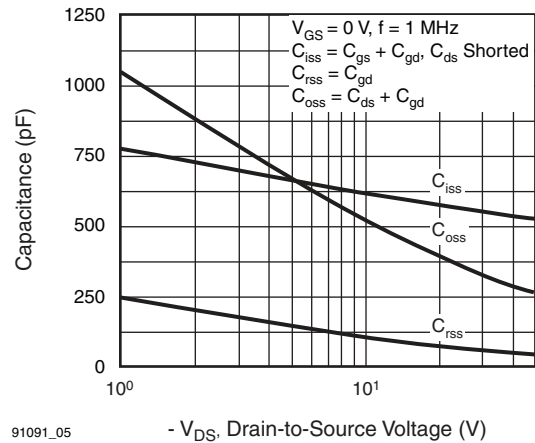


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

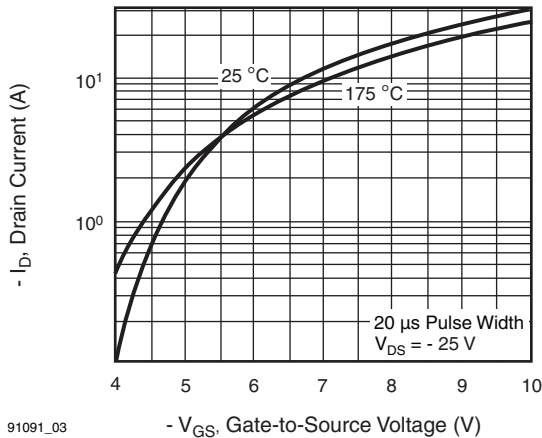


Fig. 3 - Typical Transfer Characteristics

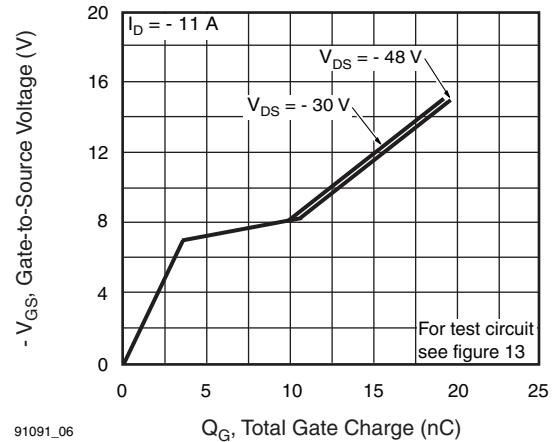


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

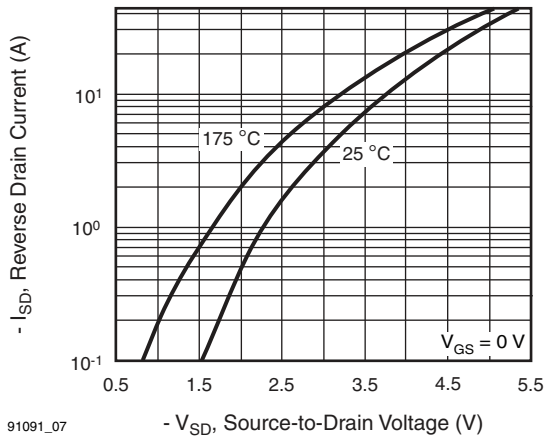


Fig. 7 - Typical Source-Drain Diode Forward Voltage

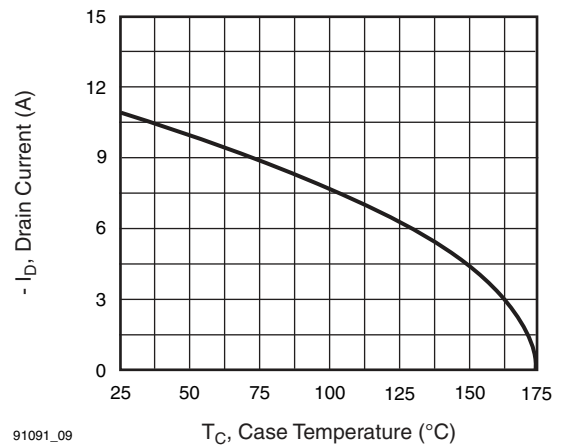


Fig. 9 - Maximum Drain Current vs. Case Temperature

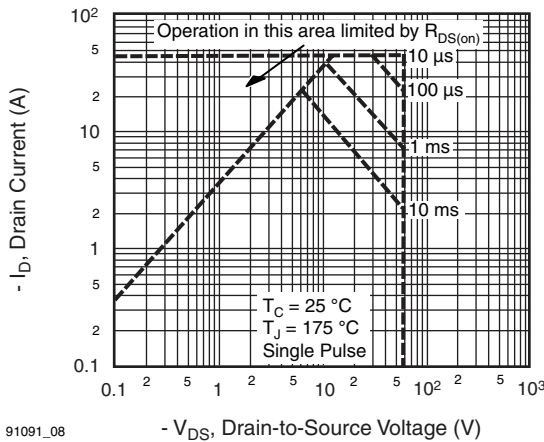


Fig. 8 - Maximum Safe Operating Area

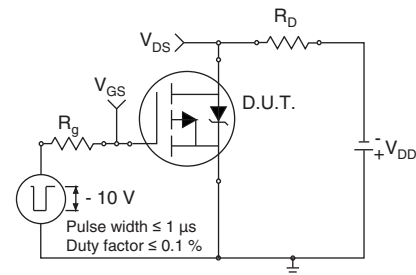


Fig. 10a - Switching Time Test Circuit

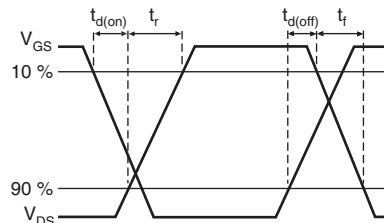


Fig. 10b - Switching Time Waveforms

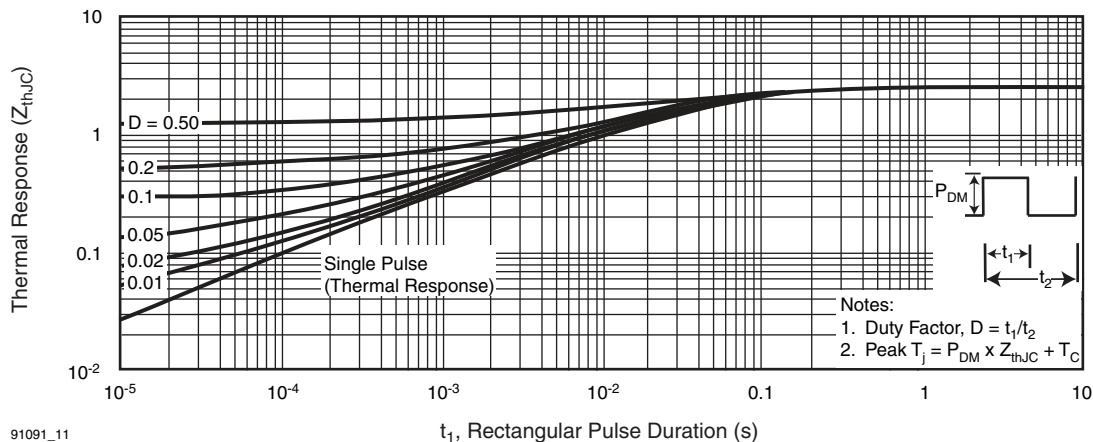


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

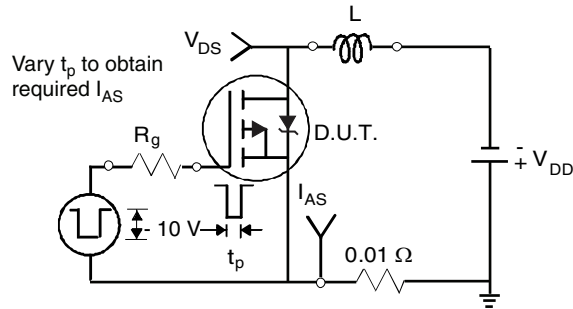


Fig. 12a - Unclamped Inductive Test Circuit

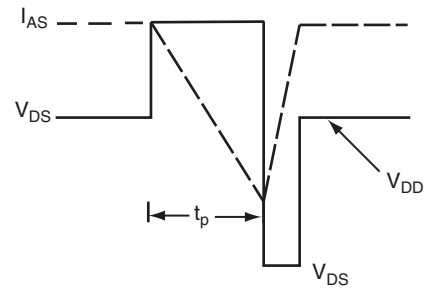


Fig. 12b - Unclamped Inductive Waveforms

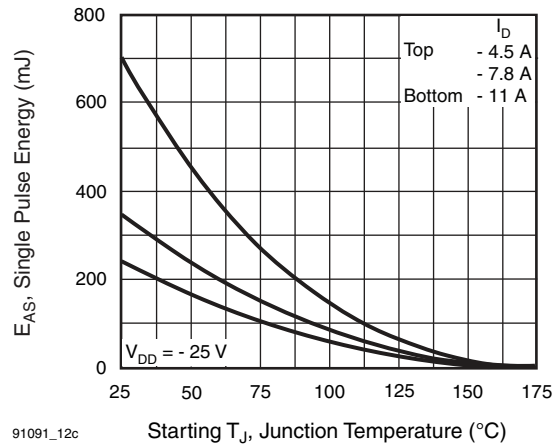


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

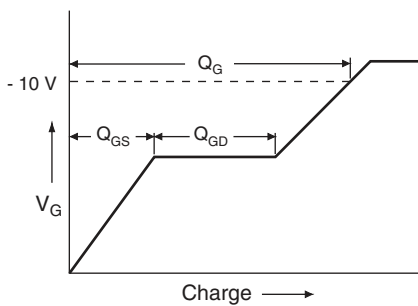


Fig. 13a - Basic Gate Charge Waveform

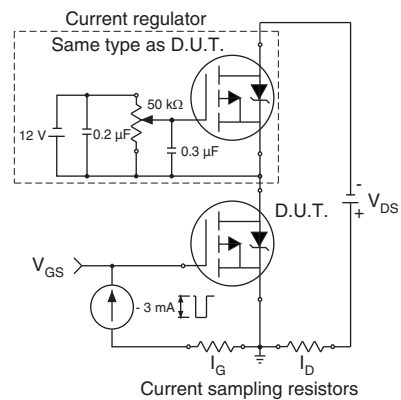


Fig. 13b - Gate Charge Test Circuit

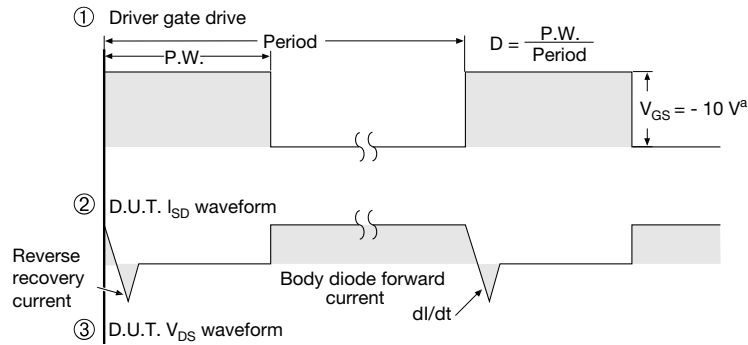
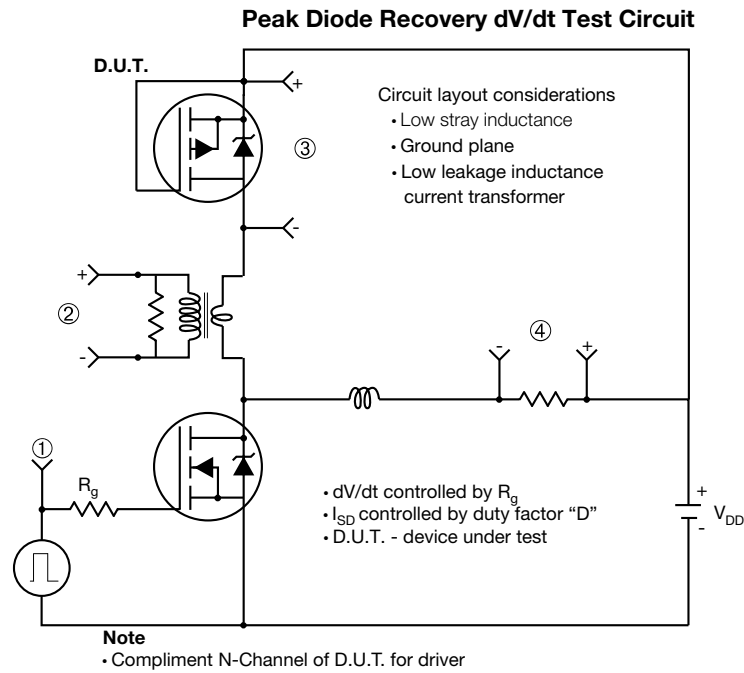


Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91091.

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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