

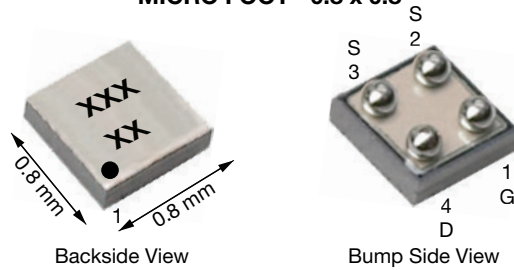


**THE DATASHEET OF
SI8809EDB-T2-E1**



P-Channel 20 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---------------------|-----------------------------------|---------------------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) ^a | Q _g (TYP.) |
| -20 | 0.090 at V _{GS} = -4.5 V | -2.6 | 6 nC |
| | 0.119 at V _{GS} = -2.5 V | -2.3 | |
| | 0.155 at V _{GS} = -1.8 V | -2 | |

MICRO FOOT® 0.8 x 0.8


Marking Code: xx = AE
 xxx = Date/Lot traceability code

Ordering Information:
 Si8809EDB-T2-E1 (lead (Pb)-free and halogen-free)

FEATURES

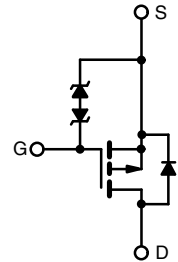
- TrenchFET® power MOSFET
- Ultra small 0.8 mm x 0.8 mm outline
- Ultra thin 0.357 mm height
- Typical ESD protection 1000 V HBM
- High speed switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- Portable devices such as cell phones, smart phones, tablet PCs and media players
- Load switch
- Battery switch



P-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|-------------------|------|--|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V _{DS} | -20 | V | |
| Gate-Source Voltage | V _{GS} | ± 8 | | |
| Continuous Drain Current (T _J = 150 °C) | T _A = 25 °C | -2.6 ^a | A | |
| | T _A = 70 °C | -2.1 ^a | | |
| | T _A = 25 °C | -1.9 ^b | | |
| | T _A = 70 °C | -1.5 ^b | | |
| Pulsed Drain Current (t = 300 μs) | I _{DM} | -13 | | |
| Continuous Source-Drain Diode Current | T _A = 25 °C | -0.7 ^a | A | |
| | T _A = 25 °C | -0.4 ^b | | |
| Maximum Power Dissipation | T _A = 25 °C | 0.9 ^a | W | |
| | T _A = 70 °C | 0.6 ^a | | |
| | T _A = 25 °C | 0.5 ^b | | |
| | T _A = 70 °C | 0.3 ^b | | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | -55 to +150 | °C | |
| Soldering Recommendations (Peak Temperature) ^c | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | |
|---|-------------------|---------|---------|------|
| PARAMETER | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum Junction-to-Ambient ^{a, d} | R _{thJA} | 105 | 135 | °C/W |
| Maximum Junction-to-Ambient ^{b, e} | | 200 | 260 | |

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- Maximum under steady state conditions is 185 °C/W.
- Maximum under steady state conditions is 330 °C/W.



| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|--------------------------------------|---|------|-------|-------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0, I _D = -250 μA | -20 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | I _D = -250 μA | - | -9 | - | mV/°C |
| V _{GS(th)} Temperature Coefficient | ΔV _{GS(th)} /T _J | | - | 2.1 | - | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = -250 μA | -0.4 | - | -0.9 | V |
| Gate-Source Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 4.5 V | - | - | ± 1 | μA |
| | | V _{DS} = 0 V, V _{GS} = ± 8 V | - | - | ± 10 | |
| Zero Gate Voltage Drain Current | I _{DSS} | V = -20 V, V _{GS} = 0 V | - | - | -1 | |
| | | V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C | - | - | -10 | |
| On-State Drain Current ^a | I _{D(on)} | V ≤ -10 V, V _{GS} = -4.5 V | -5 | - | - | A |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = -4.5 V, I _D = -1.5 A | - | 0.075 | 0.090 | Ω |
| | | V _{GS} = -2.5 V, I _D = -1.5 A | - | 0.097 | 0.119 | |
| | | V _{GS} = -1.8 V, I _D = -0.5 A | - | 0.125 | 0.155 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = -10 V, I _D = -1.5 A | - | 8 | - | S |
| Dynamic ^b | | | | | | |
| Total Gate Charge | Q _g | V _{DS} = -10 V, V _{GS} = -8 V, I _D = -1.5 A | - | 9.8 | 15 | nC |
| | | | - | 6 | 10 | |
| Gate-Source Charge | Q _{gs} | V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -1.5 A | - | 0.8 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 1.85 | - | |
| Gate Resistance | R _g | f = 1 MHz | - | 10 | - | Ω |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = -10 V, R _L = 3.7 Ω I _D ≅ -1.5 A, V _{GEN} = -4.5 V, R _g = 1 Ω | - | 15 | 30 | ns |
| Rise Time | t _r | | - | 20 | 40 | |
| Turn-Off Delay Time | t _{d(off)} | | - | 30 | 60 | |
| Fall Time | t _f | | - | 10 | 20 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = -10 V, R _L = 3.7 Ω I _D ≅ -1.5 A, V _{GEN} = -8 V, R _g = 1 Ω | - | 10 | 20 | |
| Rise Time | t _r | | - | 10 | 20 | |
| Turn-Off Delay Time | t _{d(off)} | | - | 25 | 50 | |
| Fall Time | t _f | | - | 7 | 15 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | - | - | -0.7 | A |
| Pulse Diode Forward Current | I _{SM} | | - | - | -13 | |
| Body Diode Voltage | V _{SD} | I _S = -1.5 A, V _{GS} = 0 | - | -0.8 | -1.2 | V |
| Body Diode Reverse Recovery Time | t _{rr} | I _F = -1.5 A, di/dt = 100 A/μs, T _J = 25 °C | - | 20 | 40 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | - | 10 | 20 | nC |
| Reverse Recovery Fall Time | t _a | | - | 15 | - | ns |
| Reverse Recovery Rise Time | t _b | | - | 5 | - | |

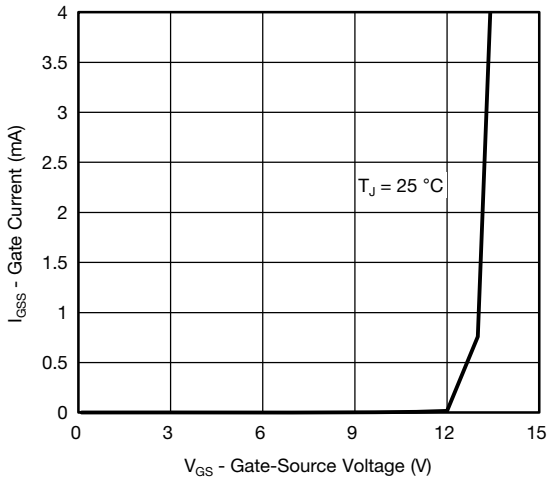
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

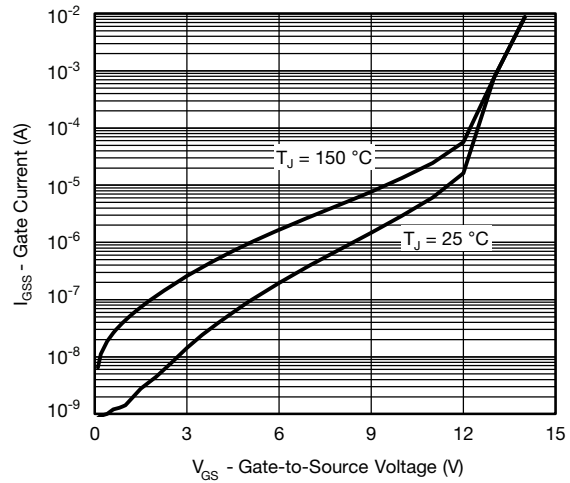
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



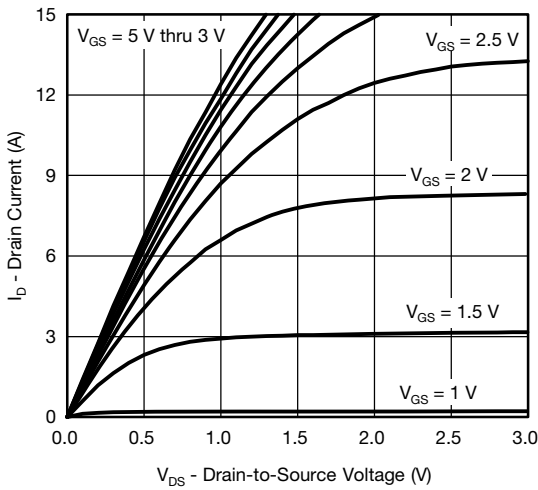
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



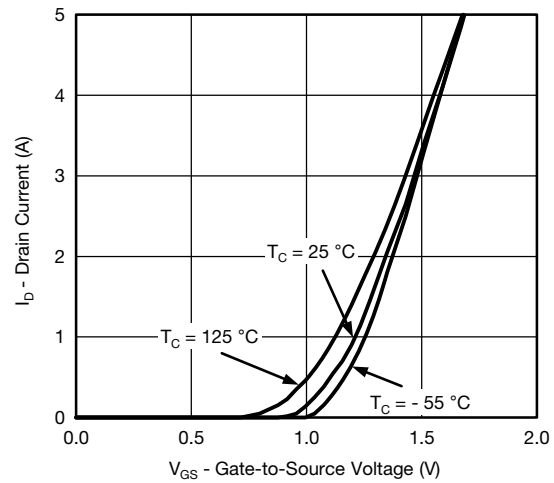
Gate Current vs. Gate-Source Voltage



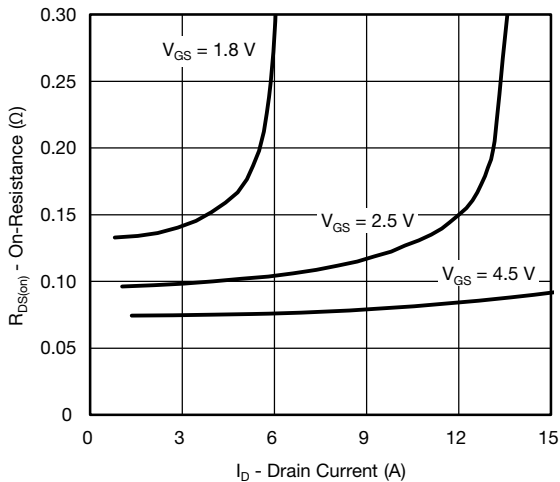
Gate Current vs. Gate-Source Voltage



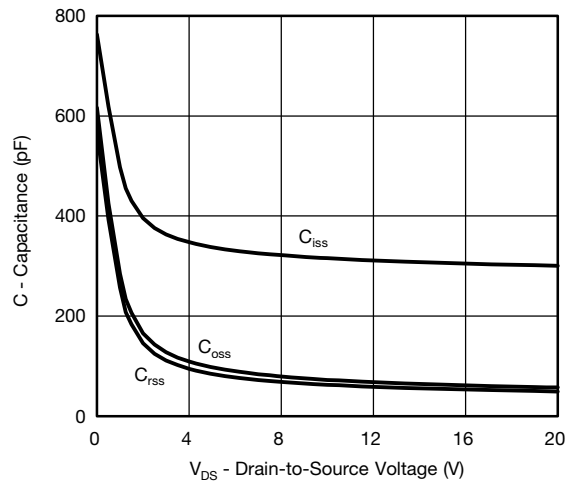
Output Characteristics



Transfer Characteristics

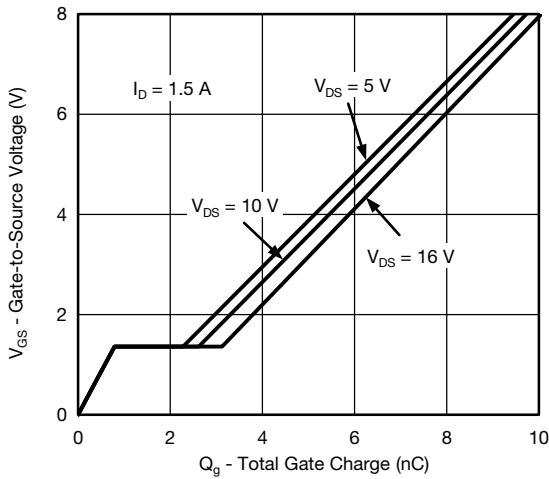


On-Resistance vs. Drain Current

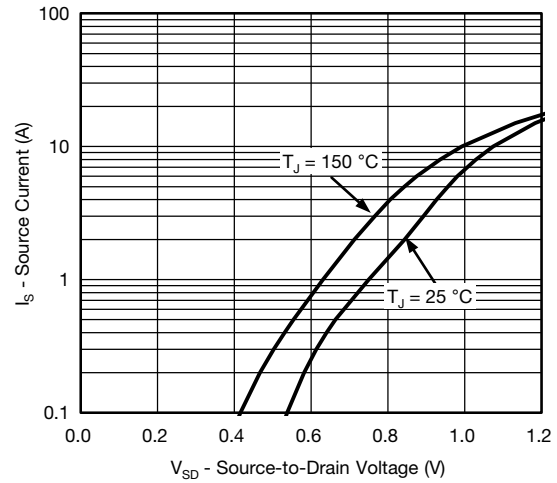


Capacitance

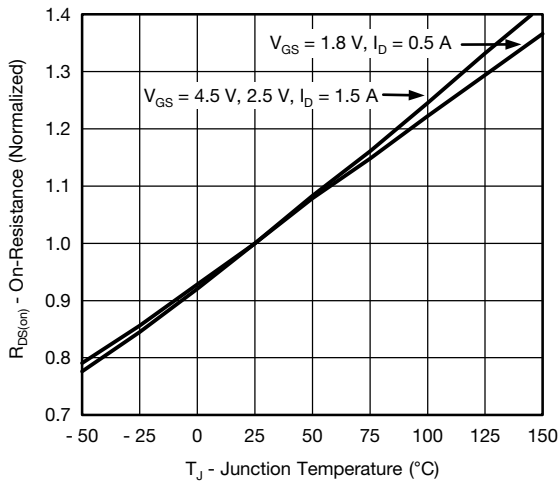
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



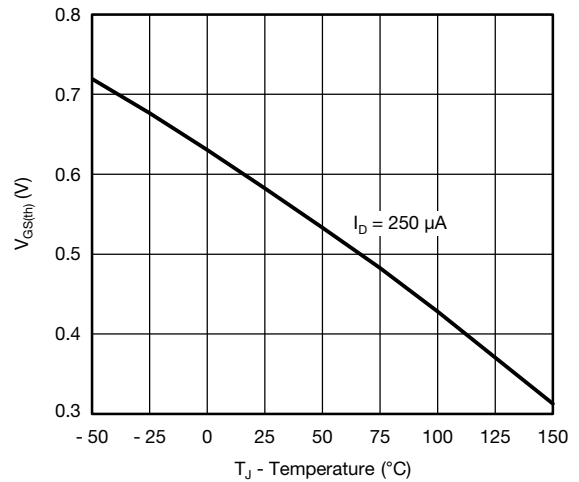
Gate Charge



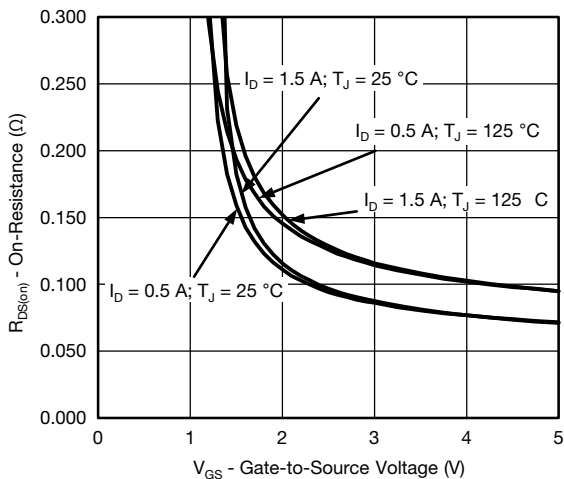
Source-Drain Diode Forward Voltage



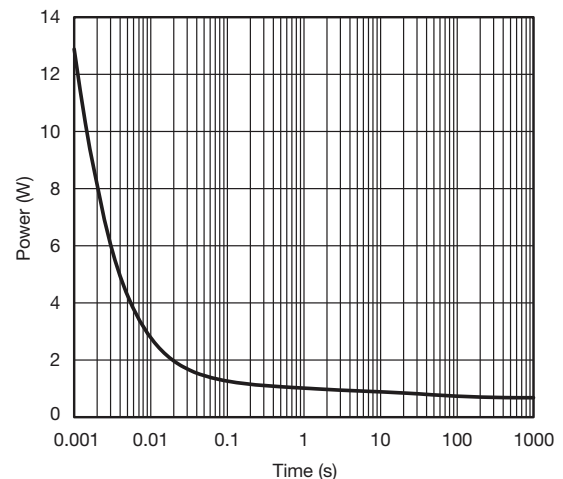
On-Resistance vs. Junction Temperature



Threshold Voltage

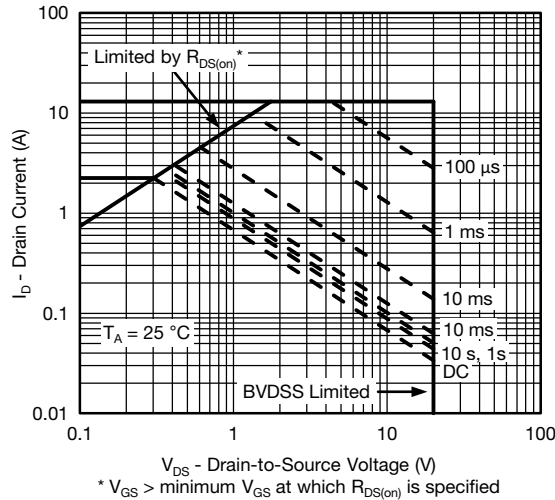


On-Resistance vs. Gate-to-Source Voltage

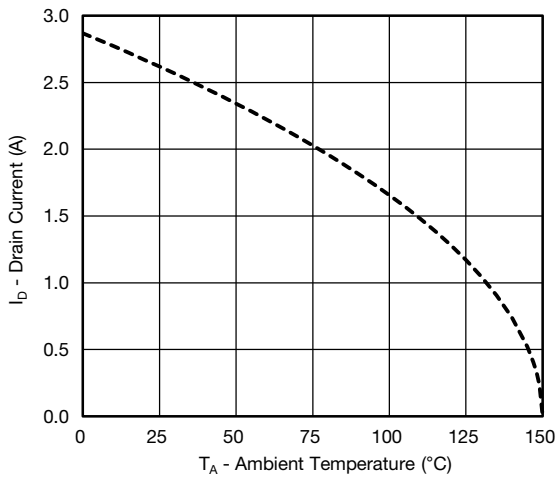


Single Pulse Power (Junction-to-Ambient)

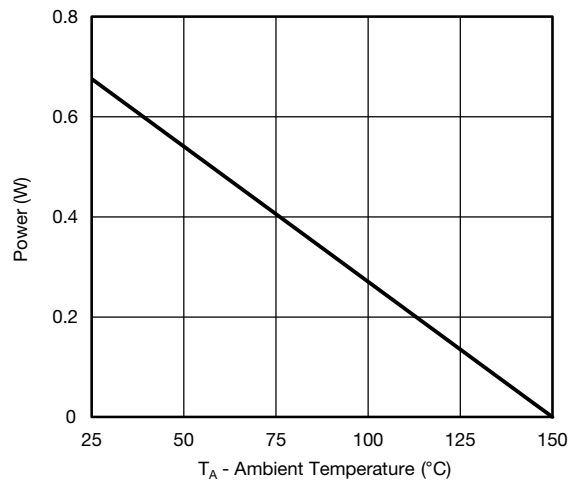
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating*



Power Derating

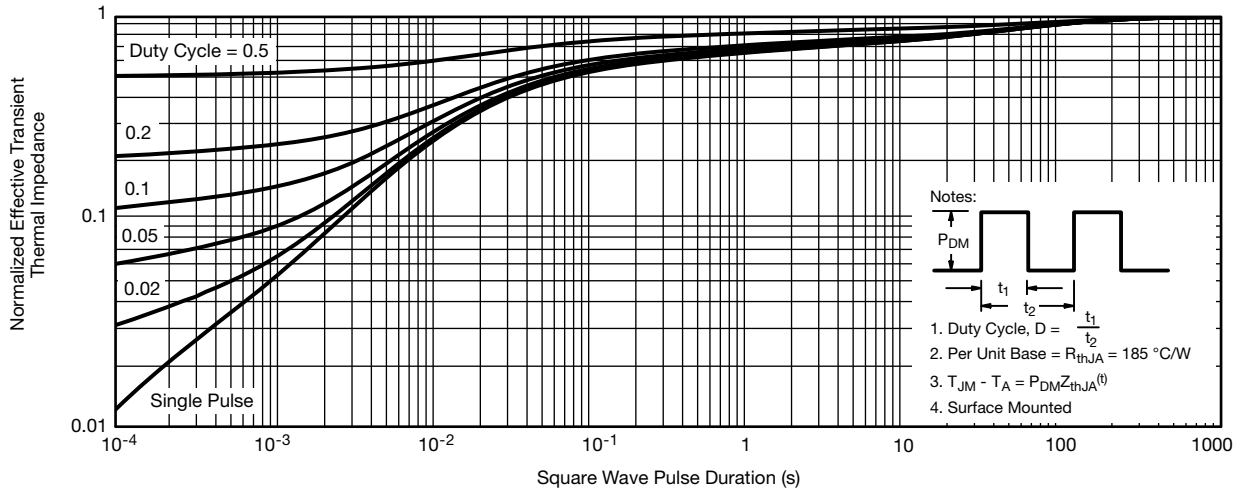
Note

When mounted on 1" x 1" FR4 with full copper.

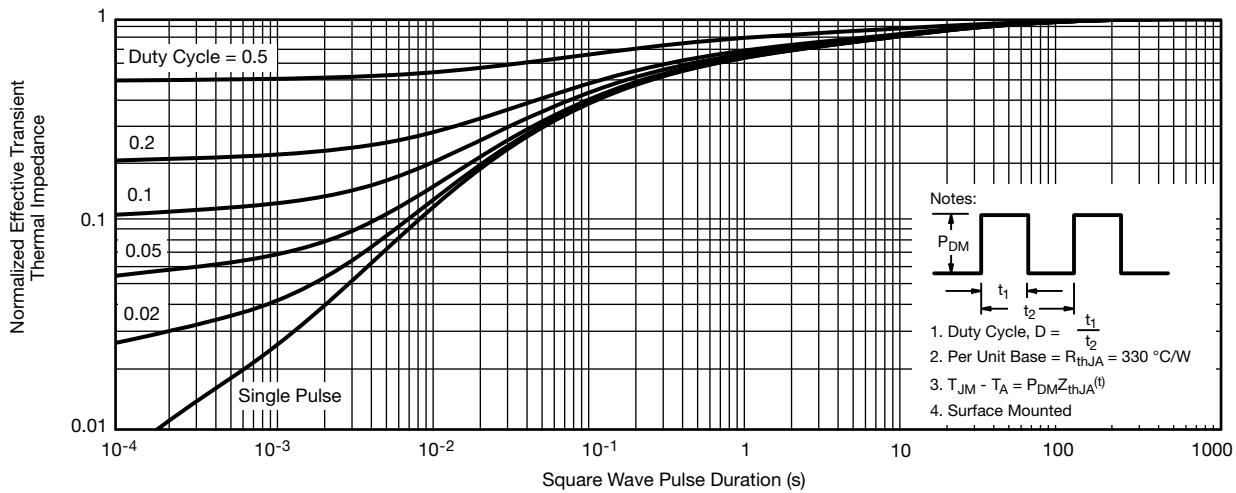
* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^\circ\text{C}$, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



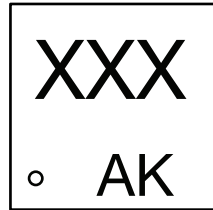
Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Maximum Copper)



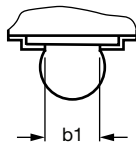
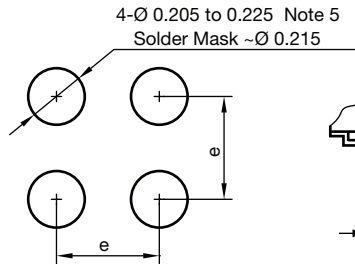
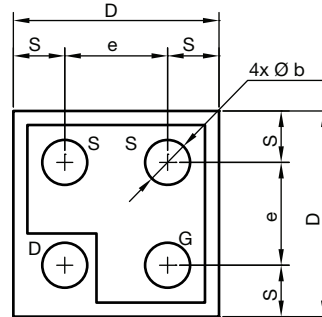
Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Minimum Copper)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63301.

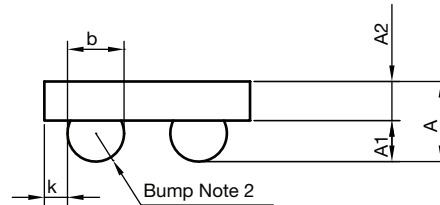
MICRO FOOT®: 4-Bump (0.8 mm x 0.8 mm, 0.4 mm Pitch)



Mark on Backside of die



Note 4



Notes

- (1) Laser mark on the backside surface of die
- (2) Bumps are 95.5 % Sn,3.8 % Ag,0.7 % Cu
- (3) "i" is the location of pin 1
- (4) "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- (5) Non-solder mask defined copper landing pad.

| DIM. | MILLIMETERS ^a | | | INCHES | | |
|------|--------------------------|-------|-------|--------|--------|--------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.328 | 0.365 | 0.402 | 0.0129 | 0.0144 | 0.0158 |
| A1 | 0.136 | 0.160 | 0.184 | 0.0053 | 0.0062 | 0.0072 |
| A2 | 0.192 | 0.205 | 0.218 | 0.0076 | 0.0081 | 0.0086 |
| b | 0.200 | 0.220 | 0.240 | 0.0078 | 0.0086 | 0.0094 |
| b1 | 0.175 | | | 0.0068 | | |
| e | 0.400 | | | 0.0157 | | |
| S | 0.160 | 0.180 | 0.200 | 0.0062 | 0.0070 | 0.0078 |
| D | 0.720 | 0.760 | 0.800 | 0.0283 | 0.0299 | 0.0314 |
| K | 0.040 | 0.070 | 0.100 | 0.0015 | 0.0027 | 0.0039 |

Note

a. Use millimeters as the primary measurement.

ECN: T15-0053-Rev. A, 16-Feb-15
DWG: 6033



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