



THE DATASHEET OF GWS4621L



GWS4621L

Dual 20V N-Channel Power MOSFET

FN8784
Rev.2.00
Jun 20, 2017

The GWS4621L is a dual 20V, 8.8mΩ, N-channel power MOSFET used for Li-ion battery protection. It is offered in a 1.85mmx1.85mm LGA with a very low thickness profile, 0.29mm typical thickness. It has extremely high power density, reducing the board size of the Li-ion battery power system. Designed for handheld devices with a high level of ESD protection.

PRODUCT SUMMARY			
$V_{(BR)SSS}$	$I_D = 250\mu A$	20V	Minimum
$r_{DS(ON)}$	$V_{GS} = 4.5V$	8.8mΩ	Typical

Features

- Monolithic dual MOSFET
- Low $r_{DS(ON)}$ in a small footprint
- Ultra low gate charge and figure of merit
- LGA chip scale package
- Low thermal resistance

Applications

- Li-ion battery protection
- Portable devices, cell phones, PDA
- Rated for short-circuit and overcurrent protection
- Integrated G-S diodes provide ESD protection of 2.5kV HBM

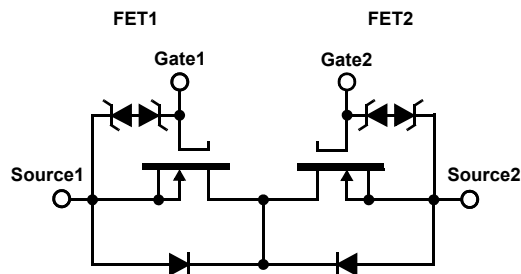


FIGURE 1. EQUIVALENT CIRCUIT

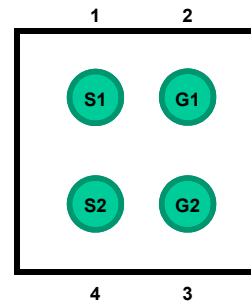
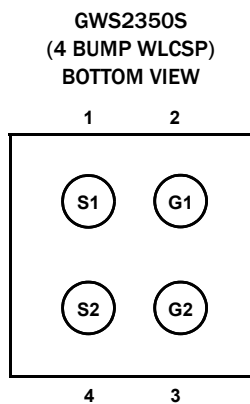


FIGURE 2. PAD VIEW, 1.815mm x 1.815mm

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
GWS4621L	21	-55 to +150	4 BUMP WLCSP

Pin Configuration



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	S1	Source of FET1
2	G1	Gate of FET1
3	G2	Gate of FET2
4	S2	Source of FET2

Absolute Maximum Ratings (Note 1)

Source-to-Source Voltage (V_{DS})	-20V
Gate-to-Source Voltage (V_{GS})	$\pm 8V$
Source Current (I_S) (Note 2)	
$T_A = +25^\circ C$	10.1A (10s), 6.5A (Steady State)
$T_A = +70^\circ C$	8.1A (10s), 5.2A (Steady State)
Source Current (RthjFoot) $T_F = +25^\circ C$	1.5A (Steady State)
Pulsed Source Current (I_{SM})	60A
ESD Rating	
Human Body Model	2.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^\circ C/W$)	θ_{JF} ($^\circ C/W$)
$t \leq 10s$	35	
Steady State	85	16
Maximum Power Dissipation (P_D) (Note 2)		
$T_A = +25^\circ C$	3.6W (10s) 1.47W (Steady State)	
$T_A = +70^\circ C$	2.29W (10s) 0.94W (Steady State)	
Junction and Storage Temperature Range (T_J, T_{stg})	-55 $^\circ C$ to +150 $^\circ C$	
Pb-Free Reflow Profile	see TB493	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. $T_J = +25^\circ C$ unless otherwise noted.
2. Surface mounted on FR4 board.

Electrical Characteristics $T_J = +25^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP (Note 4)	MAX (Note 3)	UNIT	
STATIC							
$V_{(BR)SSS}$	Source-to-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20			V	
I_{SSS}	Zero Gate Voltage Source Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA	
I_{GSS}	Gate Body Leakage	$V_{DS} = 0V, V_{GS} = \pm 6V$			± 10	μA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1mA$	0.5	0.8	1.5	V	
$r_{DS(ON)}$	Drain-to-Source On-State Resistance (Note 5)	$V_{GS} = 4.5V, I_D = 3A$	6.0	8.8	9.8	m Ω	
		$V_{GS} = 4.0V, I_D = 3A$	7.0	9.0	10.3	m Ω	
		$V_{GS} = 3.1V, I_D = 3A$	8.0	10.0	12.0	m Ω	
		$V_{GS} = 2.5V, I_D = 3A$	9.0	11.5	13.5	m Ω	
$r_{SS(ON)}$	Source-to-Source On-State Resistance (Note 5)	$V_{GS} = 4.5V, I_S = 3A$	$T_J = +25^\circ C$	12.0	17.5	19.5	m Ω
			$T_J = +50^\circ C$	12.0	21.0	23.0	m Ω
		$V_{GS} = 4.0V, I_S = 3A$	$T_J = +25^\circ C$	14.0	18.0	20.5	m Ω
			$T_J = +50^\circ C$	14.0	22.0	24.0	m Ω
		$V_{GS} = 3.1V, I_S = 3A$	$T_J = +25^\circ C$	16.0	20.0	24.0	m Ω
			$T_J = +50^\circ C$	16.0	23.0	27.0	m Ω
V_{SS}	Source-to-Source Diode Voltage	$V_{GS} = 0, I_S = 6.5A$	$T_J = +25^\circ C$	0.8	1.0	V	
			$T_J = +50^\circ C$				
DYNAMIC							
Q_g	Total Gate Charge	$V_{SS} = 10V, I_S = 5.0A, V_{GS} = 4.0V$		11		nC	
C_{iss}	Input Capacitance	$V_{SS} = 10V, V_{GS} = 0V, f = 1MHz$		1125		pF	
C_{oss}	Output Capacitance			375		pF	
C_{rss}	Reverse Transfer Capacitance			188		pF	

NOTES:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
4. Typical values are for $T_A = +25^\circ C$.
5. Good Kelvin measurement required.

Test Circuit Examples for Measuring FET1 Key Parameters

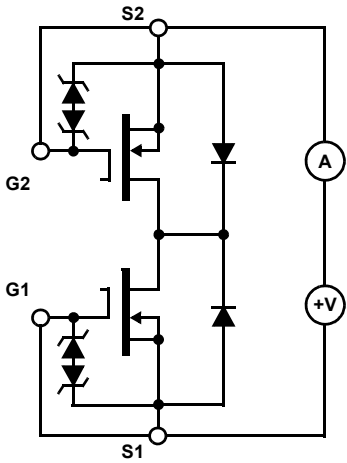


FIGURE 3. I_{SSS} TEST CIRCUIT

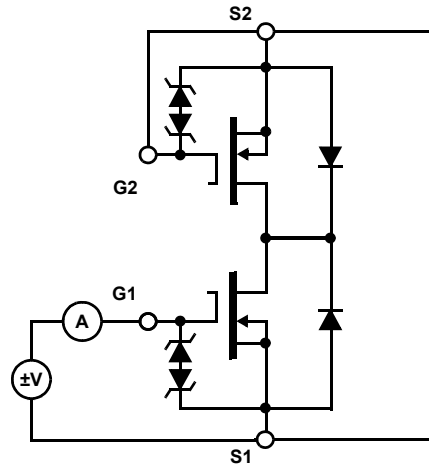


FIGURE 4. I_{GSS} TEST CIRCUIT

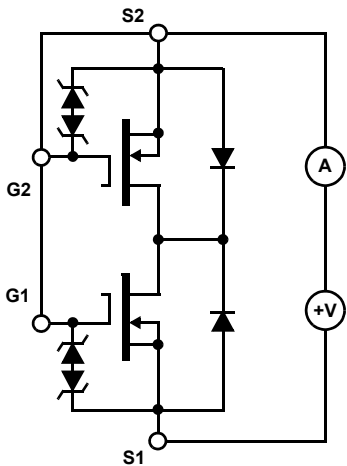


FIGURE 5. $V_{GS(th)}$ TEST CIRCUIT

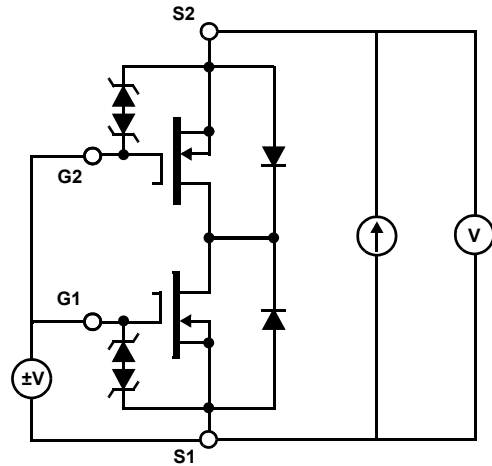


FIGURE 6. $r_{SS(ON)}$ TEST CIRCUIT

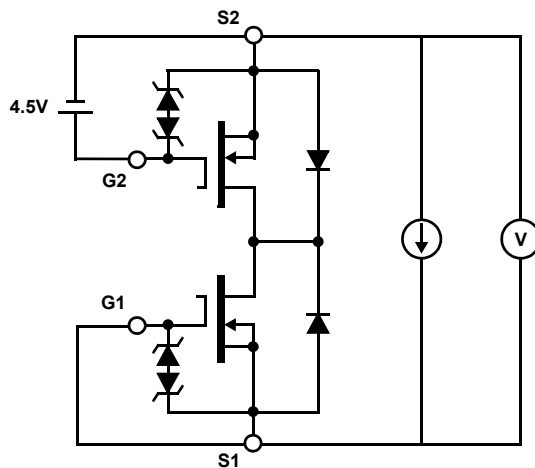


FIGURE 7. V_{FS-S} TEST CIRCUIT

Typical Performance Curves

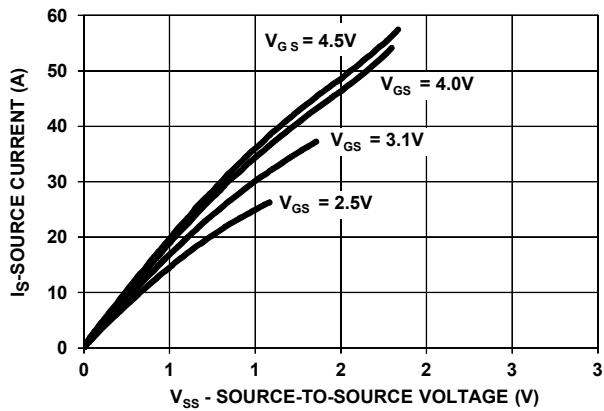


FIGURE 8. OUTPUT CHARACTERISTICS

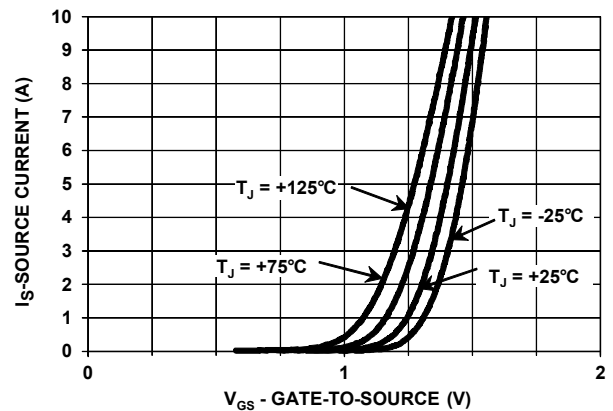


FIGURE 9. TRANSFER CHARACTERISTICS

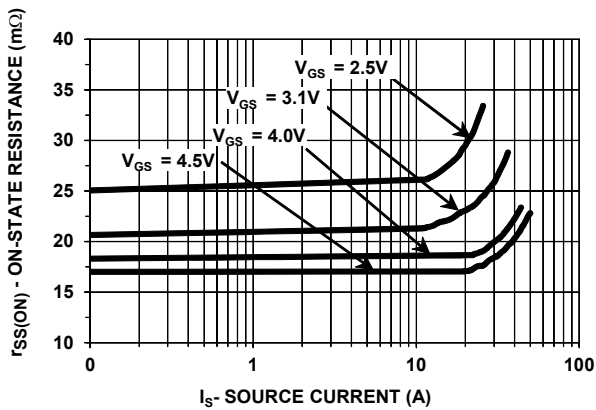


FIGURE 10. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs SOURCE CURRENT

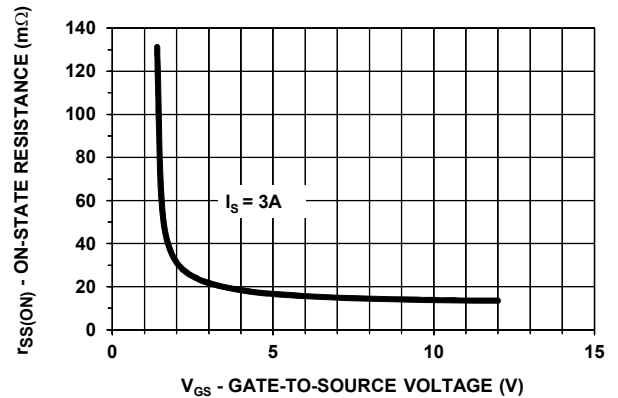


FIGURE 11. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

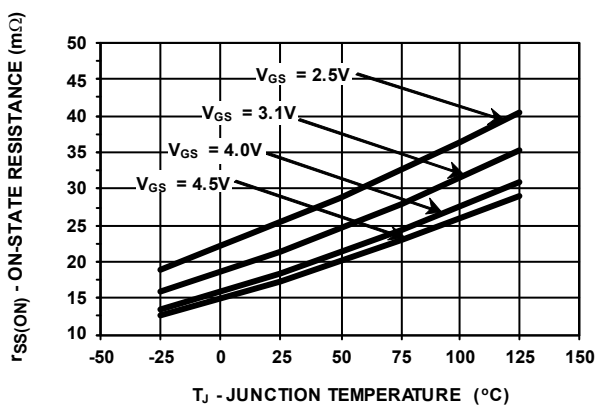


FIGURE 12. SOURCE-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

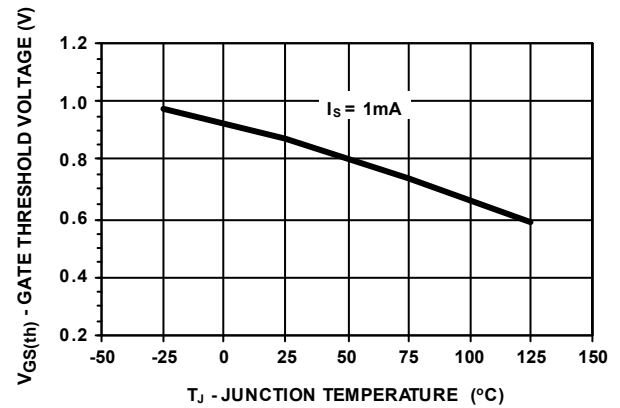


FIGURE 13. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

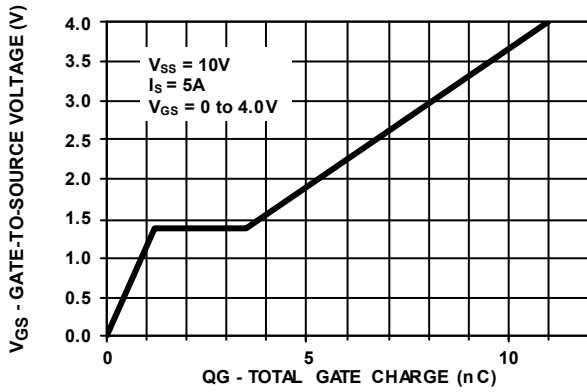


FIGURE 14. GATE CHARGE

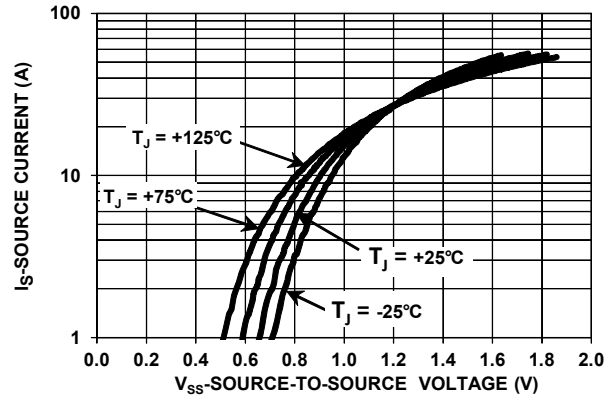


FIGURE 15. SOURCE-TO-SOURCE DIODE FORWARD VOLTAGE

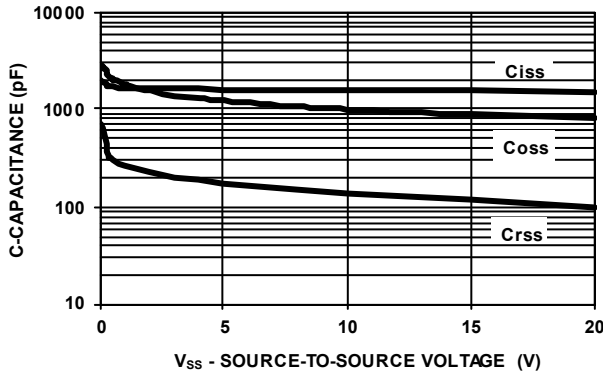


FIGURE 16. CAPACITANCE

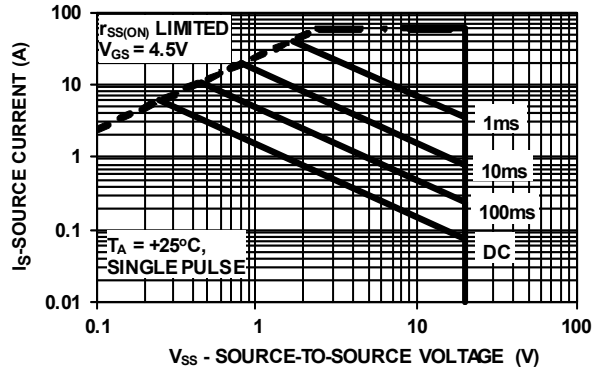


FIGURE 17. MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

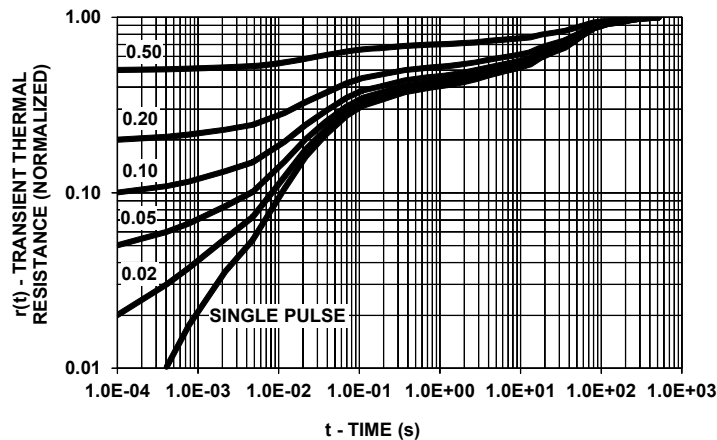


FIGURE 18. TRANSIENT THERMAL RESPONSE, JUNCTION-TO-AMBIENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jun 20, 2017	FN8784.2	Applied new header/footer. Updated About Intersil section.
Dec 21, 2015	FN8784.1	Added "Note 1. $T_J = +25^\circ\text{C}$ unless otherwise noted." to Abs Max on page 3.
Oct 30, 2015	FN8784.0	Initial release

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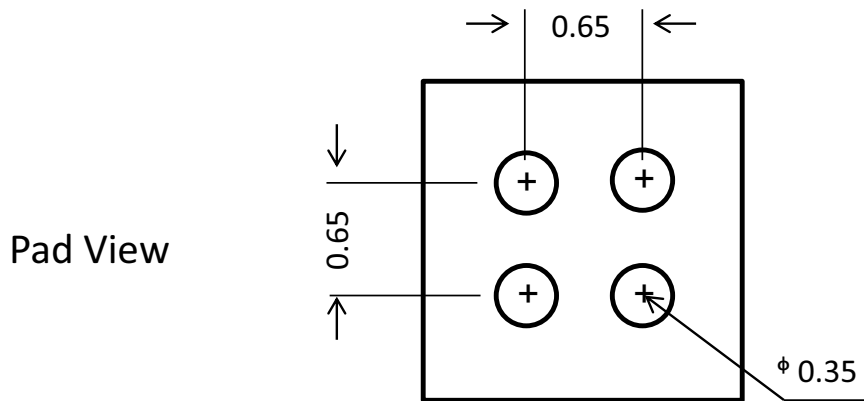
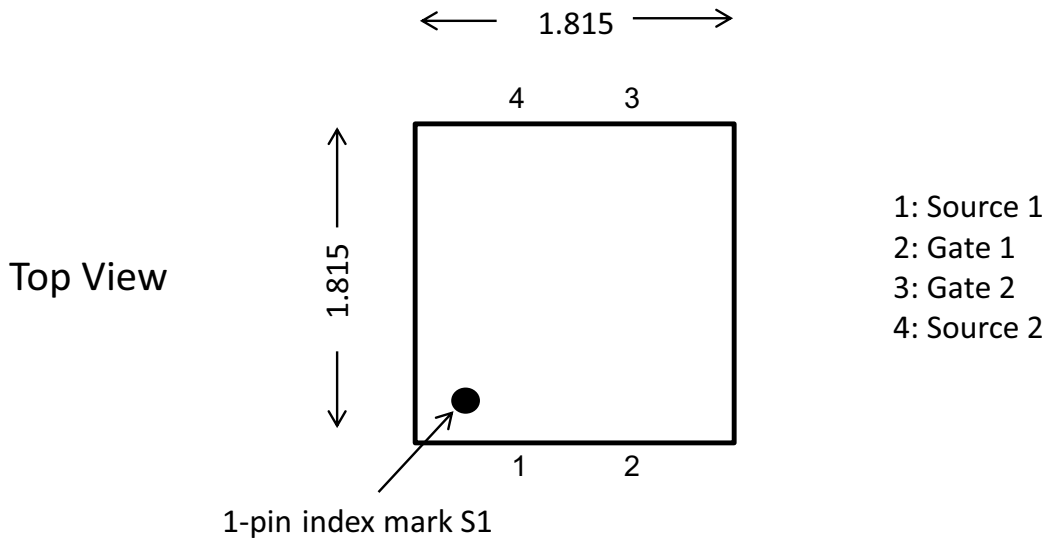
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Outline Drawing (Unit: mm)



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