

BUK95/9609-55A

TrenchMOS™ logic level FET

Rev. 01 — 21 February 2002

Product data

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9509-55A in SOT78 (TO-220AB)

BUK9609-55A in SOT404 (D²-PAK).

2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

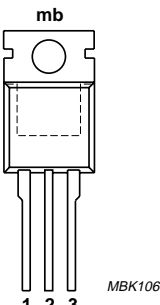
3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V and 24 V loads
 - ◆ Motors, lamps and solenoids.

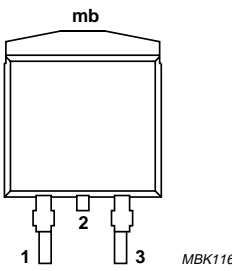
4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

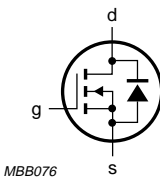
Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) ^[1]		
3	source (s)		
mb	mounting base; connected to drain (d)		



SOT78 (TO-220AB)



SOT404 (D²-PAK)



Symbol

[1] It is not possible to make connection to pin 2 of the SOT404 package.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	108	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	211	W
T_j	junction temperature		-	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 5\text{ V}; I_D = 25\text{ A}$	7.6	9	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	-	10	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	6.4	8	mΩ

6. Limiting values

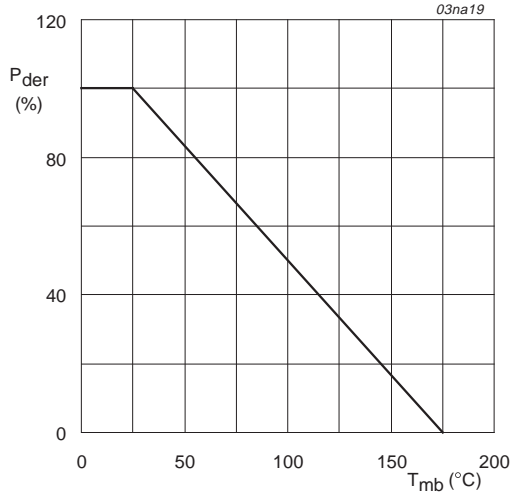
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	±15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	[1] -	108	A
			[2] -	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	433	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	211	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	[1] -	108	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	433	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_{mb} = 25\text{ °C}$	-	400	mJ

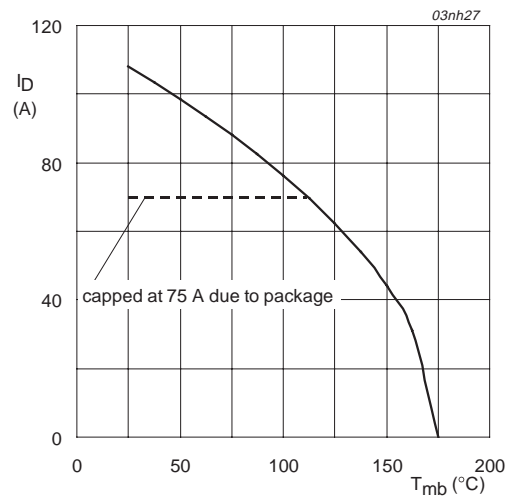
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



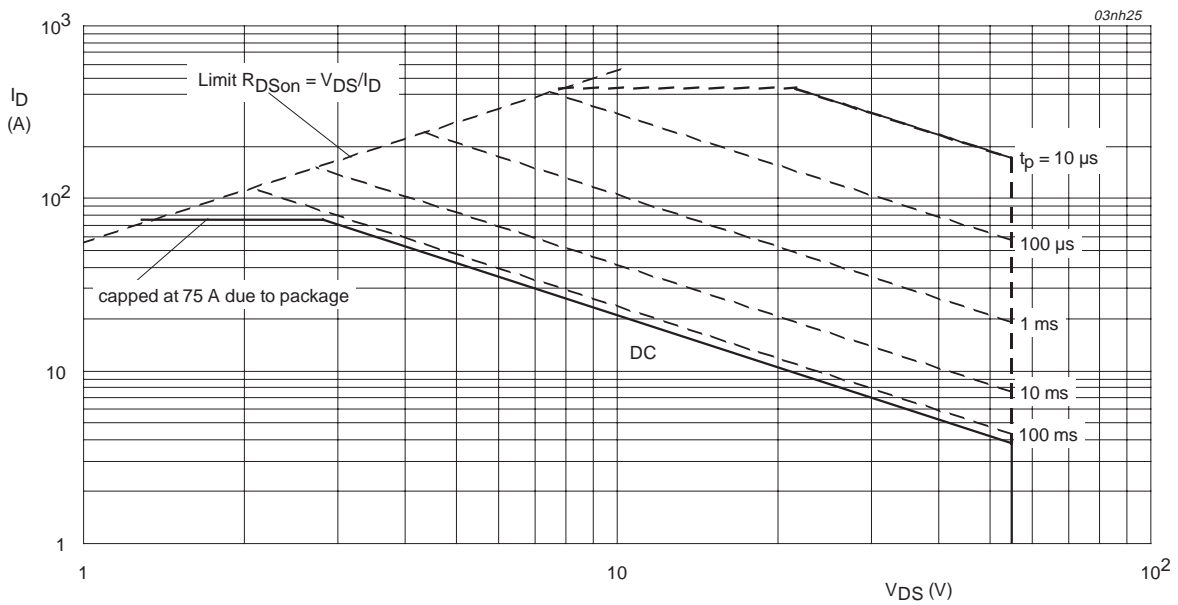
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 4.5$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.71	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	-	60	-	K/W
		mounted on a printed circuit board; minimum footprint; SOT404 package	-	50	-	K/W

7.1 Transient thermal impedance

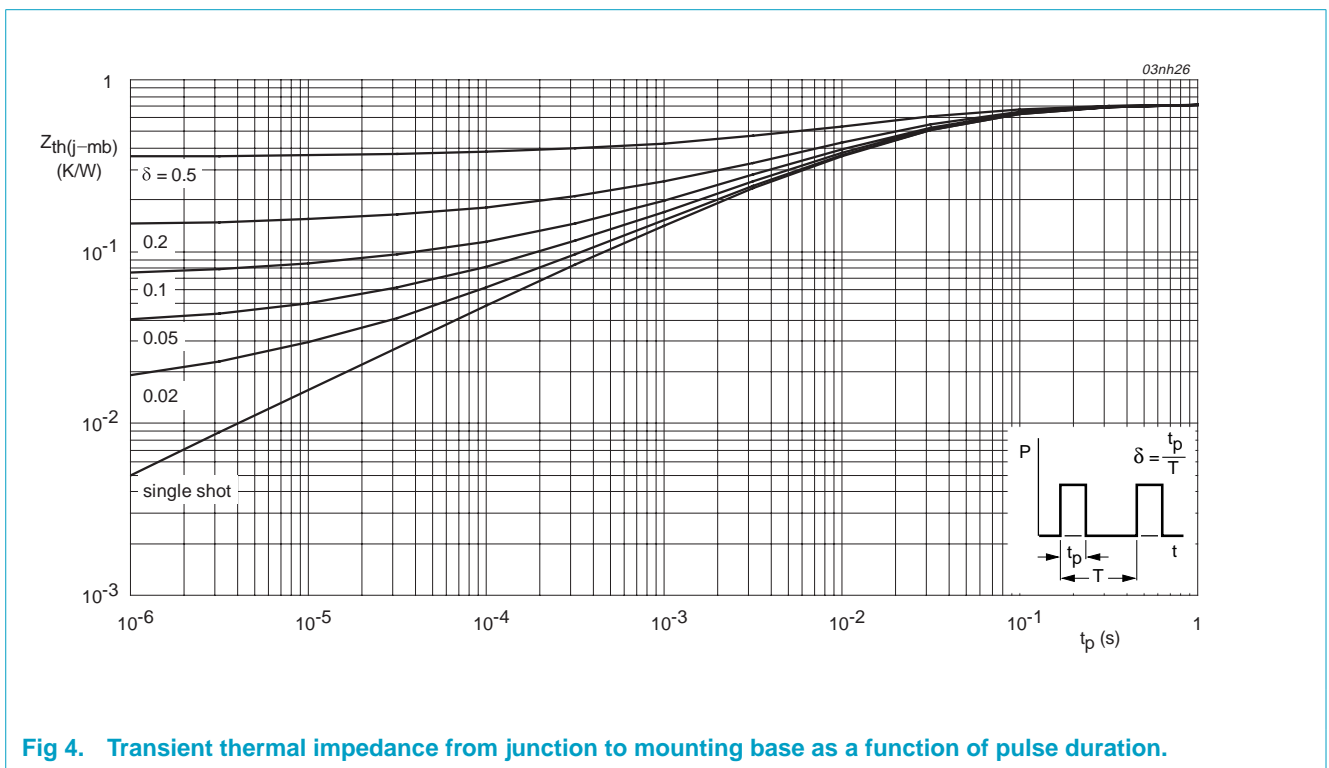


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

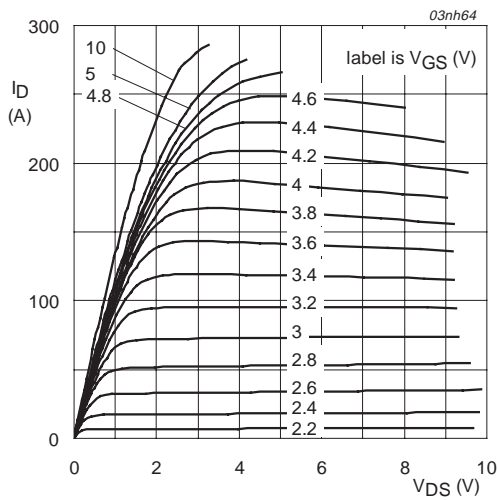
Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	7.6	9	m Ω
		$T_j = 175\text{ °C}$	-	-	18	m Ω
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	-	-	10	m Ω
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	-	6.4	8	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; V_{DD} = 44\text{ V};$ $I_D = 25\text{ A};$ Figure 14	-	60	-	nC
Q_{gs}	gate-to-source charge		-	9	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	29	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ Figure 12	-	3475	4633	pF
C_{oss}	output capacitance		-	570	682	pF
C_{riss}	reverse transfer capacitance		-	360	493	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$ $V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega$	-	33	-	ns
t_r	rise time		-	149	-	ns
$t_{d(off)}$	turn-off delay time		-	197	-	ns
t_f	fall time		-	131	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
		from contact screw on mounting base to centre of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to centre of die SOT404	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

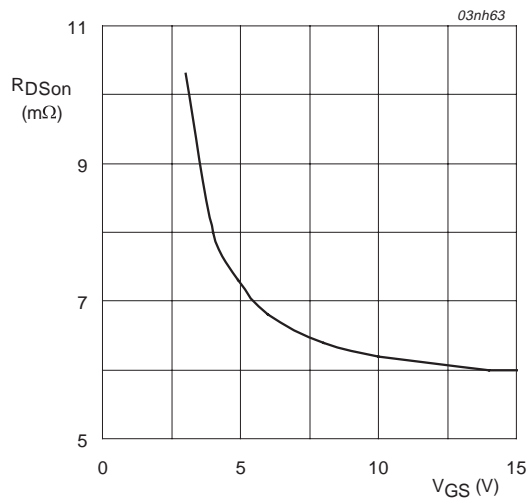
Table 5: Characteristics...continued
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$	-	70	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 25\text{ V}$	-	160	-	nC



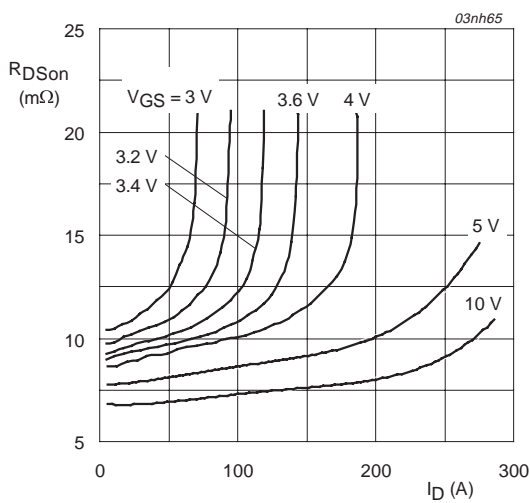
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



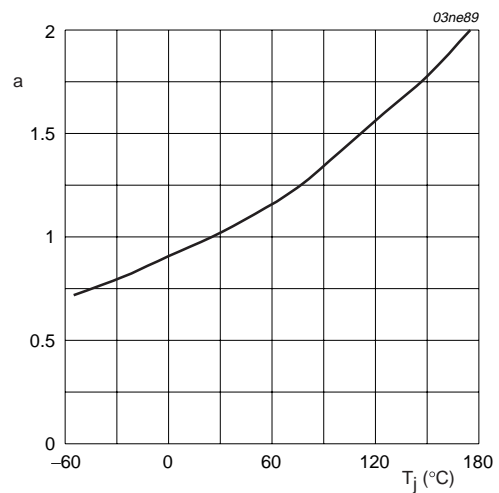
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



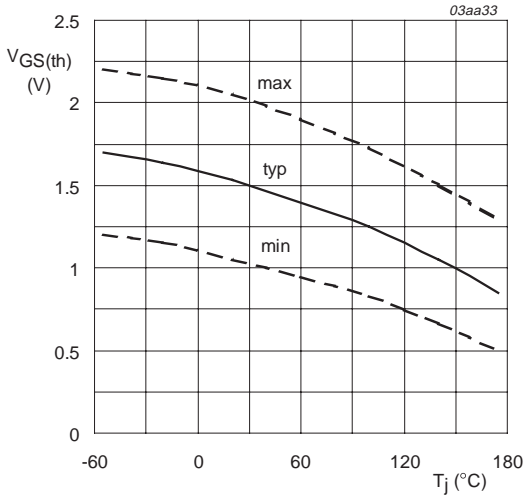
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



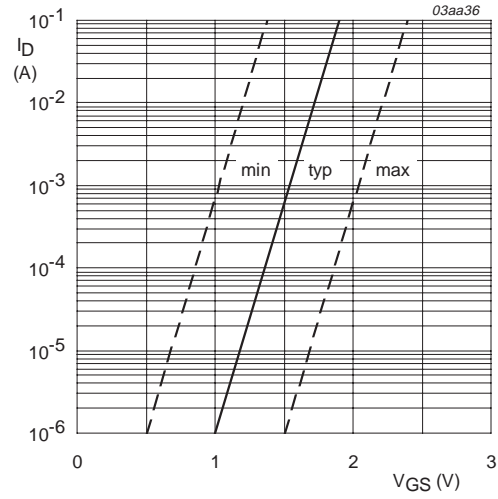
$a = R_{DSon}/R_{DSon}(25\text{ }^\circ\text{C})$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



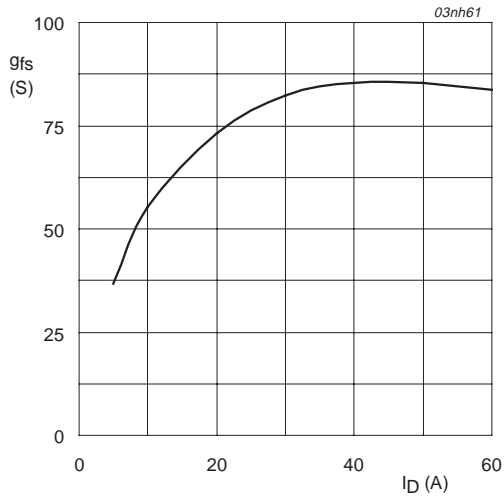
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



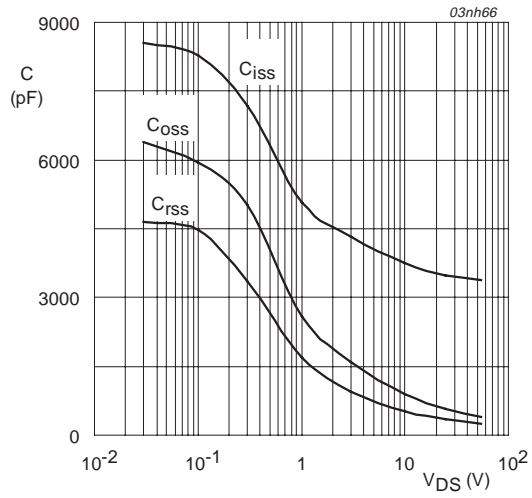
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



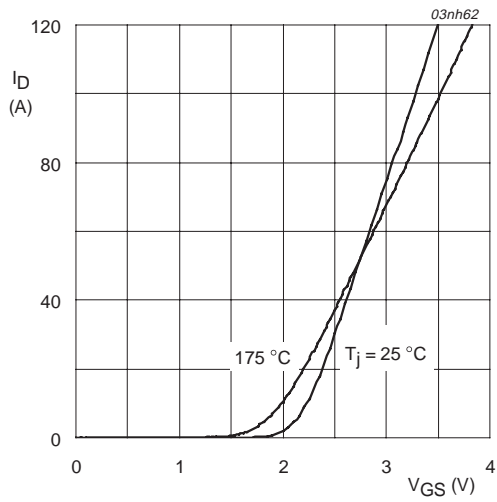
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



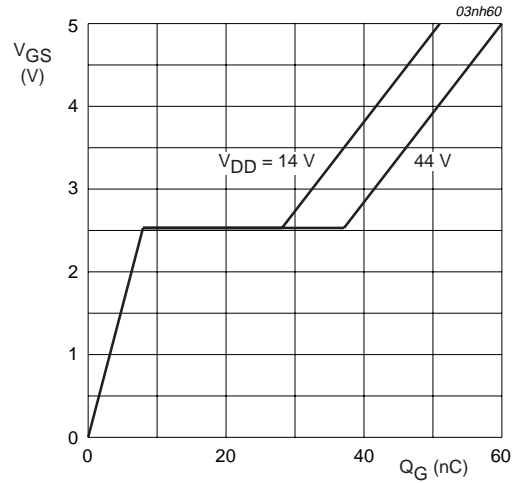
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



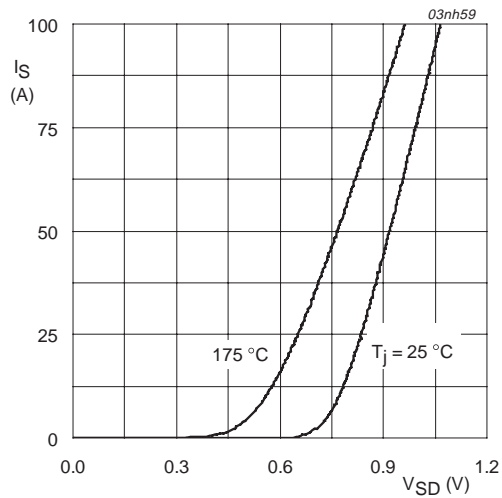
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

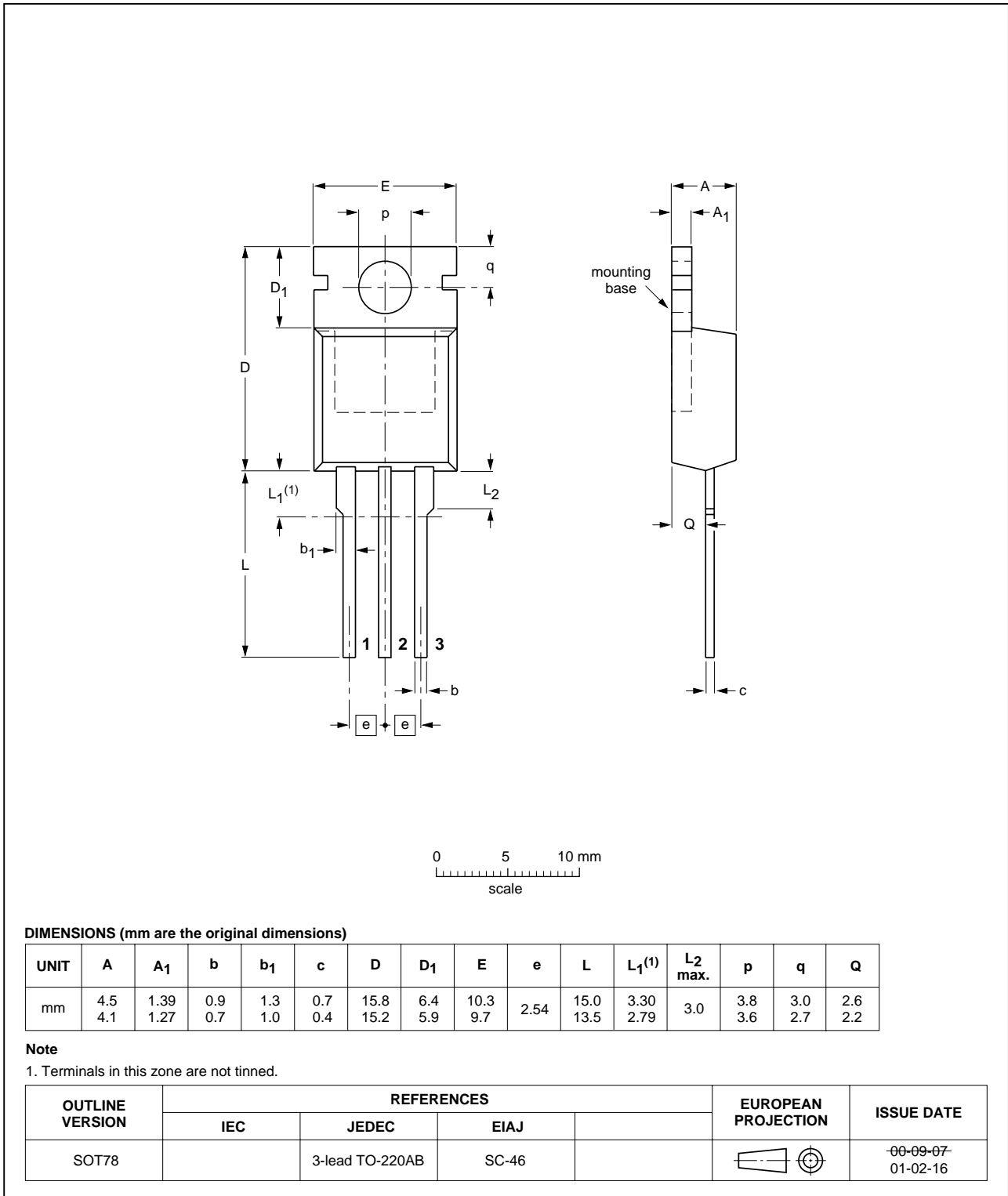


Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404

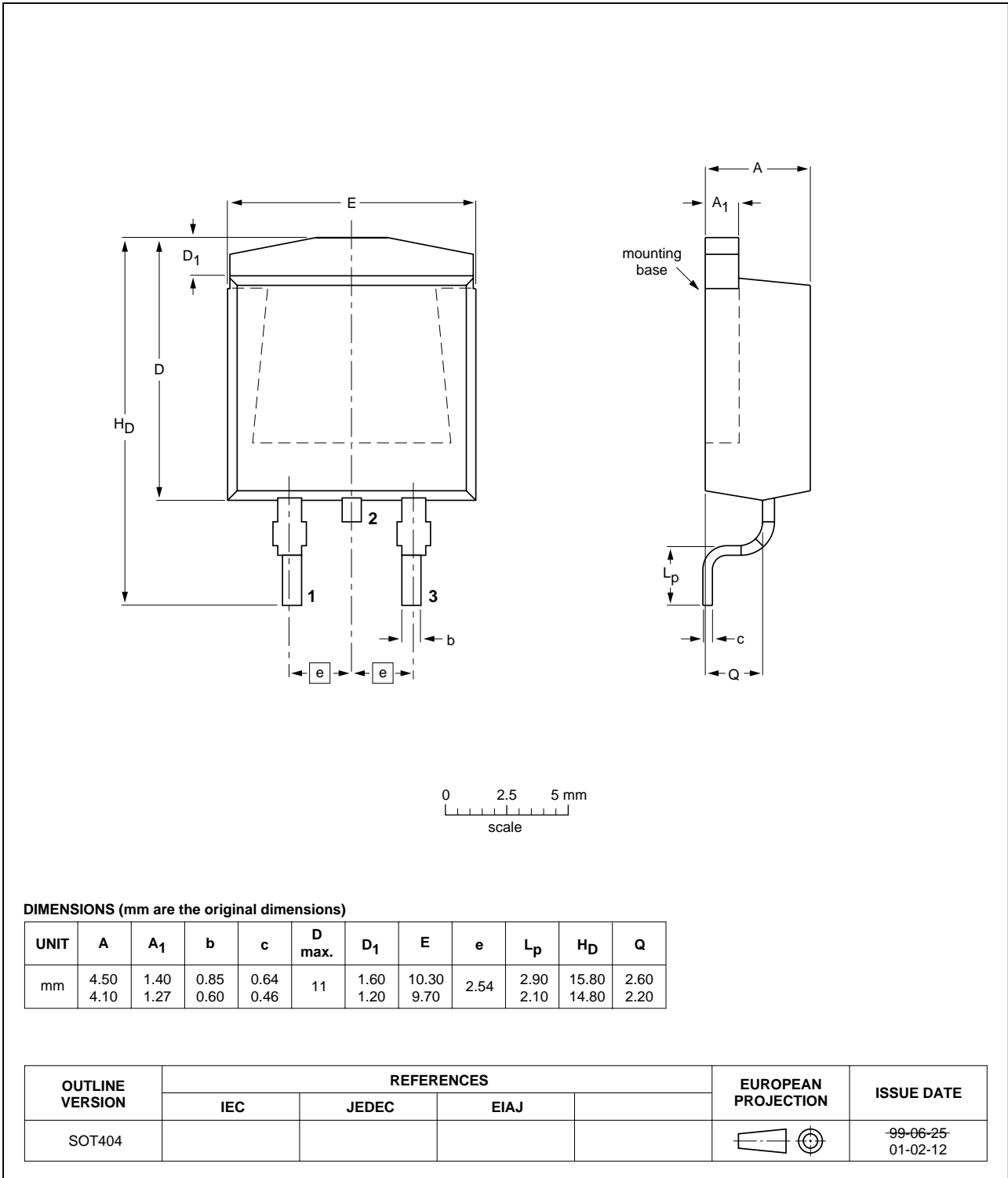
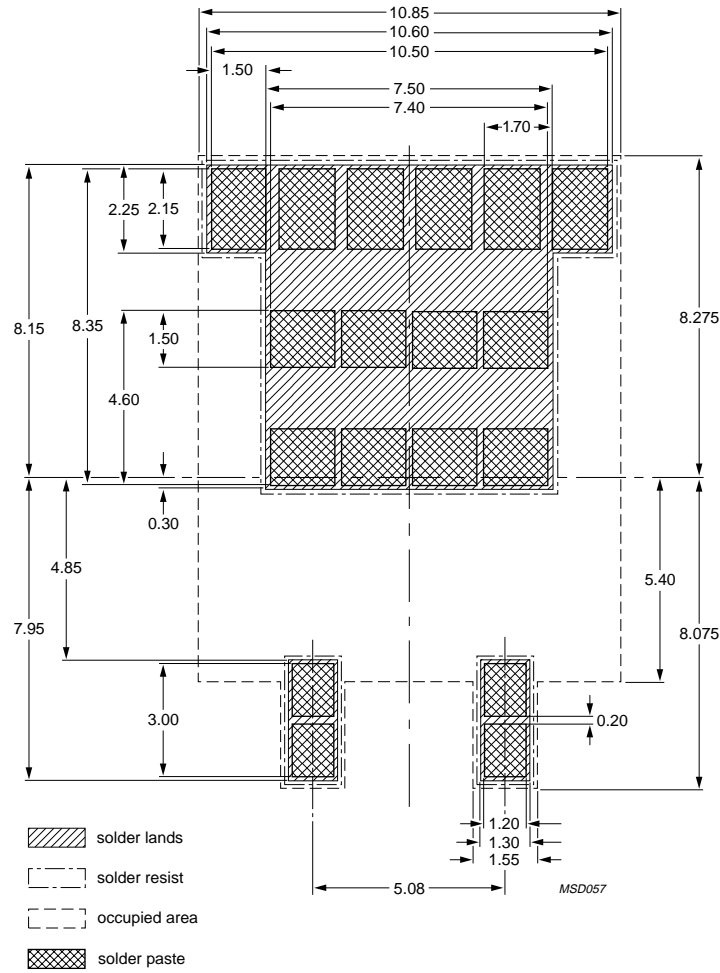


Fig 17. SOT404 (D²-PAK).

10. Soldering



Dimensions in mm.

Fig 18. Reflow soldering footprint for SOT404.

11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20020221	-	Product data; initial version.

12. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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