

BUK9518-55A; BUK9618-55A

TrenchMOS™ logic level FET

Rev. 01 — 27 August 2001

Product data

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9518-55A in SOT78 (TO-220AB)

BUK9618-55A in SOT404 (D²-PAK).

2. Features

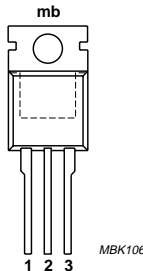
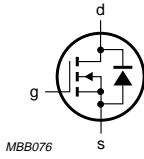
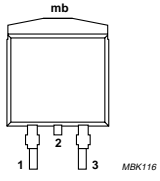
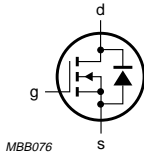
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V and 24 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		
		SOT78 (TO-220AB)	SOT404 (D ² -PAK)



PHILIPS

5. Quick reference data

Table 2: Quick reference data

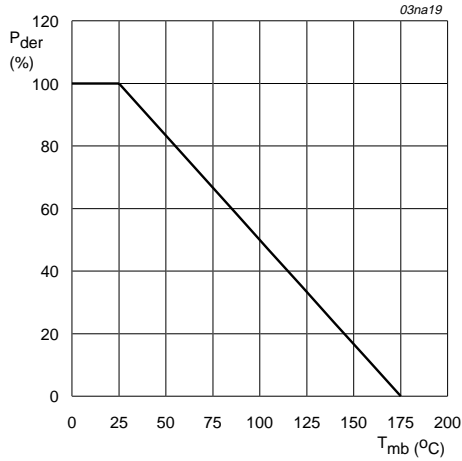
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	–	61	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	–	136	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 5\text{ V}; I_D = 25\text{ A}$	14	18	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	–	19	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	12	16	mΩ

6. Limiting values

Table 3: Limiting values

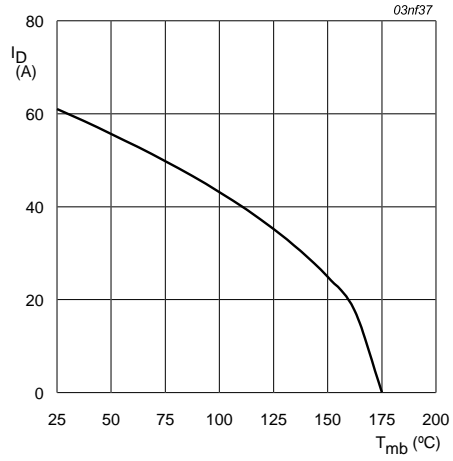
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	55	V
V_{GS}	gate-source voltage (DC)		–	±15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	–	61	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	–	43	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	–	246	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	–	136	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	–	61	A
I_{DRM}	pulsed reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	246	A
Avalanche ruggedness					
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 61\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_{mb} = 25\text{ °C}$	–	127	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

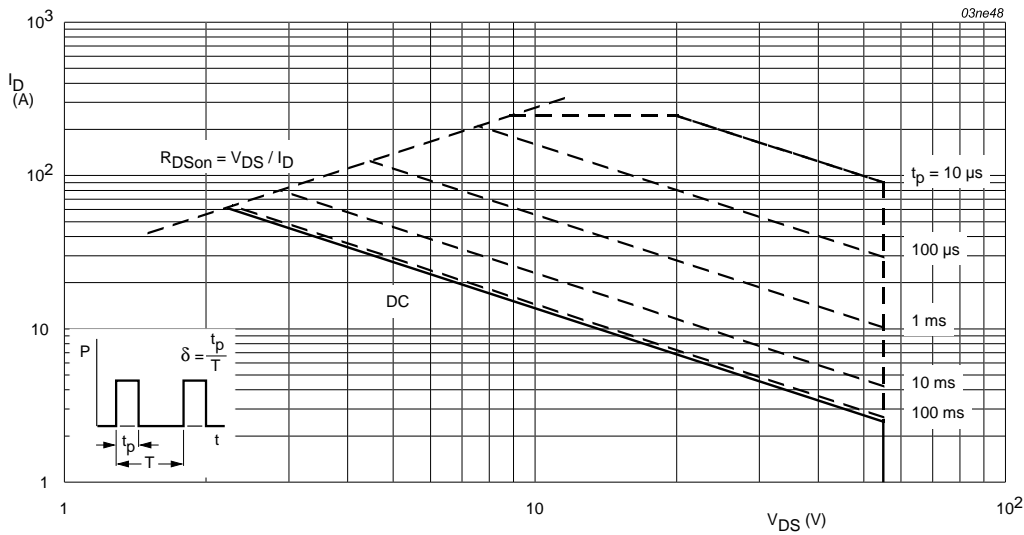
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 4.5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	60	K/W
		mounted on printed circuit board; minimum footprint; SOT404 package	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.1	K/W

7.1 Transient thermal impedance

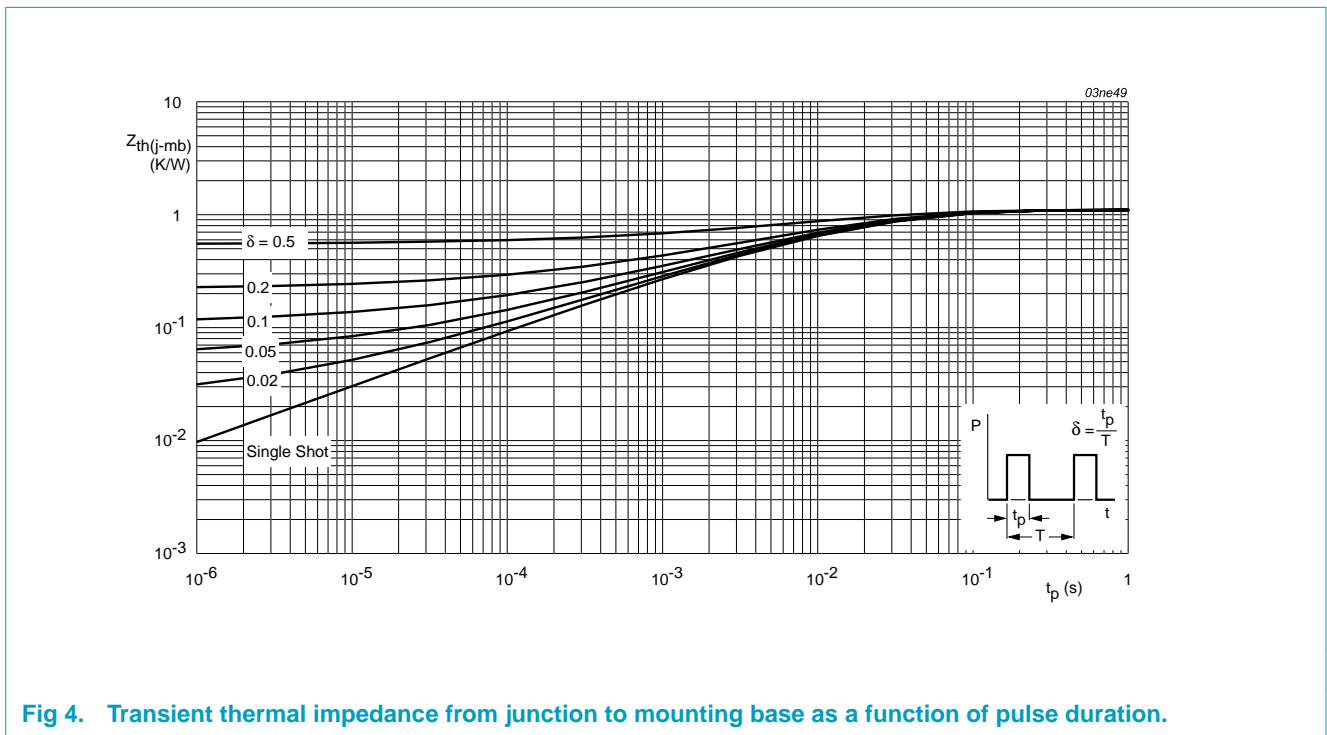


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

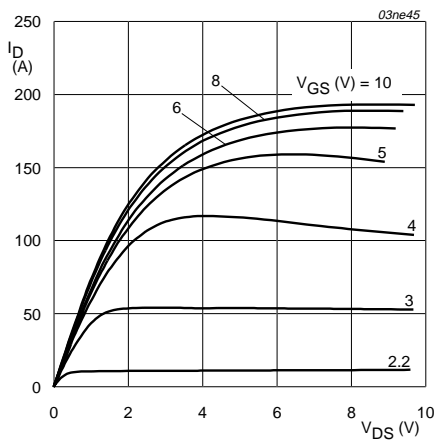
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V T _j = 25 °C	55	–	–	V
		T _j = –55 °C	50	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	–	–	V
		T _j = –55 °C	–	–	2.3	V
I _{DSS}	drain-source leakage current	V _{DS} = 55 V; V _{GS} = 0 V T _j = 25 °C	–	0.05	10	μA
		T _j = 175 °C	–	–	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	–	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; Figure 7 and 8 T _j = 25 °C	–	14	18	mΩ
		T _j = 175 °C	–	–	36	mΩ
		V _{GS} = 4.5 V; I _D = 25 A	–	–	19	mΩ
		V _{GS} = 10 V; I _D = 25 A	–	12	16	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	V _{GS} = 5 V; V _{DD} = 44 V; I _D = 25 A; Figure 14	–	34	–	nC
Q _{gs}	gate-to-source charge		–	4.5	–	nC
Q _{gd}	gate-to-drain (Miller) charge		–	14	–	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 12	–	1660	2210	pF
C _{oss}	output capacitance		–	290	350	pF
C _{rss}	reverse transfer capacitance		–	190	270	pF
t _{d(on)}	turn-on delay time	V _{DD} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _G = 10 Ω	–	21	–	ns
t _r	rise time		–	126	–	ns
t _{d(off)}	turn-off delay time		–	95	–	ns
t _f	fall time		–	97	–	ns
L _d	internal drain inductance	from drain lead 6 mm from package to centre of die	–	4.5	–	nH
		from contact screw on mounting base to centre of die SOT78	–	3.5	–	nH
		from upper edge of drain mounting base to centre of die SOT404	–	2.5	–	nH
L _s	internal source inductance	from source lead to source bond pad	–	7.5	–	nH

Table 5: Characteristics...continued

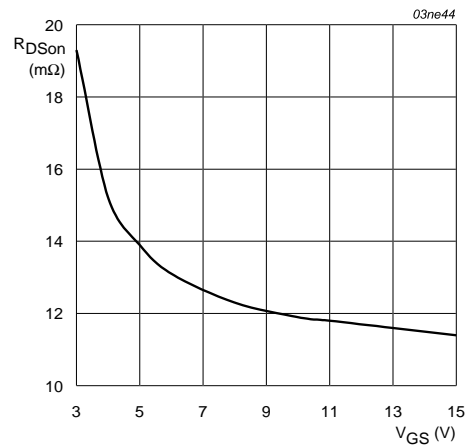
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	–	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$	–	53	–	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	–	101	–	nC



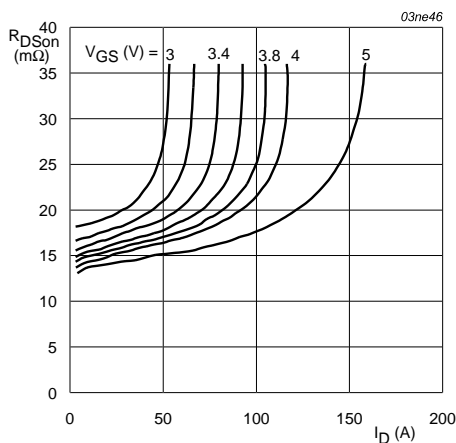
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



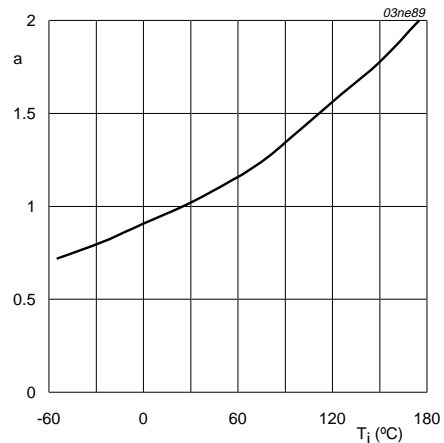
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



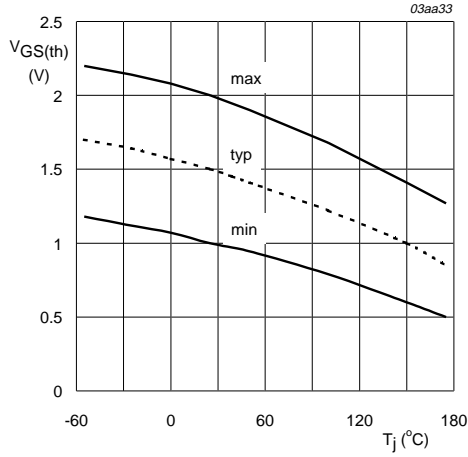
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



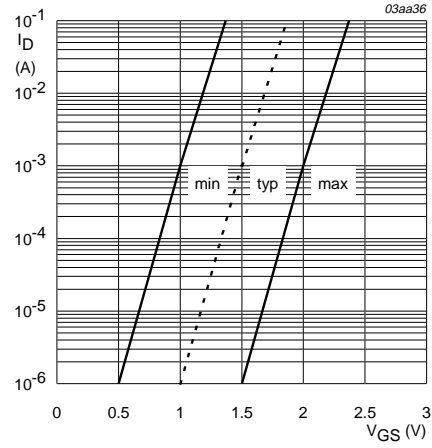
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



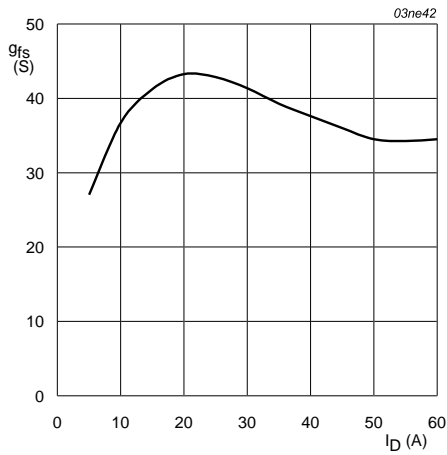
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



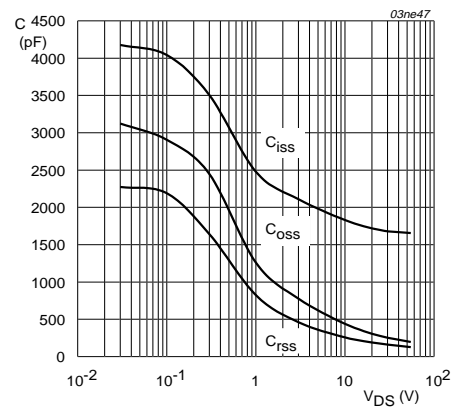
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



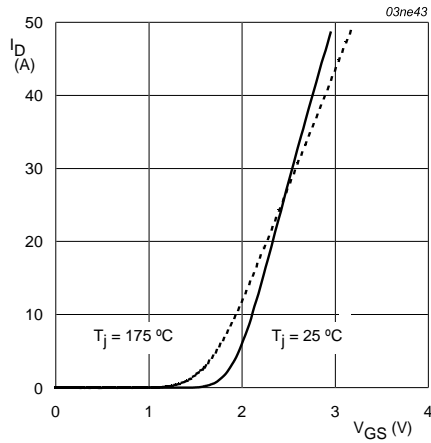
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



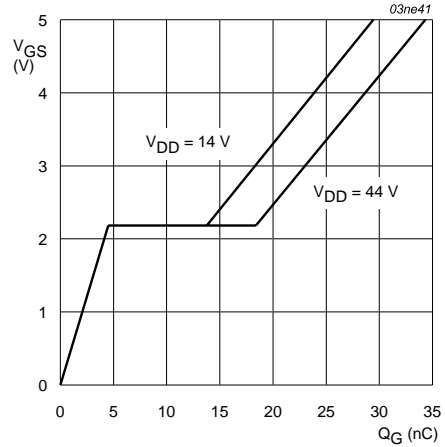
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



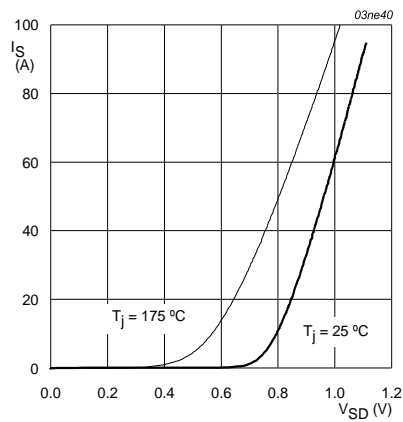
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ °C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



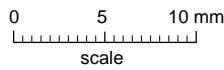
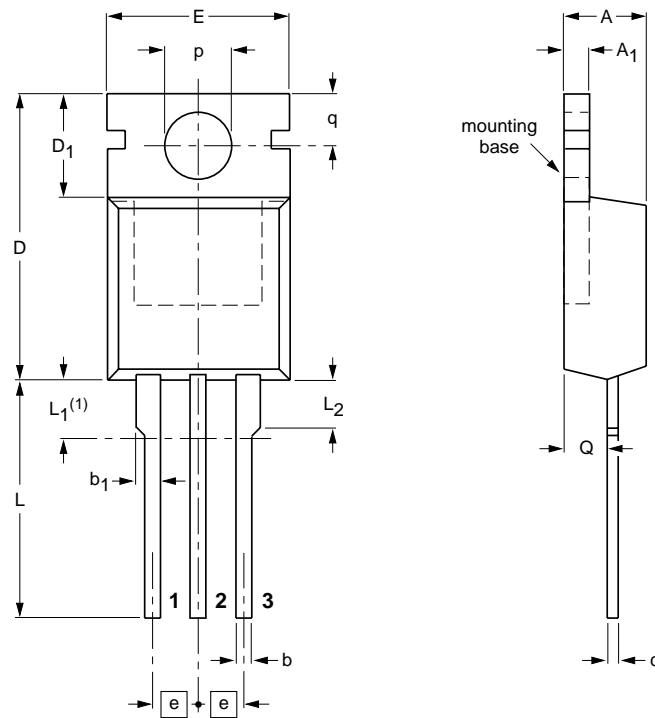
$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07 01-02-16

Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404

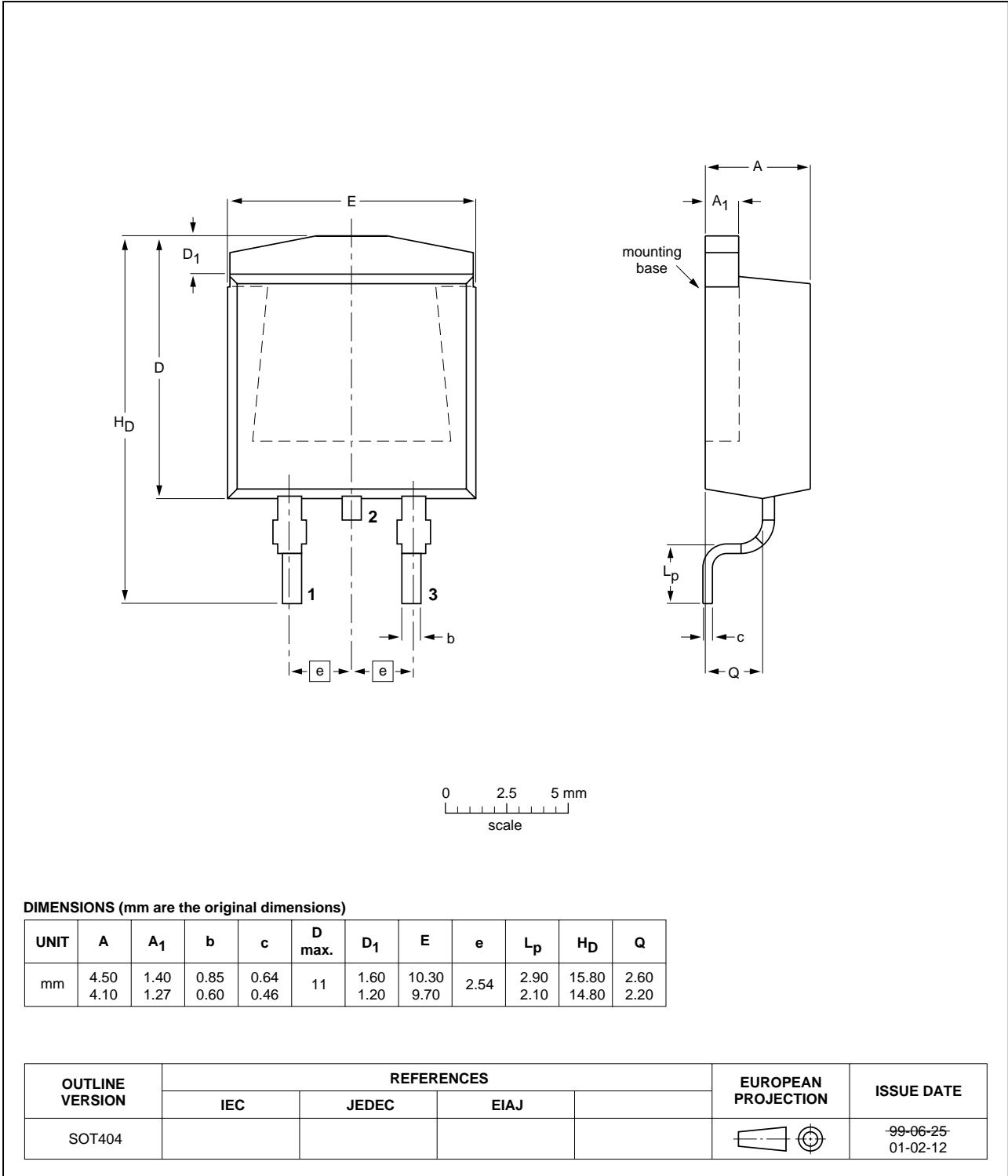
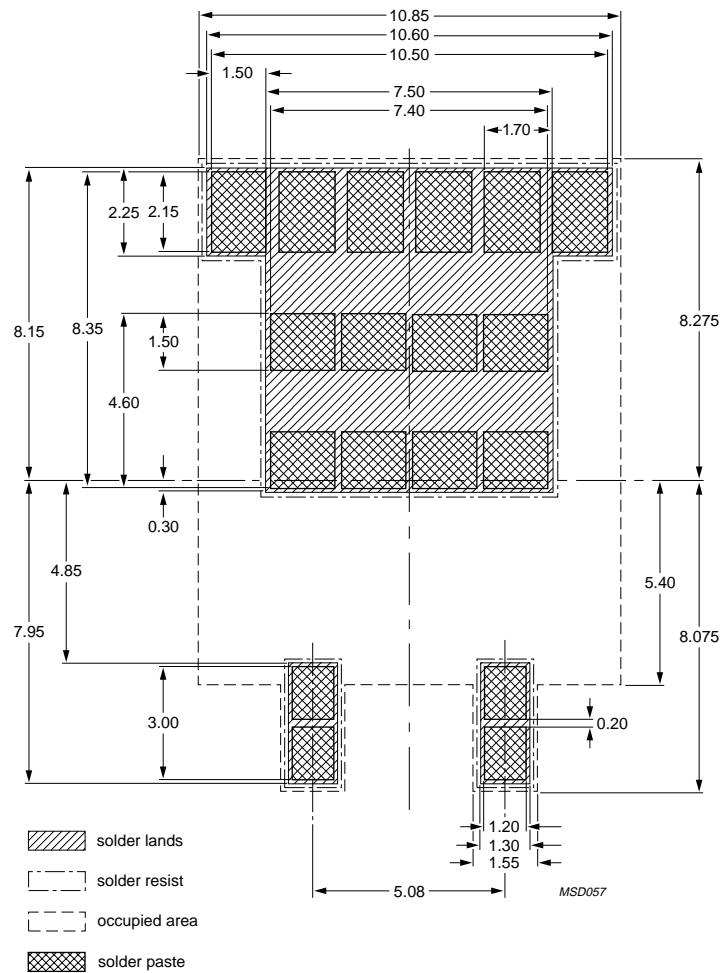


Fig 17. SOT404 (D²-PAK).

10. Soldering



Dimensions in mm.

Fig 18. Reflow soldering footprint for SOT404.

11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010827	-	Product data; initial version

12. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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