THE DATASHEET OF

ISL91128IINZ-T7A

ISL91128

High Efficiency Buck-Boost Regulator with 4.5A Switches and I²C Interface

FN8732
Rev.3.00
May 3, 2018

The ISL91128 is a high-current, buck-boost switching regulator for systems using new battery chemistries. It uses the Renesas proprietary buck-boost algorithm to maintain voltage regulation while providing excellent efficiency and very low output voltage ripple when the input voltage is close to the output voltage. The device also includes a selectable Bypass mode for low power consumption in applications that have a Sleep or Low Power mode.

The ISL91128 is capable of delivering at least 2.2A continuous output current (V_{OUT} = 3.3V) across a battery voltage range of 2.5V to 4.35V. This maximizes the energy utilization of advanced, single-cell Li-ion battery chemistries that have significant capacity left at voltages below the system voltage. Its fully synchronous low ON-resistance 4-switch architecture and a low quiescent current of only 30µA optimize efficiency under all load conditions.

The ISL91128 supports a broader set of programmable features that can be accessed using an I²C bus interface. With a programmable output voltage range of 1.9V to 5.0V, the ISL91128 is ideal for applications requiring dynamically changing supply voltages. A programmable slew rate can be selected to provide smooth transitions between output voltage settings.

The ISL91128 is available in a 20 bump, 0.4mm pitch WLCSP (2.15mmx1.74mm) with a 2.5MHz switching frequency, which further reduces the size of external components.

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between Buck and Boost modes
- I²C interface
- Input voltage range: 1.8V to 5.5V
- Continuous output current: up to 2.4A (PVIN = 2.5V, V_{OUT} = 3.3V)
- High efficiency: up to 96%
- 30µA quiescent current maximizes light-load efficiency
- Selectable bypass power saving mode operation
- 2.5MHz switching frequency minimizes external component size
- Fully protected for short-circuit, over-temperature, and undervoltage
- Small 2.15mmx1.74mm WLCSP

Applications

- Brownout-free system voltage for smart phones and tablet PCs
- Wireless communication devices
- 2G/3G/4G RF power amplifiers

Related Literature

For a full list of related documents, visit our website

- ISL91128 product page

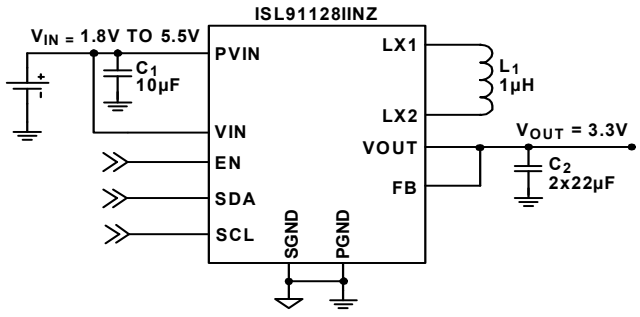


FIGURE 1. TYPICAL APPLICATION

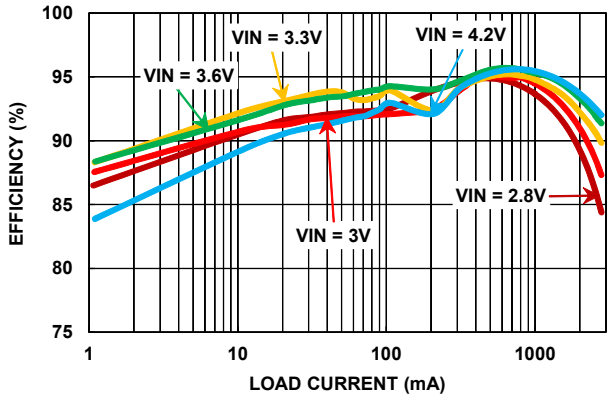


FIGURE 2. EFFICIENCY: V_{OUT} = 3.3V, T_A = +25°C

Block Diagram

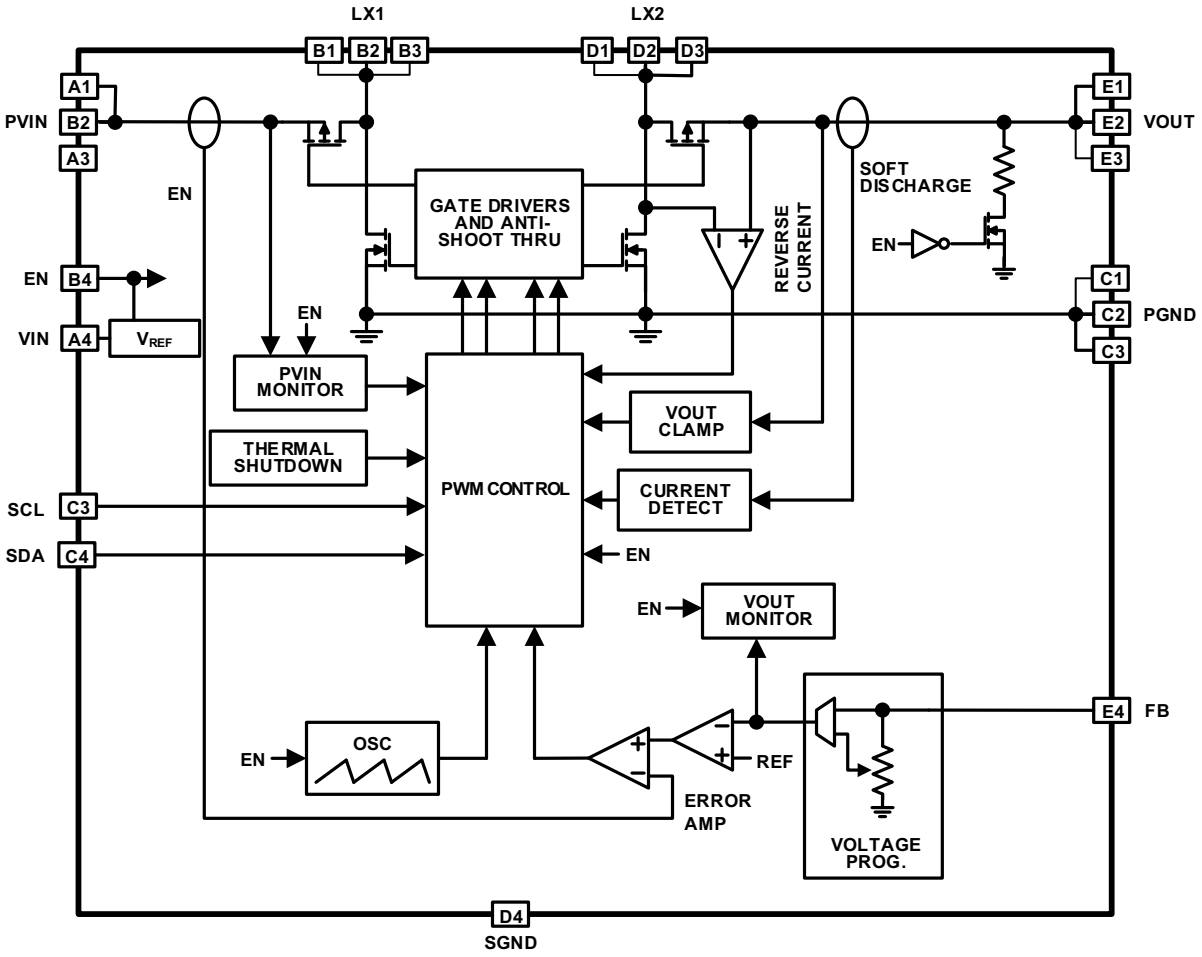
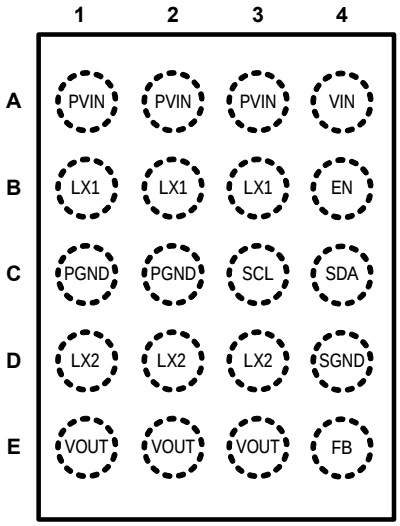


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL91128
(20 BALL WLCSP, 0.4mm PITCH)
TOP VIEW, BUMPS DOWN



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A1, A2, A3	PVIN	Power input. Range: 1.8V to 5.5V. Connect 2x10µF capacitors to PGND.
B1, B2, B3	LX1	Inductor connection, input side
C1, C2	PGND	Power ground for high switching current
D1, D2, D3	LX2	Inductor connection, output side
E1, E2, E3	VOUT	Buck-boost regulator output. Connect 2x22µF capacitors to PGND.
C4	SDA	I^2C data input
C3	SCL	I^2C clock input
A4	VIN	Supply input. Range: 1.8V to 5.5V.
B4	EN	Logic input, drive HIGH to enable device.
D4	SGND	Analog ground pin
E4	FB	Voltage feedback pin. Connect to VOUT

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	DEFAULT OUTPUT VOLTAGE (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL91128IINZ-T	GAYC	3.3	-40 to +85	3k	20 Ball WLCSP	W4x5.20M
ISL91128IINZ-T7A	GAYC	3.3	-40 to +85	250	20 Ball WLCSP	W4x5.20M
ISL91128IIN-EVKIT1Z	Evaluation Board Kit for ISL91128IINZ					
ISL91128IIN-EVZ	Evaluation Board for ISL91128IINZ					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL91128 product information page. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	BUCK-BOOST REGULATION	BYPASS	DYNAMIC VOLTAGE SCALING	I^2C	PACKAGE
ISL91127	Yes	No	No	No	WLCSP
ISL91127IR	Yes	No	No	No	QFN
ISL91128	Yes	Yes	Yes	Yes	WLCSP

NOTE: For the full family of ISL911xx buck-boost regulators, please visit our website.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2. . . . . -0.3V to 6.5VDC, -2V to 7V for 10ns
FB (Adjustable Version) . . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} Versions) . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JS-001-2010). 2.5kV
Machine Model (Tested per JESD22-A115C) 250V
Charged Device Model (Tested per JS-002-2014) 1kV
Latch-Up (Tested per JESD-78D; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
20 Ball WLCSP Package (Notes 4, 5)	72	16

Maximum Junction Temperature . . . . . .+125°C
Storage Temperature Range. . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range . . . . . .1.8V to 5.5V
Maximum Load Current
V_{IN} = 2.5V V_{OUT} = 3.3V 2.2ADC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a trace at the middle of one side. See TB379.

Analog Specifications

$V_{IN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 10\mu F$, $C_2 = 2x22\mu F$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}	V_{IN} needs to be higher than the I^2C pull-up voltage	**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.725	**1.795**	V
		Falling	**1.550**	1.650		V
V_{IN} Supply Current	I_{VIN}	PFM mode, no external load on V_{OUT} (Note 8), V_{IN} = 4.5V		30	**45**	µA
V_{IN} Supply Current, Bypass	I_{BYP}	Bypass mode, V_{IN} = 4.5V		6.0		µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		0.05	**1.00**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V_{OUT}	I_{OUT} = 100mA, V_{IN} = 3.6V	**1.95**		**5.00**	V
Output Voltage Accuracy		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
Line Regulation, PWM Mode	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 500mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		±5		mV/V
Load Regulation, PWM Mode	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 1000mA		±0.05		mV/mA
Line Regulation, PFM Mode	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 100mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
Load Regulation, PFM Mode	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising	**5.25**		**5.95**	V
Output Voltage Clamp Hysteresis				400		mV
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}		**2.10**	2.50	**2.90**	MHz
Minimum On-Time	$t_{ON(MIN)}$			80		ns
LX1 Pin Leakage Current	$I_{PFETLEAK}$	V_{IN} = 3.6V	**-1**		**1**	µA

Analog Specifications

$V_{IN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 10\mu F$, $C_2 = 2x22\mu F$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
LX2 Pin Leakage Current	$I_{NFETLEAK}$	V_{IN} = 3.6V	**-1**		**1**	µA
SOFT-START AND SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Buck mode. V_{IN} = 4V, V_{OUT} = 3.3V, I_O = 200mA		2		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Boost mode. V_{IN} = 2V, V_{OUT} = 3.3V, I_O = 200mA		2		ms
V_{OUT} Soft Discharge ON-Resistance	R_{DISCHG}	EN < V_{IL}		120		Ω
POWER MOSFET						
Input P-Channel MOSFET ON-Resistance	$R_{DS(ON)\_PI}$	V_{IN} = 3.6V, I_O = 200mA		30		mΩ
Output P-Channel MOSFET ON-Resistance	$R_{DS(ON)\_PO}$	V_{IN} = 3.6V, I_O = 200mA		27		mΩ
Input N-Channel MOSFET ON-Resistance	$R_{DS(ON)\_NI}$	V_{IN} = 3.6V, I_O = 200mA		25		mΩ
Output N-Channel MOSFET ON-Resistance	$R_{DS(ON)\_NO}$	V_{IN} = 3.6V, I_O = 200mA		25		mΩ
P-Channel MOSFET Peak Current Limit	I_{PK_LMT}	V_{IN} = 3.6V	**4.0**	4.2	**5.2**	A
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM		V_{IN} = 3.6V, V_{OUT} = 3.3V		200		mA
Load Current Threshold, PWM to PFM		V_{IN} = 3.6V, V_{OUT} = 3.3V		75		mA
Thermal Shutdown				155		°C
Thermal Shutdown Hysteresis				30		°C
LOGIC INPUTS						
Input Leakage	I_{LEAK}	V_{IN} = 3.6V		0.05	**1**	µA
Input HIGH Voltage	V_{IH}	V_{IN} = 3.6V	**1.4**			V
Input LOW Voltage	V_{IL}	V_{IN} = 3.6V			**0.4**	V

I²C Interface Timing Specification

For SCL and SDA pins, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP (Note 7)	MAX (Note 9)	UNIT
Pin Capacitance	C_{pin}				15	pF
SCL Frequency	f_{SCL}				400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{sp}	Any pulse narrower than the maximum specification is suppressed			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing V_{IL}, until SDA exits the V_{IL} to V_{IH} window			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing V_{IH} during a STOP condition, to SDA crossing V_{IH} during the following START condition	1300			ns
Clock LOW Time	t_{LOW}	Measured at the V_{IL} crossings	1300			ns
Clock HIGH Time	t_{HIGH}	Measured at the V_{IH} crossings	600			ns

I²C Interface Timing Specification For SCL and SDA pins, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP (Note 7)	MAX (Note 9)	UNIT
START Condition Set-Up Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing V_{IH}	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL} to SCL falling edge crossing V_{IH}	600			ns
Input Data Set-Up Time	$t_{SU:DAT}$	From SDA exiting the V_{IL} to V_{IH} window, to SCL rising edge crossing V_{IL}	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing V_{IH} to SDA entering the V_{IL} to V_{IH} window	0			ns
STOP Condition Set-Up Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH}, to SDA rising edge crossing V_{IL}	600			ns
STOP Condition Hold Time for Read or Volatile Only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing V_{IH}	1300			ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing V_{IL}, until SDA enters the V_{IL} to V_{IH} window	0			ns
SDA and SCL Rise Time	t_R	From V_{IL} to V_{IH}	20 + 0.1 x Cb		250	ns
SDA and SCL Fall Time	t_F	From V_{IH} to V_{IL}	20 + 0.1 x Cb		250	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip	10		400	pF
SDA and SCL Bus Pull-Up Resistor Off-Chip	Rpu	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for T_A = +25°C and V_{IN} = 3.6V.
8. Quiescent current measurements are taken when the output is not switching.
9. Limits established by characterization and are not production tested.

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A.

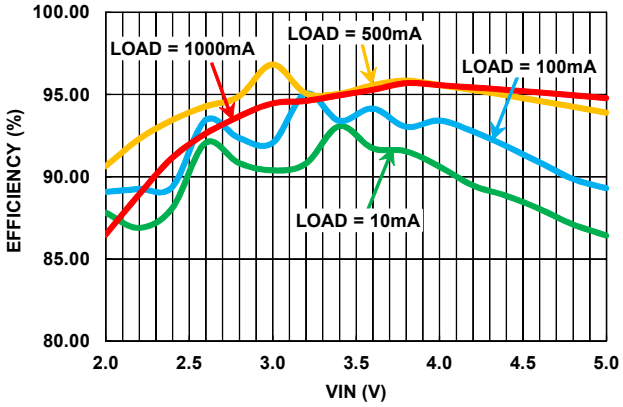


FIGURE 4. EFFICIENCY vs INPUT VOLTAGE

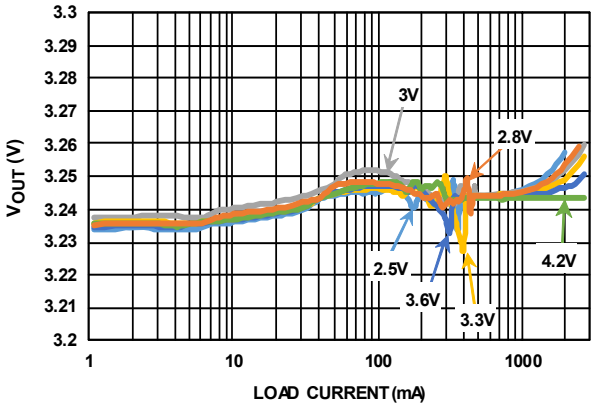


FIGURE 5. OUTPUT VOLTAGE vs LOAD CURRENT

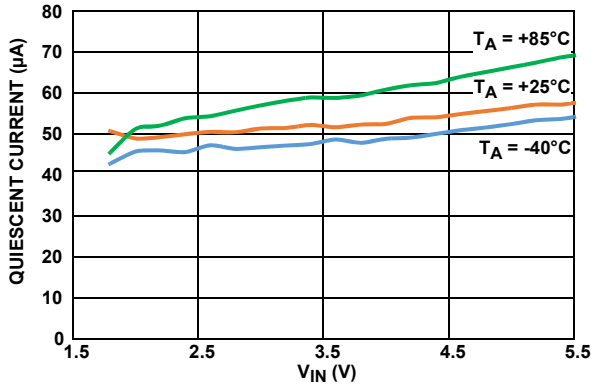


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V, MODE = HIGH)

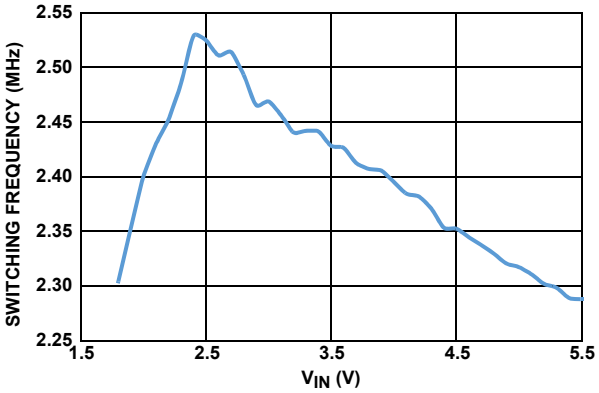


FIGURE 7. SWITCHING FREQUENCY vs INPUT VOLTAGE

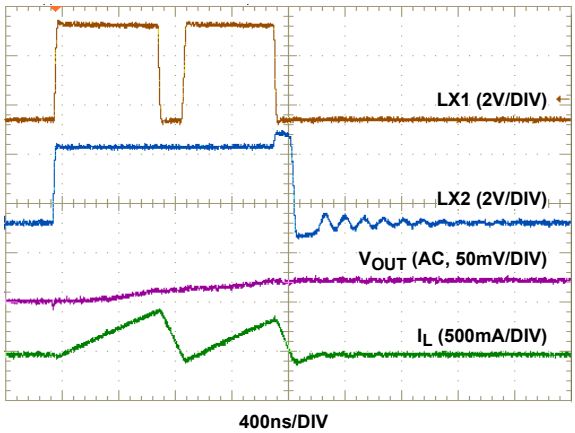


FIGURE 8. STEADY-STATE OPERATION IN PFM (V_{IN} = 3.3V, V_{OUT} = 3.3V, NO LOAD)

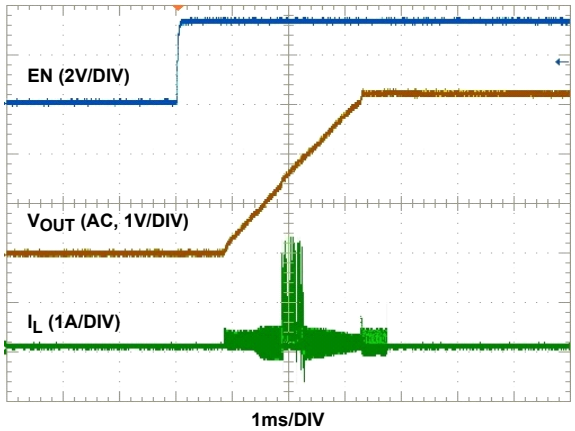


FIGURE 9. SOFT-START (V_{IN} = 3.6V, V_{OUT} = 3.3V, NO LOAD)

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

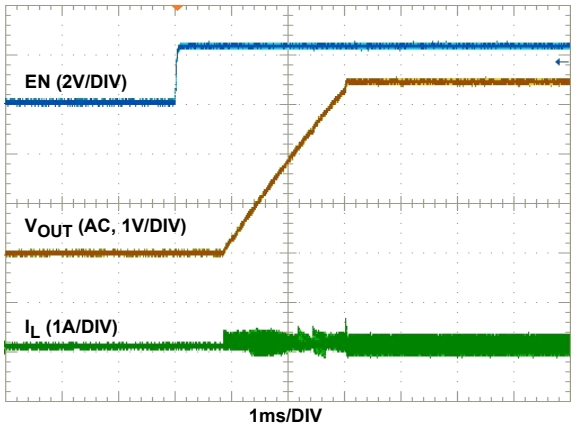


FIGURE 10. SOFT-START (V_{IN} = 2.5V, V_{OUT} = 3.3V, NO LOAD)

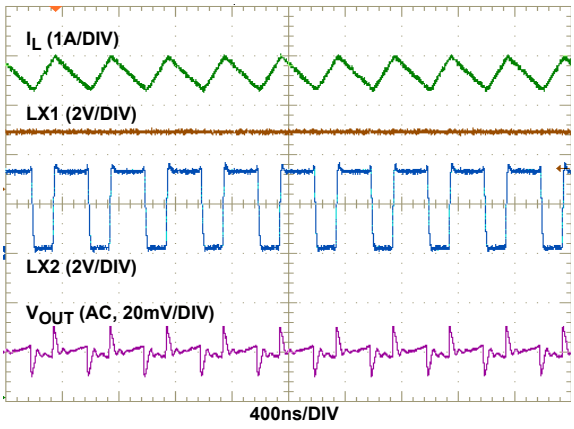


FIGURE 11. STEADY-STATE OPERATION (V_{IN} = 2.5V, V_{OUT} = 3.3V, 2A LOAD)

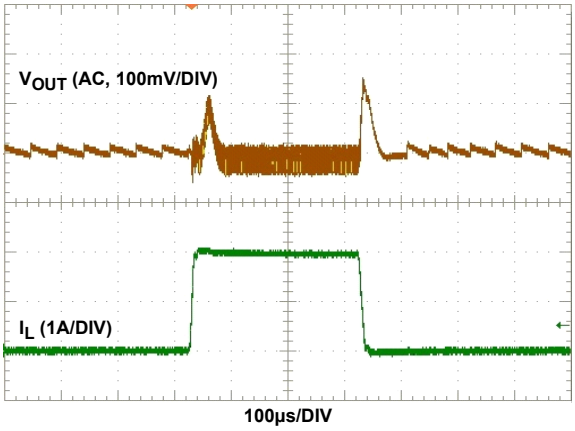


FIGURE 12. 0A TO 2A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

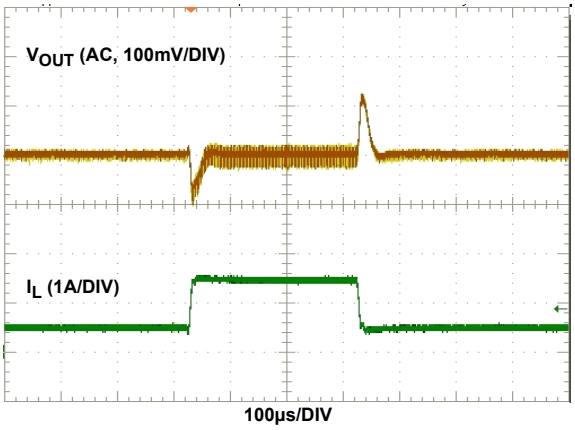


FIGURE 13. 0.5A TO 1.5A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

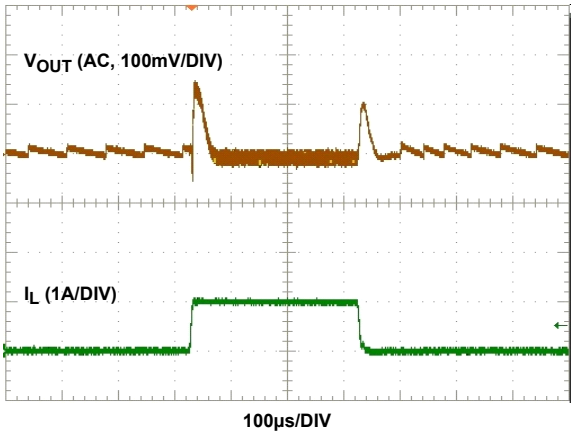


FIGURE 14. 0A TO 1A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

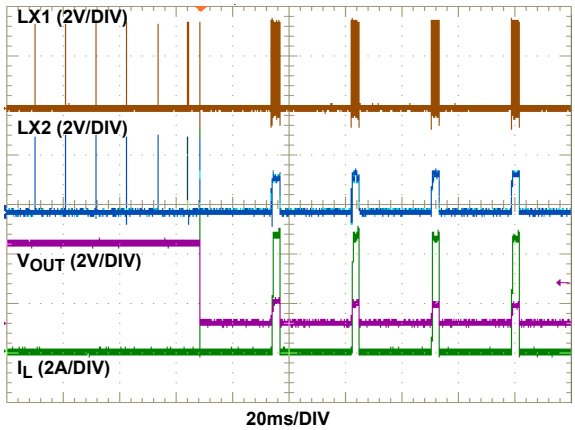


FIGURE 15. OUTPUT SHORT-CIRCUIT BEHAVIOR (V_{IN} = 3.6V, V_{OUT} = 3.3V)

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

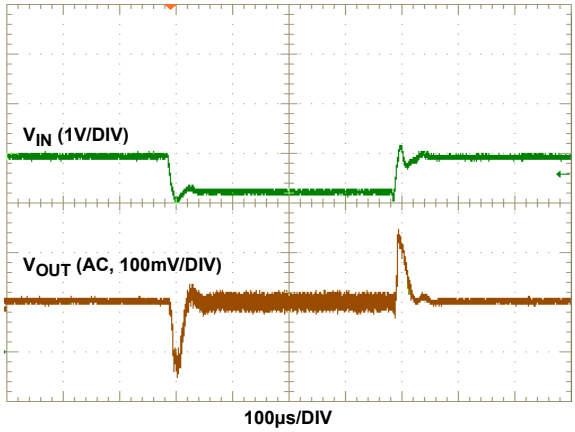


FIGURE 16. 4V TO 3.2V LINE TRANSIENT (V_{OUT} = 3.3V, LOAD = 1A)

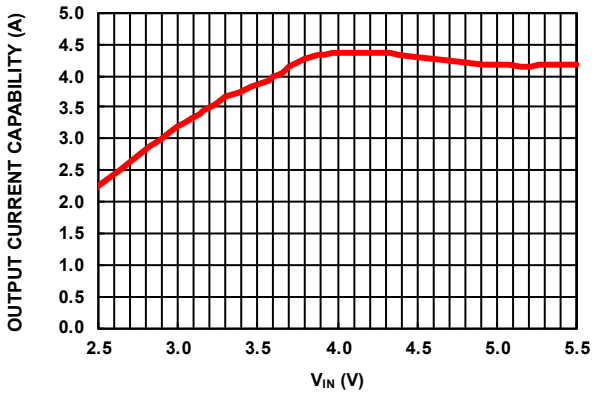


FIGURE 17. OUTPUT CURRENT CAPABILITY: V_{OUT} = 3.3V, T_A = +25°C

Functional Description

Functional Overview

The ISL91128 implements a complete buck-boost switching regulator with PWM controller, internal switches, references, protection circuitry, and control inputs. Refer to the "Block Diagram" on page 2.

The PWM controller automatically switches between Buck and Boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram" on page 2, the ISL91128 provides four power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides an operating voltage source required for stable V_{REF} generation. Separate ground pins (SGND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

The device enable by asserting the EN pin HIGH. Driving EN LOW invokes a power-down mode in which most internal device functions are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and GND is activated to slowly discharge the output capacitor. This internal resistor has a typical 120Ω resistance. The soft discharge function can be disabled through the I^2C interface (see Table 5 on page 14).

POR Sequence and Soft-Start

Asserting the EN pin HIGH allows the device to power up. The following events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. A typical 1ms delay occurs between assertion of the EN pin and the start of the switching regulator soft-start ramp.

When the target output voltage is higher than the input voltage, the device transitions from Buck mode to Boost mode during the soft-start sequence. During this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into Boost mode takes longer than soft-start into Buck mode. The total soft-start time into Buck operating mode is typically 2ms, whereas the typical soft-start time into Boost operating mode is typically 3ms. Increasing the load current increases these typical soft-start times.

Short-Circuit Protection

The ISL91128 provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91128 if the die temperature reaches +155°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +125°C (typical), the device resumes normal operation. When exiting thermal shutdown, the ISL91128 executes its soft-start sequence.

Buck-Boost Conversion Topology

The ISL91128 operates in either Buck or Boost mode. When operating in conditions where PVIN is close to VOUT, the ISL91128 alternates between Buck and Boost mode as necessary to provide a regulated output voltage.

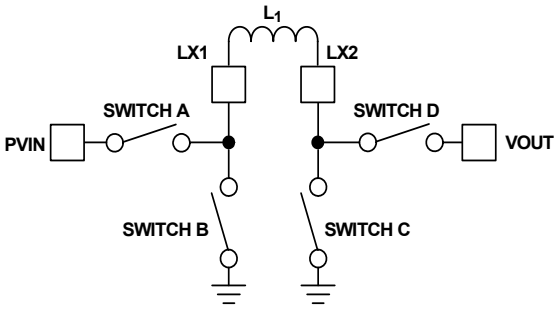


FIGURE 18. BUCK-BOOST TOPOLOGY

Figure 18 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

In Buck PWM mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In Boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate in Discontinuous mode during PFM operation. During PFM operation in Boost mode, the ISL91128 closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns off Switches A and C, then turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller. Switch B stays on after the multiple PFM pulses to hold LX1 to GND, which reduces EMI noise (see Figure 8 on page 7).

Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91128 rapidly and smoothly switches from Boost to Buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

I^2C Serial Interface

The ISL91128 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL91128 operates as a slave device in all applications. The SCL and SDA pins are open drain and need external pull-up resistors connected with a proper voltage level, for example, 3.3V. Pull the SCL and SDA pins to GND if the I^2C interface is not used.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Bypass Mode Operation

Bypass mode is always enabled and can be disabled by writing a ‘1’ to Bit 5 in the Mode Control register. When this function is disabled, setting the EN pin to ‘0’ will disable the device. To prevent the device from going into Bypass mode at power-up, EN should be set to ‘1’ or connected to VIN before power is applied.

When the device enters Bypass mode, both high-side FETs are turned ON, passing the input voltage to the output through the two high-side FETs and the inductor. In Bypass mode, all other blocks are turned off to minimize quiescent current consumption. There should be at least 1ms of time delay between entry into or exit out of Bypass mode, when transitioning between Bypass mode and a Voltage Regulation mode. Note there is no overcurrent protection in Bypass mode.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 19). Upon power-up of the ISL91128, the SDA pin is in the Input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL91128 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 19). A START condition is ignored during the power-up sequence and when EN input is low.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 19). A STOP condition at the end of a write operation initiates the reconfiguration of the ISL91128's voltage feedback loop as necessary to provide the programmed output voltage.

An Acknowledge (ACK), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 20).

The ISL91128 responds with an ACK after recognition of a START condition followed by a valid identification byte and once again after successful receipt of a register address byte. The ISL91128 also responds with an ACK after receiving a data byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

A valid Identification byte contains 0b0011100 as the seven MSBs, corresponding to the ISL91128 I^2C slave address. The LSB of the identification byte is the Read/$\overline{\text{Write}}$ bit. Its value is "1" for a Read operation and "0" for a Write operation (see Table 2).

TABLE 2. IDENTIFICATION BYTE FORMAT

0	0	1	1	1	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

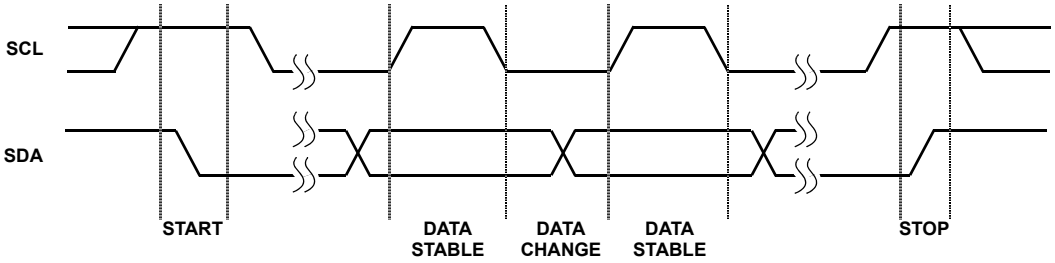


FIGURE 19. VALID DATA CHANGES, START, AND STOP CONDITIONS

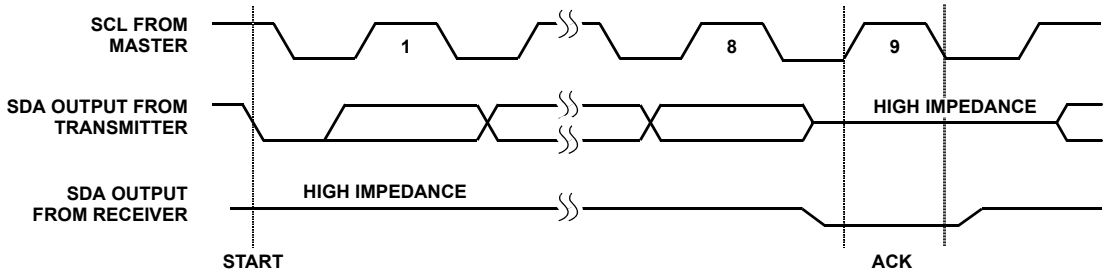


FIGURE 20. ACKNOWLEDGE RESPONSE FROM RECEIVER

Write Operation

A write operation requires a START condition, followed by a valid identification byte (containing the slave address with the R/$\overline{W}$ bit set to 0), a valid register address byte, a data byte, and a STOP condition. After each of the three bytes, the ISL91128 responds with an ACK. The master sends a STOP to complete the command.

STOP conditions that terminate write operations must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte or before one full data byte + ACK is sent, then the ISL91128 ignores the command and not change output voltage or other settings.

Read Operation

Figure 22 shows a Read operation. It consists of four bytes.

- The host generates a START condition, then transmits an Identification byte (containing the slave address with the R/$\overline{W}$ bit set to 0).
- The ISL91128 responds with an ACK.
- The host transmits the register address byte and the ISL91128 responds with another ACK.
- The host generates a repeat START condition or a STOP condition followed by a START condition.
- The host transmits an identification byte (containing the slave address with the R/$\overline{W}$ bit set to 1).
- The ISL91128 responds with an ACK, indicating it is ready to begin providing the requested data.
- The ISL91128 transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin.
- When transmission of the data byte is complete, the host generates a Not Acknowledge (NACK) condition followed by a STOP condition. This completes the I^{2}C Read operation.

The ISL91128 register map supports two registers (see Tables 3 through 5). Attempts to read other register addresses are not supported and should not be attempted. Similarly, the ISL91128 does not support I^{2}C block reads and writes.

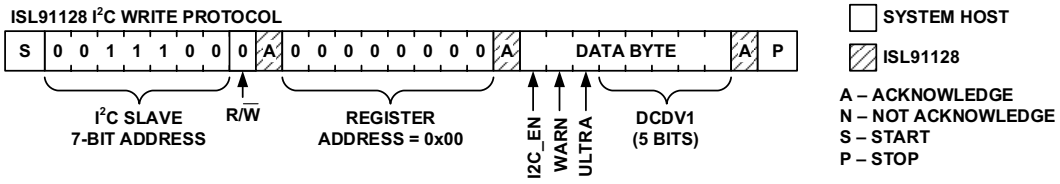


FIGURE 21. I^{2}C REGISTER WRITE PROTOCOL

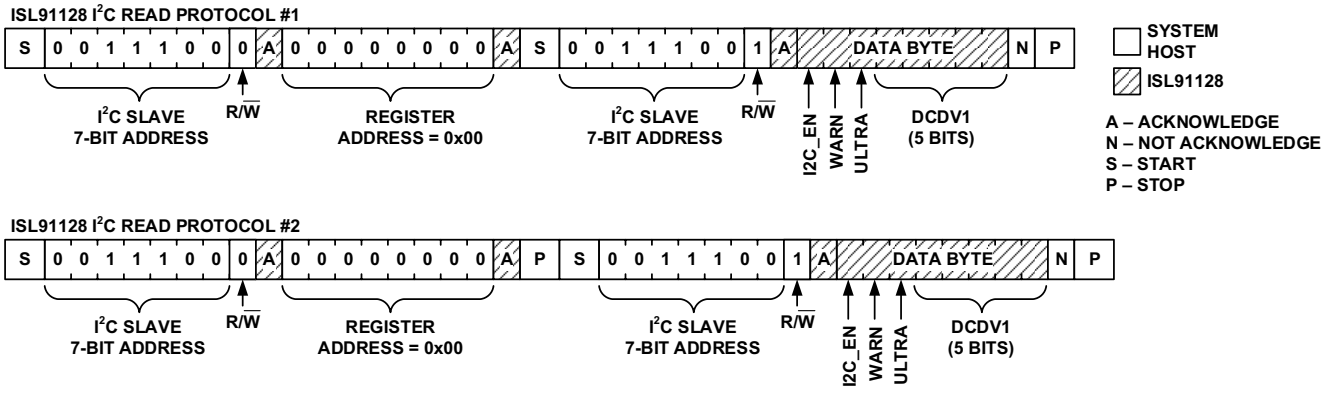


FIGURE 22. I^{2}C REGISTER READ PROTOCOL

Digital Slew Rate Control

When changing voltages using the I²C interface, the ISL91128 can be programmed to control the rate of voltage increase or decrease as it transitions from one voltage setting to the next. Details about the digital slew rate settings can be found in Table 5 on page 14.

Register Description

The ISL91128 has two I²C accessible control registers that set output voltage, operating mode, and digital slew rate.

TABLE 3. REGISTER ADDRESS 0x00: VOLTAGE CONTROL

BIT	NAME	TYPE	RESET	DESCRIPTION
5:0	DCDOUT	R/W	00000	V_{OUT} programming. See Table 4.
6	ULTRA	R/W	0	Ultrasonic mode select. Not applicable in forced PWM mode: 0: Ultrasonic feature disabled 1: Ultrasonic feature enabled
7	I2CEN	R/W	0	I²C programming enable bit: 0: Device ignores I²C command, and uses factory programmed default DCDOUT and ULTRA settings. 1: Device uses the I²C programmed DCDOUT and ULTRA settings.

Bits DCDOUT[5:0] set the output voltage, as shown in Equation 1 and Table 4. The ISL91128 output voltage range is 1.90V to 5.0V.

$$V_{OUT} = 1.9V + (n - 1) \bullet 0.05, \text{ where } n = 1 \text{ to } 63 \quad \text{(EQ. 1)}$$

The power-up output voltage will be at 3.3V. To change to other voltages after power-up, write the VOLTAGE CONTROL register for 3.3V (0b011101) before enabling the 'I2CEN' bit in the VOLTAGE CONTROL register. Then enable the 'I2CEN' bit and write the desired output voltage code to the VOLTAGE CONTROL register.

TABLE 4. DCDOUT[5:0] VALUE vs OUTPUT VOLTAGE

DCDOUT[5:0]	OUTPUT VOLTAGE (V)
0b000001	1.90
0b000010	1.95
0b000011	2.00
0b000100	2.05
0b000101	2.10
0b000110	2.15
0b000111	2.20
0b001000	2.25
0b001001	2.30
0b001010	2.35
0b001011	2.40
0b001100	2.45
0b001101	2.50
0b001110	2.55
0b001111	2.60

TABLE 4. DCDOUT[5:0] VALUE vs OUTPUT VOLTAGE (Continued)

DCDOUT[5:0]	OUTPUT VOLTAGE (V)
0b010000	2.65
0b010001	2.70
0b010010	2.75
0b010011	2.80
0b010100	2.85
0b010101	2.90
0b010110	3.95
0b010111	3.00
0b011000	3.05
0b011001	3.10
0b011010	3.15
0b011011	3.20
0b011100	3.25
0b011101	3.30
0b011110	3.35
0b011111	3.40
0b100000	3.45
0b100001	3.50
0b100010	3.55
0b100011	3.60
0b100100	3.65
0b100101	3.70
0b100110	3.75
0b100111	3.80
0b101000	3.85
0b101001	3.90
0b101010	3.95
0b101011	4.00
0b101100	4.05
0b101101	4.10
0b101110	4.15
0b101111	4.20
0b110000	4.25
0b110001	4.30
0b110010	4.35
0b110011	4.40
0b110100	4.45
0b110101	4.50
0b110110	4.55
0b110111	4.60
0b111000	4.65
0b111001	4.70
0b111010	4.75
0b111011	4.80

TABLE 4. DCDOUT[5:0] VALUE vs OUTPUT VOLTAGE (Continued)

DCDOUT[5:0]	OUTPUT VOLTAGE (V)
0b111100	4.85
0b111101	4.90
0b111110	4.95
0b111111	5.00

TABLE 5. REGISTER ADDRESS 0x01: MODE CONTROL

BIT	NAME	TYPE	RESET	DESCRIPTION
2:0	SLEWRATE	R/W	000	Slew rate control (typical), expressed as µs per LSB change in DCDOUT value: 0b000 = 0.8µs/ΔLSB 0b001 = 1.6µs/ΔLSB 0b010 = 3.2µs/ΔLSB 0b011 = 6.4µs/ΔLSB 0b100 = 12.8µs/ΔLSB 0b101 = 25.6µs/ΔLSB 0b110 = 51.2µs/ΔLSB 0b111 = 102.4µs/ΔLSB
3	MODE	R/W	0	Mode control, 1 = Forced PWM 0 = Auto PFM/PWM
4	DISCHARGE	R/W	0	Soft discharge, 1 = Active, 0 = OFF
5	Bypass	R/W	0	Bypass entry: 1 = Disable Bypass mode, 0 = Enable Bypass mode
7:6	Reserved	R/W	00	

Applications Information

Component Selection

The ISL91128 requires only three external power components to implement the buck-boost converter: an inductor, an input capacitor, and an output capacitor.

Inductor Selection

Use an inductor with high frequency core material (for example, ferrite core) to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications in which radiated noise must be minimized, a toroidal or shielded inductor can be used (refer to Table 7).

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 2x10µF. The recommended V_{OUT} capacitor value is 2x22µF.

TABLE 6. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91128. The input and output capacitors should be positioned as close to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible, and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

TABLE 7. INDUCTOR VENDOR INFORMATION

MANUFACTURER	MANUFACTURER PART NUMBER	DESCRIPTION	DIMENSION (mm)	WEBSITE
Toko	1277AS-H-1R0M	1µH, 20%, DCR = 34mΩ (typical), I_{SAT} = 4.6A (typical)	3.2x2.5x1.2	www.toko.com
	FDSD0312-H-1R0M	1µH, 20%, DCR = 43mΩ (typical), I_{SAT} = 4.5A (typical)	3.2x3.0x1.2	
Coilcraft	XFL4020-102ME	1µH, 20%, DCR = 11mΩ (typical), I_{SAT} = 5.1A (typical)	4.0x4.0x2.1	www.coilcraft.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 3, 2018	FN8732.3	Added a test condition for Input Voltage Range on page 4. Removed About Intersil section and updated disclaimer.
Jul 7, 2017	FN8732.2	Table 4 on page 14, 0b111110 output voltage changed from 5.95 to 4.95.
Jun 15, 2017	FN8732.1	Updated Related Literature section on page 1. Updated Table 1 on page 3. - changed “VSEL” column to “Dynamic Voltage Scaling” and made ISL91128 parameter “Yes”. - removed “and DVS” from I2C column. Added ISL91128EVKIT1Z to ordering information table on page 3 Removed ISLUSBMINIEVAL1Z (dongle and cables) from ordering information table on page 3 - the kit includes the dongle and cables and they will not be offered as a stand-alone item.
Aug 3, 2016	FN8732.0	Initial release

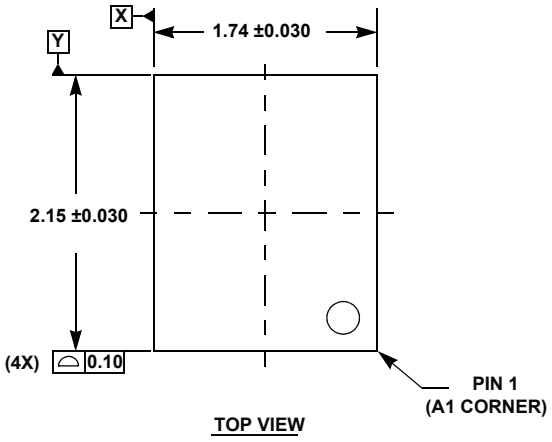
Package Outline Drawing

For the most recent package outline drawing, see W4x5.20M.

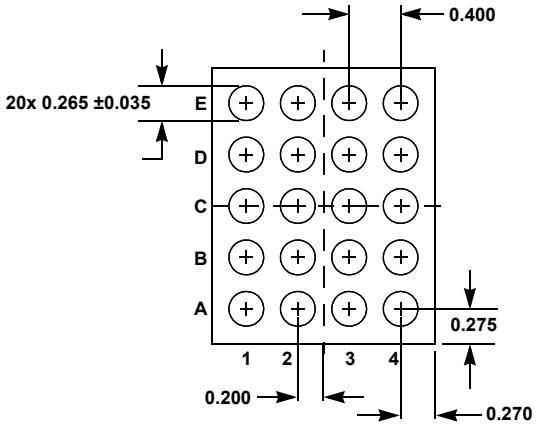
W4x5.20M

20 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm PITCH)

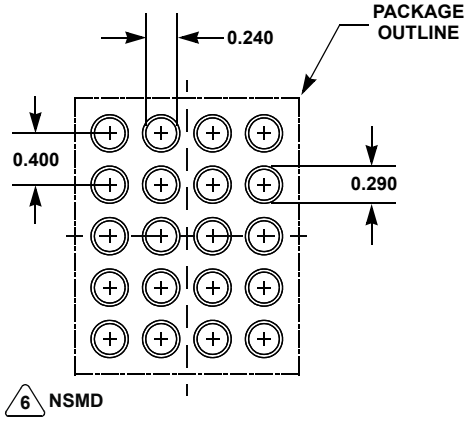
Rev 0, 01/15



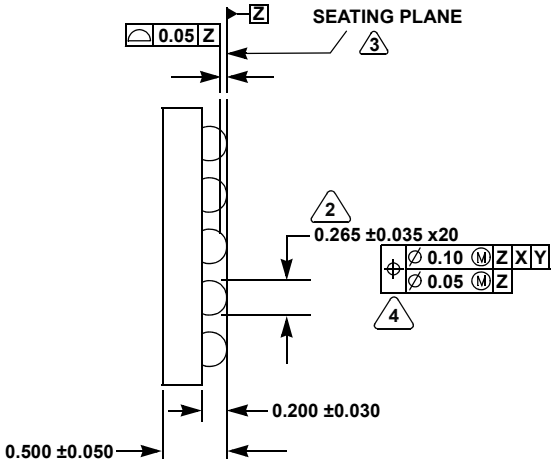
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

10. Dimensions and tolerance per ASMEY 14.5 - 1994.
11. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
12. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
13. Bump position designation per JESD 95-1, SPP-010.
14. All dimensions are in millimeters.
15. NSMD refers to non-solder mask defined pad design per TB451.

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