



**THE DATASHEET OF
NTB0102GT,115**



NTB0102

Dual supply translating transceiver; auto direction sensing; 3-state

Rev. 5.2 — 12 June 2023

Product data sheet

1 General description

The NTB0102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied with any voltage between 1.2 V and 3.6 V and $V_{CC(B)}$ can be supplied with any voltage between 1.65 V and 5.5 V. This flexibility makes the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V).

Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range:
 - $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
 - HBM JESD22-A114E Class 2 exceeds 2500 V for A port
 - HBM JESD22-A114E Class 3B exceeds 15000 V for B port
 - CDM JESD22-C101E exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTB0102DP	t02	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
NTB0102GT	t02	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
NTB0102GF	t2	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
NTB0102JK	t2	X2SON8	super thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.32 mm	SOT2015-1



3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method ^[1]	Minimum order quantity	Temperature
NTB0102DP	NTB0102DP,125	TSSOP8	REEL 7" Q3 NDP	3000	-40 °C to +125 °C
NTB0102GT	NTB0102GT,115	XSON8	REEL 7" Q1 NDP	5000	-40 °C to +125 °C
NTB0102GF	NTB0102GF,115	XSON8	REEL 7" Q1 NDP	5000	-40 °C to +125 °C
NTB0102JK	NTB0102JKZ	X2SON8	REEL 7" Q1 NDP SSB	6000	-40 °C to +125 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

4 Functional diagram

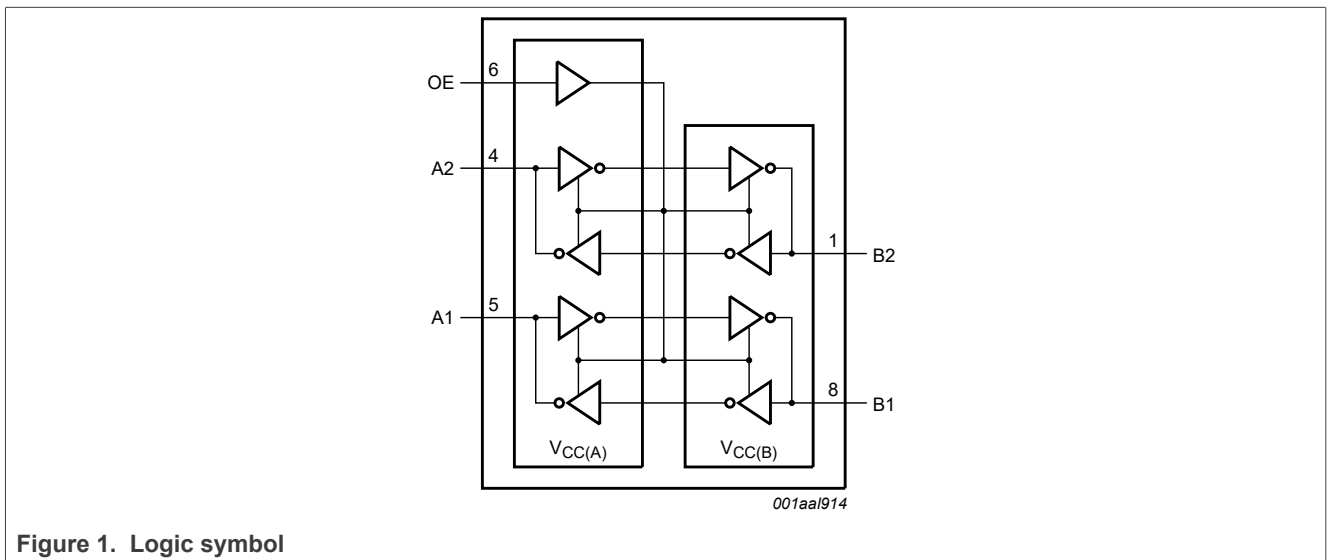
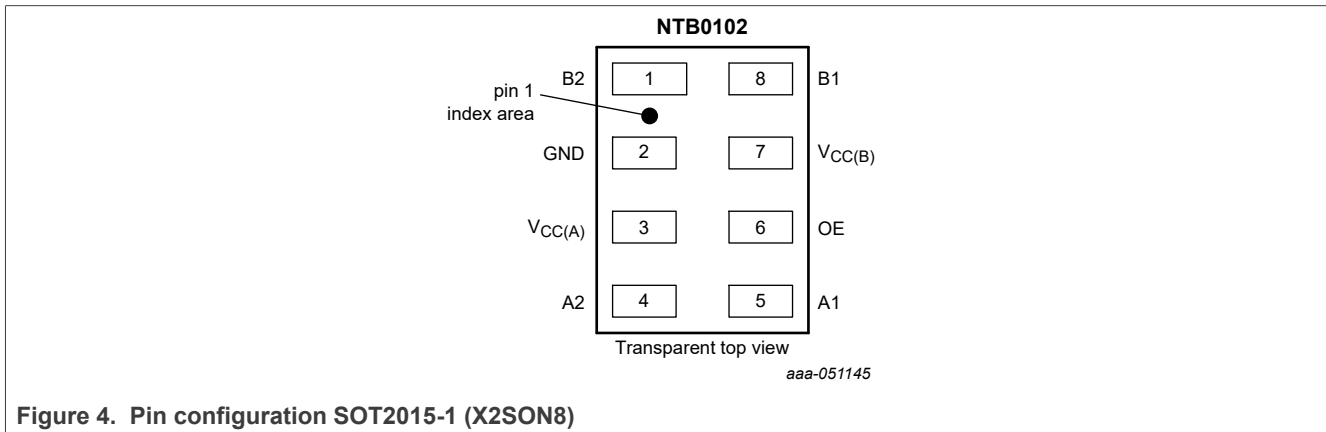
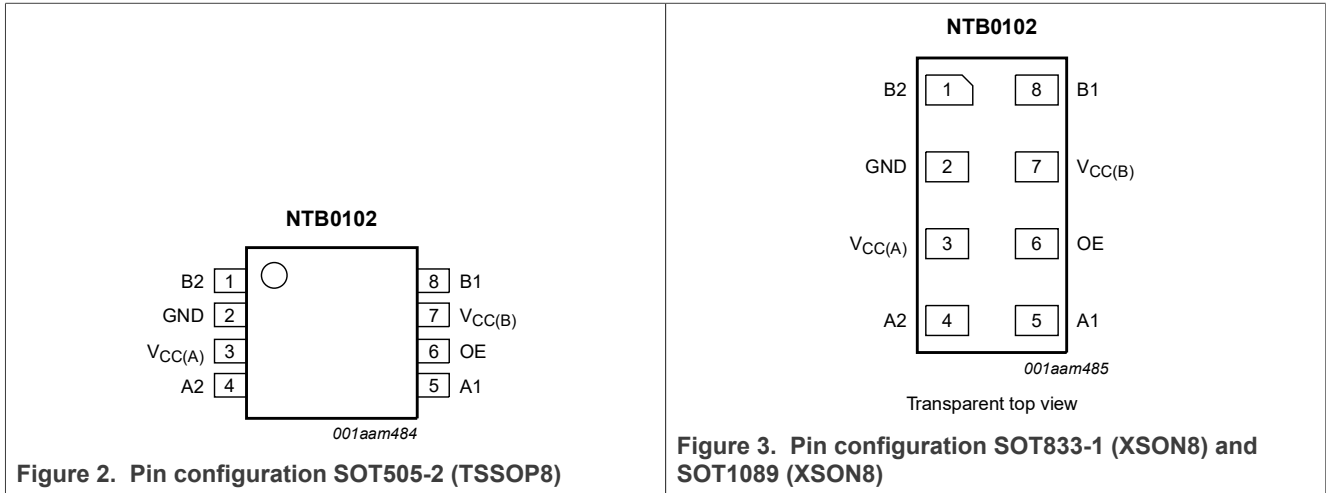


Figure 1. Logic symbol

5 Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	1, 8	data input or output (referenced to V _{CC(B)})
GND	2	ground (0 V)
V _{CC(A)}	3	supply voltage A
A2, A1	4, 5	data input or output (referenced to V _{CC(A)})
OE	6	output enable input (active HIGH; referenced to V _{CC(A)})
V _{CC(B)}	7	supply voltage B

6 Functional description

Table 4. Function table^[1]

Supply voltage		Input	Input/output	
V _{CC(A)}	V _{CC(B)}	OE	An	Bn
1.2 V to V _{CC(B)}	1.65 V to 5.5 V	L	Z	Z
1.2 V to V _{CC(B)}	1.65 V to 5.5 V	H	input or output	output or input
GND ^[2]	GND ^[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into Power-down mode.

7 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC(A)}	supply voltage A			-0.5	+6.5	V
V _{CC(B)}	supply voltage B			-0.5	+6.5	V
V _I	input voltage		^[1]	-0.5	+6.5	V
V _O	output voltage	Active mode	^{[1][2][3]}	-0.5	V _{CCO} + 0.5	V
		Power-down or 3-state mode	^[1]	-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
I _O	output current	V _O = 0 V to V _{CCO}	^[2]	-	±50	mA
I _{CC}	supply current	I _{CC(A)} or I _{CC(B)}		-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[4]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] V_{CCO} + 0.5 V should not exceed 6.5 V.

[4] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

8 Recommended operating conditions

Table 6. Recommended operating conditions^{[1][2]}

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC(A)}	supply voltage A			1.2	3.6	V
V _{CC(B)}	supply voltage B			1.65	5.5	V
V _I	input voltage			0	5.5	V

Dual supply translating transceiver; auto direction sensing; 3-state

Table 6. Recommended operating conditions^{[1][2]} ...continued

Symbol	Parameter	Conditions	Min	Max	Unit
V _O	output voltage	Power-down or 3-state mode; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V			
		A port	0	3.6	V
		B port	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCi} or both at GND.

[2] V_{CC(A)} must be less than or equal to V_{CC(B)}.

9 Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	A port; V _{CC(A)} = 1.2 V; I _O = -20 μA	-	1.1	-	V
V _{OL}	LOW-level output voltage	A port; V _{CC(A)} = 1.2 V; I _O = 20 μA	-	0.09	-	V
I _I	input leakage current	OE input; V _I = 0 V to 3.6 V; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	-	±1	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V to V _{CCO} ; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	[1]	-	±1	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0 V to 5.5 V	-	-	±1	μA
		B port; V _I or V _O = 0 V to 5.5 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0 V to 3.6 V	-	-	±1	μA
I _{CC}	supply current	V _I = 0 V or V _{CCi} ; I _O = 0 A	[2]			
		I _{CC(A)} ; V _{CC(A)} = 1.2 V; V _{CC(B)} = 1.65 V to 5.5 V	-	0.05	-	μA
		I _{CC(B)} ; V _{CC(A)} = 1.2 V; V _{CC(B)} = 1.65 V to 5.5 V	-	3.3	-	μA
		I _{CC(A)} + I _{CC(B)} ; V _{CC(A)} = 1.2 V; V _{CC(B)} = 1.65 V to 5.5 V	-	3.5	-	μA
C _I	input capacitance	OE input; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	1.0	-	pF
C _{I/O}	input/output capacitance	A port; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	4.0	-	pF
		B port; V _{CC(A)} = 1.2 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	7.5	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

[2] V_{CCi} is the supply voltage associated with the input.

Dual supply translating transceiver; auto direction sensing; 3-state

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
V_{OH}	HIGH-level output voltage	$I_O = -20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
V_{OL}	LOW-level output voltage	$I_O = 20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	-	0.4	-	0.4	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	0.4	-	0.4	V
I_I	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	± 2	-	± 5	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$ [2]	-	± 2	-	± 10	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 0\text{ V}; V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	± 2	-	± 10	μA
		B port; V_I or $V_O = 0\text{ V to }5.5\text{ V}; V_{CC(B)} = 0\text{ V}; V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	± 2	-	± 10	μA
I_{CC}	supply current	$V_I = 0\text{ V or }V_{CCI}; I_O = 0\text{ A}$ [1]					
		$I_{CC(A)}$ OE = LOW; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	3	-	15	μA

Table 9. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
		OE = HIGH; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	3	-	20	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	2	-	15	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-	-2	-	-15	μA
		I _{CC(B)}					
		OE = LOW; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	5	-	15	μA
		OE = HIGH; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	5	-	20	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	-2	-	-15	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-	2	-	15	μA
		I _{CC(A)} + I _{CC(B)}					
		V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	8	-	40	μA

[1] V_{CCI} is the supply voltage associated with the input.
 [2] V_{CCO} is the supply voltage associated with the output.

10 Dynamic characteristics

Table 10. Typical dynamic characteristics for temperature 25 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for waveforms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	V _{CC(B)}				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
V _{CC(A)} = 1.2 V; T _{amb} = 25 °C							
t _{pd}	propagation delay	A to B	5.9	4.8	4.4	4.2	ns
		B to A	5.6	4.8	4.5	4.4	ns
t _{en}	enable time	OE to A, B	0.5	0.5	0.5	0.5	μs
t _{dis}	disable time	OE to A; no external load	[2] 6.9	6.9	6.9	6.9	ns
		OE to B; no external load	[2] 9.5	8.6	8.5	8.0	ns
		OE to A	81	69	83	68	ns
		OE to B	81	69	83	68	ns
t _t	transition time	A port	4.0	4.0	4.1	4.1	ns
		B port	2.6	2.0	1.7	1.4	ns
t _{sk(o)}	output skew time	between channels	[3] 0.2	0.2	0.2	0.2	ns
t _W	pulse width	data inputs	15	13	13	13	ns
f _{data}	data rate		70	80	80	80	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}

Dual supply translating transceiver; auto direction sensing; 3-state

- [2] Delay between OE going LOW and when the outputs are actually disabled.
- [3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1 V											
t _{pd}	propagation delay	A to B	1.4	12.9	1.2	10.1	1.1	10.0	0.8	9.9	ns
		B to A	0.9	14.2	0.7	12.0	0.4	11.7	0.3	13.7	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	11.9	1.0	11.9	1.0	11.9	1.0	11.9	ns
		OE to B; no external load ^[2]	1.0	16.9	1.0	15.2	1.0	14.1	1.0	13.8	ns
		OE to A	-	320	-	260	-	260	-	280	ns
		OE to B	-	200	-	200	-	200	-	200	ns
t _t	transition time	A port	0.9	5.1	0.9	5.1	0.9	5.1	0.9	5.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t _{sk(o)}	output skew time	between channels ^[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t _W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f _{data}	data rate		-	40	-	40	-	40	-	40	Mbps
V_{CC(A)} = 1.8 V ± 0.15 V											
t _{pd}	propagation delay	A to B	1.6	11.0	1.4	7.7	1.3	6.8	1.2	6.5	ns
		B to A	1.5	12.0	1.3	8.4	1.0	7.6	0.9	7.1	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	11.0	1.0	11.0	1.0	11.0	1.0	11.0	ns
		OE to B; no external load ^[2]	1.0	15.4	1.0	13.5	1.0	12.4	1.0	12.1	ns
		OE to A	-	260	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	-	200	ns
t _t	transition time	A port	0.8	4.1	0.8	4.1	0.8	4.1	0.8	4.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t _{sk(o)}	output skew time	between channels ^[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t _W	pulse width	data inputs	20	-	17	-	17	-	17	-	ns
f _{data}	data rate		-	49	-	60	-	60	-	60	Mbps
V_{CC(A)} = 2.5 V ± 0.2 V											
t _{pd}	propagation delay	A to B	-	-	1.1	6.3	1.0	5.2	0.9	4.7	ns
		B to A	-	-	1.2	6.6	1.1	5.1	0.9	4.4	ns

Dual supply translating transceiver; auto direction sensing; 3-state

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	V _{CC(B)}								Unit	
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max		
t _{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	μs	
t _{dis}	disable time	OE to A; no external load	^[2]	-	-	1.0	9.2	1.0	9.2	1.0	9.2	ns
		OE to B; no external load	^[2]	-	-	1.0	11.9	1.0	10.7	1.0	10.2	ns
		OE to A		-	-	-	200	-	200	-	200	ns
		OE to B		-	-	-	200	-	200	-	200	ns
t _t	transition time	A port		-	-	0.7	3.0	0.7	3.0	0.7	3.0	ns
		B port		-	-	0.7	3.2	0.5	2.5	0.4	2.7	ns
t _{sk(o)}	output skew time	between channels	^[3]	-	-	-	0.5	-	0.5	-	0.5	ns
t _W	pulse width	data inputs		-	-	12	-	10	-	10	-	ns
f _{data}	data rate			-	-	-	85	-	100	-	100	Mbps
V_{CC(A)} = 3.3 V ± 0.3 V												
t _{pd}	propagation delay	A to B		-	-	-	-	0.9	4.7	0.8	4.0	ns
		B to A		-	-	-	-	1.0	4.9	0.9	3.8	ns
t _{en}	enable time	OE to A, B		-	-	-	-	-	1.0	-	1.0	μs
t _{dis}	disable time	OE to A; no external load	^[2]	-	-	-	-	1.0	9.2	1.0	9.2	ns
		OE to B; no external load	^[2]	-	-	-	-	1.0	10.1	1.0	9.6	ns
		OE to A		-	-	-	-	-	260	-	260	ns
		OE to B		-	-	-	-	-	200	-	200	ns
t _t	transition time	A port		-	-	-	-	0.7	2.5	0.7	2.5	ns
		B port		-	-	-	-	0.5	2.5	0.4	2.7	ns
t _{sk(o)}	output skew time	between channels	^[3]	-	-	-	-	-	0.5	-	0.5	ns
t _W	pulse width	data inputs		-	-	-	-	10	-	10	-	ns
f _{data}	data rate			-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}

[2] Delay between OE going LOW and when the outputs are actually disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

Dual supply translating transceiver; auto direction sensing; 3-state

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}								Unit	
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC(A)} = 1.5 V ± 0.1 V												
t _{pd}	propagation delay	A to B	1.4	15.9	1.2	13.1	1.1	13.0	0.8	12.9	ns	
		B to A	0.9	17.2	0.7	15.0	0.4	14.7	0.3	16.7	ns	
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs	
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	12.5	1.0	12.5	1.0	12.5	1.0	12.5	ns	
		OE to B; no external load ^[2]	1.0	18.1	1.0	16.2	1.0	14.9	1.0	14.6	ns	
		OE to A	-	340	-	280	-	280	-	300	ns	
		OE to B	-	220	-	220	-	220	-	220	ns	
t _t	transition time	A port	0.9	7.1	0.9	7.1	0.9	7.1	0.9	7.1	ns	
		B port	0.9	6.5	0.6	5.2	0.5	4.8	0.4	4.7	ns	
t _{sk(o)}	output skew time	between channels ^[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns	
t _W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns	
f _{data}	data rate		-	40	-	40	-	40	-	40	Mbps	
V_{CC(A)} = 1.8 V ± 0.15 V												
t _{pd}	propagation delay	A to B	1.6	14.0	1.4	10.7	1.3	9.8	1.2	9.5	ns	
		B to A	1.5	15.0	1.3	11.4	1.0	10.6	0.9	10.1	ns	
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs	
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	11.5	1.0	11.5	1.0	11.5	1.0	11.5	ns	
		OE to B; no external load ^[2]	1.0	16.5	1.0	14.5	1.0	13.3	1.0	12.7	ns	
		OE to A	-	280	-	250	-	250	-	250	ns	
		OE to B	-	220	-	220	-	220	-	220	ns	
t _t	transition time	A port	0.8	6.2	0.8	6.1	0.8	6.1	0.8	6.1	ns	
		B port	0.9	5.8	0.6	5.2	0.5	4.8	0.4	4.7	ns	
t _{sk(o)}	output skew time	between channels ^[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns	
t _W	pulse width	data inputs	22	-	19	-	19	-	19	-	ns	
f _{data}	data rate		-	45	-	55	-	55	-	55	Mbps	
V_{CC(A)} = 2.5 V ± 0.2 V												
t _{pd}	propagation delay	A to B	-	-	1.1	9.3	1.0	8.2	0.9	7.7	ns	
		B to A	-	-	1.2	9.6	1.1	8.1	0.9	7.4	ns	
t _{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	µs	
t _{dis}	disable time	OE to A; no external load ^[2]	-	-	1.0	9.6	1.0	9.6	1.0	9.6	ns	

Dual supply translating transceiver; auto direction sensing; 3-state

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	V _{CC(B)}								Unit	
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max	Min	Max		
		OE to B; no external load	[2]	-	-	1.0	12.6	1.0	11.4	1.0	10.8	ns
		OE to A		-	-	-	220	-	220	-	220	ns
		OE to B		-	-	-	220	-	220	-	220	ns
t _t	transition time	A port		-	-	0.7	5.0	0.7	5.0	0.7	5.0	ns
		B port		-	-	0.7	4.6	0.5	4.8	0.4	4.7	ns
t _{sk(o)}	output skew time	between channels	[3]	-	-	-	0.5	-	0.5	-	0.5	ns
t _W	pulse width	data inputs;		-	-	14	-	13	-	10	-	ns
f _{data}	data rate			-	-	-	75	-	80	-	100	Mbps
V_{CC(A)} = 3.3 V ± 0.3 V												
t _{pd}	propagation delay	A to B		-	-	-	-	0.9	7.7	0.8	7.0	ns
		B to A		-	-	-	-	1.0	7.9	0.9	6.8	ns
t _{en}	enable time	OE to A, B		-	-	-	-	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load	[2]	-	-	-	-	1.0	9.5	1.0	9.5	ns
		OE to B; no external load	[2]	-	-	-	-	1.0	10.7	1.0	9.6	ns
		OE to A		-	-	-	-	-	280	-	280	ns
		OE to B		-	-	-	-	-	220	-	220	ns
t _t	transition time	A port		-	-	-	-	0.7	4.5	0.7	4.5	ns
		B port		-	-	-	-	0.5	4.1	0.4	4.7	ns
t _{sk(o)}	output skew time	between channels	[3]	-	-	-	-	-	0.5	-	0.5	ns
t _W	pulse width	data inputs		-	-	-	-	10	-	10	-	ns
f _{data}	data rate			-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}

[2] Delay between OE going LOW and when the outputs are actually disabled.

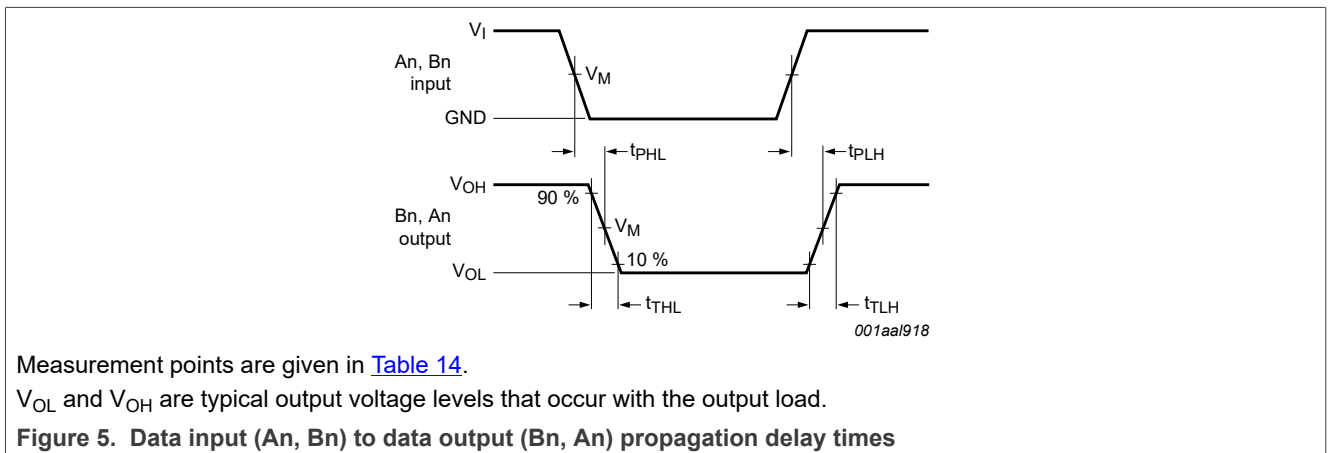
[3] Skew between any two outputs of the same package switching in the same direction.

Table 13. Typical power dissipation capacitance
 Voltages are referenced to GND (ground = 0 V).^{[1][2]}

Symbol	Parameter	Conditions	V _{CC(A)}								Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
			V _{CC(B)}								
			1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V		
T _{amb} = 25 °C											
C _{PD}	power dissipation capacitance	outputs enabled; OE = V _{CC(A)}									
		A port: (direction A to B)	5	5	5	5	5	5	5	5	pF
		A port: (direction B to A)	8	8	8	8	8	8	8	8	pF
		B port: (direction A to B)	18	18	18	18	18	18	18	18	pF
		B port: (direction B to A)	13	16	12	12	12	12	13	13	pF
		outputs disabled; OE = GND									
		A port: (direction A to B)	0.12	0.12	0.04	0.05	0.08	0.08	0.07	0.07	pF
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction A to B)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
B port: (direction B to A)	0.07	0.09	0.07	0.07	0.05	0.09	0.09	0.09	pF		

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
 [2] f_i = 10 MHz; V_I = GND to V_{CC}; t_r = t_f = 1 ns; C_L = 0 pF; R_L = ∞ Ω.

11 Waveforms



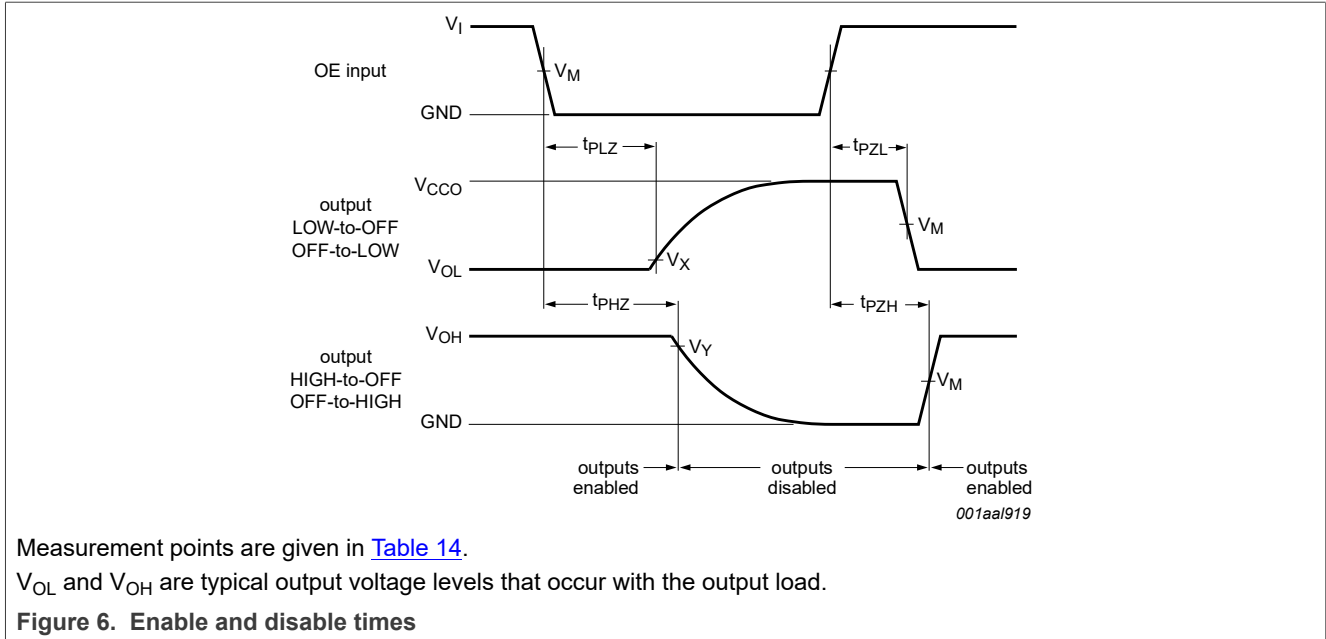


Table 14. Measurement points^[1]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.5 V \pm 0.1 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.8 V \pm 0.15 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$2.5 V \pm 0.2 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$3.3 V \pm 0.3 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$5.0 V \pm 0.5 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1] V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

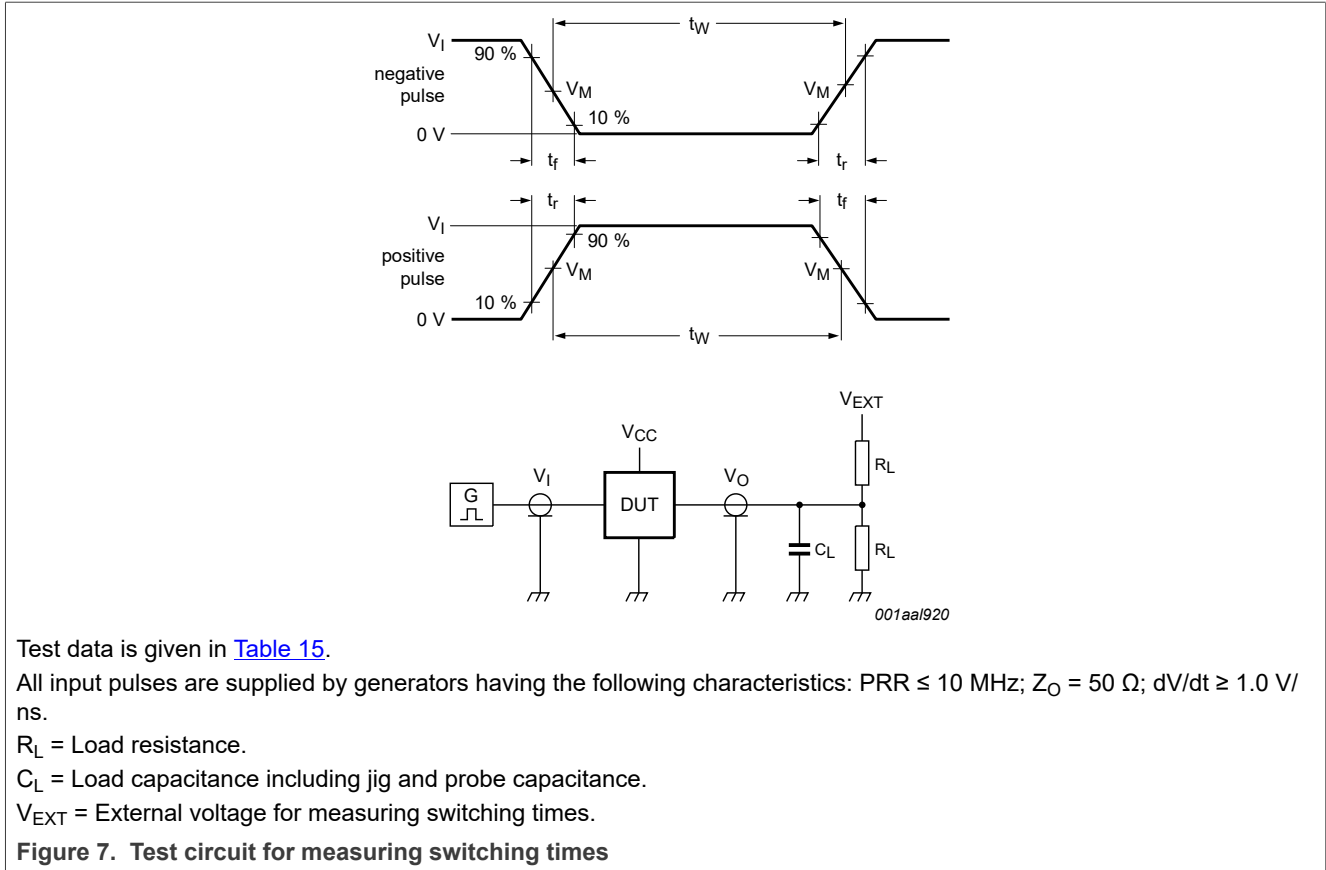


Table 15. Test data

Supply voltage		Input		Load		V _{EXT}		
V _{CC(A)}	V _{CC(B)}	V _I ^[1]	Δt/ΔV	C _L	R _L ^[2]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ} ^[3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V _{CCO}

[1] V_{CCI} is the supply voltage associated with the input.
 [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.
 [3] V_{CCO} is the supply voltage associated with the output.

12 Application information

12.1 Applications

Voltage level-translation applications. The NTB0102 can be used to interface between devices or systems operating at different supply voltages. See [Figure 8](#) for a typical operating circuit using the NTB0102.

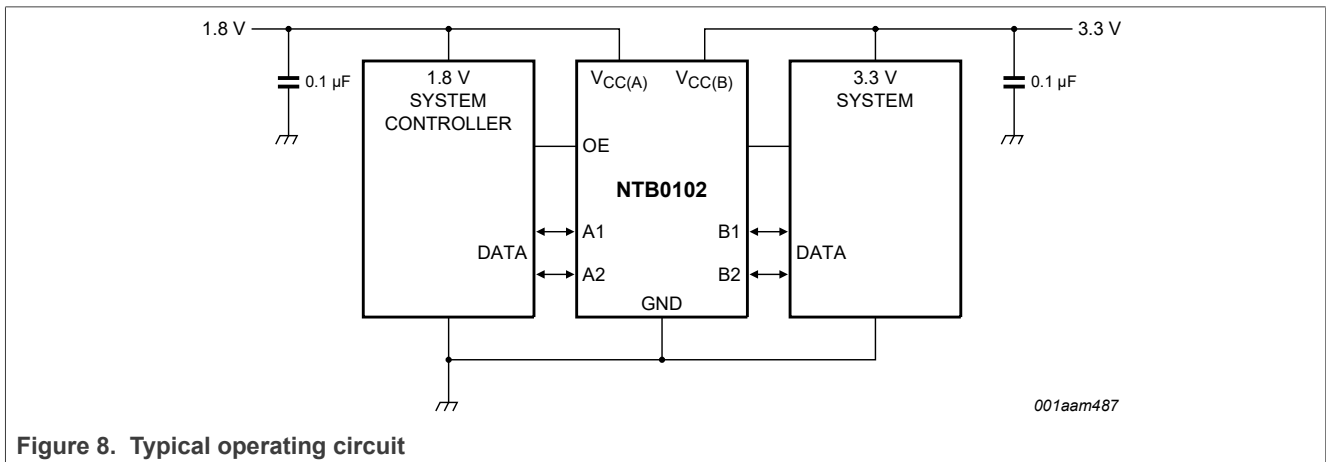


Figure 8. Typical operating circuit

12.2 Architecture

The architecture of the NTB0102 is shown in [Figure 9](#). The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of NTB0102 can maintain a defined output level, however, the output architecture is designed to be weak. This design enables an external driver to override the drivers when data on the bus starts flowing in the opposite direction. The output of one-shot circuits detect rising or falling edges on the A or B ports. During a rising edge, the one-shot circuits turn on the PMOS transistors (T1, T3) for a short duration, accelerating the LOW-to-HIGH transition. Similarly, during a falling edge, the one-shot circuits turn on the NMOS transistors (T2, T4) for a short duration, accelerating the HIGH-to-LOW transition. During output transitions, the typical output impedance is 70 Ω at $V_{CCO} = 1.2\text{ V to }1.8\text{ V}$, 50 Ω at $V_{CCO} = 1.8\text{ V to }3.3\text{ V}$ and 40 Ω at $V_{CCO} = 3.3\text{ V to }5.0\text{ V}$.

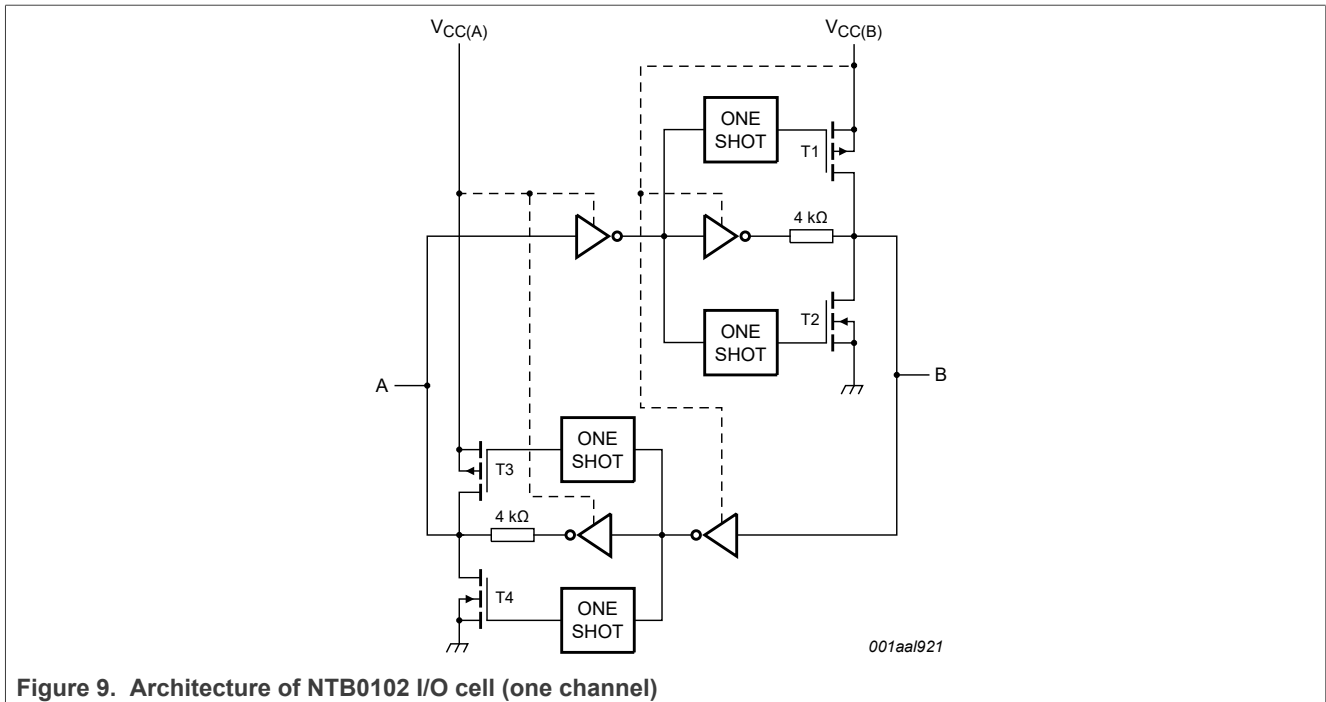


Figure 9. Architecture of NTB0102 I/O cell (one channel)

12.3 Input driver requirements

For correct operation, the device driving the data I/Os of the NTB0102 must have a minimum drive capability of ± 2 mA. See Figure 10 for a plot of typical input current versus input voltage.

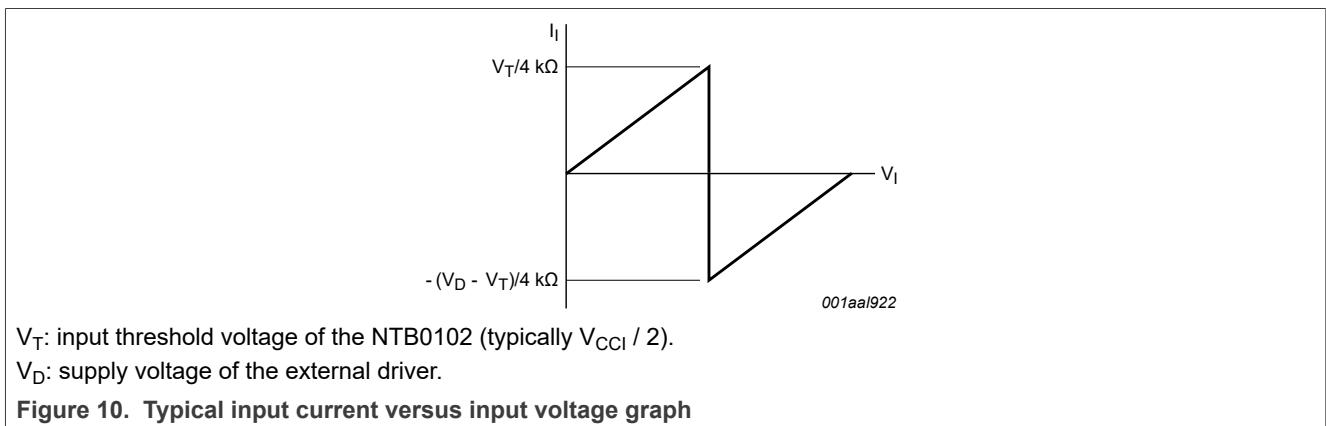


Figure 10. Typical input current versus input voltage graph

12.4 Power-up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$. However, during power-up, $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTB0102 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

12.5 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE

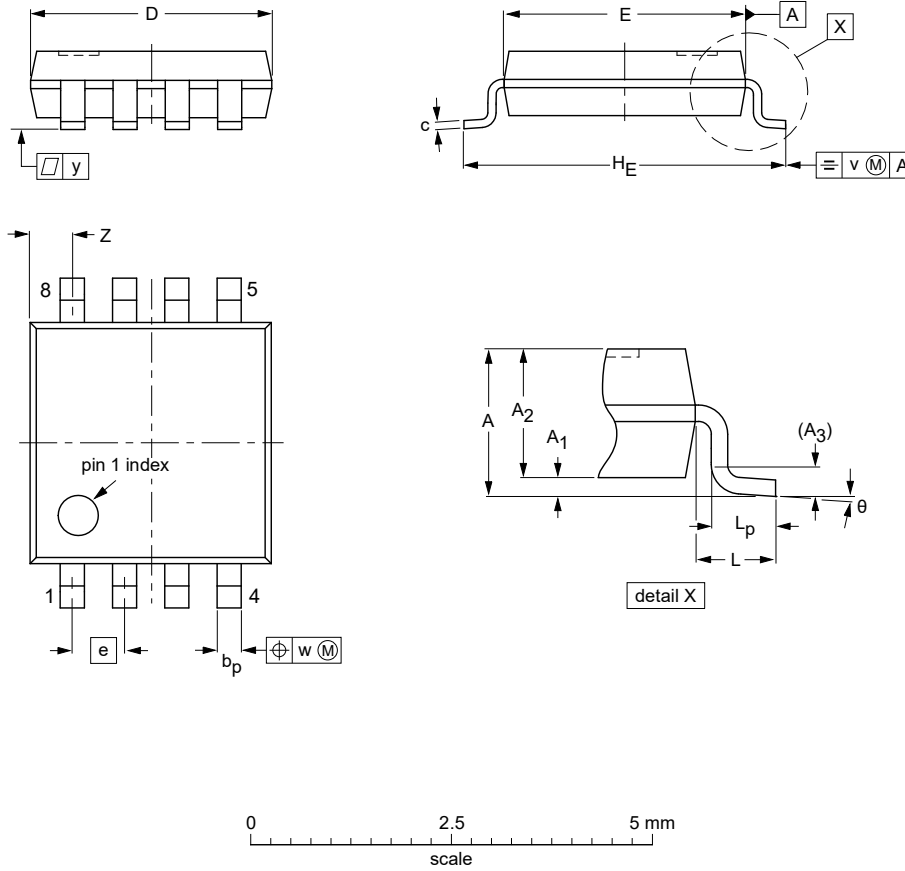
goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time that must be allowed for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

12.6 Pull-up or pull-down resistors on I/O lines

As mentioned previously the NTB0102 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be above 50 k Ω . For this reason, the NTB0102 is not recommended for use in open-drain driver applications such as 1-Wire or I²C-bus. For these applications, the NTS0102-Q100 level translator is recommended.

13 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

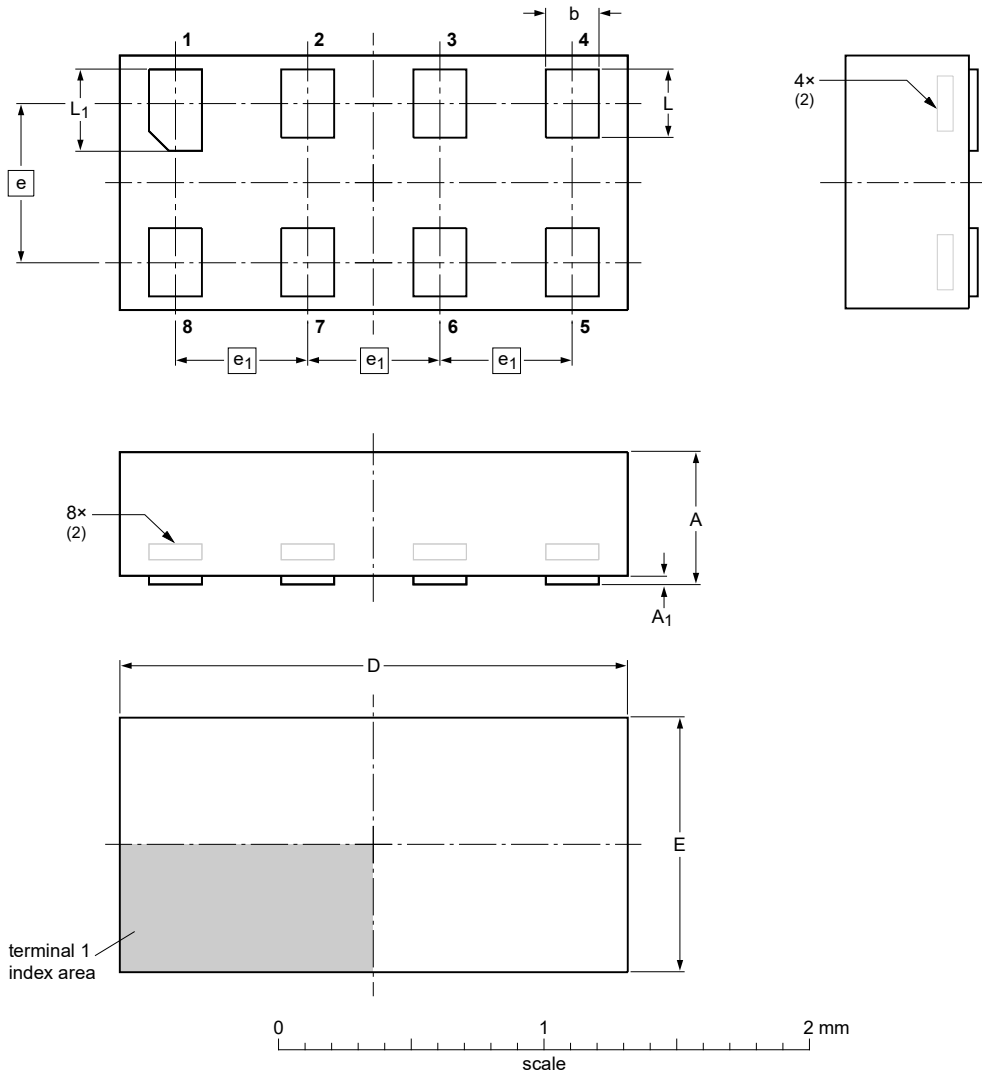
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT505-2		---			02-01-16

Figure 11. Package outline SOT505-2 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		07-11-14 07-12-07

Figure 12. Package outline SOT833-1 (XSON8)

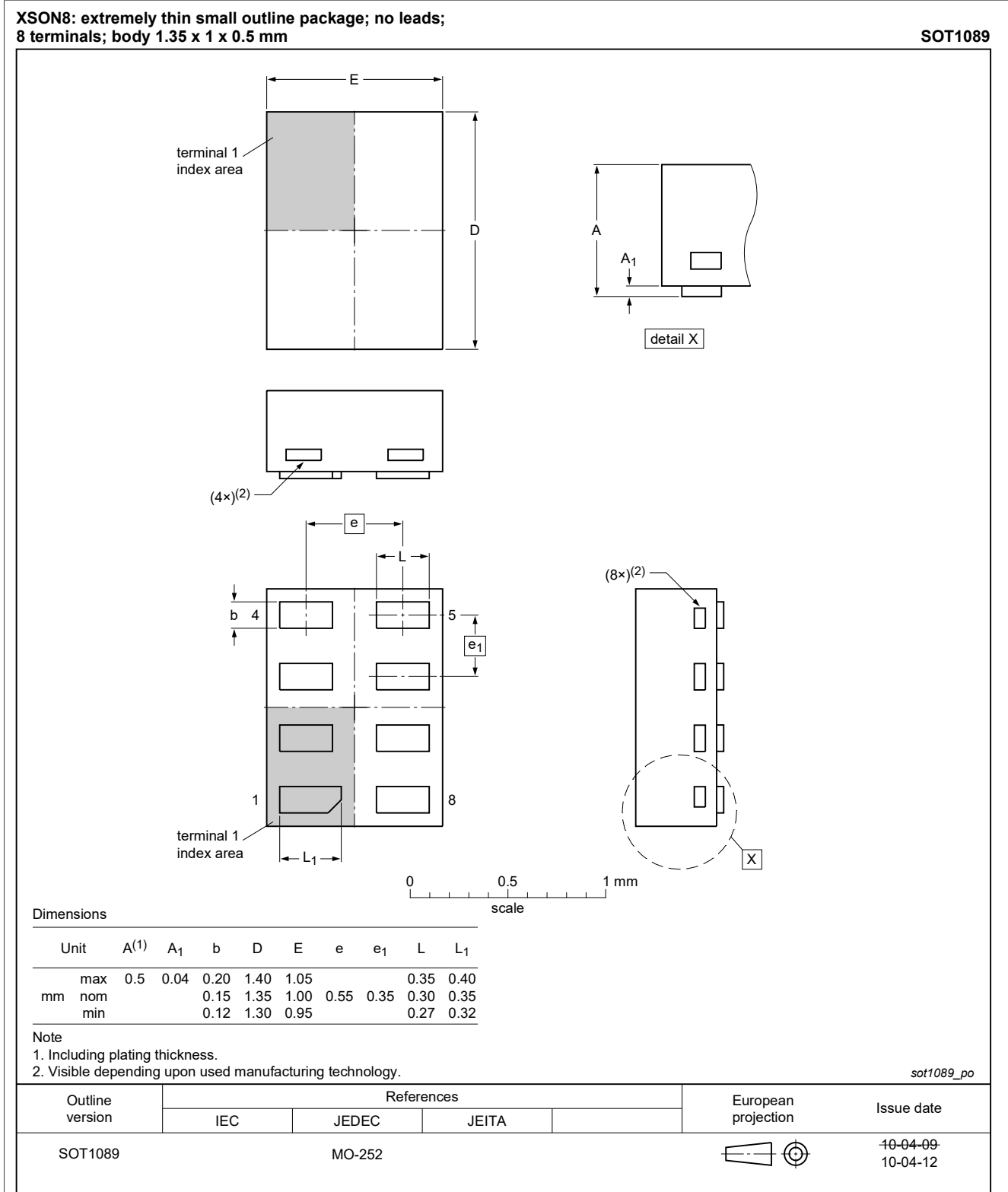


Figure 13. Package outline SOT1089 (XSON8)

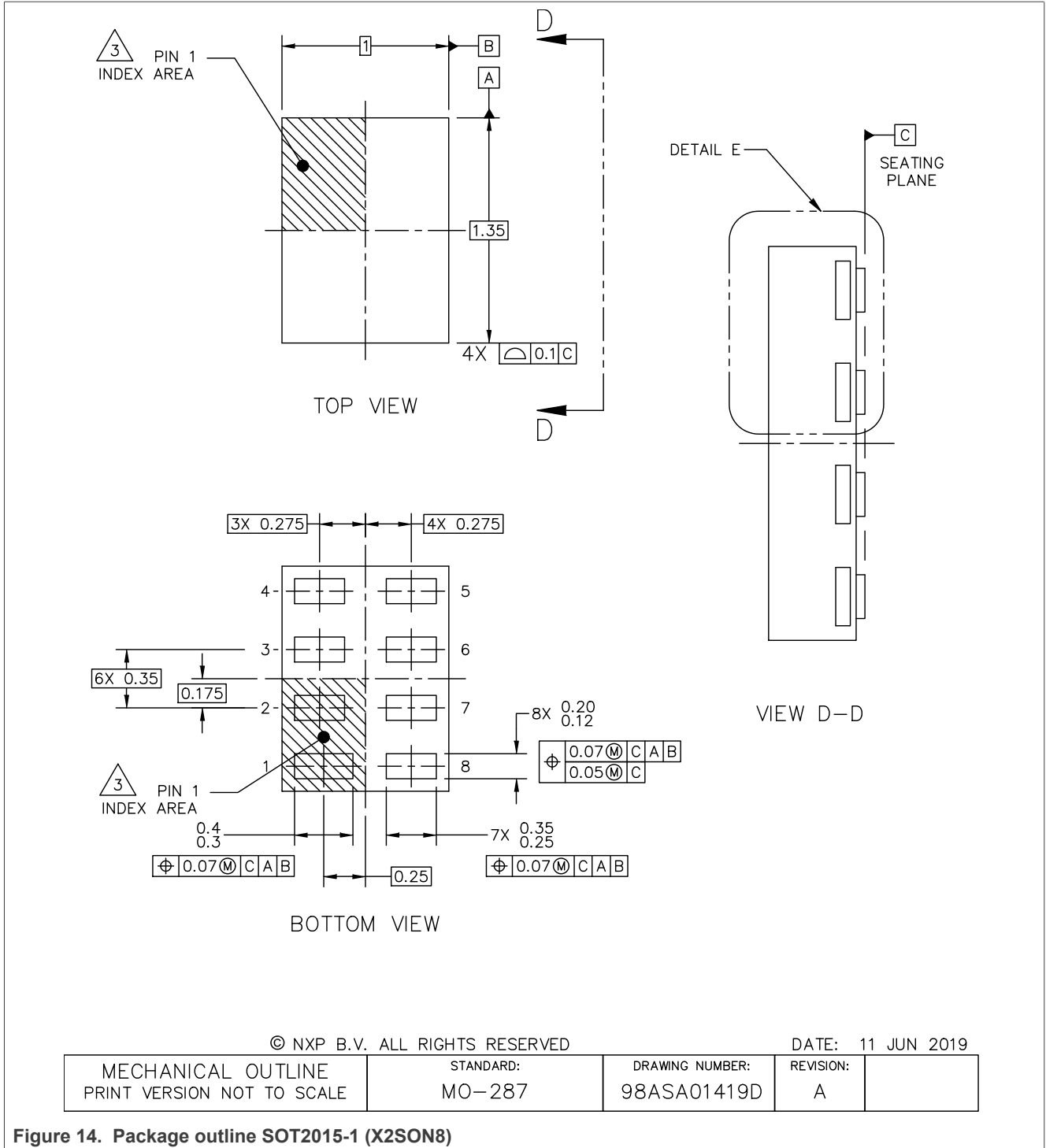


Figure 14. Package outline SOT2015-1 (X2SON8)

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#) and [Table 17](#)

Table 16. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).

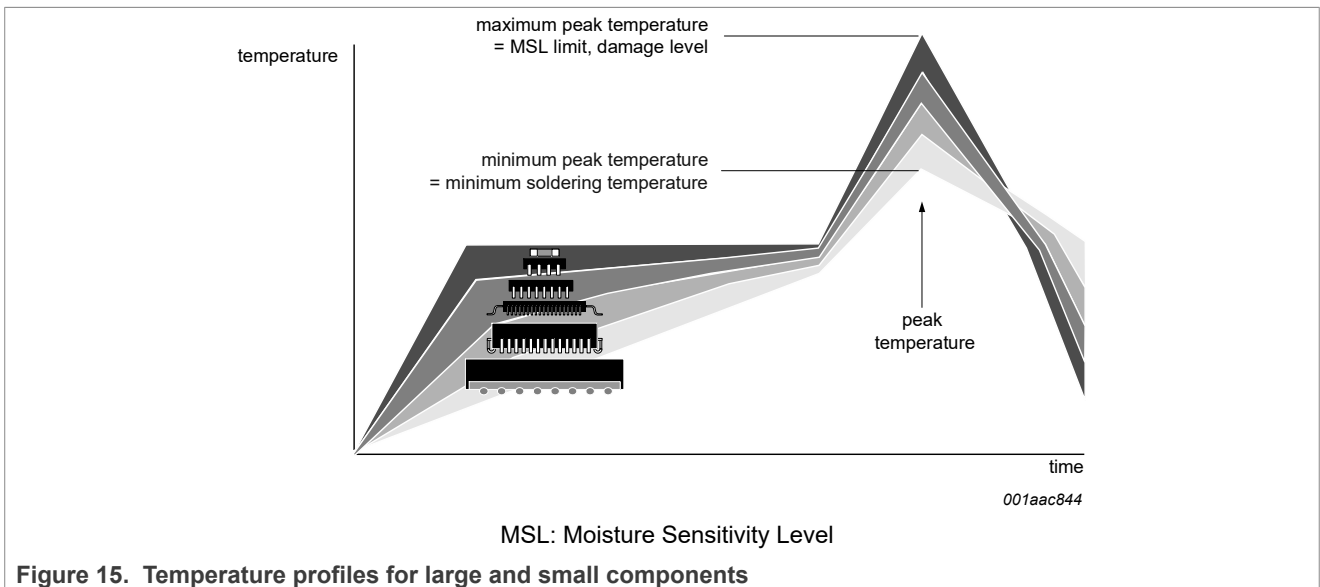


Figure 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15 Soldering: PCB footprints

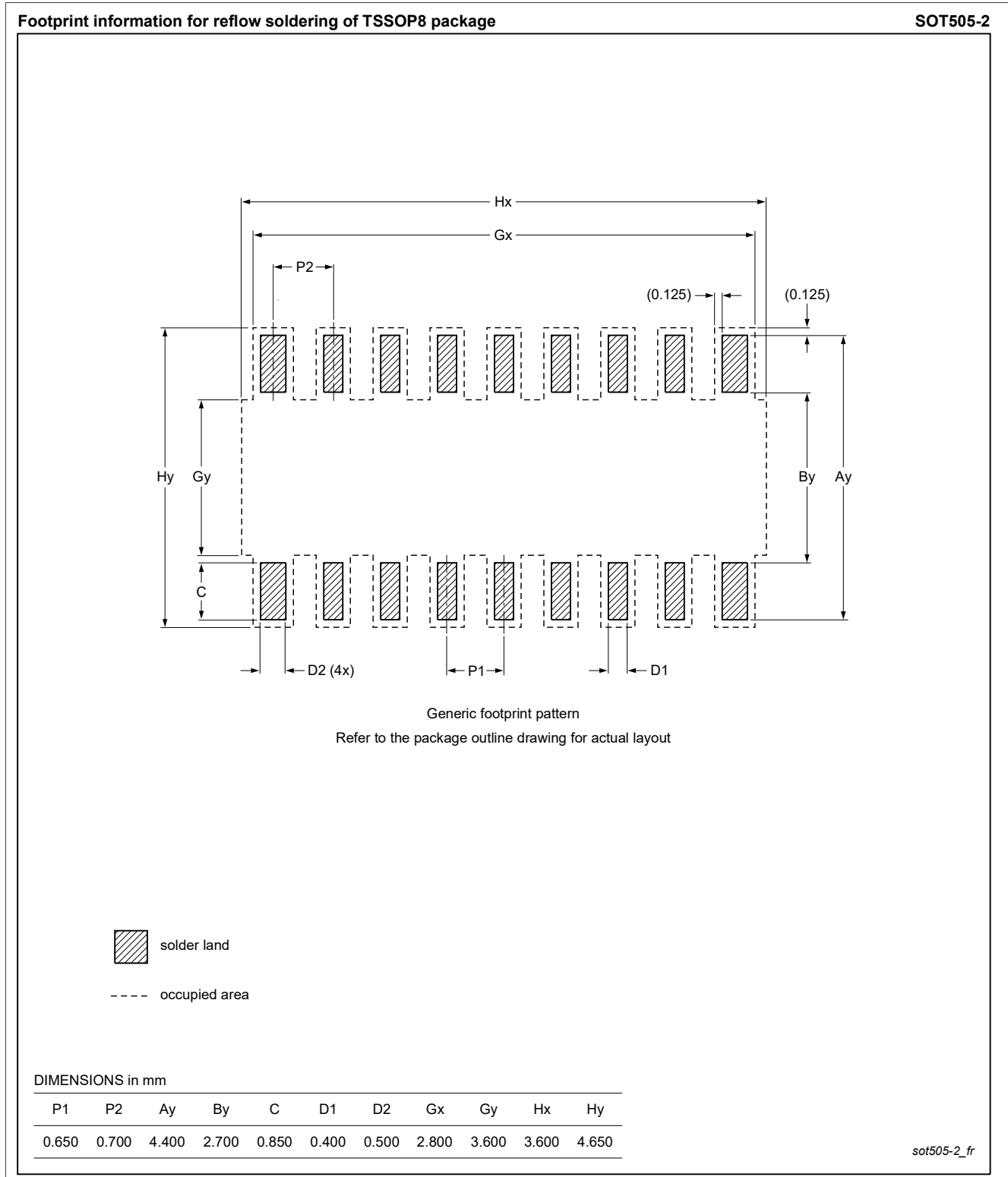
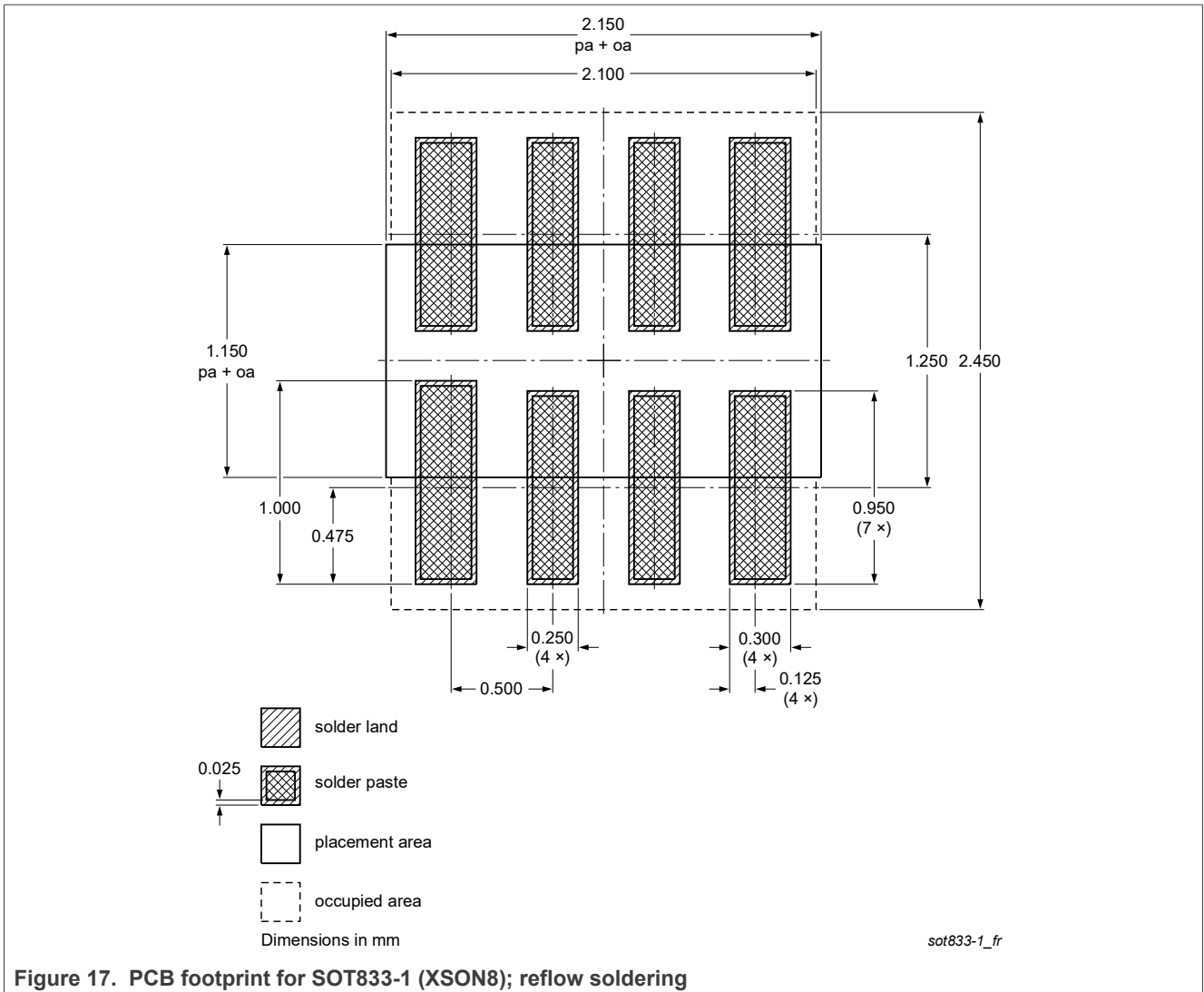
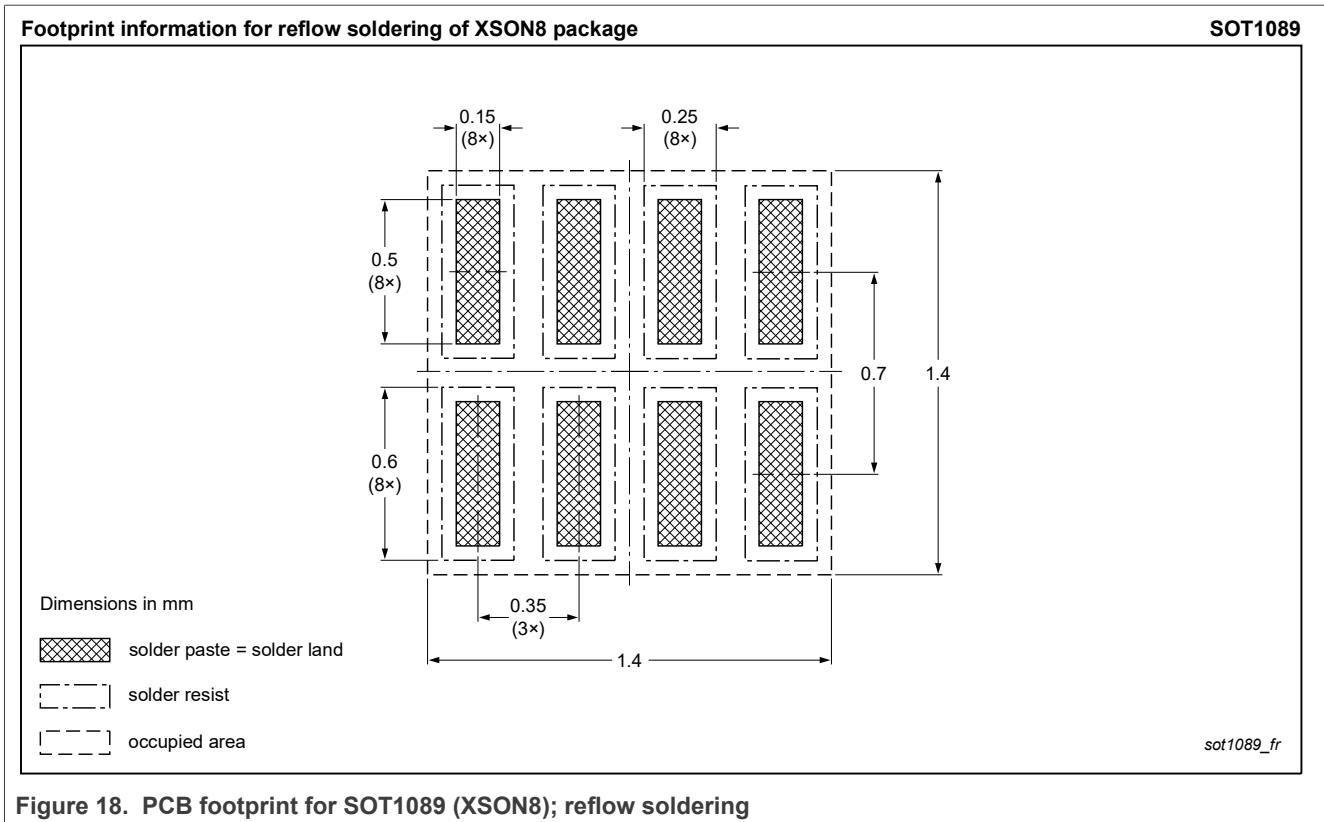
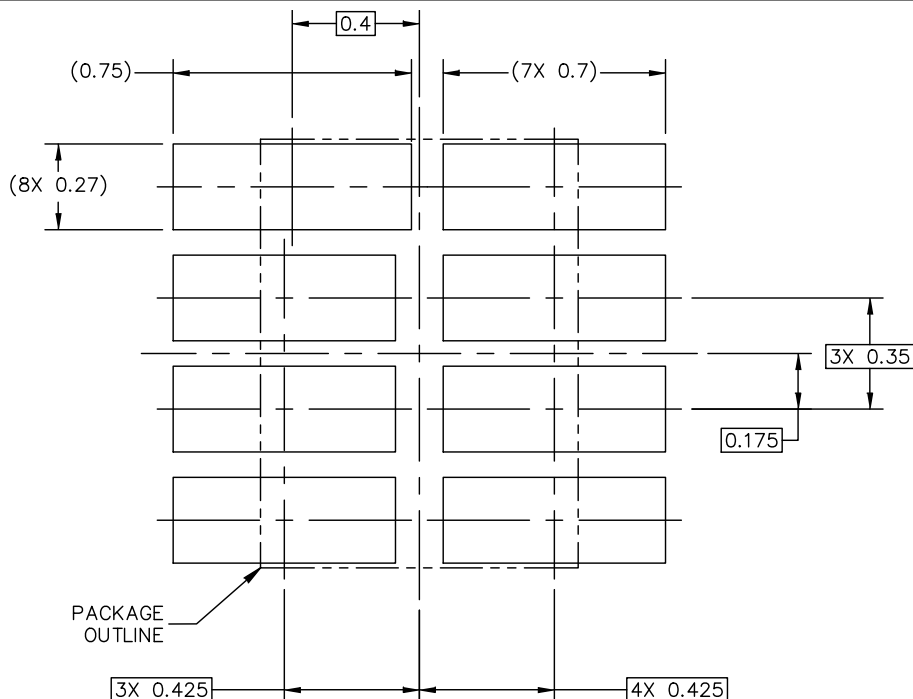


Figure 16. PCB footprint for SOT505-2 (TSSOP8); reflow soldering







PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

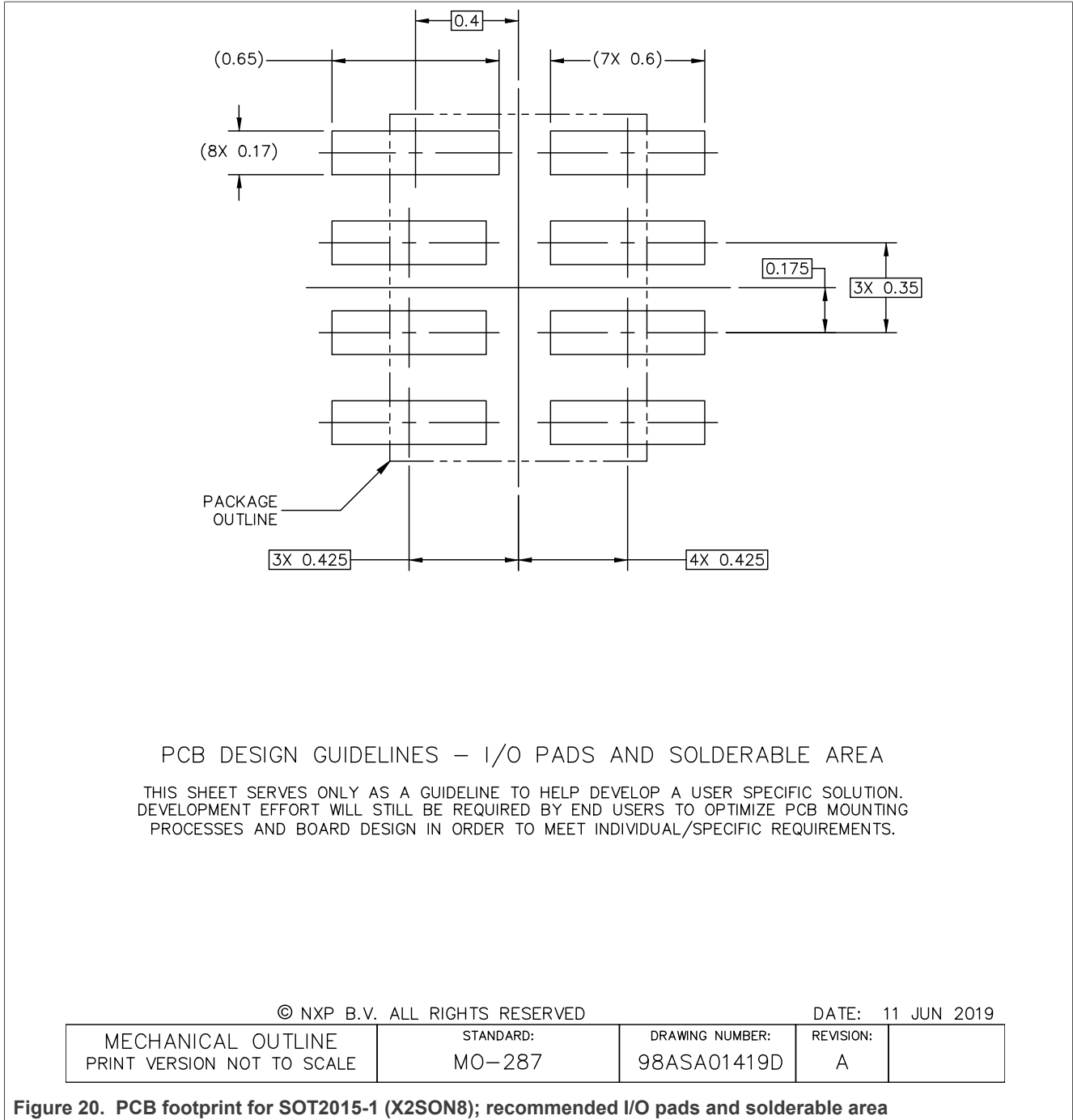
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 11 JUN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-287	DRAWING NUMBER: 98ASA01419D	REVISION: A	
--	---------------------	--------------------------------	----------------	--

Figure 19. PCB footprint for SOT2015-1 (X2SON8); recommended solder mask opening pattern



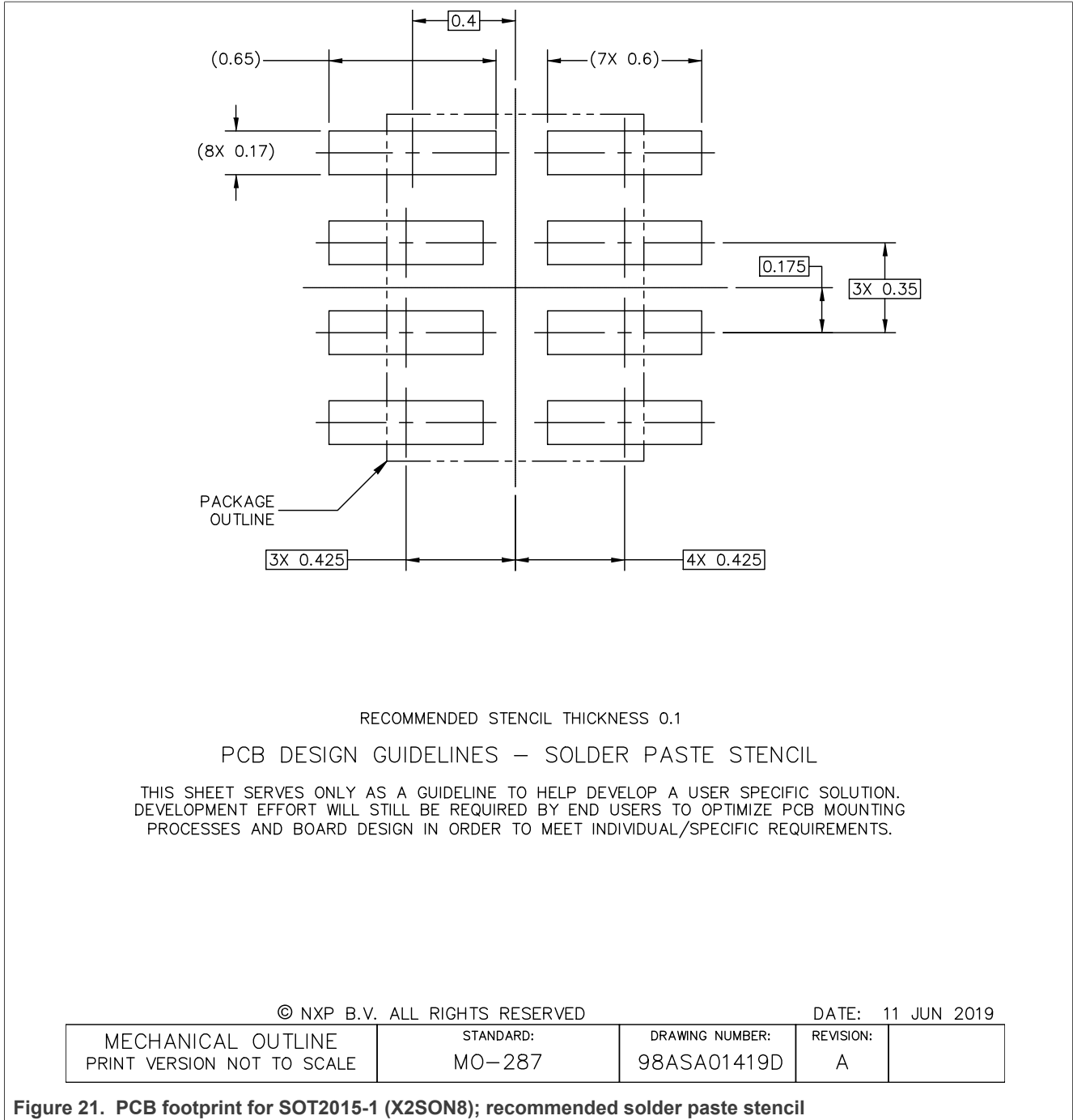


Figure 21. PCB footprint for SOT2015-1 (X2SON8); recommended solder paste stencil

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.
5. MIN METAL GAP SHOULD BE 0.15 MM.

© NXP B.V. ALL RIGHTS RESERVED		DATE: 11 JUN 2019		
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-287	DRAWING NUMBER: 98ASA01419D	REVISION: A	

Figure 22. PCB footprint for SOT2015-1 (X2SON8); notes

16 Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

Table 18. Abbreviations...continued

Acronym	Description
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PRR	Pulse Repetition Rate

17 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTB0102 v.5.2	20230612	Product data sheet	-	NTB0102 v.5.1
Modifications:	<ul style="list-style-type: none"> Corrected topside mark for NTB0102JK 			
NTB0102 v.5.1	20230602	Product data sheet	-	NTB0102 v.5
NTB0102 v.5	20220420	Product data sheet	-	NTB0102 v.4
NTB0102 v.4	20130123	Product data sheet	-	NTB0102 v.3
NTB0102 v.3	20111110	Product data sheet	-	NTB0102 v.2
NTB0102 v.2	20110428	Product data sheet	-	NTB0102 v.1
NTB0102 v.1	20100922	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

18.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

18.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
3.1	Ordering options	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	7
11	Waveforms	12
12	Application information	15
12.1	Applications	15
12.2	Architecture	15
12.3	Input driver requirements	16
12.4	Power-up	16
12.5	Enable and disable	16
12.6	Pull-up or pull-down resistors on I/O lines	17
13	Package outline	18
14	Soldering of SMD packages	22
14.1	Introduction to soldering	22
14.2	Wave and reflow soldering	22
14.3	Wave soldering	22
14.4	Reflow soldering	22
15	Soldering: PCB footprints	24
16	Abbreviations	30
17	Revision history	31
18	Legal information	32

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- [⊖ View NTB0102GT,115 on WIN SOURCE](#)
- [⊖ NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management