THE DATASHEET OF

VSC7420XJQ-02

www.win-source.net 0086-755-83957316

VSC7420-02, VSC7421-02, and VSC7422-02 Datasheet
Family of Gigabit Ethernet Switches

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1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.3

Revision 4.3 of this datasheet was published in January 2019. The following is a summary of the changes implemented in the datasheet:

- Frame Arrival section was updated. For more information, see Frame Arrival, page 6.
- MIIM Interface in Slave Mode section was updated with a note. For more information, see MIIM Interface in Slave Mode, page 104.
- VeriPHY™ Cable Diagnostics section was updated. For more information, see VeriPHY™ Cable Diagnostics, page 32.
- VeriPHY control registers were deleted. For more information, see PHY:PHY_EXT1, page 403.

1.2 Revision 4.2

Revision 4.2 of this datasheet was published in July 2018. In revision 4.2 of the document, a ball-grid array (BGA) package option of the device was added. The following is a summary of the additions to the datasheet.

- Pin information for the BGA package device was added. For more information, see Pin Descriptions for VSC7420XJQ-02, page 437, Pin Descriptions for VSC7421XJQ-02, page 486, and Pin Descriptions for VSC7422XJQ-02, page 537.
- BGA package outline drawing was added. For more information, see Package Drawing, page 585.
- Thermal specifications for the BGA package was added. For more information, see Thermal Specifications, page 587.
- Ordering information was updated to reflect the availability of BGA devices. For more information, see Ordering Information, page 595.

1.3 Revision 4.1

Revision 4.1 of this datasheet was published in July 2018. In revision 4.1 of the document, the VSC7420-04, VSC7421-04, and VSC7422-04 part numbers were added to reflect the availability of devices with extended operating temperature ranges of
–40 °C ambient to 125 °C junction. For more information, see Ordering Information: BGA Package, page 596.

1.4 Revision 4.0

Revision 4.0 of this datasheet was published in December 2012. The following is a summary of the changes implemented in the datasheet:

- Errata items, which were previously published in the *VSC7420-02, VSC7421-02, and VSC7422-02 Errata revision 1.0* as open issues, are now reconciled in the datasheet. Now that the information is available in the datasheet, the previously published errata document no longer applies, and it has been removed from the Microsemi Web site.
- It was clarified that the VCore-Ie CPU frequency is 250 MHz, and the VCore-Ie system frequency is 125 MHz.

1.5 Revision 2.0

Revision 2.0 of this datasheet was published in September 2012. This was the first publication of the document.

2 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC7420-02, VSC7421-02, and VSC7422-02 devices. It is intended for system designers and software developers.

In addition to the datasheet, Microsemi maintains an extensive part-specific library of support and collateral materials that you may find useful in developing your own product. Depending upon the Microsemi device, this library may include:

- Application notes that provide detailed descriptions of the use of the particular Microsemi product to solve real-world problems
- White papers published by industry experts that provide ancillary and background information useful in developing products that take full advantage of Microsemi product designs and capabilities
- User guides that describe specific techniques for interfacing to the particular Microsemi products
- Reference designs showing the Microsemi device built in to applications in ways intended to exploit its relative strengths
- Software Development Kits with sample commands and scripts
- Presentations highlighting the operational features and specifications of the devices to assist in developing your own product road map
- Input/Output Buffer Information specification (IBIS) models to help you create and support the interfaces available on the particular Microsemi product

Visit and register as a user on the Microsemi Web site to keep abreast of the latest innovations from research and development teams and the most current product and application documentation. The address of the Microsemi Web site is www.Microsemi.com.

2.1 Register Notation

This datasheet uses the following general register notation:

<TARGET>:<REGISTER_GROUP>:<REGISTER>.<FIELD>

<REGISTER_GROUP> is not always present. In that case, the following notation is used:

<TARGET>::<REGISTER>.<FIELD>

When a register group does exist, it is always prepended with a target in the notation.

In sections where only one register is discussed, or the target (and register group) is known from the context, the <TARGET>:<REGISTER_GROUP>: may be omitted for brevity, and uses the following notation:

<REGISTER>.<FIELD>

Also, when a register contains only one field, the .<FIELD> is not included in the notation.

2.2 Standard References

This document uses the following industry references.

Table 1 • **Referenced Documents**

Document	Title	Revision
IEEE		
IEEE 802.1ad	802.1Q Amendment 4: Provider Bridges	-2005
IEEE 802.1D	Media Access Control (MAC) Bridges	-2004
IEEE 802.1Q	Virtual Bridged Local Area Networks	-2005
IEEE 802.3	Local and metropolitan area networks — Specific requirements Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications	-2008
IEEE 802.3az	Standard for Information Technology - Telecommunications and Information Exchange Between Systems - Local and Metropolitan Area Networks - Specific Requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications - Amendment: Media Access Control Parameters, Physical Layers and Management Parameters for Energy-Efficient Ethernet	-2010
IETF		
RFC-2236	Internet Group Management Protocol, Version 2 (IGMPv2)	November 1997
RFC-2710	Multicast Listener Discovery for IPv6 (MLDv1)	October 1999
RFC-2819	Remote Network Monitoring (RMON) MIB	May 2000
RFC-2863	The Interfaces Group MIB	June 2000
RFC-3635	Definitions of Managed Objects for Ethernet-like Interface Types	September 2003
Other		
ENG-46158	Cisco Serial GMII (SGMII) Specification	1.7
EDCS-540123	Cisco QSGMII Specification	1.3

2.3 Terms and Abbreviations

The following terms and abbreviations are used throughout this document.

Table 2 • **Terms and Abbreviations**

Term	Explanation
DEI	IEEE Drop Eligible Indicator.
PB	IEEE 802.1AD Provider Bridging (also known as “Q-in-Q”).
PCP	IEEE Priority Code Point interpretation of Ethernet Priority (also known as 802.1p) bits.
VID	IEEE VLAN Identifier.
Classified VLAN	The final VLAN ID classification of a frame used in the forwarding process.

3 Product Overview

The SparX-III family of Gigabit Ethernet switches are pin-compatible devices with port counts ranging from 10 Gigabit Ethernet ports to 25 Gigabit Ethernet ports. The switches integrate up to 12 Gigabit copper PHYs and provide both SGMII and quad SGMII (QSGMII) interfaces. Up to two ports can run at 2.5 Gbps.

These devices provide a rich set of Ethernet switching features such as Layer-2 forwarding with basic VLAN and QoS processing enabling delivery of differentiated services. Each product in the family contains an 8051 CPU enabling light management of the switch. Optionally, the switches can be managed from an external CPU using a serial interface or a MIIM interface.

The SparX-III family contains the following three products:

- VSC7420-02 supports 8× 1G copper PHYs + 2× 2.5G SGMII
- VSC7421-02 supports two major port configurations:

  12× 1G copper PHY + 2× 1G SGMII + 2× 2.5G SGMII

  12× 1G copper PHY + 1× 2.5G SGMII + 1× QSGMII
- VSC7422-02 supports 12× 1G copper PHYs + 3× QSGMII + 1× 2.5G SGMII

3.1 General Features

- All 1G Ethernet ports are tri-speed 10/100/1000 Mbps ports
- All 2.5G Ethernet ports are quad-speed 10/100/1000/2500 Mbps ports
- Integrated copper transceivers are compliant with IEEE 802.3ab and support Microsemi ActiPHY™ link down power savings and PerfectReach™ smart cable reach algorithm
- SGMII ports support both 100-BASE-FX and 1000-BASE-X-SERDES
- Four megabits of integrated shared packet memory
- Fully nonblocking wire-speed switching performance for all frame sizes
- Eight priorities and eight queues per port
- Policing per queue and per port
- DWRR scheduler/shaper per queue and per port with a mix of strict and weighted queues
- Energy Efficient Ethernet (IEEE 802.3az) is supported by both the switch core and the internal copper PHYs
- VCore-Ie CPU system with integrated 8051

3.1.1 Layer-2 Switching

- 8,192 MAC addresses
- 4,096 VLANs (IEEE 802.1Q)
- Push and pop of VLAN tags
- Link aggregation (IEEE 802.3ad)
- Link aggregation traffic distribution is programmable and based on Layer 2 through Layer 4 information
- Wire-speed hardware-based learning and CPU-based learning configurable per port
- Independent and shared VLAN learning
- Provider Bridging (VLAN Q-in-Q) support (IEEE 802.1ad)
- Rapid Spanning Tree Protocol support (IEEE 802.1w)
- Jumbo frame support up to 9.6 kilobytes with programmable MTU per port

3.1.2 Multicast

- 8K L2 multicast group addresses with 64 port masks
- 8K IPv4/IPv6 multicast groups
- Internet Group Management Protocol version 2 (IGMPv2) support
- Multicast Listener Discovery (MLDv1) support

3.1.3 Quality of Service

- Eight QoS queues per port with strict or deficit weighted round-robin scheduling (DWRR)
- DSCP translation, both ingress and/or egress
- DSCP remarking based on QoS class
- PCP and DEI remarking based on QoS class
- Per-queue and per-port policing and shaping, programmable in steps of 100 kbps
- Full-duplex flow control (IEEE 802.3X) and half-duplex backpressure, symmetric and asymmetric

3.1.4 Security

- Generic storm controllers for flooded broadcast, flooded multicast, and flooded unicast traffic
- Selectable CPU queues for segregation of CPU redirected traffic, with 8 queues supported
- Per-port, per-address registration for snooping of reserved IEEE MAC addresses (BPDU, GARP)
- Port-based and MAC-based access control (IEEE 802.1X)
- Per-port CPU-based learning with option for secure CPU-based learning
- Per-port ingress and egress mirroring
- Mirroring per VLAN

3.1.5 Management

- 8051 CPU system with 64 kilobytes of internal RAM
- CPU frame extraction (eight queues) and injection (two queues), which enables efficient data transfer between Ethernet ports and CPU
- Fourteen pin-shared general-purpose I/Os
- Serial LED controller controlling up to 32 ports with four LEDs each
- Serial GPIO controller
- PHY management controller
- Per-port 32-bit counter set with support for the RMON statistics group (RFC 2819) and SNMP interfaces group (RFC 2863)

3.2 Applications

VSC7420-02, VSC7421-02, and VSC7422-02 target the unmanaged and web-managed Ethernet switch equipment in the SMB.

3.3 Related Products

VSC7424-02 SparX-III managed Gigabit Ethernet switch: 10 ports with 8 integrated PHYs and 2 SGMIIs

VSC7425-02 SparX-III managed Gigabit Ethernet switch: 18 ports with 12 integrated PHYs and 6 SGMIIs

VSC7426-02 SparX-III managed Gigabit Ethernet switch: 24 ports with 12 integrated PHYs and 3 QSGMII

VSC7427-02 SparX-III managed Gigabit Ethernet switch: 26 ports with 12 integrated PHYs, 3 QSGMII, and 2 SGMIIs

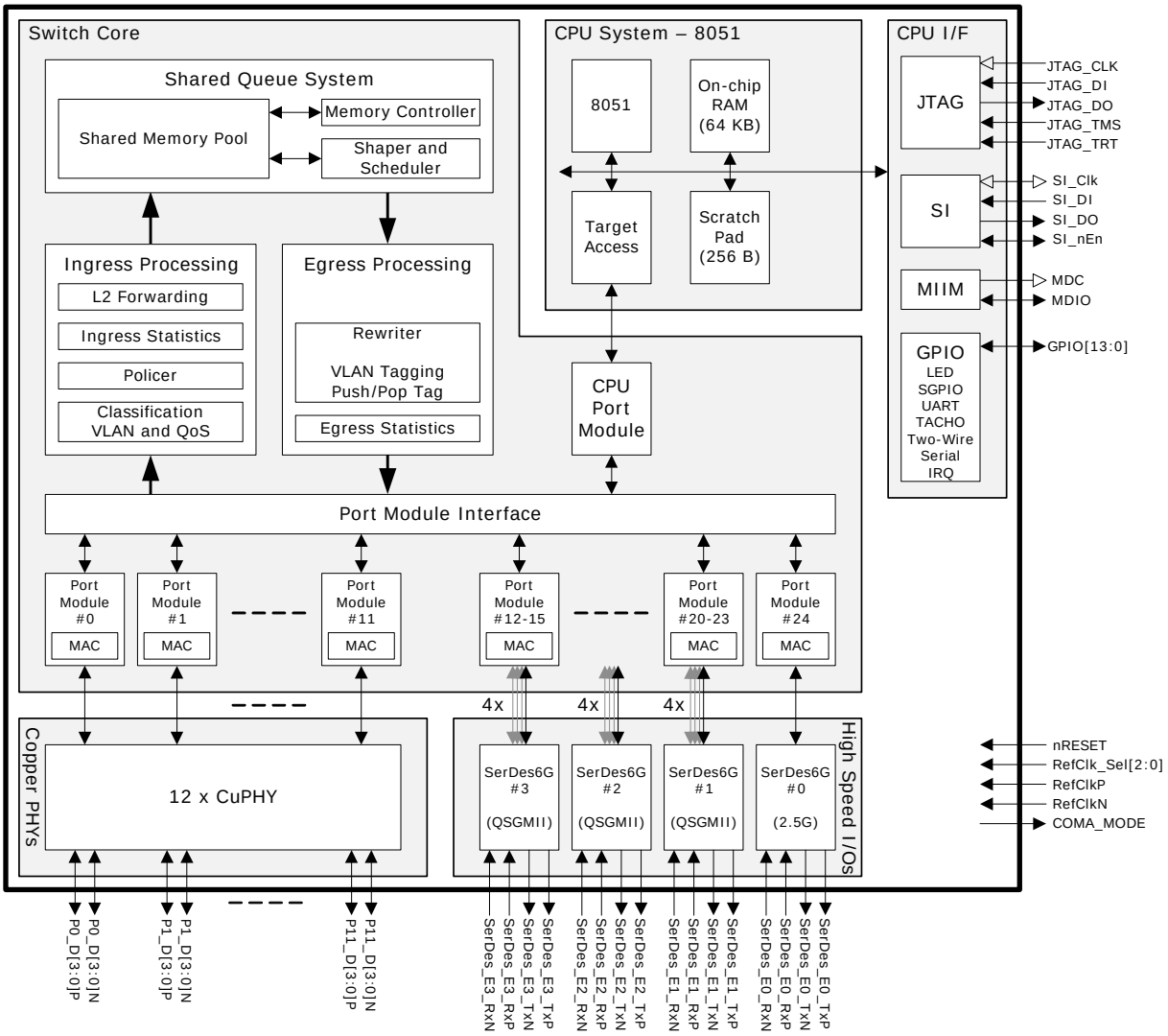
The VSC7424-02, VSC7425-02, VSC7426-02, and VSC7427-02 family of fully managed Layer-2 Ethernet switches provides comprehensive support for QoS, VLAN, and security. They include advanced classification through the Microsemi Contents Aware Processor (VCAP), as well as a CPU system enabled with a 416 MHz MIPS 24KEc™ CPU.

3.4 Functional Overview

This section provides an overview all major blocks and functions involved in the bridging operation in the same order as a frame traverses through the devices. It also outlines other major functionality of the device such as the CPU port module, the CPU system, and CPU interfaces.

The following illustration shows the block diagram for the VSC7422-02. The other devices in the family have similar block diagrams.

Figure 1 • **VSC7422-02 Block Diagram**



3.4.1 Frame Arrival

The Ethernet interfaces receive incoming frames and forward these to the port modules. Supported interfaces include copper transceivers, QSGMII, SGMII, and SerDes.

The integrated low-power copper transceivers support full duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps. The key PHY features are:

- Low power consumption in all modes through ActiPHY™ link down power savings, PerfectReach™ smart cable reach algorithm, and IEEE 802.3az Energy Efficient Ethernet idle power savings.
- VeriPHY® cable diagnostics suite provides extensive network cable operating conditions and status.

The device features a serial LED controller interface for driving LED pins on both internal and external PHYs.

The 1G SGMII and 2.5G SGMII ports support both 100BASE-X and 1000BASE-X-SERDES.

Each port module contains a Media Access Controller (MAC) that performs a full suite of checks, such as VLAN Tag-aware frame size checking, frame check sequence (FCS) checking, and pause frame identification.

Each port module connecting to a SerDes macro contains a Physical Coding Sublayer (PCS) which perform 8 bits/10 bits encoding, auto-negotiation of link speed and duplex mode, and monitoring of the link status.

Full-duplex is supported for all speeds, and half-duplex is supported for 10 Mbps and 100 Mbps. Symmetric and asymmetric pause flow control are both supported.

All Ethernet ports support Energy Efficient Ethernet (EEE) according to IEEE 802.3az. The shared queue system is capable of controlling the operating states, active or low-power, of the PCS or the internal PHYs. Both the PCS and PHYs understand the line signaling as required for EEE. This includes signaling of active, sleep, quiet, refresh, and wake.

Each QSGMII port can multiplex four port modules onto one I/O interface. Each of the underlying port modules has its own MAC and PCS and can negotiate link speed and duplex mode independently of the other port modules.

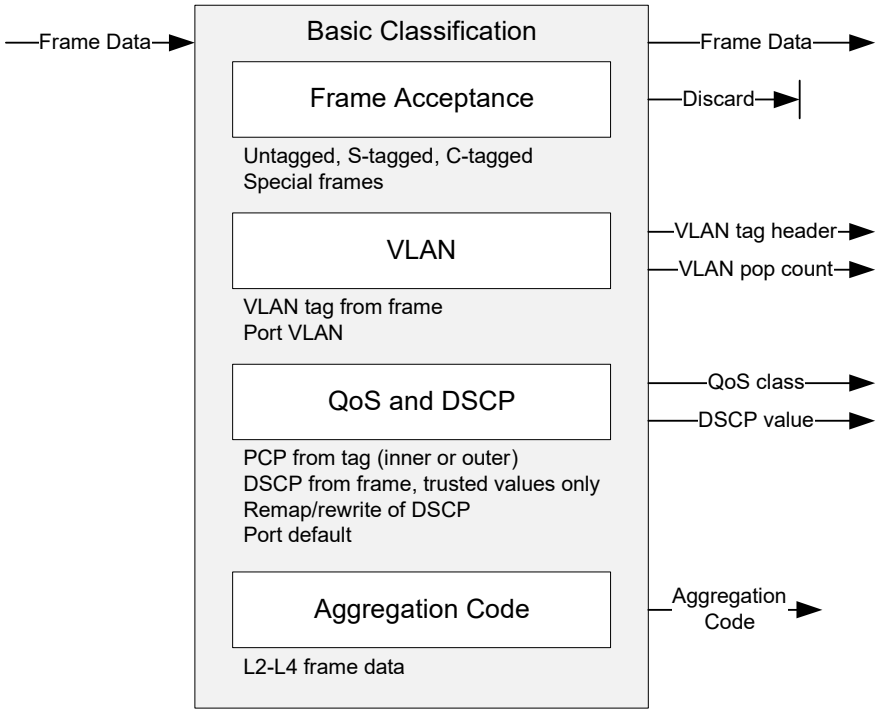
3.4.2 Frame Classification

Each frame is sent to the ingress processing module for classification to a VLAN, classification to a Quality of Service (QoS) class, policing, collecting statistics, security enforcement, and Layer-2 forwarding.

The classification engine can understand up to two VLAN tags and can look for Layer-3 and Layer-4 information behind two VLAN tags. If frames are triple tagged, the higher-layer protocol information is not extracted.

The following illustration shows the frame classification.

Figure 2 • **Frame Classification**



The classification classifies each frame to a VLAN, a QoS class, DSCP value, and an aggregation code. The basic classification also performs a general frame acceptance check.

Frame Acceptance The frame acceptance filter checks for valid combinations of VLAN tags against the ingress port's VLAN acceptance filter where it is possible to configure rules for accepting untagged, priority-tagged, C-, and S-tagged frames. In addition, the filter also enables discarding of frames with illegal MAC addresses (for instance null MAC address or multicast source MAC address).

VLAN Every incoming frame is classified to a VLAN by the basic VLAN classification. This is based on the VLAN in the frame, or if the frame is untagged or the ingress port is VLAN unaware, it is based on the ingress port's default VLAN. A VLAN classification includes the whole TCI (PCP, DEI, and VID) and also the TPID (C-tag or S-tag).

For double-tagged frames, it is selectable whether the inner or the outer tag is used.

The devices can recognize S-tagged frames with the standard TPID (0x88A8) or S-tagged frames using a custom programmable value. One custom value is supported by the devices.

QoS and DSCP Each frame is classified to a Quality of Service (QoS) class. The QoS class is used throughout the devices for providing queuing, scheduling, and congestion control guarantees to the frame according to what is configured for that specific QoS class.

The QoS class is assigned based on the class of service information in the frame's VLAN tags (PCP and DEI) and/or the DSCP values from the IP header. Both IPv4 and IPv6 are supported. If the frame is non-IP or untagged, the port's default QoS class is used.

The DSCP values can be remapped before being used for QoS. This is done using a common table mapping the incoming DSCP to a new value. Remapping is enabled per port. In addition, for each DSCP value, it is possible to specify whether the value is trusted for QoS purposes.

Each IP frame is also classified to an internal DSCP value. By default, this value is taken from the IP header but it may be remapped using the common DSCP mapping table or rewritten based on the assigned QoS class. The classified DSCP value may be written into the frame at egress – this is programmable in the rewriter.

Aggregation Code Finally, the basic classification calculates an aggregation code, which is used to select between ports that are member of a link aggregation group. The aggregation code is based on selected Layer-2 through Layer-4 information, such as MAC addresses, IP addresses, IPv6 flow label, and TCP/UDP port numbers. The aggregation code ensures that frames belonging to the same conversation are using the same physical ports in a link aggregation group.

3.4.3 Policing

Each frame is subject to a number of different policing operations. The devices feature per queue and per port programmable policers. It is programmable per port whether to use the port policer and the queue policers. It is also programmable whether the policers are working in serial or in parallel.

Each frame is counted in associated statistics reflecting the ingress port and the QoS class. The statistics can count bytes or frames.

Finally, the analyzer contains a group of storm control policers that are capable of policing various kinds of flooding traffic as well as CPU directed learn traffic. These policers are global policers working on all frames received by the switch.

All policers can measure frame rates or bit rates.

3.4.4 Layer-2 Forwarding

After the policers, the Layer-2 forwarding block (the analyzer) handles all fundamental bridging operations and maintains the associated MAC table, the VLAN table, and the aggregation table. The devices implement an 8K MAC table and a 4K VLAN table.

The main task of the analyzer is to determine the destination port set of each frame. This forwarding decision is based on various information such as the frame's ingress port, source MAC address, destination MAC address, and the VLAN identifier, as well as mirroring, and the destination port's link aggregation configuration.

The switch performs Layer-2 forwarding of frames. For unicast and Layer-2 multicast frames, this means forwarding based on the destination MAC address and the VLAN. For IPv4 multicast frames, the switch performs Layer-2 forwarding, but based on Layer-3 information.

The following describes some of the contributions to the Layer-2 forwarding:

- VLAN classification VLAN-based forward filtering include source port filtering, destination port filtering, VLAN mirroring, asymmetric VLANs, and so on.
- MAC addresses Destination and source MAC address lookups in the MAC table determine if a frame is a learn frame, a flood frame, a multicast frame, or a unicast frame.
- Learning By default, the devices perform wire-speed learning on all ports. However, certain ports could be configured with secure learning enabled, where an incoming frame with unknown source MAC address is classified as a “learn frame” and is redirected to the CPU. The CPU performs the learning decision and also decides whether the frame is forwarded.

  Learning can also be disabled. In that case, it does not matter if the source MAC address is in the MAC table.
- Link aggregation A frame targeted at a link aggregate is further processed to determine which of the link aggregate group ports the frame must be forwarded to.
- Mirroring Mirror probes may be set up in different places in the forwarding path for monitoring purposes. As part of a mirror a copy of the frame is sent either to the CPU or to another port.

3.4.5 Shared Queue System and Egress Scheduler

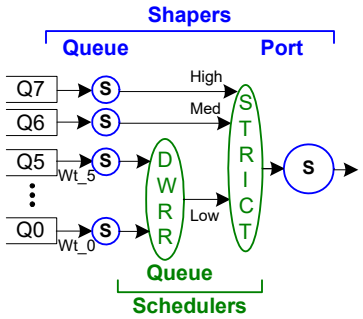
The analyzer provides the destination port set of a frame to the shared queue system. It is the queue system's task to control the frame forwarding to all destination ports.

The shared queue system embeds 4Mbits of memory that can be shared between all queues and ports. The queue system implements egress queues per priority per ingress port. The sharing of resources between queues and ports is controlled by an extensive set of thresholds.

The overall frame latency through the switch is low due to the shared queue system only storing the frame once.

Each egress port implements a scheduler and shapers as shown in the following illustration. Per egress port, the scheduler sees the outcome of aggregating the egress queues (one per ingress port per Qos class) into eight queues, one queue per QoS class. The aggregation is done in a round-robin fashion per QoS class serving all ingress ports equally.

Figure 3 • **Egress Scheduler and Shaper**



When transmitting frames from the shared queue system out on an egress port, frames are scheduled within the port using one of two methods:

- Strict priority – frames with the highest priority are always transmitted before frames with lower priority.
- Deficit Weighted Round Robin (DWRR) – queues 6 and 7 are always strict, and queues 0 through 5 are weighted. Each queue sets a weight ranging from 0 to 31.

In addition, each egress port implements shapers, one per egress queue and one per port.

3.4.6 Rewriter and Frame Departure

Before transmitting the frame on the egress line, the rewriter can modify selected fields in the frame, such as VLAN tags, DSCP value, and FCS.

The rewriter controls the final VLAN tagging of frames based on the classified VLAN, the VLAN pop count, and egress-determined VLAN actions. The egress VLAN actions are by default given by the

egress port settings. These include normal VLAN operations such as pushing a VLAN tag, untagging for specific VLANs, and simple translations of DEI and PCP.

The PCP and DEI bits in the VLAN tag are subject to remarking based on translating the classified tag header or by using the classified QoS value from ingress.

In addition, the DSCP value in IP frames can be updated using the classified DSCP value from ingress. The DSCP value can be remapped at egress before writing it into the frame.

Finally, the rewriter updates the FCS if the frame was modified before the frame is transmitted.

The egress port module controls the flow control exchange of pause frames with a neighboring device when the interconnection link operates in full-duplex flow control mode. When the connected device triggers flow control through transmission of a pause frame, the MAC stops the egress scheduler's forwarding of frames out of the port. Traffic then builds up in the queue system but sufficient queuing is available to ensure wire speed lossless operation.

In half-duplex operation, the port module's egress path responds to back pressure generation from a connected device by collision detection and frame retransmission.

3.4.7 CPU Port Module

The CPU port module contains eight CPU extraction queues and two CPU injection queues. These queues provide an interface for exchanging frames between the internal CPU system and the switch core. An external CPU using the serial interface can also inject and extract frames to and from the switch core by using the CPU port module. Additionally, any Ethernet interface on the devices can be used for extracting and injecting frames.

The switch core can intercept a variety of different frame types and copy or redirect these to the CPU extraction queues. The classifier can identify a set of well-known frames such as IEEE reserved destination MAC addresses (BPDUs, GARPs), as well as IP-specific frames (IGMP, MLD). In addition, frames can be intercepted based on the MAC table, the VLAN table, or the learning process.

Whenever a frame is copied or redirected to the CPU, a CPU extraction queue number is associated with the frame and used by the CPU port module when enqueuing the frame into the 8 CPU extraction queues. The CPU extraction queue number is programmable for every interception option in the switch core.

3.4.8 CPU System and Interfaces

The devices feature a VCore-Ie CPU system containing a 208 MHz 8051 CPU. It is suitable for basic switch tasks such as simple runtime protocols and port state monitoring. VCore-Ie includes 64 kilobytes of internal storage, which can be used for code and data.

In addition to the integrated processor, the CPU system permits the attachment of an external CPU. For configuration of switch register, an external CPU can use a serial interface. For frame transfers, the external CPU has the option of using the serial interface or an SGMII port.

The devices include a GPIO interface with 14 individually configurable pins. Through the GPIOs, various interfaces are supported by the devices:

- Two-wire serial interface (two GPIO pins)
- UART (two GPIO pins)
- External interrupt (one interrupt pin)
- Serial GPIO (SGPIO) and LED interface (four GPIO pins)
- Fan controller with speed input and pulse-width-modulated output (two GPIO pins)

The Serial GPIO and LED interface can specifically be used for driving external LEDs for the internal and external copper PHYs or for serializing external interrupts, for instance link down events from external PHYs, before being input to the devices.

Finally, each of the devices has two MII management controllers; one for the internal PHYs and one connected to the MIIM interface for controlling external PHYs.

4 Functional Descriptions

This section provides detailed information about the functional aspects of the VSC7420-02, VSC7421-02, and VSC7422-02 Gigabit Ethernet switch devices, available configurations, operational features, and testing functionality.

4.1 Port Modules

The port modules contain the following functional blocks:

- MAC
- PCS (ports connecting to a high-speed I/O SerDes macro)

Ports connecting to one of the integrated copper transceivers do not have a PCS.

4.1.1 Port Module Numbering and Macro Connections

The port modules connect to the interface macros. The interface macros can be of two types:

- Internal copper PHY
- SERDES6G macro

The interface macros connect to the external interface pins. For more information about the SerDes macros and integrated copper transceivers, see SERDES6G, page 18 and Copper Transceivers, page 24. Which switch core port modules are connected to which interface macros depends on part number and for some parts on internal configuration.

VSC7421-02 can be used in two different port configurations: switch mode 0 or switch mode 1. The VSC7420-02 and VSC7422-02 devices run in switch mode 0. The switch mode is controlled through DEVCPU_GCB::MISC_CFG.SW_MODE.

The following table lists the mapping from the switch core port modules to the interface macros. Empty cells in the table imply that the port module number is not in use for the specific part number.

When programming registers depending on port numbers, the switch core port module number must always be used. Examples of this are when accessing port module registers (PORT::) or using port masks in system or analyzer registers (SYS::, ANA::).

The number next to the interface macro type (for example, “3” in cell SERDES6G, 3) indicates either the macro number or the internal PHY number that must be used when addressing the macros and PHYs for programming.

Table 3 • **Port Mapping from Switch Core Port Module to Interface Macros**

Switch Core Port Module	VSC7420-02	VSC7421-02 Switch Mode 0	VSC7421-02 Switch Mode 1	VSC7422-02
0-7	CuPHY, 0-7	CuPHY, 0-7	CuPHY, 0-7	CuPHY, 0-7
8-11		CuPHY, 8-11	CuPHY, 8-11	CuPHY, 8-11
12-15		SERDES6G, 3		SERDES6G, 3
16			SERDES6G, 3	SERDES6G, 2
17				SERDES6G, 2
18				SERDES6G, 2
19			SERDES6G, 2	SERDES6G, 2
20-23				SERDES6G, 1
24	SERDES6G, 1		SERDES6G, 1	
25	SERDES6G, 0	SERDES6G, 0	SERDES6G, 0	SERDES6G, 0

Table 3 • **Port Mapping from Switch Core Port Module to Interface Macros *(continued)***

Switch Core Port Module	VSC7420-02	VSC7421-02 Switch Mode 0	VSC7421-02 Switch Mode 1	VSC7422-02
26	CPU port	CPU port	CPU port	CPU port

4.1.2 MAC

This section provides information about the high-level functionality and the configuration options of the Media Access Controller (MAC) that is used in each of the port modules.

The MAC supports the following speeds and duplex modes:

- PHY ports support 10/100/1000 Mbps in full-duplex mode and 10/100 Mbps in half-duplex mode.
- SERDES6G ports support 10/100/1000 Mbps in full-duplex mode and 10/100 Mbps in half-duplex mode.

  The MACs also support 2500 Mbps in full-duplex mode as follows:
  VSC7420-02: Port modules 24 and 25.
  VSC7421-02: Port modules 24 and 25 in switch mode 1. In switch mode 0, port module 25.
  VSC7422-02: Port module 25.

The following table lists the registers associated with configuring the MAC.

Table 4 • **MAC Configuration Registers**

Register	Description	Replication
CLOCK_CFG	Reset and speed configuration	Per port
MAC_ENA_CFG	Enabling of Rx and Tx data paths	Per port
MAC_MODE_CFG	Port mode configuration	Per port
MAC_MAXLEN_CFG	Maximum length configuration	Per port
MAC_TAGS_CFG	VLAN tag length configuration	Per port
MAC_ADV_CHK_CFG	Type length configuration	Per port
MAC_IFG_CFG	Interframe gap configuration	Per port
MAC_HDX_CFG	Half-duplex configuration	Per port
MAC_FC_CFG	Flow control configuration	Per port
MAC_FC_MAC_LOW_CFG	LSB of SMAC used in pause frames	Per port
MAC_FC_MAC_HIGH_CFG	MSB of SMAC used in pause frames	Per port
MAC_STICKY	Sticky bit recordings	Per port

4.1.2.1 Resets

There are a number of resets in the port module. All of the resets can be set and cleared simultaneously. By default, all blocks are in the reset state. With reference to register CLOCK_CFG, the resets are:

- MAC_RX_RST — Reset of the MAC receiver
- MAC_TX_RST — Reset of the MAC transmitter
- PORT_RST — Reset of the ingress and egress queues
- PHY_RST — Reset of the integrated PHY (only present for port modules connecting to a PHY)
- PCS_RX_RST — Reset of the PCS decoder (only present for port modules connecting to a SerDes macro)
- PCS_TX_RST — Reset of the PCS encoder (only present for port modules connecting to a SerDes macro)

When changing the MAC configuration, the port must go through a reset cycle. This is done by writing register CLOCK_CFG twice. On the first write, the reset bits are set. On the second write, the reset bits are cleared. Bits that are not reset bits in CLOCK_CFG must keep their new value for both writes.

For more information about resetting a port, see Port Reset Procedure, page 127.

4.1.2.2 Port Mode Configuration

The MAC provides a number of handles for configuring the port mode. With reference to the MAC_MODE_CFG, MAC_IFG_CFG, and MAC_ENA_CFG registers, the handles are:

- Duplex mode (FDX_ENA). Half or full duplex.
- Data sampling (GIGA_MODE_ENA). Must be 1 in 1 Gbps and 2.5 Gbps and 0 in 10 Mbps and 100 Mbps.
- Enabling transmission and reception of frames (TX_ENA/RX_ENA). Clearing RX_ENA stops the reception of frames and further frames are discarded. An ongoing frame reception is interrupted. Clearing TX_ENA stops the dequeuing of frames from the egress queues, which means that frames are held back in the egress queues. An ongoing frame transmission is completed.
- Tx to Tx inter-frame gap (TX_IFG).

For ports connecting to an internal PHY, the link speed is determined by the PHY. For other ports, the link speed is configured using CLOCK_CFG.LINK_SPEED with the following options:

- Link speed (CLOCK_CFG.LINK_SPEED)
  1 Gbps (125 MHz clock)

  Ports 24 and 25: 1 Gbps or 2.5 Gbps (125 MHz or 312.5 MHz clock). The actual clock frequency depends on the SerDes configuration.

  100 Mbps (25 MHz clock)

  10 Mbps (2.5 MHz clock)

4.1.2.3 Half-Duplex Mode

A number of special configuration options are available for half-duplex (HDX) mode:

- **Seed for back-off randomizer** Field MAC_HDX_CFG.SEED seeds the randomizer used by the backoff algorithm. Use MAC_HDX_CFG.SEED_LOAD to load a new seed value.
- **Backoff after excessive collision** Field MAC_HDX_CFG.WEXC_DIS determines whether the MAC backs off after an excessive collision has occurred. If set, backoff is disabled after excessive collisions.
- **Retransmission of frame after excessive collision** Field MAC_HDX_CFG.RETRY_AFTER_EXC_COL_ENA determines if the MAC retransmits frames after an excessive collision has occurred. If set, a frame is not dropped after excessive collisions, but the backoff sequence is restarted. Although this is a violation of IEEE 802.3, it is useful in non-dropping half-duplex flow control operation.
- **Late collision timing** Field MAC_HDX_CFG.LATE_COL_POS adjusts the border between a collision and a late collision in steps of 1 byte. According to IEEE 802.3, section 21.3, this border is permitted to be on data byte 56 (counting frame data from 1); that is, a frame experiencing a collision on data byte 55 is always retransmitted, but it is never retransmitted when the collision is on byte 57. For each higher LATE_COL_POS value, the border is moved 1 byte higher.
- **Rx-to-Tx inter-frame gap** The sum of MAC_IFG_CFG.RX_IFG1 and MAC_IFG_CFG.RX_IFG2 establishes the time for the Rx-to-Tx inter-frame gap. RX_IFG1 is the first part of half-duplex Rx-to-Tx inter-frame gap. Within RX_IFG1, this timing is restarted if carrier sense (CRS) has multiple high-low transitions (due to noise). RX_IFG2 is the second part of half-duplex Rx-to-Tx inter-frame gap. Within RX_IFG2, transitions on CRS are ignored.

When enabling a port for half-duplex mode, the switch core must also be enabled (SYS::FRONT_PORT_MODE.HDX_MODE).

4.1.2.4 Frame and Type/Length Check

The MAC supports frame lengths of up to 16 kilobytes. The maximum length accepted by the MAC is configurable in MAC_MACLEN_CFG.MAX_LEN.

The MAC allows tagged frames to be 4 bytes longer and double-tagged frames to be 8 bytes longer than the specified maximum length (MAC_TAGS_CFG.VLAN_LEN_AWR_ENA). The MAC must be configured to look for VLAN tags. By default, EtherType 0x8100 identifies a VLAN tag. In addition, a custom EtherType can be configured in MAC_TAGS_CFG.TAG_ID. The MAC can be configured to look for none, one, or two tags (MAC_TAG_CFG.VLAN_AWR_ENA, MAC_TAG_CFG.VLAN_DBL_AWR_ENA).

The type/length check (MAC_ADV_CHK_CFG.LEN_DROP_ENA) causes the MAC to discard frames with type/length errors (in-range and out-of-range errors).

4.1.2.5 Flow Control

In full-duplex mode, the MAC provides independent support for transmission of pause frames and reaction to incoming pause frames. This allows for asymmetric flow control configurations.

The MAC obeys received pause frames (MAC_FC_CFG.RX_FC_ENA) by pausing the egress traffic according to the timer values specified in the pause frames.

The transmission of pause frames is triggered by assertion of a flow control condition in the ingress queues caused by a queue filling exceeding a watermark. For more information, see Shared Queue System, page 66. The MAC handles the formatting and transmission of the pause frame. The following configuration options are available:

- Transmission of pause frames (MAC_CFG_CFG.TX_FC_ENA).
- Pause timer value used in transmitted pause frames (MAC_FC_CFG.PAUSE_VAL_CFG).
- Flow control cancellation when the ingress queues de-assert the flow control condition by transmission of a pause frame with timer value 0 (MAC_FC_CFG.ZERO_PAUSE_ENA).
- Source MAC address used in transmitted pause frames (MAC_FC_MAC_HIGH_CFG, MAC_FC_MAC_LOW_CFG).

The MAC has the option to discard incoming frames when the remote link partner is not obeying the pause frames transmitted by the MAC. The MAC discards an incoming frame if a Start-of-Frame is seen after the pause frame was transmitted. It is configurable how long reaction time is given to the link partner (MAC_FC_CFG.FC_LATENCY_CFG). The benefit of this approach is that the queue system is not risking being overloaded with frames due to a non-complying link partner.

In half-duplex mode, the MAC does not react to received pause frames. If the flow control condition is asserted by the ingress queues, the industry-standard backpressure mechanism is used. Together with the ability to retransmit frames after excessive collisions (MAC_HDX_CFG.RETRY_AFTER_EXC_COL_ENA), this enables non-dropping half-duplex flow control.

4.1.2.6 Frame Aging

The following table lists the registers associated with frame aging.

Table 5 • **Frame Aging Configuration Registers**

Register	Description	Replication
SYS::FRM_AGING	Frame aging time	None
REW::PORT_CFG.AGE_DIS	Disable frame aging	Per port

The MAC supports frame aging where frames are discarded if a maximum transit delay through the switch is exceeded. All frames, including CPU-injected frames, are subject to aging. The transit delay is time from when a frame is fully received until that frame is scheduled for transmission through the egress MAC. The maximum allowed transit delay is configured in SYS::FRM_AGING.

Frame aging can be disabled per port (REW::PORT_CFG.AGE_DIS).

Discarded frames due to frame aging are counted in the c_tx_aged counter.

4.1.3 PCS

This section provides information about the Physical Coding Sublayer (PCS) block, where the auto-negotiation process establishes mode of operation for a link. The PCS supports both SGMII mode and two SerDes modes, 1000BASE-X and 100BASE-FX.

The PCS block is only available in port modules 12 through 25.

The following table lists the registers associated with PCS.

Table 6 • **PCS Configuration Registers**

Registers	Description	Replication
PCS1G_CFG	PCS configuration	Per PCS
PCS1G_MODE_CFG	PCS mode configuration	Per PCS
PCS1G_SD_CFG	Signal detect configuration	Per PCS
PCS1G_ANEG_CFG	Configuration of the PCS auto-negotiation process	Per PCS
PCS1G_ANEG_NP_CFG	Auto-negotiation next page configuration	Per PCS
PCS1G_LB_CFG	Loop-back configuration	Per PCS
PCS1G_ANEG_STATUS	Status signaling of the PCS auto-negotiation process	Per PCS
PCS1G_ANEG_NP_STATUS	Status signaling of the PCS auto-negotiation next page process	Per PCS
PCS1G_LINK_STATUS	Link status	Per PCS
PCS1G_LINK_DOWN_CNT	Link down counter	Per PCS
PCS1G_STICKY	Sticky bit register	Per PCS

The PCS is enabled in PCS1G_CFG.PCS_ENA and supports both SGMII and 1000BASE-X SERDES mode (PCS_MODE_CFG.SGMII_MODE_ENA), as well as 100-BASE-FX. For information about enabling 100BASE-FX, see 100BASE-FX, page 18.

The PCS also supports the IEEE 802.3, Clause 66 unidirectional mode, where the transmission of data is independent of the state of the receive link (PCS_MODE_CFG.UNIDIR_MODE_ENA).

4.1.3.1 Auto-Negotiation

Auto-negotiation is enabled in PCS1G_ANEG_CFG.ANEG_ENA. To restart the auto-negotiation process, PCS1G_ANEG_CFG.ANEG_RESTART_ONE_SHOT must be set.

In SGMII mode (PCS_MODE_CFG.SGMII_MODE_ENA=1), matching the duplex mode with the link partner must be ignored (PCS1G_ANEG_CFG.SW_RESOLVE_ENA). Otherwise, the link is kept down when the auto-negotiation process fails.

The advertised word for the auto-negotiation process (base page) is configured in PCS1G_ANEG_CFG.ADV_ABILITY. The next page information is configured in PCS1G_ANEG_NP_CFG.NP_TX.

When the auto-negotiation state machine has exchanged base page abilities, the PCS1G_ANEG_STATUS.PAGE_RX_STICKY is asserted indicating that the link partner's abilities were received (PCS1G_ANEG_STATUS.LP_ADV_ABILITY).

If next page information is exchanged, PAGE_RX_STICKY must be cleared, next page abilities must be written to PCS1G_ANEG_NP_CFG.NP_TX, and PCS1G_ANEG_NP_CFG.NP_LOADED_ONE_SHOT must be set. When the auto-negotiation state machine has exchanged the next page abilities, the PCS1G_ANEG_STATUS.PAGE_RX_STICKY is asserted again, indicating that the link partner's next

page abilities were received (PCS1G_ANEG_STATUS.LP_NP_RX). Additional exchanges of next page information are possible using the same procedure.

After the last next page is received, the auto-negotiation state machine enters the IDLE_DETECT state and the PCS1G_ANEG_STATUS.PR bit is set indicating that ability information exchange (base page and possible next pages) is finished and software can now resolve priority. Appropriate actions, such as Rx or Tx reset, or auto-negotiation restart, can then be taken, based on the negotiated abilities. The LINK_OK state is reached one link timer period later.

When the auto-negotiation process reaches the LINK_OK state, PCS1G_ANEG_STATUS.ANEG_COMPLETE is asserted.

4.1.3.2 Link Surveillance

The current link status can be observed through PCS1G_LINK_STATUS.LINK_STATUS. The LINK_STATUS is defined as either the PCS synchronization state or as bit 15 of PCS1G_ANEG_STATUS.LP_ADV_ABILTY, which carries information about the link status of the attached PHY in SGMII mode.

Link down is defined as the auto-negotiation state machine being in neither the AN_DISABLE_LINK_OK state nor the LINK_OK state for one link timer period. If a link down event occurs, PCS1G_STICKY.LINK_DOWN_STICKY is set, and PCS1G_LINK_DOWN_CNT is incremented. In SGMII mode, the link timer period is 1.6 ms; in SerDes mode, the link timer period is 10 ms.

The PCS synchronization state can be observed through PCS1G_LINK_STATUS.SYNC_STATUS. Synchronization is lost when the PCS is not able to recover and decode data received from the attached serial link.

4.1.3.3 Signal Detect

The PCS can be enabled to react to loss of signal through signal detect (PCS1G_SD_CFG.SD_ENA). At loss of signal, the PCS Rx state machine is restarted, and frame reception stops. If signal detect is disabled, no action is taken upon loss of signal. The polarity of signal detect is configurable in PCS1G_SD_CFG.SD_POL.

The source of signal detect is selected in PCS1G_SD_CFG.SD_SEL to either the SerDes PMA or the PMD receiver. If the SerDes PMA is used as source, the SerDes macro provides the signal detect. If the PMD receiver is used as source, signal detect is sampled externally through one of the GPIO pins on the devices. For more information about the configuration of the GPIOs and signal detect, see GPIO Controller, page 114.

PCS1G_LINK_STATUS.SIGNAL_DETECT contains the current value of the signal detect input.

4.1.3.4 Tx Loopback

For debug purposes, the Tx data path in the PCS can be looped back into the Rx data path. This feature is enabled through PCS1G_LB_CFG.TBI_HOST_LB_ENA.

4.1.3.5 Test Patterns

The following table lists the registers associated with configuring test patterns.

Table 7 • **Test Pattern Registers**

Registers	Description	Replication
PCS1G_TSTPAT_MODE_CFG	Test pattern configuration	Per PSC
PCS1G_TSTPAT_MODE_STATUS	Test pattern status	Per PCS

PCS1G_TSTPAT_MODE_CFG.JTP_SEL overwrites normal operation of the PCS and enables generation of jitter test patterns for debugging. The jitter test patterns are defined in IEEE 802.3, Annex 36A, and the following patterns are supported:

- High frequency test pattern
- Low frequency test pattern

- Mixed frequency test pattern
- Continuous random test pattern with long frames
- Continuous random test pattern with short frames

PCS1G_TSTPAT_MODE_STATUS register holds information about error and lock conditions while running the jitter test patterns.

4.1.3.6 Low Power Idle

The following table lists the registers associated with low power idle (LPI).

Table 8 • **Low Power Idle Registers**

Registers	Description	Replication
PCS1G_LPI_CFG	Configuration of the PCS Low Power Idle process	Per PSC
PCS1G_LPI_WAKE_ERROR_CNT	Error counter	Per PCS
PCS1G_LPI_STATUS	Low Power Idle status	Per PCS

The PCS supports Energy Efficient Ethernet (EEE) as defined by IEEE 802.3az. The PCS converts Low Power Idle (LPI) encoding between the MAC and the serial interface transparently. In addition, the PCS provides control signals allowing to stop data transmission in the SerDes macro. During low power idles the serial transmitter in the SerDes macro can be powered down, only interrupted periodically while transmitting refresh information, which allows the receiver to notice that the link is still up but in power down mode.

When a SERDES6G macro operating in QSGMII mode is enabled for powering down of the serial transmitter during low power idles, one of the four PCSs connected to the macro must be selected master (PCS1G_LPI_CFG.QSGMII_MS_SEL). The master PCS sends refresh information to the attached receivers periodically. Note that the serial transmitter can only power down when all four attached ports are in low power idle.

For more information about powering down the serial transmitter in the SerDes macros, see SERDES6G, page 18.

It is not necessary to enable the PCS for EEE, because it is controlled indirectly by the shared queue system. It is possible, however, to manually force the PCS into the low power idle mode through PCS1G_LPI_CFG.TX_ASSERT_LPIDLE. During LPI mode, the PCS constantly encodes low power idle with periodical refreshes. For more information about EEE, see Energy Efficient Ethernet, page 73.

The current low power idle state can be observed through PCS1G_LPI_STATUS for both receiver and transmitter:

- RX_LPI_MODE: Set if the receiver is in low power idle mode.
- RX_QUIET: Set if the receiver is in the Quiet state of the low power idle mode. If cleared while RX_LPI_MODE is set, the receiver is in the refresh state of the low power idle mode.

The same is observable for the transmitter through TX_LPI_MODE and TX_QUIET.

If an LPI symbol is received, the RX_LPI_EVENT_STICKY bit is set, and if an LPI symbol is transmitted, the TX_LPI_EVENT_STICKY bit is set. These events are sticky.

The PCS1G_LPI_WAKE_ERROR_CNT wake-up error counter increments when the receiver detects a signal and the PCS is not synchronized. This can happen when the transmitter fails to observe the wake-up time or if the receiver is not able to synchronize in time.

4.1.3.7 100BASE-FX

The following table lists the registers associated with 100BASE-FX configuration.

Table 9 • **100BASE-FX Registers**

Registers	Description	Replication
PCS_FX100_CFG	Configuration of the PCS 100BASE-FX mode	Per PSC
PCS_FX100_STATUS	Status of the PCS 100BASE-FX mode	Per PCS

The PCS supports a 100BASE-FX mode in addition to the SGMII and 1000BASE-X SerDes modes. The 100BASE-FX mode uses 4-bit/5-bit coding as specified in IEEE 802.3 Clause 24 for fiber connections. The 100BASE-FX mode is enabled through PCS_FX100_CFG.PCS_ENA, which masks out all PCS1G related registers.

The following options are available:

Far-End Fault facility In 100BASE-FX, the PCS supports the optional Far-End Fault facility. Both Far-End Fault generation (PCS_FX100_CFG.FEF_GEN_ENA) and Far-End Fault Detection (PCS_FX100_CFG.FEF_CHK_ENA) are supported. An Far-End Fault incident is recorded in PCS_FX100_STATUS.FEF_FOUND.

Signal Detect 100BASE-FX has a similar signal detect scheme to the SGMII and SerDes modes. For 100BASE-FX, PCS_FX100_CFG.SD_ENA enables signal detect, PCS_FX100_CFG.SD_POL controls the polarity, and PCS_FX100_CFG.SD_SEL selects the input source. The current status of the signal detect input can be observed through PCS_FX100_STATUS.SIGNAL_DETECT. For more information about signal detect, see Signal Detect, page 16.

Link Surveillance The PCS synchronization status can be observed through PCS_FX100_STATUS.SYNC_STATUS. When synchronization is lost, the link breaks and PCS_FX100_STATUS.SYNC_LOST_STICKY is set. The PCS continuously tries to recover the link.

Unidirectional mode 100BASE-FX has a similar unidirectional mode as SGMII and SerDes modes. PCS_FX100_CFG.UNIDIR_MODE_ENA enables unidirectional mode.

4.2 SERDES6G

The SERDES6G is a high-speed SerDes interface that operates at 100 Mbps (100BASE-FX), 1 Gbps (SGMII/SerDes), 2.5 Gbps (SGMII), and 4 Gbps (QSGMII). The 100BASE-FX mode is supported by oversampling.

The following table lists the registers associated with SERDES6G.

Table 10 • **SERDES6G Registers**

Registers	Description	Replication
SERDES6G_COMMON_CFG	Common configuration	Per SerDes
SERDES6G_DES_CFG	Deserializer configuration	Per SerDes
SERDES6G_IB_CFG	Input buffer configuration	Per SerDes
SERDES6G_IB_CFG1	Input buffer configuration	Per SerDes
SERDES6G_SER_CFG	Serializer configuration	Per SerDes
SERDES6G_OB_CFG	Output buffer configuration	Per SerDes
SERDES6G_OB_CFG1	Output buffer configuration	Per SerDes
SERDES6G_PLL_CFG	PLL configuration	Per SerDes
SERDES6G_MISC_CFG	Miscellaneous configuration	Per SerDes

For increased performance in specific application environments, SERDES6G supports the following:

- Baud rate support, configurable from 1 Gbps to 4 G, for quarter, half, and full rate modes
- Programmable loop bandwidth and phase regulation for the deserializer
- Configurable input buffer features such as signal detect/loss of signal (LOS) options
- Configurable output buffer features, such as programmable de-emphasis, amplitude drive levels, and slew rate control
- Synchronous Ethernet support
- Loopbacks for system test

4.2.1 SERDES6G Basic Configuration

The SERDES6G is enabled in SERDES6G_COMMON_CFG.ENA_LANE. By default, the SERDES6G is held in reset and must be released before the interface is active. This is done through SERDES6G_COMMON_CFG.SYS_RST and SERDES6G_MISC_CFG.LANE_RST.

4.2.1.1 SERDES6G Parallel Interface Configuration

The SERDES6 block includes a parallel data interface, which can operate in two different modes. It must be set according to the mode of operation (SERDES6G_COMMON_CFG.IF_MODE). For 100 Mbps, 1 Gbps, and 2.5 Gbps operation, the 10-bit mode is used, and for 4 Gbps operation (QSGMII), the 20-bit mode is used.

4.2.1.2 SERDES6G PLL Frequency Configuration

To operate the SERDES6G block at the correct frequency, configure the internal macro as follows. The PLL calibration is enabled through SERDES6G_PLL_CFG.PLL_FSM_ENA.

1. Configure SERDES6G_PLL_CFG.PLL_FSM_CTRL_DATA in accordance with data rates listed in the following two tables.
2. Set SYS_RST = 0 (active) and PLL_FSM_ENA = 0 (inactive).
3. Set SYS_RST = 1 (deactive) and PLL_FSM_ENA = 1 (active).

Table 11 • **PLL Configuration**

Mode	SERDES6G_PLL_CFG.PLL_FSM_CTRL_DATA
SGMII/SerDes, 1 Gbps data	60
SGMII, 2.5 Gbps data	48
QSGMII, 4 Gbps data	120

4.2.1.3 SERDES6G Frequency Configuration

The following table lists the range of data rates that are supported by SERDES6G.

Table 12 • **SERDES6 Frequency Configuration Registers**

Configuration	SGMII/SerDes 1 Gbps	SGMII 2.5 Gbps	QSGMII 4 Gbps
SERDES6G_PLL_CFG.PLL_ROT_FRQ	0	1	0
SERDES6G_PLL_CFG.PLL_ROT_DIR	1	0	0
SERDES6G_PLL_CFG.PLL_ENA_ROT	0	1	0
SERDES6G_COMMON_CFG.QRATE	1	0	0
SERDES6G_COMMON_CFG.HRATE	0	1	0

4.2.2 SERDES6G Loopback Modes

The SERDES6G interface supports two different loopback modes for testing and debugging data paths: equipment loopback and facility loopback.

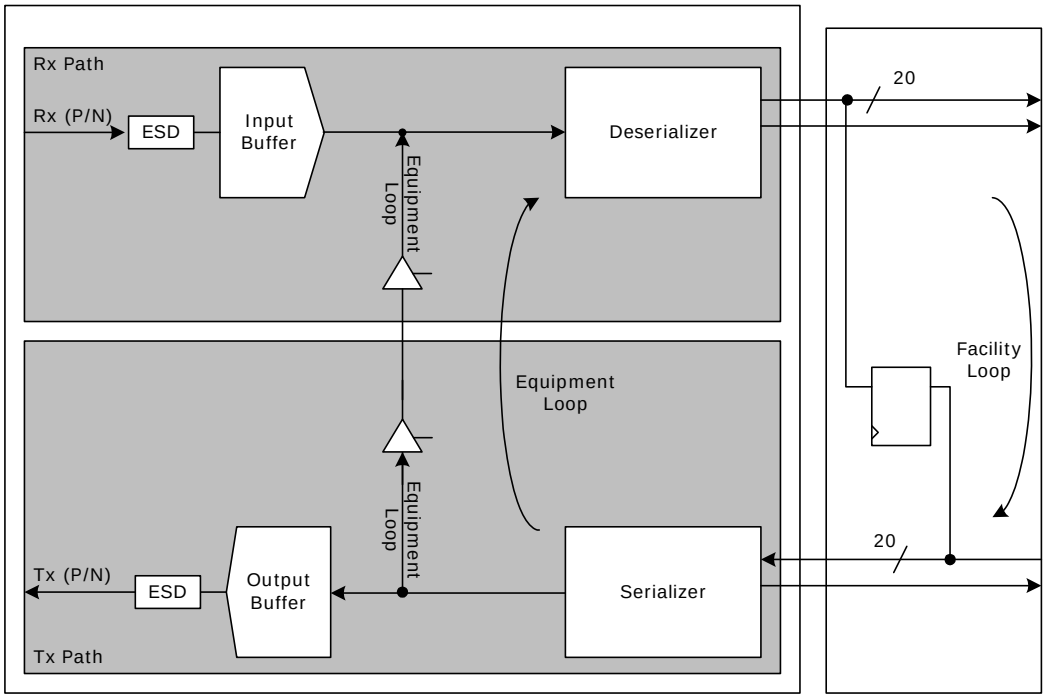
Equipment loopback (SERDES6G_COMMON_CFG.ENA_ELOOP) Data is looped back from serializer output to the deserializer input, and the receive clock is recovered. The equipment loopback includes all transmit and receive functions, except for the input and output buffers. The Tx data can still be observed on the output.

Facility loopback (SERDES6G_COMMON_CFG.ENA_FLOOP) The clock and parallel data output from deserializer are looped back to the serializer interface. Incoming serial data passes through the input buffer, the CDR, the deserializer, back to the serializer, and finally out through the output buffer.

Only one of the loopbacks can be enabled at the same time.

The following illustration shows the loopback paths for the SERDESG6.

Figure 4 • **SERDES Loopback**



4.2.3 SERDES6G Deserializer Configuration

The SERDES6G block includes digital control logic that interacts with the analog modules within the block and compensates for the frequency offset between the received data and the internal high-speed reference clock. To gain high jitter performance, the phase regulation is a PI-type regulator, whose proportional (P) and integrative (I) characteristics can be independently configured.

The integrative part of the phase regulation loop is configured in SERDES6G_DES_CFG.DES_PHS_CTRL. The limits of the integrator are programmable, allowing different settings for the integrative regulation while guaranteeing that the proportional part still is stronger than the integrative part. Integrative regulation compensates frequency modulation from DC up to cut-off frequency. Frequencies above the cut-off frequency are compensated by the proportional part.

The DES_BW_HYST register field controls the time constant of the integrator independently of the proportional regulator. The range of DES_BW_HYST is programmable as follows:

- Full rate mode = 3 to 7
- Half-rate mode = 2 to 7
- Quarter-rate mode = 1 to 7

The lower the configuration setting, the smaller the time-constant of the integrative regulation. For normal operation, configure DES_BW_HYST to 5.

The cut-off-frequency is calculated to:

fco = 1/(2 × PI × 128 × PLL period × 32 × 2^(DES_BW_HYST + 1 – DES_BW_ANA))

PLL period = 1/(*n* × data rate)

where, *n* = 1 (full rate mode), 2 (half-mode) or 4 (quarter-rate mode)

The integrative regulator can compensate a static frequency offset within the programmed limits down to a remaining frequency error of below 4 ppm. In steady state, the integrator toggles between two values around the exact value, and the proportional part of the phase regulation takes care of the remaining phase error.

After a device reset, the phase regulation may be 180° out of phase compared to the incoming data, resulting in a deadlock condition at the sampling stage of the deserializer. To prevent this situation, the SERDES6G provides a 180° deadlock protection mechanism (SERDES6G_DES_CFG.DES_MBTR_CTRL). If the deadlock protection mechanism is enabled, a small frequency offset is applied to the phase regulation loop. The offset is sufficient to move the sampling point out of the 180° deadlock region, while at the same time, small enough to allow the regulation loop to compensate when the sample point is within the data eye.

The loop bandwidth for the proportional part of the phase regulation loop is controlled by configuring SERDES6G_DES_CFG.DES_BW_ANA.

The fastest loop bandwidth setting (lowest configuration value) results in a loop bandwidth that is equal to the maximum frequency offset compensation capability. For improved jitter performance, use a setting with sufficient margin to track the expected frequency offset rather than using the maximum frequency offset. For example, if a 100 ppm offset is expected, use a setting that is four times higher than the offset. For more information about possible bandwidth selections, see Table 357, page 267.

The following table provides the limits for the frequency offset compensation. The values are theoretical limits for input signals without jitter, because the actual frequency offset compensation capability is dependent on the toggle rate of the input data and the input jitter. Note that only applicable configuration values are listed. HRATE and QRATE are the configuration settings of SERDES6G_COMMON_CFG.HRATE and SERDES6G_COMMON_CFG.QRATE.

Table 13 • **SERDES6G Loop Bandwidth**

DES_BW_ANA	Limits when HRATE = 0 QRATE = 0	Limits when HRATE = 1 QRATE = 0	Limits when HRATE = 0 QRATE = 1
2			1953 ppm
3		1953 ppm	977 ppm
4	1953 ppm	977 ppm	488 ppm
5	977 ppm	488 ppm	244 ppm
6	488 ppm	244 ppm	122 ppm
7	244 ppm	122 ppm	61 ppm

4.2.4 SERDES6G Serializer Configuration

The serializer provides the ability to align the phase of the internal clock and data to a selected source (SERDES6G_SER_CFG.SER_ENALI). The phase align logic is used when SERDES6G operates in the facility loopback mode.

4.2.5 SERDES6G Input Buffer Configuration

The SERDES6G input buffer supports configuration options for:

- Automatic input voltage offset compensation
- Loss of signal detection

The input buffer is normally AC-coupled and therefore the common-mode termination is switched off (SERDES6G_IB_CFG1.IB_CTERM_ENA). In order to support type-2 loads (DC-coupling at 1.0 V

termination voltage) according to the OIF CEI specifications, common-mode termination must be enabled.

The sensitivity of the level detect circuit can be adapted to the input signal's characteristics (amplitude and noise). The threshold value for the level detect circuit is set in SERDES6G_IB_CFG.IB_VBCOM. The default value is suitable for normal operation.

When the SerDes interface operates in 100BASE-FX mode, the input buffer of the SERDES6G macro must also be configured for 100BASE-FX (SERDES6G_IB_CFG.IB_FX100_ENA).

During test or reception of low data rate signals (for example, 100BASE-FX), the DC-offset compensation must be disabled. For all other modes, the DC-offset compensation must be enabled for optimized performance. DC-offset compensation is controlled by SERDES6G_IB_CFG1.IB_ENA_OFFSAC and SERDES6G_IB_CFG1.IB_ENA_OFFSDC.

4.2.6 SERDES6G Output Buffer Configuration

The SERDEDS6G output buffer supports the following configuration options:

- Amplitude control
- De-emphasis and output polarity inversion
- Slew rate control
- Skew adjustment
- Idle mode

The maximum output amplitude of the output buffer depends on the output buffer's supply voltage. For interface standards requiring higher output amplitudes (backplane application or interface to optical modules, for example), the output buffer can be supplied from a 1.2 V instead of a 1.0 V supply. By default, the output buffer is configured for 1.2 V mode, because enabling the 1.0 V mode when supplied from 1.2 V must be avoided. The supply mode is configured by SERDES6G_OB_CFG.OB_ENA1V_MODE.

The output buffer supports a four-tap pre-emphasis realized by one pre-cursor, the center tap, and two post cursors. The pre-cursor coefficient, C0, is configured by SERDES6G_SER_CFG.OB_PREC. C0 is a 5-bit value, with the most significant bit defining the polarity. The lower 4-bit value is hereby defined as B0. The first post-cursor coefficient, C2, is configured by SERDES6G_OB_CFG.OB_POST0. C2 is a 6-bit value, with the most significant bit defining the polarity. The lower 5-bit value is hereby defined as B2. The second post-cursor coefficient, C3, is configured by SERDES6G_SER_CFG.OB_POST1. C3 is 5-bit value, with the most significant bit defining the polarity. The lower 4-bit value is hereby defined as B3. The center-tap coefficient, C1, is a 6-bit value. Its polarity can be programmed by SERDES6G_OB_CFG.OB_POL, which is defined as p1. For normal operation SERDES6G_OB_CFG.OB_POL must be set to 1. The value of the 6 bits forming C1 is calculated by the following equation.

Equation 1: C1: (64 – (B0 + B2 + B3)) × p1

The output amplitude is programmed by SERDES6G_OB_CFG1.OB_LEV, which is a 6-bit value. This value is internally increased by 64 and defines the amplitude coefficient K. The range of K is therefore 64 to 127. The differential peak-peak output swing is given by 8.75 mV × K. The maximum peak-peak output swing depends on the data stream and can be calculated to:

Equation 2: $H(Z) = 4.375\ mVpp \times K \times (C0 \times z^{1} + C1 \times z^{0} + C2 \times z^{-1} + C3 \times z^{-2})/64$

with z^{n} denoting the current bits of the data pattern defining the amplitude of Z. The output amplitude also depends on the output buffer's supply voltage. For more information about the dependencies between the maximum achievable output amplitude and the output buffer's supply voltage, see Table 574, page 419.

The configuration bits are summarized in the following table.

Table 14 • **De-Emphasis and Amplitude Configuration**

Configuration	Value	Description
OB_PREC	Signed 5-bit value	Pre-cursor setting C0 Range is –15 to 15
OB_POST0	Signed 6-bit value	First post-cursor setting C2 Range is –31 to 31
OB_POST1	Signed 5-bit value	Second post-cursor setting C3 Range is –15 to 15
OB_LEV	Unsigned 6-bit value	Amplitude coefficient, K = OB_LEV + 64 Range is 0 to 63
OB_POL	0 1	Non-inverting mode Inverting mode

The output buffer provides additional options to configure its behavior. These options are:

- Idle mode:
  Enabling idle mode (SERDES6G_OB_CFG.OB_IDLE) results in a remaining voltage of less than 30 mV at the buffers differential outputs.
- Slew Rate:
  Slew rate can be controlled by two configuration settings. SERDES6G_OB_CFG.OB_SR_H provides coarse adjustments whereas SERDES6G_OB_CFG.OB_SR provides fine adjustments.
- Skew control:
  In 1 Gbps SGMII mode, skew adjustment is controlled by SERDES6G_OB_CFG1.OB_ENA_CAS. Skew control is not applicable to other modes.

4.2.7 SERDES6G Clock and Data Recovery (CDR) in 100BASE-FX

To enable clock and data recovery when operating SERDES6G in 100BASE-FX mode, set the following register fields:

- SERDES6G_MISC_CFG.DES_100FX_CPMD_ENA = 1
- SERDES6G_IB_CFG.IB_FX100_ENA = 1
- SERDES6G_DES_CFG.DES_CPMD_SEL = 2

4.2.8 SERDES6G Energy Efficient Ethernet

The SERDES6G block supports Energy Efficient Ethernet as defined in IEEE 802.3az. To enable the low power modes, set SERDES6G_MISC_CFG.TX_LPI_MODE_ENA and SERDES6G_MISC_CFG.RX_LPI_MODE_ENA. At this point, the attached PCS takes full control over the high-speed output and input buffer activity.

4.2.9 SERDES6G Data Inversion

The data streams in the transmit and the receive direction can be inverted using SERDES6G_MISC_CFG.TX_DATA_INV_ENA and SERDES6G_MISC_CFG.RX_DATA_INV_ENA. This effectively allows for swapping the P and N lines of the high-speed serial link.

4.2.10 SERDES6G Signal Detection Enhancements

Signal detect information from the SERDES6G macro is normally directly passed to the attached PCS. It is possible to enable a hysteresis such that the signal detect condition must be active or inactive for a certain time before it is signaled to the attached PCS.

The signal detect assertion time (the time signal detect must be active before the information is passed to a PCS) is programmable in SERDES6G_DIG_CFG.SIGDET_AST. The signal detect de-assertion time (the time signal detect must be inactive before the information is passed to a PCS) is programmable in SERDES6G_DIG_CFG.SIGDET_DST.

4.2.11 SERDES6G High-Speed I/O Configuration Bus

The high-speed SerDes macros are configured using the high-speed I/O configuration bus (MCB), which is a serial bus connecting the configuration register set with all the SerDes macros. The HSIO::MCB_SERDES6G_ADDR_CFG register is used for SERDES6G macros. The configuration busses are used for both writing to and reading from the macros.

The SERDES6G macros are programmed as follows:

- Program the configuration registers for the SERDES6G macro. For more information about configuration options, see SERDES6G, page 18.
- Transfer the configuration from the configuration registers to one or more SerDes macros by writing the address of the macro (MCB_SERDES6G_ADDR_CFG.SERDES6G_ADDR) and initiating the write access (MCB_SERDES6G_ADDR_CFG.SERDES6G_WR_ONE_SHOT).
- The SerDes macro address is a mask with one bit per macro so that one or more macros can be programmed at the same time.
- The MCB_SERDES6G_ADDR_CFG.SERDES6G_WR_ONE_SHOT are automatically cleared when the writing is done.

The configuration and status information in the SERDES6G macros can be read as follows:

- Transfer the configuration and status from one or more SerDes macros to the configuration registers by writing the address of the macro (MCB_SERDES6G_ADDR_CFG.SERDES6G_ADDR) and initiating the read access (MCB_SERDES6G_ADDR_CFG.SERDES6G_RD_ONE_SHOT).
- The SerDes macro address is a mask with one bit per macro so that configuration and status information from one or more macros can be read at the same time. When reading from more than one macro, the results from each macro are OR'ed together.
- The MCB_SERDES6G_ADDR_CFG.SERDES6G_RD_ONE_SHOT are automatically cleared when the reading is done.

4.3 Copper Transceivers

The VSC7420-02, VSC7421-02, and VSC7422-02 devices include low-power Gigabit Ethernet transceivers. The devices include the following number of transceivers:

- VSC7420-02 includes 8 transceivers, numbered 0 through 7
- VSC7421-02 and VSC7422-02 include 12 transceivers, numbered 0 through 11

This section describes the high-level functionality and operation of the built-in transceivers. The integration is kept as close to multi-chip PHY and switch designs as possible. This allows a fast path for software already running in a similar distributed design while still benefiting from the cost savings provided by the integration.

4.3.1 Register Access

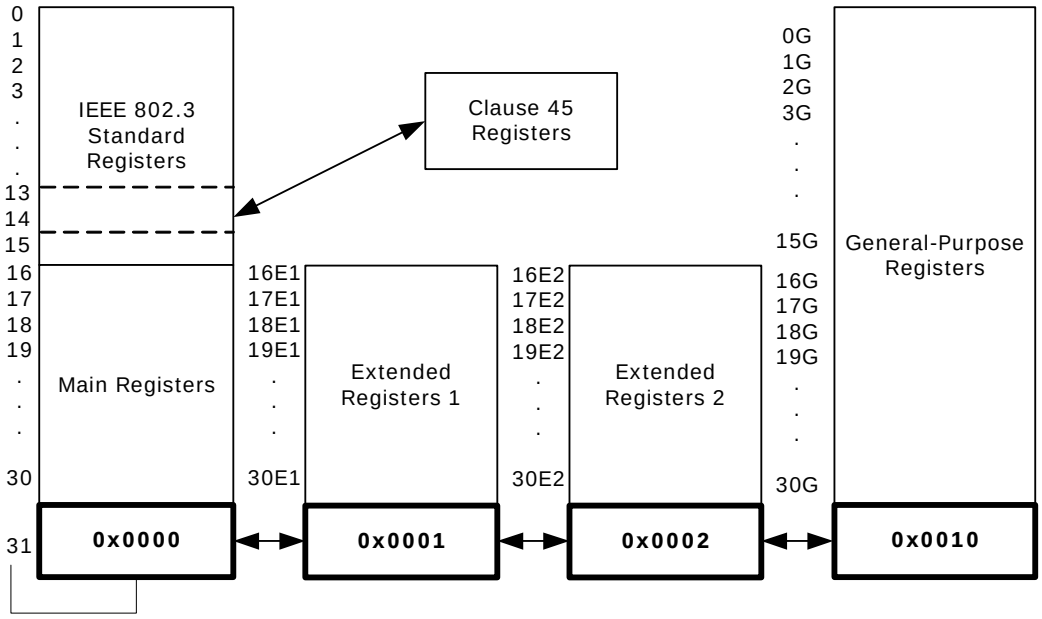
The registers of the integrated transceivers are not placed in the memory map of the switch, but are attached instead to the built-in MII management controller 0 of the devices. As a result, PHY registers are accessed indirectly through the switch registers. For more information, see MII Management Controller, page 112.

In addition to providing the IEEE 802.3 specified 16 MII Standard Set registers, the PHYs contain an extended set of registers that provide additional functionality. The devices support the following types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Two pages of extended registers with addresses from 16E1 through 30E1 and 16E2 through 30E2
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az Energy Efficient Ethernet registers

The memory mapping is controlled through PHY_MEMORY_PAGE_ACCESS::PAGE_ACCESS_CFG. The following illustration shows the relationship between the device registers and their address spaces.

Figure 5 • **Register Space Layout**



4.3.1.1 Broadcast Write

The PHYs can be configured to accept MII PHY register write operations regardless of the destination address of these writes. This is enabled in PHY_CTRL_STAT_EXT::BROADCAST_WRITE_ENA. This enabling allows similar configurations to be sent quickly to multiple PHYs without having to do repeated MII PHY write operations. This feature applies only to writes; MII PHY register read operations are still interpreted with “correct” address.

4.3.1.2 Register Reset

The PHY can be reset through software. This is enabled in PHY_CTRL::SOFTWARE_RESET_ENA. Enabling this field initiates a software reset of the PHY. Fields that are not described as sticky are returned to their default values. Fields that are described as sticky are only returned to defaults if sticky-reset is disabled through PHY_CTRL_STAT_EXT::STICKY_RESET_ENA. Otherwise, they retain their values from prior to the software reset. A hardware reset always brings all PHY registers back to their default values.

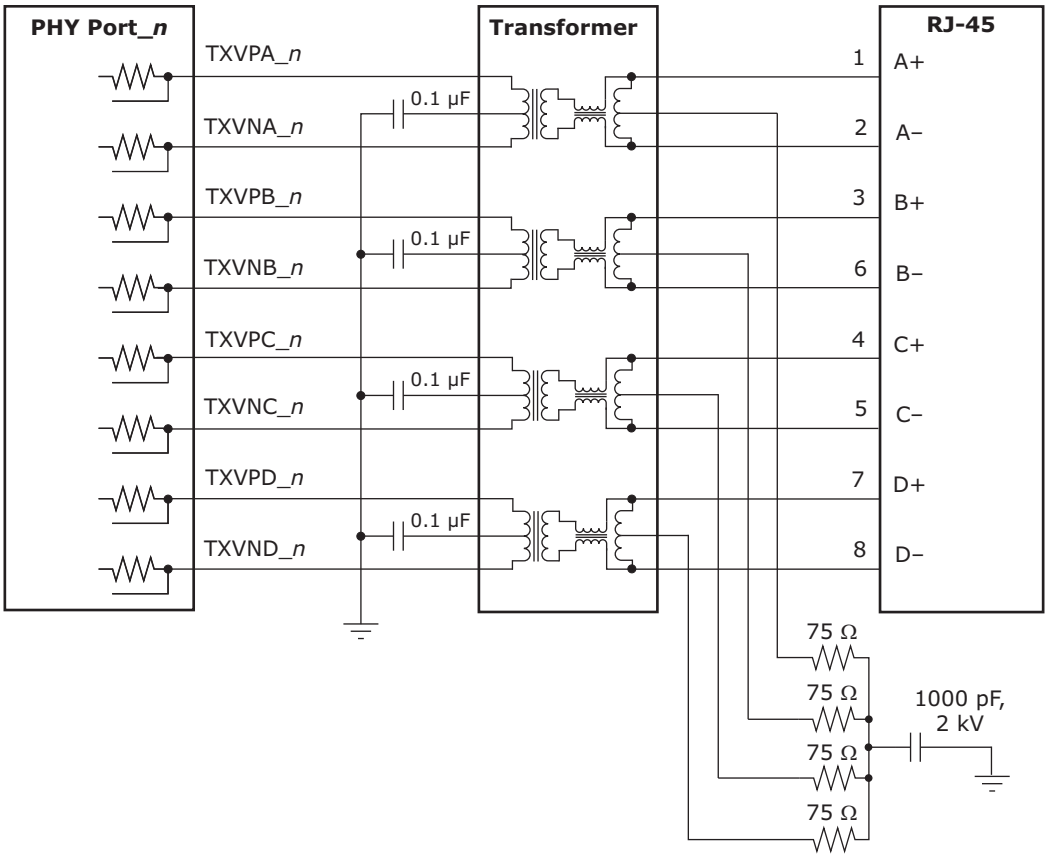
4.3.2 Cat5 Twisted Pair Media Interface

The twisted pair interfaces are compliant with IEEE 802.3-2008 and IEEE 802.3az for Energy Efficient Ethernet.

4.3.2.1 Voltage-Mode Line Driver

Unlike many other gigabit PHYs, this PHY uses a patented voltage-mode line driver that allows it to fully integrate the series termination resistors (required to connect the PHY’s Cat5 interface to an external 1:1 transformer). Also, the interface does not require placement of an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 6 • **Cat5 Media Interface**



4.3.2.2 Cat5 Autonegotiation and Parallel Detection

The integrated transceivers support twisted pair autonegotiation as defined by clause 28 of the IEEE 802.3-2008. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Auto-negotiation also allow the devices to communicate with the link partner (through the optional “next pages”) to set attributes that may not otherwise be defined by the IEEE standard.

If the Cat5 link partner does not support auto negotiation, the devices automatically use parallel detection to select the appropriate link speed.

Auto-negotiation can be disabled by clearing PHY_CTRL.AUTONEG_ENA. If auto-negotiation is disabled, the state of the SPEED_SEL_MSB_CFG, SPEED_SEL_LSB_CFG, and DUPLEX_MODE_CFG fields in the PHY_CTRL register determine the device operating speed and duplex mode. Note that while 10BASE-T and 100BASE-T do not require auto-negotiation, clause 40 defines that 1000BASE-T require auto-negotiation.

4.3.2.3 1000BASE-T Forced Mode Support

The integrated transceivers provides support for a 1000BASE-T forced test mode. In this mode, the PHY can be forced into 1000BASE-T mode and does not require manual setting of master/slave at the two ends of the link. This mode is only for test purposes. Do not use in normal operation. To configure a PHY in this mode, set PHY_EEE_CTRL.FORCE_1000BT_ENA = 1, with PHY_CTRL.SPEED_SEL_LSB_CFG = 1 and PHY_CTRL.SPEED_SEL_LSB_CFG = 0.

4.3.2.4 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the integrated transceivers include a robust automatic crossover detection feature for all three speeds on the twisted-pair interface (10BASE-

T, 100BASE-T, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with clause 40 of the IEEE 802.3-2002.

Additionally, the devices detect and correct polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. You can change the default settings using fields POL_INV_DIS and PAIR_SWAP_DIS in the PHY_BYPASS_CTRL register. Status bits for each of these functions are located in register PHY_AUX_CTRL_STAT.

The integrated transceivers can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled (PHY_CTRL.AUTONEG_ENA = 0) and the link is forced into 10/100 speeds. To enable the HP Auto-MDIX feature, set PHY_BYPASS_CTRL.FORCED_SPEED_AUTO_MDIX_DIS to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 15 • **Supported MDI Pair Combinations**

RJ-45 Pin Pairings				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

4.3.2.5 Manual MDI/MDI-X Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using PHY_EXT_MODE_CTRL.FORCE_MDI_CROSSOVER_ENA. Setting this field to 10 forces MDI, and setting 11 forces MDI-X. Leaving the bits 00 enables the MDI/MDI-X setting to be based on FORCED_SPEED_AUTO_MDIX_DIS and PAIR_SWAP_DIS in the register PHY_BYPASS_CTRL.

4.3.2.6 Link Speed Downshift

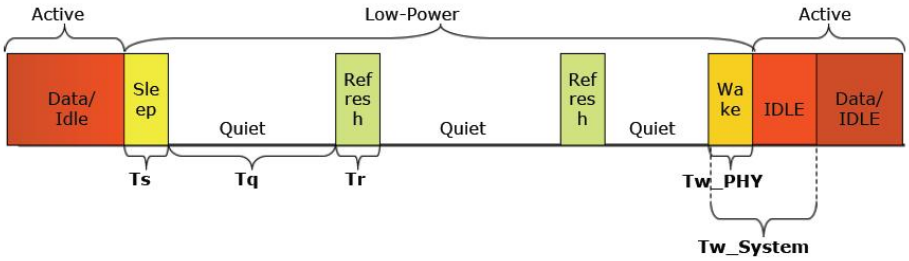
For operation in cabling environments that are incompatible with 1000BASE-T, the devices provide an automatic link speed “downshift” option. When enabled, the devices automatically change their 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to exit this state if a subsequent link partner with 1000BASE-T support is connected. This is useful in setting up in networks using older cable installations that may include only pairs A and B and not pairs C and D.

Link speed downshifting is configured and monitored using SPEED_DOWNSHIFT_STAT, SPEED_DOWNSHIFT_CFG, and SPEED_DOWNSHIFT_ENA in the register PHY_CTRL_EXT3.

4.3.2.7 Energy Efficient Ethernet

The integrated transceivers support IEEE 802.3az Energy Efficient Ethernet (EEE) currently in development. This new standard provides a method for reducing power consumption on an Ethernet link during times of low use. It uses Low Power Idles (LPI) to achieve this objective.

Figure 7 • **Energy Efficient Ethernet**



Term	Description
Sleep Time (Ts)	**Duration PHY sends Sleep symbols before going Quiet.**
Quiet Duration (Tq)	**Duration PHY remains Quiet before it must wake for Refresh period.**
Refresh Duration (Tr)	**Duration PHY sends Refresh symbols for timing recovery and coefficient synchronization.**
PHY Wake Time (Tw_PHY)	**Duration PHY takes to resume to Active state after decision to Wake.**
System Wake Time (Tw_System)	**Wait period where no data is transmitted to give the receiving system time to wake up.**

Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. Power is reduced during LPI by turning off unused circuits and, using this method, energy use scales with bandwidth utilization.

The transceivers use LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T operation. In addition, IEEE 802.3az defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V to approximately 3.3 V, peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and can fully interoperate with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the transceivers in 10BASE-Te mode, set PHY_EEE_CTRL.EEE_LPI_RX_100BTX_DIS to 1 for each port. Additional Energy Efficient Ethernet features are controlled through Clause 45 registers as defined in Clause 45 registers to Support Energy Efficient Ethernet.

4.3.3 LED Interface

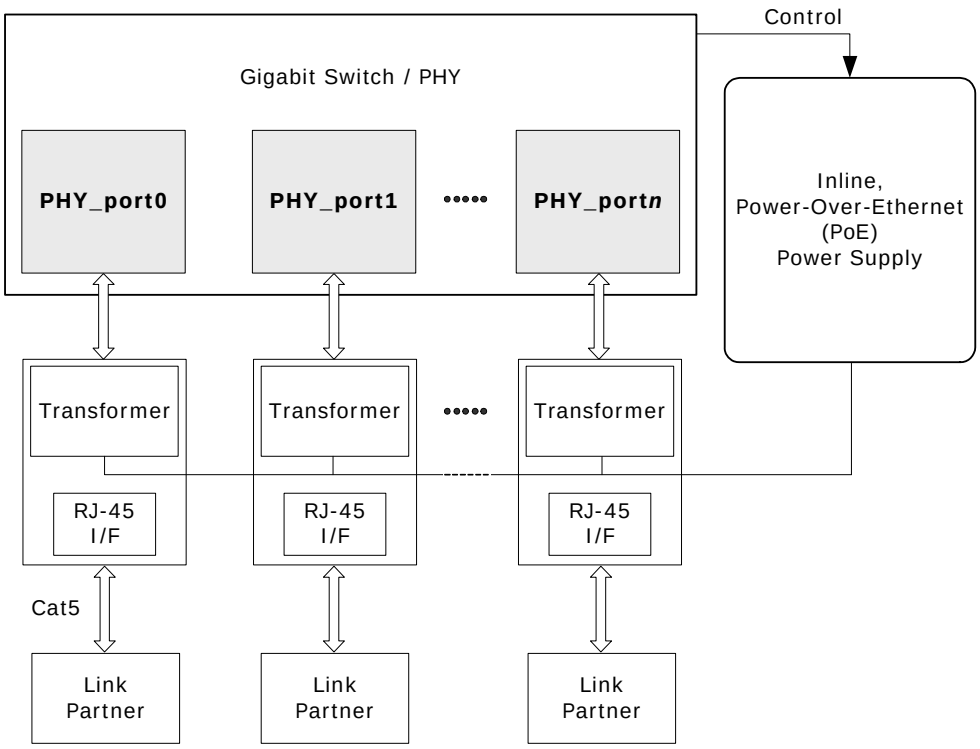
The devices also have a LED controller interface by means of the serial GPIO pins, GPIO_[3:0]. For more information, see Serial GPIO Controller, page 115.

4.3.4 Ethernet Inline Powered Devices

The integrated transceivers can detect legacy inline powered devices in Ethernet network applications. The inline powered detection capability can be part of a system that allows for IP-phone and other devices, such as wireless access points, to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a Private Branch Exchange (PBX) office switch over the telephone cabling. This can eliminate the need of an external power supply for an IP-phone. It also enables the inline powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or some other uninterruptable power source).

The following illustration shows an example of this type of application.

Figure 8 • **Inline Powered Ethernet Switch**



The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP); that is, in turn, capable of receiving inline power.

1. Enable the inline powered device detection mode on each transceiver using its serial management interface. Set PHY_CTRL_EXT4.INLINE_POW_DET_ENA to 1.
2. Ensure that the Auto-Negotiation Enable bit (register 0.12) is also set to 1. In the application, the devices send a special Fast Link Pulse (FLP) signal to the LP. Reading PHY_CTRL_EXT4.INLINE_POW_DET_STAT returns 00 during the search for devices that require Power-over-Ethernet (PoE).
3. The transceiver monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered-down state. This is reported when PHY_CTRL_EXT4.INLINE_POW_DET_STAT reads back 01. If an LP device does not loop back the FLP after a specific time, PHY_CTRL_EXT4.INLINE_POW_DET_STAT automatically resets to 10.
4. If the transceiver reports that the LP needs PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection if PHY_CTRL_EXT4.INLINE_POW_DET_STAT automatically resets to 10, and then automatically changes to its normal auto-negotiation process. A link is then auto-negotiated and established when the link status bit is set (PHY_STAT.LINK_STAT is set to 1).
6. In the event of a link failure (indicated when PHY_STAT.LINK_STAT reads 0), the inline power must be disabled to the inline powered device external to the PHY. The transceiver disables its normal auto-negotiation process and re-enables its inline powered device detection mode.

4.3.5 IEEE 802.3af PoE Support

The integrated transceivers are also compatible with switch designs intended for use in systems that supply power to Data Terminal Equipment (DTE) by means of the MDI or twisted pair cable, as described in clause 33 of the IEEE 802.3af.

4.3.6 ActiPHY™ Power Management

In addition to the IEEE-specified power-down control bit (PHY_CTRL.POWER_DOWN_ENA), the devices also include an ActiPHY power management mode for each PHY. The ActiPHY mode enables

support for power-sensitive applications. It uses a signal detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY “wakes up” at a programmable interval and attempts to wake-up the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the integrated transceivers is enabled on a per-port basis during normal operation at any time by setting PHY_AUX_CTRL_STAT.ACTIPHY_ENA to 1.

Three operating states are possible when ActiPHY mode is enabled:

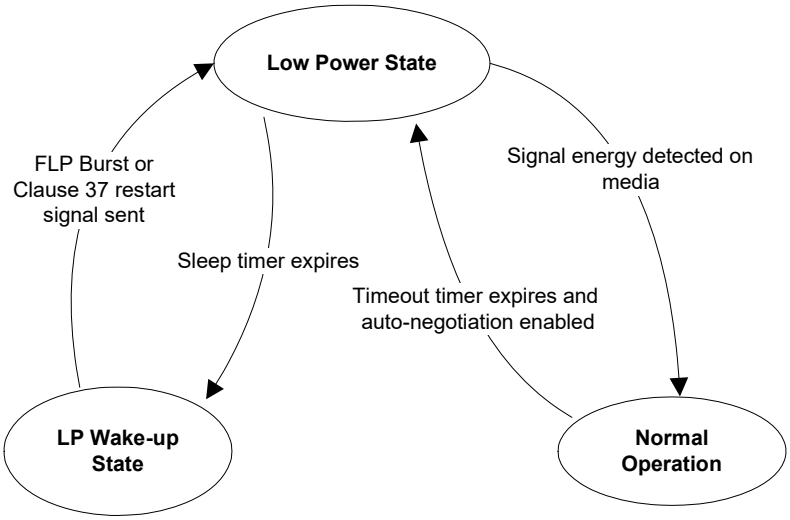
- Low power state
- LP wake-up state
- Normal operating state (link up state)

The PHY switches between the low power state and the LP wake-up state at a programmable rate (the default is two seconds) until signal energy is detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described. If auto-negotiation is disabled and the link is forced to use 10BT or 100BTX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 9 • **ActiPHY State Diagram**



4.3.6.1 Low Power State

All major digital blocks are powered down in the lower power state.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY transitions from the low power state to the LP wake-up state periodically based on the programmable sleep timer

(PHY_CTRL_EXT3.ACTIPHY_SLEEP_TIMER). The actual sleep time duration is random, from –80 ms to +60 ms, to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

After sending signal energy on the relevant media, the PHY returns to the low power state.

4.3.6.2 Link Partner Wake-up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

After sending signal energy on the relevant media, the PHY returns to the low power state.

4.3.6.3 Normal Operating State

In normal operation, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using ACTIPHY_LINK_TIMER_MSB_CFG and ACTIPHY_LINK_TIMER_LSB_CFG in the PHY_AUX_CTRL_STAT register. It then enters the low power state.

4.3.7 Testing Features

The integrated transceivers include several testing features designed to facilitate performing system-level debugging.

4.3.7.1 Core Voltage and I/O Voltage Monitor

The VSC7420-02, VSC7421-02, and VSC7422-02 device contains a monitoring circuit that provides a readout of the I/O and core supply voltages. The voltage value that is read out is accurate to within ±25 mV for the core and low voltage I/O supplies (0.9 V to 1.4 V) and ±50 mV for the high voltage I/O supplies (2.25 V to 2.75 V).

4.3.7.2 Ethernet Packet Generator (EPG)

The Ethernet Packet Generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for Copper Cat5 media to isolate problems between the MAC and the PHY, or between a local PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the PHY is connected to a live network.

To use the EPG feature, set PHY_1000BT_EPG2.EPG_ENA to 1.

When PHY_1000BT_EPG2.EPG_RUN_ENA is set to 1, the PHY begins transmitting Ethernet packets based on the settings in the PHY_1000BT_EPG1 and PHY_1000BT_EPG2 registers. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If PHY_1000BT_EPG1.TRANSMIT_DURATION_CFG is set to 0, PHY_1000BT_EPG1.EPG_RUN_ENA is cleared automatically after 30,000,000 packets are transmitted.

4.3.7.3 CRC Counters

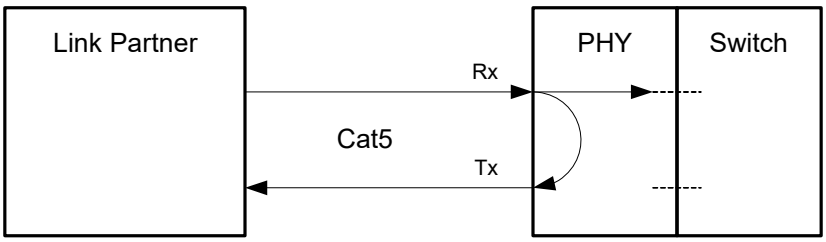
Two separate CRC counters are available in the PHY: a 14-bit good CRC counter available through PHY_CRC_GOOD_CNT.CRC_GOOD_PKT_CNT and a separate 8-bit bad CRC counter in PHY_CTRL_EXT4.CRC_1000BT_CNT.

4.3.7.4 Far-End Loopback

The far-end loopback testing feature is enabled by setting PHY_CTRL_EXT1.FAR_END_LOOPBACK_ENA to 1. When enabled, it forces incoming data from a link

partner on the current media interface, into the MAC interface of the PHY, to be re-transmitted back to the link partner on the media interface as shown in the following illustration. The incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

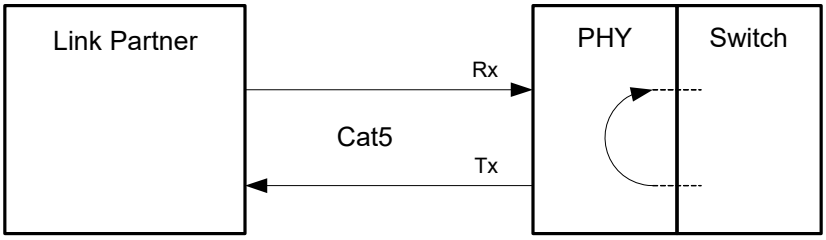
Figure 10 • **Far-End Loopback Diagram**



4.3.7.5 Near-End Loopback

When the near-end loopback testing feature is enabled (by setting PHY_CTRL.LOOPBACK_ENA to 1), data on the transmit data pins (TXD) is looped back in the PCS block, onto the device receive data pins (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network.

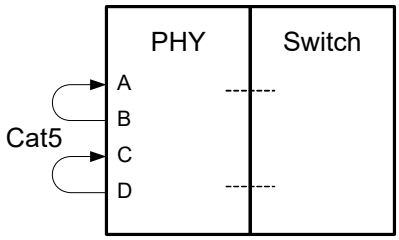
Figure 11 • **Near-End Loopback Diagram**



4.3.7.6 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using the connector loopback feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A must be connected to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 12 • **Connector Loopback Diagram**



When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required, executed in the following steps:

1. Enable the 1000BASE-T connector loopback. Set PHY_CTRL_EXT2.CON_LOOPBACK_1000BT_ENA to 1.
2. Disable pair swap correction. Set PHY_CTRL_EXT2.CON_LOOPBACK_1000BT_ENA to 1.

4.3.8 VeriPHY™ Cable Diagnostics

The VSC7420-02, VSC7421-02, and VSC7422-02 devices include a comprehensive suite of cable diagnostic functions that are available through the onboard processor. These functions enable cable operating conditions and status to be accessed and checked.

The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate common faults that can occur on the Cat5 twisted pair cabling.

For the functional details of the VeriPHY suite and operating instructions, see *ENT-AN0125, PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics Feature* Application Note.

4.4 Statistics

The following table lists the registers for the statistics module.

Table 16 • **Counter Registers**

Register	Description	Replication
SYS::STAT:CNT	Data register for reading port counters	Per counter per port
SYS::STAT_CFG.STAT_CLEAR_SHOT	Clears port counters	
SYS::STAT_CFG.STAT_CLEAR_PORT	Selects which port's counters to clear	
SYS::STAT_CFG.TX_GREEN_CNT_MODE	Controls whether to counts bytes or frames for Tx priority counters	
SYS::STAT_CFG.DROP_GREEN_CNT_MODE	Controls whether to counts bytes or frames for drop priority counters	
ANA::AGENCTRL.GREEN_COUNT_MODE ANA::AGENCTRL.RED_COUNT_MODE	Controls whether to counts bytes or frames for Rx priority counters	

All counters for all ports are sharing a common statistics block with directly addressable counters. Each counter is 32 bits wide, which is large enough to ensure a wrap-around time longer than 13 seconds.

Each switch core port has 43 Rx counters, 18 FIFO drop counters, and 31 Tx counters.

The following table defines the per-port available Rx counters and lists the counter's base address in the common statistics block.

Table 17 • **Rx Counters in the Statistics Block**

Type	Short Name	Base Address	Description
Rx	c_rx_oct	0x000	Received octets in good and bad frames.
Rx	c_rx_uc	0x001	Number of good unicasts.
Rx	c_rx_mc	0x002	Number of good multicasts.
Rx	c_rx_bc	0x003	Number of good broadcasts.
Rx	c_rx_short	0x004	Number of short frames with valid CRC (<64 bytes).
Rx	c_rx_frag	0x005	Number of short frames with invalid CRC (<64 bytes).
Rx	c_rx_jabber	0x006	Number of long frames with invalid CRC (according to MAXLEN.MAX_LENGTH).
Rx	c_rx_crc	0x007	Number of CRC errors, alignment errors and RX_ER events.
Rx	c_rx_sz_64	0x008	Number of 64-byte frames in good and bad frames.
Rx	c_rx_sz_65_127	0x009	Number of 65-127-byte frames in good and bad frames.

Table 17 • **Rx Counters in the Statistics Block *(continued)***

Type	Short Name	Base Address	Description
Rx	c_rx_sz_128_255	0x00A	Number of 128-255-byte frames in good and bad frames.
Rx	c_rx_sz_256_511	0x00B	Number of 256-511-byte frames in good and bad frames.
Rx	c_rx_sz_512_1023	0x00C	Number of 512-1023-byte frames in good and bad frames.
Rx	c_rx_sz_1024_1526	0x00D	Number of 1024-1526-byte frames in good and bad frames.
Rx	c_rx_sz_jumbo	0x00E	Number of 1527-MAXLEN.MAX_LENGTH-byte frames in good and bad frames.
Rx	c_rx_pause	0x00F	Number of received pause frames.
Rx	c_rx_control	0x010	Number of MAC control frames received.
Rx	c_rx_long	0x011	Number of long frames with valid CRC (according to MAXLEN.MAX_LENGTH).
Rx	c_rx_cat_drop	0x012	Number of frames dropped due to classifier rules.
Rx	c_rx_red_prio_0	0x013	Number of received frames classified to QoS class 0 and discarded by a policer.
Rx	c_rx_red_prio_1	0x014	Number of received frames classified to QoS class 1 and discarded by a policer.
Rx	c_rx_red_prio_2	0x015	Number of received frames classified to QoS class 2 and discarded by a policer.
Rx	c_rx_red_prio_3	0x016	Number of received frames classified to QoS class 3 and discarded by a policer.
Rx	c_rx_red_prio_4	0x017	Number of received frames classified to QoS class 4 and discarded by a policer
Rx	c_rx_red_prio_5	0x018	Number of received frames classified to QoS class 5 and discarded by a policer.
Rx	c_rx_red_prio_6	0x01A	Number of received frames classified to QoS class 6 and discarded by a policer.
Rx	c_rx_red_prio_7	0x01B	Number of received frames classified to QoS class 7 and discarded by a policer.
Rx	c_rx_green_prio_0	0x024	Number of received frames classified to QoS class 0 and marked green by a policer.
Rx	c_rx_green_prio_1	0x025	Number of received frames classified to QoS class 1 and marked green by a policer.
Rx	c_rx_green_prio_2	0x026	Number of received frames classified to QoS class 2 and marked green by a policer.
Rx	c_rx_green_prio_3	0x027	Number of received frames classified to QoS class 3 and marked green by a policer.
Rx	c_rx_green_prio_4	0x028	Number of received frames classified to QoS class 4 and marked green by a policer.
Rx	c_rx_green_prio_5	0x029	Number of received frames classified to QoS class 5 and marked green by a policer.

Table 17 • **Rx Counters in the Statistics Block *(continued)***

Type	Short Name	Base Address	Description
Rx	c_rx_green_prio_6	0x02A	Number of received frames classified to QoS class 6 and marked green by a policer.
Rx	c_rx_green_prio_7	0x02B	Number of received frames classified to QoS class 7 and marked green by a policer.

The following table defines the per-port available FIFO drop counters and lists the counter address.

Table 18 • **FIFO Drop Counters in the Statistics Block**

Type	Short Name	Base Address	Description
Drop	c_dr_local	0xC00	Number of frames discarded due to no destinations.
Drop	c_dr_tail	0xC01	Number of frames discarded due to no more memory in the queue system (tail drop).
Drop	c_dr_green_prio_0	0xC0A	Number of FIFO discarded frames classified to QoS class 0.
Drop	c_dr_green_prio_1	0xC0B	Number of FIFO discarded frames classified to QoS class 1.
Drop	c_dr_green_prio_2	0xC0C	Number of FIFO discarded frames classified to QoS class 2.
Drop	c_dr_green_prio_3	0xC0D	Number of FIFO discarded frames classified to QoS class 3.
Drop	c_dr_green_prio_4	0xC0E	Number of FIFO discarded frames classified to QoS class 4.
Drop	c_dr_green_prio_5	0xC0F	Number of FIFO discarded frames classified to QoS class 5
Drop	c_dr_green_prio_6	0xC10	Number of FIFO discarded frames classified to QoS class 6.
Drop	c_dr_green_prio_7	0xC11	Number of FIFO discarded frames classified to QoS class 7.

The following table defines the per-port available Tx counters and lists the counter address.

Table 19 • **Tx Counters in the Statistics Block**

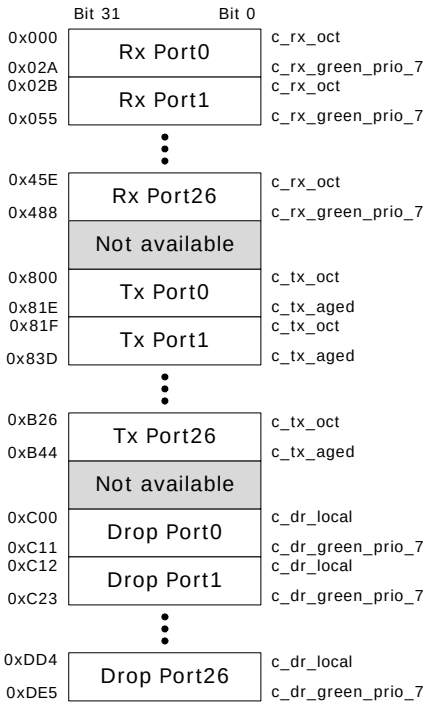
Type	Short Name	Base Address	Description
Tx	c_tx_oct	0x800	Transmitted octets in good and bad frames.
Tx	c_tx_uc	0x801	Number of good unicasts.
Tx	c_tx_mc	0x802	Number of good multicasts.
Tx	c_tx_bc	0x803	Number of good broadcasts.
Tx	c_tx_col	0x804	Number of transmitted frames experiencing a collision. An excessive collided frame gives 16 counts.
Tx	c_txdrop	0x805	Number of frames dropped due to excessive collisions or late collisions.

Table 19 • **Tx Counters in the Statistics Block *(continued)***

Type	Short Name	Base Address	Description
Tx	c_txpause	0x806	Number of transmitted pause frames in 1 Gbps full-duplex. Transmitted pause frames in 10/100 Mbps full-duplex are not counted.
Tx	c_tx_sz_64	0x807	Number of 64-byte frames in good and bad frames.
Tx	c_tx_sz_65_127	0x808	Number of 65-127-byte frames in good and bad frames.
Tx	c_tx_sz_128_255	0x809	Number of 128-255-byte frames in good and bad frames.
Tx	c_tx_sz_256_511	0x80A	Number of 256-511-byte frames in good and bad frames.
Tx	c_tx_sz_512_1023	0x80B	Number of 512-1023-byte frames in good and bad frames.
Tx	c_tx_sz_1024_1526	0x80C	Number of 1024-1526-byte frames in good and bad frames.
Tx	c_tx_sz_jumbo	0x80D	Number of 1527-MAXLEN.MAX_LENGTH-byte frames in good and bad frames.
Tx	c_tx_green_prio_0	0x816	Number of transmitted frames classified to QoS class 0
Tx	c_tx_green_prio_1	0x817	Number of transmitted frames classified to QoS class 1
Tx	c_tx_green_prio_2	0x818	Number of transmitted frames classified to QoS class 2
Tx	c_tx_green_prio_3	0x819	Number of transmitted frames classified to QoS class 3
Tx	c_tx_green_prio_4	0x81A	Number of transmitted frames classified to QoS class 4
Tx	c_tx_green_prio_5	0x81B	Number of transmitted frames classified to QoS class 5
Tx	c_tx_green_prio_6	0x81C	Number of transmitted frames classified to QoS class 6
Tx	c_tx_green_prio_7	0x81D	Number of transmitted frames classified to QoS class 7
Tx	c_tx_aged	0x81E	Number of frames dropped due to frame aging.

The counters are placed in a directly addressable RAM as shown in the following illustration.

Figure 13 • **Counter Layout**



The reading of a counter uses direct addressing. The following shows the address to use when reading a given counter for a port:

- Rx counter: Rx counter's base address + 43*port
- Tx counter: Tx counter's base address + 31*port
- Drop counter: Drop counter's base address + 18*port

For information about Rx counter base addresses, see Table 17, page 33. For information about Tx counter base addresses, see Table 19, page 35. For information about drop counter base addresses, see Table 18, page 35.

Writing to register STAT_CFG.STAT_CLEAR_SHOT clears all associated counters in the port module specified in STAT_CFG.STAT_CLEAR_PORT.

It is possible to select whether to count frames or bytes for the following specific counters:

- The Rx priority counters (c_rx_red_prio_*, c_rx_green_prio_*, where x is 0 through 7).
- The Tx priority counters (c_tx_green_prio_*, where x is 0 through 7).
- The Drop priority counters (c_dr_green_prio_*, where x is 0 through 7).

The Rx priority counters are programmed through ANA::AGENCTRL, and the Tx and drop priority counters are programmed through SYS::STAT_CFG. When counting bytes, the frame length excluding inter frame gap and preamble is counted.

For testing purposes, all counters are both readable and writable. All counters wrap around to 0 when reaching the maximum.

For more information about how the counters map to relevant MIBs, see Port Counters, page 128.

4.5 Classifier

The switch core includes a common classifier, which determines a number of properties affecting the forwarding of each frame through the switch. These properties are:

- Frame acceptance filtering – Drop illegal frame types.
- QoS classification – Assign one of eight QoS classes to the frame.
- DSCP classification - Assign one of 64 DSCP values to the frame.
- VLAN classification – Extract tag information from the frame or use the port VLAN.

- Link aggregation code generation – Generate the link aggregation code.
- CPU forwarding determination – Determine CPU Forwarding and CPU extraction queue number

4.5.1 General Data Extraction Setup

This section provides information about the overall settings for data extraction controlling the other tasks in the classifier, analyzer, and rewriter.

The following table lists the registers associated with general data extraction.

Table 20 • **General Data Extraction Registers**

Register	Description	Replication
SYS::PORT_MODE.L3_PARSE_CFG	Enables the use of Layer 3 and 4 protocol information for classification and frame processing.	Per port
SYS::VLAN_ETYPE_CFG	Ethernet Type for S-tags in addition to default value 0x88A8.	None
ANA:PORT.VLAN_CFG.VLAN_INNER_TAG_ENA	Enables using inner VLAN tag for basic classification if available in incoming frame.	Per port

In the devices, it is programmable which VLAN tags are recognized. The use of Layer-3 and Layer-4 information for classification and forwarding can also be controlled.

The devices recognize three different VLAN tags:

- Customer tags (C-TAGs), which use TPID 0x8100.
- Service tags (S-TAGs), which use TPID 0x88A8 (IEEE 802.1ad).
- Service tags (S-TAGs), which use a custom TPID programmed in SYS::VLAN_ETYPE_CFG.

The devices can parse and use information from up to two VLAN tags of any of the kinds described above.

By default, the outer VLAN tag is extracted and used for the classification. However, there is an option to use the inner VLAN tag instead for frames with at least two VLAN tags. This is controlled in VLAN_CFG.VLAN_INNER_TAG_ENA and affects both QoS and VLAN classification as well as the frame acceptance filter.

Various blocks in the devices use Layer-3 and Layer-4 information for classification and forwarding. Layer-3 and Layer-4 information can be extracted from a frame with up to two VLAN tags. Frames with more than two VLAN tags are considered non-IP frames.

The actual use of Layer-3 and Layer-4 information for classification, forwarding, and rewriting is enabled in SYS::PORT_MODE.L3_PARSE_CFG. The following blocks are affected by this functionality:

- Classification: QoS and DSCP classification, link aggregation code generation, CPU forwarding
- Analyzer: Flooding and forwarding of IP multicast frames
- Rewriter: Rewriting of IP information

4.5.2 Frame Acceptance Filtering

The following table lists the registers associated with frame acceptance filtering.

Table 21 • **Frame Acceptance Filtering Registers**

Register	Description	Replication
PORT::PORT_MISC	Configures forwarding of special frames	Per port

Table 21 • **Frame Acceptance Filtering Registers *(continued)***

Register	Description	Replication
ANA:PORT:DROP_CFG	Configures discarding of illegal frame types	Per port

Based on the configurations in the DROP_CFG and PORT_MISC registers, the classifier instructs the queue system to drop or forward certain frames types, such as:

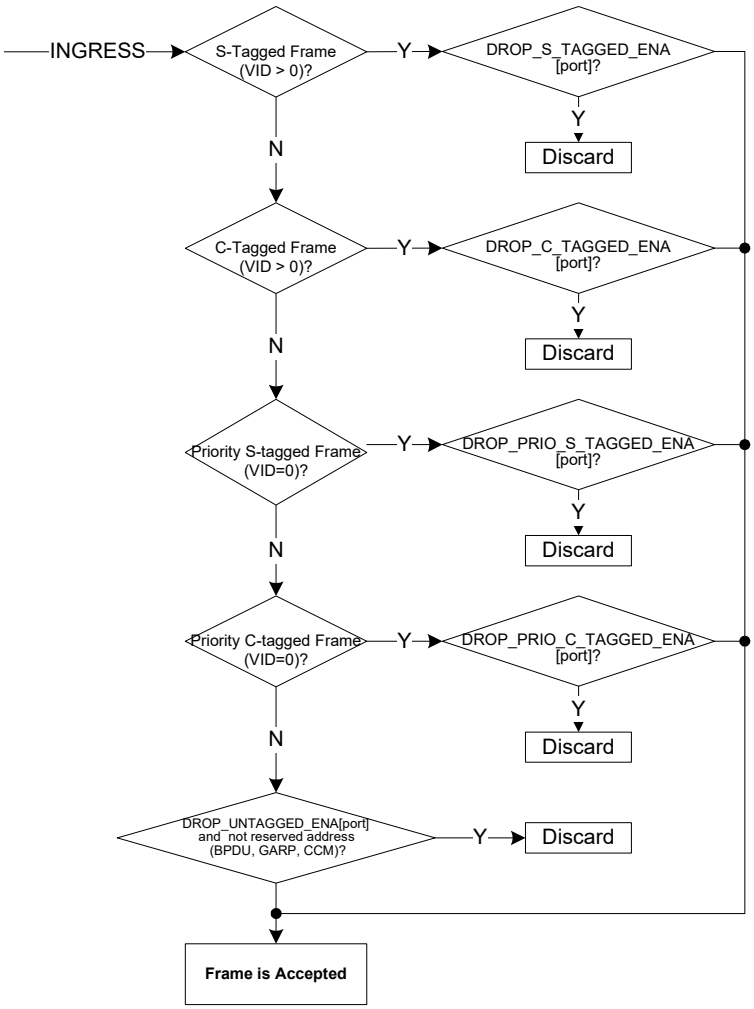
- Frames with a multicast source MAC address
- Frames with a null source or null destination MAC address (address = 0x000000000000)
- Frames with errors signaled by the MAC (for example, an FCS error)
- MAC control frames
- Pause frames after flow control processing in the MAC.
- Untagged frames (excluding frames with reserved destination MAC addresses from the BPDU, GARP, and Link trace/CCM address ranges).
- Priority S-tagged frames
- Priority C-tagged frames
- VLAN S-tagged frames
- VLAN C-tagged frames

By default, MAC control frames, pause frames, and frames with errors are dropped by the classifier.

The VLAN acceptance filter decides whether a frame's VLAN tagging is allowed on the port. By default, the outer VLAN tag is used as input to the filter, however, there is an option to use the inner VLAN tag instead for double tagged frames (VLAN_CFG.VLAN_INNER_TAG_ENA).

The following illustration shows the flowchart for the VLAN acceptance filter.

Figure 14 • **VLAN Acceptance Filter**



If the frame is accepted by the VLAN acceptance filter, it can still be discarded in other places of the switch, such as:

- Policers, due to traffic exceeding a peak information rate.
- Analyzer, due to forwarding decisions such as VLAN ingress filtering.
- Queue system, due to lack of resources, frame aging, or excessive collisions.

4.5.3 QoS and DSCP Classification

This section provides information about the functions in the QoS and DSCP classification. The two tasks are described one, because the tasks have a significant amount of functionality in common.

The following table lists the registers associated with QoS and DSCP classification.

Table 22 • **QoS and DSCP Classification Registers**

Register	Description	Replication
ANA.PORT.QOS_CFG	Configuration of the overall classification flow for QoS and DSCP.	Per port
ANA:PORT:QOS_PCP_DEI_MAP_CFG	Mapping from (DEI, PCP) to (QoS).	Per port per DEI per PCP

Table 22 • **QoS and DSCP Classification Registers *(continued)***

Register	Description	Replication
ANA::DSCP_CFG	DSCP configuration per DSCP value.	Per DSCP
ANA::DSCP_REWR_CFG	DSCP rewrite values per QoS class.	Per QoS

The classification provides the user with control of the QoS and DSCP classification algorithm. The result of the basic classification are the following frame properties, which follow the frame through the switch:

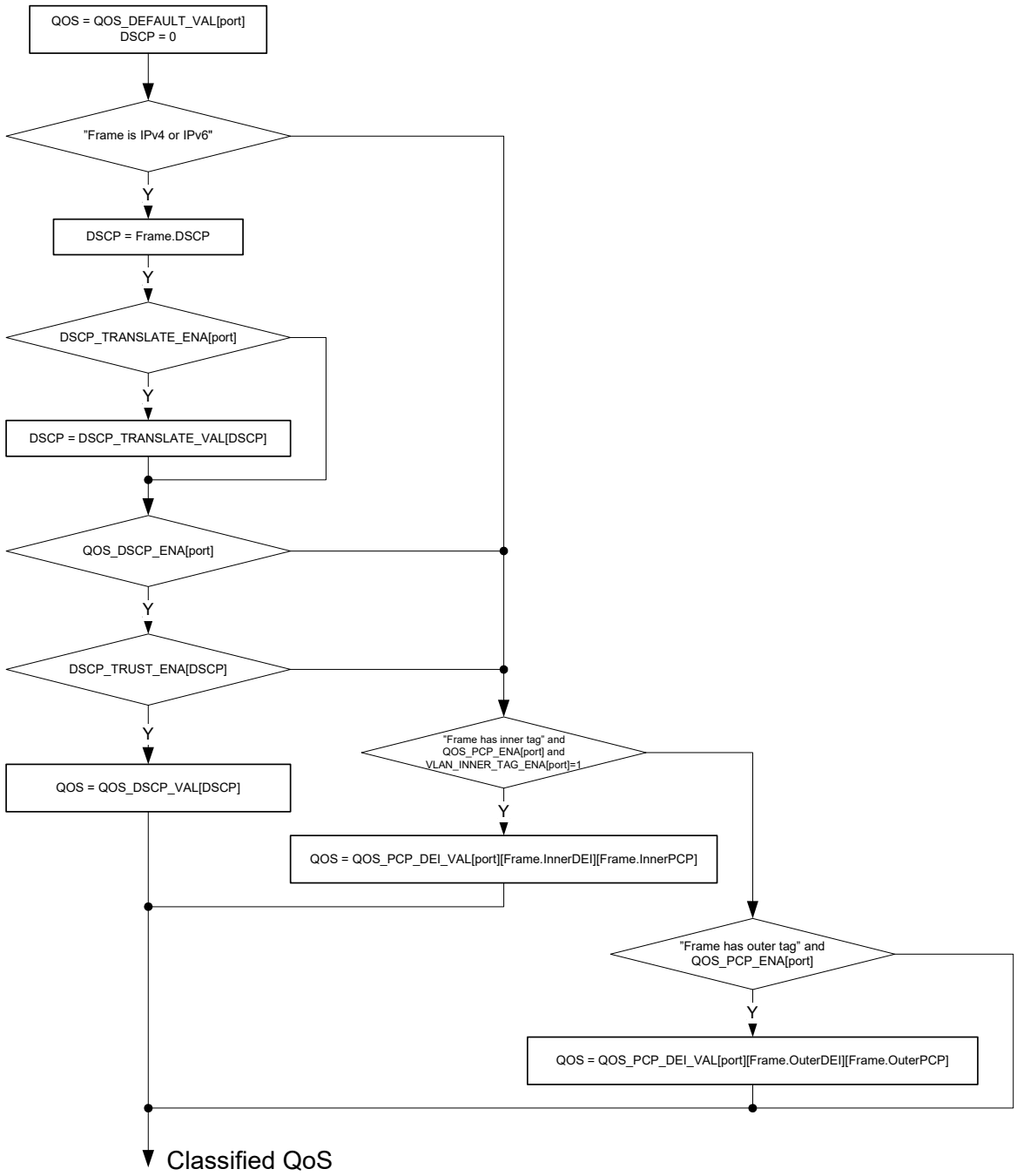
- The frame's QoS class. This class is encoded in a 3-bit field, where 7 is the highest priority QoS class and 0 is the lowest priority QoS class. The QoS class is used by the queue system when enqueuing frames and when evaluating resource consumptions, for policing, statistics, and rewriter actions.
- The frame's DSCP. This value is encoded in a 6-bit fields. The DSCP value is forwarded with the frame to the rewriter where it is translated and rewritten into the frame. The DSCP value is only applicable to IPv4 and IPv6 frames.

The classifier looks for the following fields in the incoming frame to determine the QoS and DSCP classification:

- Port default QoS class. The default DSCP value is the frame's DSCP value. For non-IP frames, the DSCP is 0 and it not used elsewhere in the switch.
- Priority Code Point (PCP) when the frame is VLAN tagged or priority tagged. There is an option to use the inner tag for double tagged frames (VLAN_CFG.VLAN_INNER_TAG_ENA). Both S-tagged and C-tagged frames are considered.
- Drop Eligible Indicator (DEI) when the frame is VLAN tagged or priority tagged. There is an option to use the inner tag for double tagged frames (VLAN_CFG.VLAN_INNER_TAG_ENA). Both S-tagged and C-tagged frames are considered.
- DSCP (all 6 bits, both for IPv4 and IPv6 packets). The classifier can look for the DSCP value behind up to two VLAN tags.

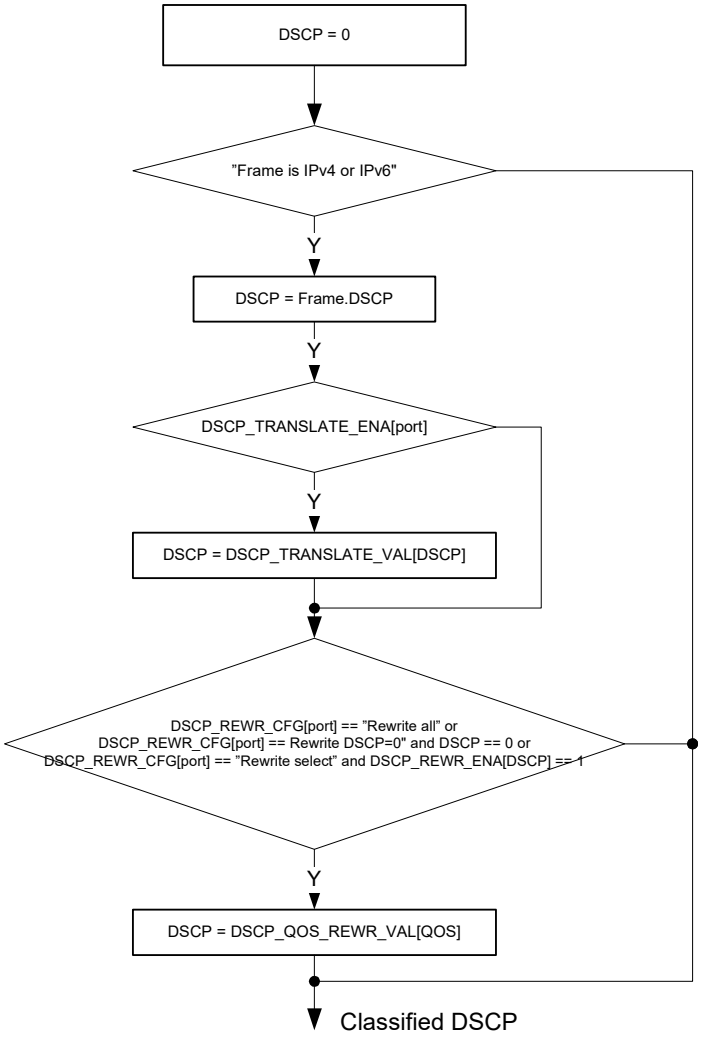
The following illustration shows the flow chart of QoS classification.

Figure 15 • **QoS Classification Flow Chart**



The following illustration shows the flow chart for DSCP classification.

Figure 16 • **DSCP Classification Flow Chart**



The translation part of the DSCP classification is common for both QoS and DSCP classification.

4.5.4 VLAN Classification

The following table lists the registers associated with VLAN classification.

Table 23 • **VLAN Configuration Registers**

Register	Description	Replication
ANA:PORT:VLAN_CFG	Configures the port's processing of VLAN information in VLAN-tagged and priority-tagged frames. Configures the port-based VLAN.	Per port

The VLAN classification determines a tag header for all frames. The tag header includes the following information:

- Priority Code Point (PCP)
- Drop Eligible Indicator (DEI)
- VLAN Identifier (VID)
- Tag Protocol Identifier (TPID) type (TAG_TYPE). This field informs whether tag used for classification was a C-tag or an S-tag.

The tag header determined by the classifier is carried with the frame through the switch and is used in various places such as the analyzer for forwarding and the rewriter for egress tagging operations.

The devices recognize three kinds of tags based on the TPID, which is the EtherType in front of the tag:

- Customer tags (C-TAGs), which use TPID 0x8100.
- Service tags (S-TAGs), which use TPID 0x88A8 (IEEE 802.1ad).
- Service tags (S-TAGs), which use a custom TPID programmed in SYS::VLAN_ETYPE_CFG.

For customer tags and service tags, both VLAN tags (tags with nonzero VID) and priority tags (tags with VID = 0) are processed.

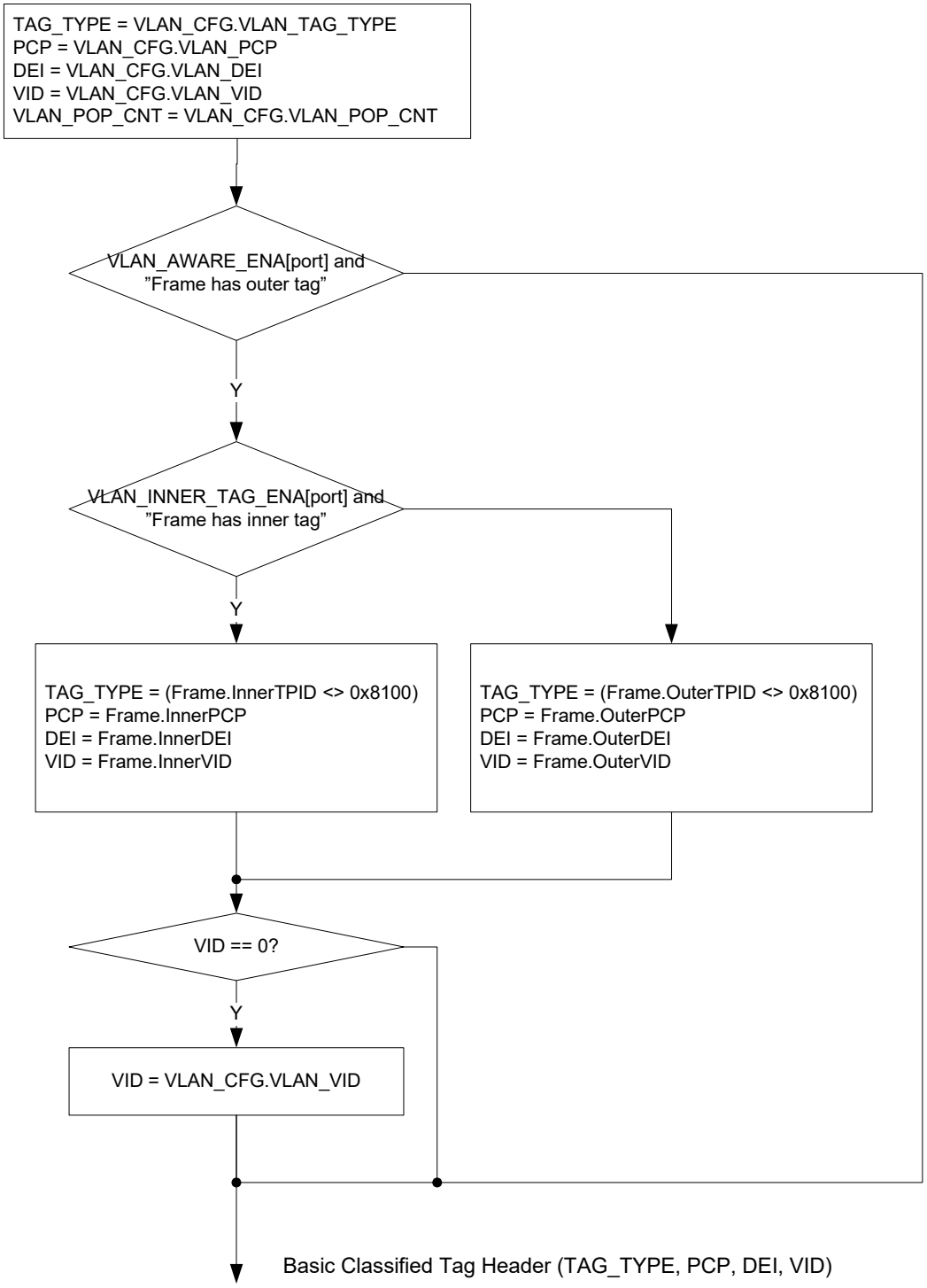
The tag header is either retrieved from a tag in the incoming frame or from a default port-based tag header. The port-based tag header is configured in ANA:PORT:VLAN_CFG.

For double tagged frames, there is an option to use the inner tag instead of the outer tag (VLAN_CFG.VLAN_INNNER_TAG_ENA).

In addition to the tag header, the ingress port decides the number of VLAN tags to pop at egress (VLAN_POP_CNT). If the configured number of tags to pop is greater than the actual number of tags in the frame, the number is reduced to the number of actual tags in the frame.

The following illustration shows the flow chart for basic VLAN classification.

Figure 17 • **Basic VLAN Classification Flow Chart**



4.5.5 Link Aggregation Code Generation

This section provides information about the functions in link aggregation code generation.

The following table lists the registers associated with aggregation code generation.

Table 24 • **Aggregation Code Generation Registers**

Register	Description	Replication
ANA::AGGR_CFG	Configures use of Layer-2 through Layer-4 flow information for link aggregation code generation.	Common

The classifier generates a link aggregation code, which is used in the analyzer when selecting to which port in a link aggregation group a frame is forwarded.

The following contributions to the link aggregation code is configured in the AGGR_CFG register:

- Destination MAC address—use the lower 12 bits of the DMAC.
- Source MAC address—use the lower 12 bits of the SMAC.
- IPv6 flow label—use the 20 bits of the flow label.
- IPv4 source and destination IP addresses—use the lower 8 bits of the SIP and DIP.
- TCP/UDP source and destination port for IPv4 and IPv6 frames—use the lower 8 bits of the SPORT and DPORT.
- Random aggregation code—use a pseudo-random number instead of the frame information.

Each of the enabled contributions are XOR'ed together, yielding a 4-bit aggregation code ranging from 0 to 15. For more information about how the aggregation code is used, see Link Aggregation, page 153.

4.5.6 CPU Forwarding Determination

The following table lists the registers associated with CPU forwarding.

Table 25 • **CPU Forwarding Determination**

Register	Description	Replication
CPU_FWD_CFG	Enables CPU forwarding for various frame types	Per port
CPU_FWD_BPDU_CFG	Enables CPU forwarding per BPDU address	Per port
CPU_FWD_GARP_CFG	Enables CPU forwarding per GARP address	Per port
CPU_FWD_CCM_CFG	Enables CPU forwarding per CCM/Link trace address	Per port
CPUQ_CFG	CPU extraction queues for various frame types	None
CPUQ_8021_CFG	CPU extraction queues for BPDU, GARP, and CCM addresses.	None

The classifier has support for determining whether certain frames must be forwarded to the CPU extraction queues. Other parts of the device can also determine CPU forwarding, for example, the analyzer, based on MAC table entries. All events leading to CPU forwarding are OR'ed together, and the final CPU extraction queue mask, which is available to the user, contains the sum of all events leading to CPU extraction. For more information, see CPU Extraction and Injection, page 162.

Upon CPU forwarding by the classifier, the frame type determines whether the frame is redirected or copied to the CPU. Any frame type or event causing a redirection to the CPU cause all front ports to be removed from the forwarding decision - only the CPU receives the frame. When copying a frame to the CPU, the normal forwarding of the frame is unaffected.

The following table lists the frame types, with respect to CPU forwarding, that are recognized by the classifier.

Table 26 • **Frame Type Definitions for CPU Forwarding**

Frame	Condition	Copy/Redirect
BPDU frames. Reserved Addresses (IEEE 802.1D 7.12.6)	DMAC = 0x0180C2000000 to 0x0180C20000F (BPDUs and various Slow protocols supporting spanning tree, link aggregation, port authentication)	Redirect
Reserved ALLBRIDGE address	DMAC = 0x0180C2000010	Redirect
GARP Application Addresses (IEEE 802.1D 12.5)	DMAC = 0x0180C2000020 to 0x0180C200002F	Redirect
CCM/Link Trace Addresses (IEEE P802.1ag)	DMAC = 0x0180C2000030 to 0x0180C200003F	Redirect
IGMP	DMAC = 0x01005E000000 to 0x01005E7FFFFF EtherType = IPv4 IP Protocol = IGMP	Redirect
MLD	DMAC = 0x333300000000 to 0x3333FFFFFFFF EtherType = IPv6 IPv6 Next Header = 0 Hop-by-hop options header with the first option being a Router Alert option with the MLD message (Option Type = 5, Opt Data Len = 2, Option Data = 0).	Redirect
IPv4 Multicast Ctrl	DMAC = 0x01005E000000 to 0x01005E7FFFFF EtherType = IPv4 IP protocol is not IGMP IPv4 DIP inside 224.0.0.x	Copy
Source port	All frames received on enabled ingress port	Copy
All other frames		

4.6 Analyzer

The analyzer module is responsible for a number of tasks:

- Determining the set of destination ports, also known as the forwarding decision, for frames received by port modules. This includes Layer-2 forwarding, CPU-forwarding, mirroring, and SFlow sampling.
- Keeping track of network stations and their MAC addresses through MAC address learning and aging.
- Holding VLAN membership information (configured by CPU) and applying this to the forwarding decision.

The analyzer consists of three main blocks:

- MAC table
- VLAN table
- Forwarding Engine

The MAC and VLAN tables are the main databases used by the forwarding engine. The forwarding engine determines the forwarding decision and initiates learning in the MAC table when appropriate.

The analyzer operates on analyzer requests initiated by the port modules. For each received frame, the port module requests the analyzer to determine the forwarding decision.The analyzer request contains the following frame information:

- Destination and source MAC addresses.
- Physical port number where the frame was received (referred to as PPORT).
- Logical port number where the frame was received (referred to as LPORT).
  By default, LPORT and PPORT are the same. However, when using link aggregation, multiple physical ports map to the same logical port. The LPORT value for each physical port is configured in ANA:PORT:PORT_CFG.PORTID_VAL in the analyzer.
- Frame properties derived by the classifier:
  Classified VID
  Link aggregation code
  Basic CPU forwarding
  CPU forwarding for special frame types determined by the classifier

Based on this information, the analyzer determines an analyzer reply, which is returned to the ingress port modules. The analyzer reply contains:

- The forwarding decision (referred to as DEST). This mask contains 27 bits, 1 bit for each front port and the CPU port.
- The final CPU extraction queue mask (referred to as CPUQ). This mask contains 8 bits, 1 bit for each CPU extraction queue.

The terms PPORT, LPORT, DEST and CPUQ, as previously defined, are used throughout the remainder of this section.

4.6.1 MAC Table

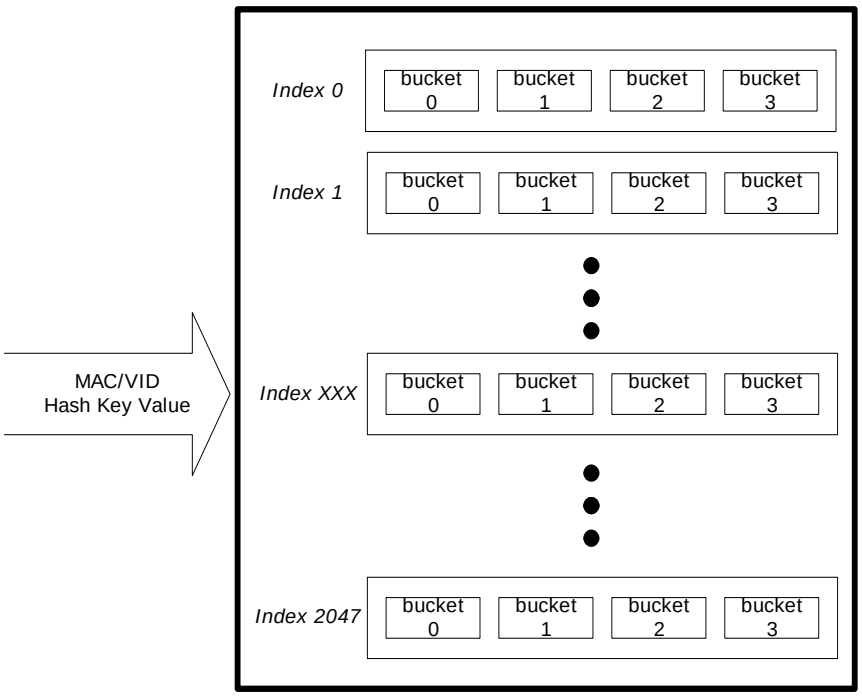
This section provides information about the MAC table block in the analyzer. The following table lists the registers associated with MAC table access.

Table 27 • **MAC Table Access**

Register	Description	Replication
MACHDATA	MAC address and VID when accessing the MAC table.	None
MACLDATA	MAC address when accessing the MAC table.	None
MACTINDX	Direct address into the MAC table for direct read and write.	None
MACACCESS	Flags and command when accessing the MAC table.	None
MACTOPTIONS	Flags when accessing the MAC table	None
AUTOAGE	Age scan period.	None
AGENCTRL	Controls the default values for new entries in MAC table.	None
ENTRYLIM	Controls limits on number of learned entries per port	Per port
LEARNDISC	Counts the number of MAC table entries not learned due lack of storage in the MAC table	None

The analyzer contains a MAC table with 8192 entries containing information about stations learned by the devices. The table is organized as a hash table with four buckets and 2048 rows. Each row is indexed by an 11-bit hash value, which is calculated based on the station's (MAC, VID) pair, as shown in the following illustration.

Figure 18 • **MAC Table Organization**



The following table lists the fields for each entry in the MAC table.

Table 28 • **MAC Table Entry**

Field	Bits	Description
VALID	1	Entry is valid.
MAC	48	The MAC address of the station (primary key).
VID	12	VLAN identifier that the station is learned with (primary key).
DEST_IDX	6	Destination mask index pointing to a destination mask in the destination mask table (PGID entries 0 through 63).
IP6_MASK	3	Partial IPv6 multicast destination port mask. See IPv6 Multicast Entries, page 52.
ENTRY_TYPE	2	Entry type: 0: Normal entry subject to aging. 1: Normal entry not subject to aging (locked). 2: IPv4 multicast entry not subject to aging. Full port set is encoded in MAC table entry. 3: IPv6 multicast entry not subject to aging. Full port set is encoded in MAC table entry.
AGED_FLAG	1	Entry is aged once by an age scan. See Age Scan, page 50.
MAC_CPU_COPY	1	Copy frames from or to this station to the CPU.
SRC_KILL	1	Do not forward frames from this station. **Note** This flag is not used for destination lookups.
IGNORE_VLAN	1	Do not use the VLAN_PORT_MASK from the VLAN table when forwarding frames to this station.

Entries in the MAC table can be added, deleted, or updated in three ways:

- Hardware-based learning of source MAC addresses (that is, inserting new (MAC, VID) pairs in the MAC table).
- Age scans (setting AGED_FLAG and deleting entries.)
- CPU commands (for example, for CPU-based learning.)

4.6.1.1 Hardware-Based Learning

The analyzer adds an entry to the MAC table when learning is enabled, and the MAC table does not contain an entry for a received frame's (SMAC, VID). The new entry is formatted as follows:

- VALID is set
- MAC is set to the frame's SMAC
- VID set to the frame's VID
- ENTRY_TYPE is set to 0 (normal entry subject to aging)
- DEST_IDX is set to the frame's LPORT
- MAC_CPU_COPY is set to AGENCTRL.LEARN_CPU_COPY
- SRC_KILL is set to AGENCTRL.LEARN_SRC_KILL
- IGNORE_VLAN is set to AGENCTRL.LEARN_IGNORE_VLAN
- All other fields are cleared

When a frame is received from a known station, that is, the MAC table already contains an entry for the received frame's (SMAC, VID), the analyzer can update the entry as follows.

For entries of entry type 0 (unlocked entries):

- The AGED_FLAG is cleared. This implies the station is active, avoiding the deletion of the entry due to aging.
- If the existing entry's DEST_IDX differs from the frame's LPORT, then the entry's DEST_IDX is set to the frame's LPORT. This implies the station has moved to a new port.

For entries of entry type 1 (locked entries):

- The AGED_FLAG is cleared. This implies the station is active.

Entries of entry types 2 and 3 are never updated, because their multicast MAC addresses are never used as source MAC addresses.

For more information about learning, see SMAC Analysis, page 60.

4.6.1.2 Age Scan

The analyzer scans the MAC table for inactive entries. An age scan is initiated by either a CPU command or automatically performed by the device with a configurable age scan period (AUTOAGE). The age scan checks the flag AGED_FLAG for all entries in the MAC table. If an entry's AGED_FLAG is already set and the entry is of entry type 0, the entry is removed. If the AGED_FLAG is not set, it is set to 1. The flag is cleared when receiving frames from the station identified by the MAC table entry. For more information, see Hardware-Based Learning, page 50.

4.6.1.3 CPU Commands

The following table lists the set of commands that a CPU can use to access the MAC table. The MAC table command is written to MACACCESS.MAC_TABLE_CMD. Some commands require the registers MACLDATA, MACHDATA, and MACTINDX to be preloaded before the command is issued. Some commands return information in MACACCESS, MACLDATA, and MACHDATA.

Table 29 • **MAC Table Commands**

Command	Purpose	Use
LEARN	Insert/learn new entry in MAC table. Position given by (MAC, VID)	Configure MAC and VID of the new entry in MACHDATA and MACLDATA. Configure remaining entry fields in MACACCESS. The location in the MAC table is calculated based on (MAC, VID).
FORGET	Delete/unlearn entry given by (MAC, VID)	Configure MAC and VID in MACHDATA and MACLDATA.

Table 29 • **MAC Table Commands *(continued)***

Command	Purpose	Use
AGE	Start age scan	No preload required. Issue command.
READ	Read entry pointed to by (row, column)	Configure row (0-2047) and column (0-3) of the entry to read in: MACTINDX.INDEX (row) MACTINDX.BUCKET (column) MACACCESS.VALID must be 0. When MAC_TABLE_CMD changes to IDLE, MACHDATA, MACLDATA, and MACACCESS contain the information read.
LOOKUP	Lookup entry pointed to by (MAC, VID)	Configure MAC and VID of station to look up in MACHDATA and MACLDATA. MACACCESS.VALID must be 1. Issue a READ command. When MAC_TABLE_CMD changes to IDLE, success of the lookup is indicated by MACACCESS.VALID. If successful, MACACCESS contains the entry information.
WRITE	Write entry, MAC table position given by (row, column)	Configure MAC and VID of the new entry in MACHDATA and MACLDATA. Configure remaining entry fields in MACACCESS. The location in the MAC table is given by row and column in MACTINDX.
INIT	Initialize the table	No preload required. Issue command.
GET_NEXT	Get the smallest entry in the MAC table numerically larger than the specified (MAC, VID). The VID and MAC are evaluated as a 60-bit number with the VID being most significant.	Configure MAC and VID of the starting point for the search in MACHDATA and MACLDATA. When MAC_TABLE_CMD changes to IDLE, success of the search is indicated by MACACCESS.VALID. If successful, MACHDATA, MACLDATA, and MACACCESS contain the information read.
IDLE	Indicate that MAC table is ready for new command	

4.6.1.4 Known Multicasts

From a CPU, entries can be added to the MAC table with any content. This makes it possible to add a known multicast address with multiple destination ports:

- Set the MAC and VID in MACHDATA and MACLDATA
- Set MACACCESS.ENTRY_TYPE = 1 because this is not an entry subject to aging.
- Set MACACCESS.AGED_FLAG to 0.
- Set MACACCESS.DEST_IDX to an unused value.
- Set the destination mask in the destination mask table pointed to by DEST_IDX to the desired ports.

Example All frames in VLAN 12 with MAC address 0x010000112233 are to be forwarded to ports 8, 9, and 12.

This is done by inserting the following entry in the MAC table:

VID = 12
MAC = 0x010000112233
ENTRY_TYPE = 1
VALID = 1

AGED_FLAG = 0
DEST_IDX = 40

and configuring the destination mask table:

PGID[40 = 0x1300.

IPv4 and IPv6 multicast entries can be programmed differently without using the destination mask table. This is described in the following subsection.

4.6.1.5 IPv4 Multicast Entries

MAC table entries with the ENTRY_TYPE = 2 settings are interpreted as IPv4 multicast entries.

IPv4 multicasts entries match IPv4 frames, which are classified to the specified VID, and which have DMAC = 0x01005Exxxxxx, where xxxxxx is the lower 24 bits of the MAC address in the entry.

Instead of a lookup in the destination mask table (PGID), the destination set is set to the lower 2 bits of the DEST_IDX value concatenated with the upper 24 bits of the entry MAC address. This is shown in the following table.

Table 30 • **IPv4 Multicast Destination Mask**

Destination Ports	Record Bit Field
Ports 23-0	MAC[47-24]
Ports 25-24	DEST_IDX[1-0]

Example All IPv4 multicast frames in VLAN 12 with MAC 01005E112233 are to be forwarded to ports 8, 9, and 12. This is done by inserting the following entry in the MAC table entry:

VALID = 1
VID = 12
MAC = 0x001300112233
ENTRY_TYPE = 2
DEST_IDX = 0

4.6.1.6 IPv6 Multicast Entries

MAC table entries with the ENTRY_TYPE = 3 settings are interpreted as IPv6 multicast entries:

IPv6 multicasts entries match IPv6 frames, which are classified to the specified VID, and which have DMAC=0x3333xxxxxxxx, where xxxxxxxx is the lower 32 bits of the MAC address in the entry.

Instead of a lookup in the destination mask table (PGID), the destination set is set to AGED_FLAG field concatenated with the IP6_MASK field, the DEST_IDX field and the upper 16 bits the MAC field. This is shown in the following table.

Table 31 • **IPv6 Multicast Destination Mask**

Destination Ports	Record Bit Field
Port 25	AGED_FLAG
Ports 24-22	IP6_MASK
Ports 21-16	DEST_IDX
Ports 15-0	MAC [47-32]

Example All IPv6 multicast frames in VLAN 12 with MAC 333300112233 are to be forwarded to ports 8, 9, and 12.

This is done by inserting the following entry in the MAC table entry:

VID = 12
MAC = 0x130000112233

ENTRY_TYPE = 3
VALID = 1
AGED_FLAG = 0
IP6_MASK = 0
DEST_IDX = 0

4.6.1.7 Port and VLAN Filter

The following table lists the registers associated with the port and VLAN filter.

Table 32 • **VID/Port Filters**

Register	Description	Replication
ANAGEFIL	Port and VLAN filter for limiting the target for aging and search operations on MAC table.	None

The ANAGEFIL register can be used to only hit specific VLANs or ports when doing certain operations. If the filter is enabled, it affects:

- Manual age scan command (MACACCESS.MAC_TABLE_CMD = AGE)
- The LOOKUP and GET_NEXT MAC table commands. For more information, see CPU Commands, page 50.

4.6.1.8 Shared VLAN Learning

The following table lists the location of the Filter Identifier (FID) used for shared VLAN learning.

Table 33 • **FID Definition Registers**

Register	Description	Replication
AGENCTRL.FID_MASK	Combines multiple VIDs in the MAC table.	None

In the default configuration, the device is set up to do Independent VLAN Learning (IVL), that is, MAC addresses are learned separately on each VLAN. The device also supports Shared VLAN Learning (SVL), where a MAC table entry is shared among a group of VLANs. For shared VLAN learning, a MAC address and a Filter Identifier (FID) define each MAC table entry. A set of VIDs then map to the FID.

The AGENCTRL.FID_MASK controls the mapping between FID and VIDs. The 12-bit FID_MASK masks out the corresponding bits in the VID. The FID used for learning and lookup is therefore calculated as FID = VID AND (NOT FID_MASK).

All VIDs mapping to the same FID share the same MAC table entries.

If the FID_MASK is cleared, Independent VLAN Learning is used. This is the default.

Example Configure all MAC table entries to be shared among all VLANs.

This is done by setting FID_MASK to 111111111111.

Example Split the MAC table into two separate databases: one for even VIDs and one for odd VIDs.

This is done by setting FID_MASK to 111111111110.

4.6.1.9 Learn Limit

The following table lists the registers associated with controlling the number of MAC table entries per port.

Table 34 • **Learn Limit Definition Registers**

Register	Description	Replication
ENTRYLIM	Configures maximum number of unlocked entries in the MAC table per ingress port.	Per port
PORT_CFG.LIMIT_CPU	If set, learn frames exceeding the limit are copied to the CPU.	Per port
PORT_CFG.LIMIT_DROP	If set, learn frames exceeding the limit are discarded.	Per port
LEARNDISC	The number of MAC table entries that could not be learned due to a lack of storage space.	None

The ENTRYLIM.ENTRYLIM register specifies the maximum number of unlocked entries in the MAC table that a port is allowed to use. Locked and IPMC entries are not taken into account.

After the limit is reached, both auto-learning and CPU-based learning on unlocked entries are denied. A learn frame causing the limit to be exceeded can be copied to the CPU (PORT_CFG.LIMIT_DROP) and the forwarding to other front ports can be denied (PORT_CFG.LIMIT_DROP).

The ENTRYLIM.ENTRYSTAT register holds the current number of entries in the MAC table. MAC table aging and manual removing of entries through the CPU cause the current number to be reduced. If a MAC table entry moves from one port to another port, this is also reduces the current number. If the move causes the new port's limit to be exceeded, the entry is denied and removed from the MAC table.

The LEARNDISC counts all events where a MAC table entry is not created or updated due to a learn limit.

4.6.2 VLAN Table

The following table lists the registers associated with the VLAN Table.

Table 35 • **VLAN Table Access**

Register	Description	Replication
VLANTIDX	VID to access, and VLAN flags.	None
VLANACCESS	VLAN port mask for VID and command for access	None

The analyzer has a VLAN table that contains information about the members of each of the 4096 VLANs. The following table lists fields for each entry in the VLAN table.

Table 36 • **Fields in the VLAN Table**

Field	Bits	Description
VLAN_PORT_MASK	26	One bit for each port. Set if port is member of VLAN. The CPU port is always a member of all VLANs.
VLAN_MIRROR	1	Mirror frames received in the VLAN. See Mirroring, page 63.
VLAN_SRC_CHK	1	VLAN ingress filtering. If set, frames classified to this VLAN are dropped if PPORT is not member of the VLAN.
VLAN_LEARN_DISABLED	1	Disable learning in the VLAN.

Table 36 • **Fields in the VLAN Table *(continued)***

Field	Bits	Description
VLAN_PRIV_VLAN	1	Set VLAN to private.

By default, all ports are members of all VLANs. This default can be changed through a CPU command. The following table lists the set of commands that a CPU can issue to access the VLAN table. The VLAN table command is written to VLANACCESS.VLAN_TBL_CMD.

Table 37 • **VLAN Table Commands**

Command	Purpose	Use
INIT	Initialize the table	Issue command. When VLAN_TBL_CMD changes to IDLE, initialization has completed and all ports are member of all VLANs. All flags are cleared.
READ	Read VLAN table entry for specific VID.	Configure the VLAN to read from in VLANTIDX.INDEX. When VLAN_TBL_CMD changes to IDLE, VLANACCESS and VLANTIDX contain the information read.
WRITE	Write VLAN table entry for specific VID.	Configure the VLAN to write to in VLANTIDX.INDEX. Configure the content of the VLAN record in VLANACCESS.VLANACCESS VLANTIDX.VLAN_MIRROR VLANTIDX.VLAN_SRC_CHK VLANTIDX.VLAN_LEARN_DISABLED VLANTIDX.VLAN_PRIV_VLAN
IDLE	Indicate that VLAN table is ready for new command	

4.6.3 Forwarding Engine

The analyzer determines the set of ports to which each frame is forwarded, in several configurable steps. The resulting destination port set can include any number of ports, as well as the CPU port.

The analyzer request from the port modules is passed through all the processing steps of the forwarding engine. As each step is carried out, the destination port set (DEST) and CPU extraction queue mask (CPUQ) are built up.

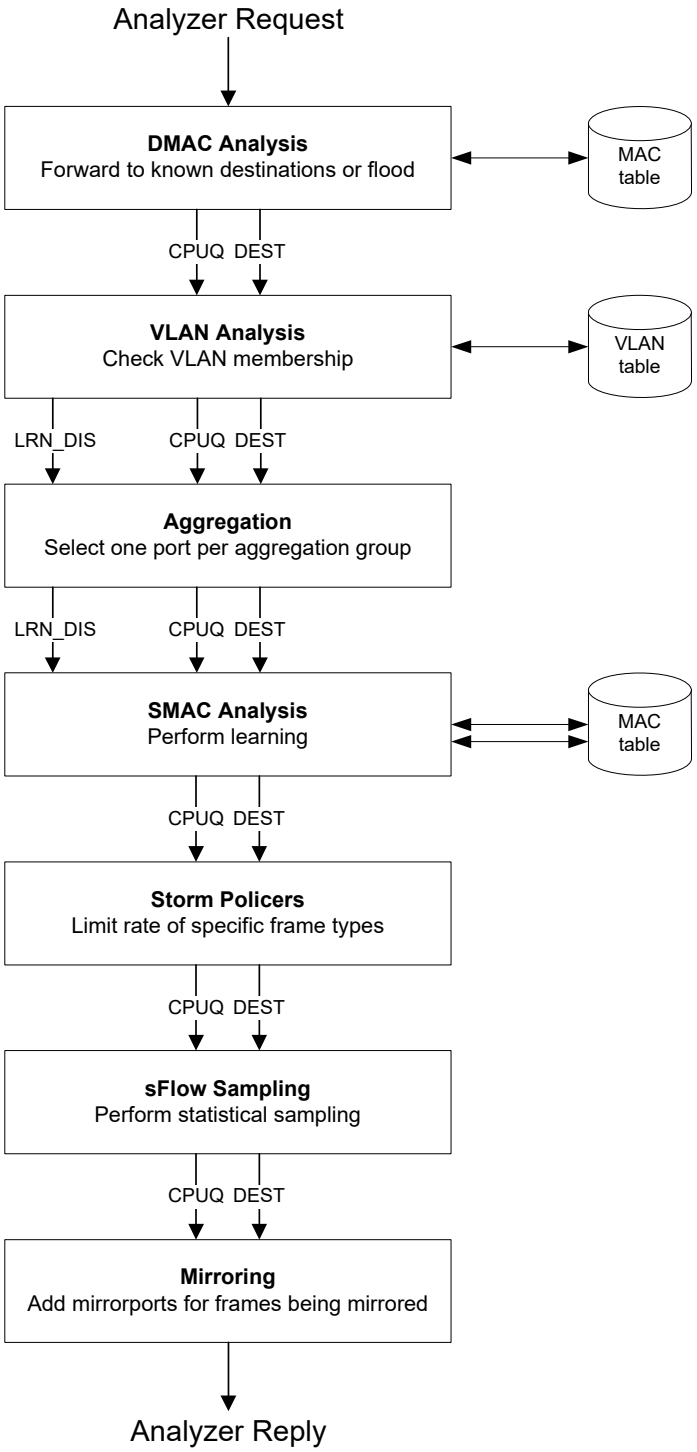
In addition to the forwarding decision, the analyzer determines which frames are subject to learning (also known as learn frames). Learn frames trigger insertion of a new entry in the MAC table or update of an existing entry. Learning is presented as part of the forwarding, because in some cases, learning changes the normal forwarding of a frame, such as secure learning.

During the processing, the analyzer determines a local frame property. The learning-disabled flag, LRN_DIS is used in the SMAC Learning step:

- If the learning-disabled flag is set, learning based on (SMAC, VID) is disabled.
- If the learning-disabled flag is cleared, learning is conducted according to the configuration in the SMAC learning step.

The following illustration shows the configuration steps in the analyzer.

Figure 19 • **Analysis Steps**



4.6.3.1 DMAC Analysis

During the DMAC analysis step, the (DMAC, VID) pair is looked up in the MAC table to get the first input to the calculation of the destination port set. For more information about the MAC table, see MAC Table, page 48.

The following table lists the registers associated with the DMAC analysis step.

Table 38 • **DMAC Analysis Registers**

Register	Description	Replication
FLOODING.FLD_UNICAST	Index into the PGID table used for flooding of unicast frames.	None
FLOODING.FLD_BROADCAST	Index into the PGID table used for flooding of broadcast frames.	None
FLOODING.FLD_MULTICAST	Index into the PGID table used for flooding of multicast frames, not flooded by the IPMC flood masks.	None
FLOODING_IPMC.FLD_MC4_CTRL	Index into the PGID table used for flooding of IPv4 multicast control frames.	None
FLOODING_IPMC.FLD_MC4_DATA	Index into the PGID table used for flooding of IPv4 multicast data frames.	None
FLOODING_IPMC.FLD_MC6_CTRL	Index into the PGID table used for flooding of IPv6 multicast control frames.	None
FLOODING_IPMC.FLD_MC6_DATA	Index into the PGID table used for flooding of IPv6 multicast data frames.	None
PGID[63:0]	Destination and flooding masks table	64
AGENCTRL. IGNORE_DMAC_FLAGS	Controls the use of MAC table flags from (DMAC, VID) entry and flooding flags	None
CPUQ_CFG	Configuration of CPU extraction queues	None

The (DMAC, VID) pair is looked up in the MAC table. If a match is found, the entry is returned and DEST is determined based on the MAC table entry. For more information, see MAC Table, page 48.

If an entry is found in the MAC table entry of ENTRY_TYPE 0 or 1 and the CPU port is set in the PGID pointed to by the MAC table entry, CPU extraction queue PGID.DST_PGID is added to the CPUQ.

If an entry is not found for the (DMAC, VID) in the MAC table, the frame is flooded. The forwarding decision is set to one of the seven flooding masks defined in ANA::FLOODING or ANA::FLOODING_IPMC, based on one of the flood type definitions listed in the following table.

Table 39 • **Forwarding Decisions Based on Flood Type**

Frame Type	Condition
IPv4 multicast data	DMAC = 0x01005E000000 to 0x01005E7FFFFF EtherType = IPv4 IP protocol is not IGMP IPv4 DIP outside 224.0.0.x
IPv6 multicast data	DMAC = 0x333300000000 to 0x3333FFFFFFFF EtherType = IPv6 IPv6 DIP outside 0xFF02::/16

Table 39 • **Forwarding Decisions Based on Flood Type *(continued)***

Frame Type	Condition
IPv4 multicast control	DMAC = 0x01005E000000 to 0x01005E7FFFFF EtherType = IPv4 IP protocol is not IGMP IPv4 DIP inside 224.0.0.x
IPv6 multicast control	DMAC = 0x333300000000 to 0x3333FFFFFFFF EtherType = IPv6 IPv6 DIP inside 0xFF02::/16
Broadcast	DMAC = 0xFFFFFFFFFFFF non-IPv4-multicast-data non-IPv6-multicast-data non-IPv4-multicast-control non-IPv6-multicast-control
Multicast	Bit 40 in DMAC = 1 non-broadcast non-IPv4-multicast-data non-IPv6-multicast-data non-IPv4-multicast-control non-IPv6-multicast-control
Unicast	Bit 40 in DMAC = 0

Additionally, the MAC table flag MAC_CPU_COPY is processed if MAC_CPU_COPY is set, if the CPU port is added to DEST, and if CPUQ_CFG.CPUQ_MAC is added to CPUQ.

The processing of this flag can be disabled through AGENCTRL.IGNORE_DMAC_FLAGS.

Finally, classifier-based CPU-forwarding is processed if:

- The classifier decided to redirect the frame to the CPU, DEST is set to the CPU port only. The corresponding CPU extraction queue is added to CPUQ.
- The classifier decided to copy the frame to the CPU, the CPU port is added to DEST. The corresponding CPU extraction queue is added to CPUQ.

For more information about frame type definitions for CPU forwarding, see Table 26, page 47.

4.6.3.2 VLAN Analysis

During the VLAN analysis step, VLAN configuration is taken into account. As a result, ports can be removed from the forwarding decision. For more information about VLAN configuration, see VLAN Table, page 54.

The following table lists the registers associated with VLAN analysis.

Table 40 • **VLAN Analysis Registers**

Register	Description	Replication
VLANMASK	If PPORT is set in this mask, and PPORT is not member of the VLAN to which the frame is classified, DEST is cleared. This is also called VLAN ingress filtering.	None
PORT_CFG.RECV_ENA	If this bit is cleared for PPORT, forwarding from this port to other front ports is disabled, and DEST is cleared.	Per port

Table 40 • **VLAN Analysis Registers *(continued)***

Register	Description	Replication
PGID[106:80]	Source port mask. Port mask per port, which specifies allowed destination ports for frames received on PPORT. By default, a port can forward to all other ports except itself.	Per port
ISOLATED_PORTS	Private VLAN mask. Isolated ports are cleared in this mask.	None
COMMUNITY_PORTS	Private VLAN mask. Community ports are cleared in this mask.	None
ADVLEARN.VLAN_CHK	If set and VLAN ingress filtering clears DEST, then SMAC learning is disabled.	None

The frame's VID is used as an address for lookup in the VLAN table and the returned VLAN information is processed as follows:

- All ports that are not members of the VLAN (VLAN_PORT_MASK) are removed from DEST, except if the (DMAC, VID) match in the MAC table has VLAN_IGNORE set, or if there is no match in the MAC table and AGENCTRL.FLOOD_IGNORE_VLAN is set.
- **Note** These two exceptions are skipped if AGENCTRL.IGNORE_DMAC_FLAGS is set.
- If the VLAN_PRIV_VLAN flag in the VLAN table is set, the VLAN is private, and isolated and community ports must be treated differently. An isolated port is identified as an ingress port for which PPORT is cleared in the ISOLATED_PORTS register. An community port is identified as an ingress port for which PPORT is cleared in the COMMUNITY_PORTS register. For frames received on an isolated port, all isolated and community ports are removed from the forwarding decision. For frames received on a community port, all isolated ports are removed from the forwarding decision.
- If VLAN ingress filtering is enabled, it is checked whether PPORT is member of the VLAN (VLAN_PORT_MASK). If this is not the case, DEST is cleared.

  VLAN ingress filtering is enabled per port in the VLANMASK register or per VLAN in the VLAN_SRC_CHK flag in the VLAN table. If either is set, VLAN ingress filtering is performed.

Next, it is checked whether the ingress port is enabled to forward frames to other front ports and the source mask (PGID[80+PPORT]) is processed as follows:

- If PORT_CFG.RECV_ENA for PPORT is 0, DEST is cleared except for the CPU port.
- Any ports, which are cleared in PGID[80+PPORT], are removed from DEST.

Finally, SMAC learning is disabled by setting the LRN_DIS flag when either of the following two conditions is fulfilled as follows:

- VLAN_LEARN_DISABLED is set in the VLAN table for the VLAN.
- A frame is subject to VLAN ingress filtering (frame dropped due to PPORT not being member of VLAN), and ADVLEARN.VLAN_CHK is set.

4.6.3.3 Aggregation

During the aggregation step, link aggregation is handled. The following table lists the registers associated with aggregation.

Table 41 • **Analyzer Aggregation Registers**

Register	Description	Replication
PGID[79:64]	Aggregation mask table.	16

The purpose of the aggregation step is to ensure that when a frame is destined for an aggregation group, it is forwarded to exactly one of the group's member ports.

For non-aggregated ports, there is a one-to-one correspondence between logical port (LPORT) and physical port (PPORT). The aggregation step does not change the forwarding decision.

For aggregated ports, all physical ports in the aggregation group map to the same logical port, and the entry in the destination mask table for the logical port includes all physical ports, which are members of the aggregation group. As a result, all but one member port must be removed from the destination port set.

The lni aggregation code generated in the classifier is used to look up an aggregation mask in the aggregation masks table. Finally, ports that are cleared in the selected aggregation mask are removed from DEST.

For more information about link aggregation, see Link Aggregation, page 153.

4.6.3.4 SMAC Analysis

During the SMAC analysis step, the MAC table is searched for a match against the (SMAC, VID), and the MAC table is updated due to learning. The learning part is skipped if the LRN_DIS flag was set by any of the previous steps.

The following table lists the registers associated with SMAC learning.

Table 42 • **SMAC Learning Registers**

Register	Description	Replication
PORT_CFG.LEARN_ENA	If set for PPORT, learning is skipped (that is, LEARNAUTO, LEARNCPU, LEARNDROP, LIMIT_CPU, LIMIT_DROP, LOCKED_PORTMOVE_CPU, and LOCKED_PORTMOVE_DROP are ignored).	Per port
PORT_CFG.LEARNAUTO	If set for PPORT, hardware-based learning is performed.	Per port
PORT_CFG.LEARNCPU	If set for PPORT, learn frames are copied to the CPU.	Per port
PORT_CFG.LEARNDROP	If set for PPORT, the CPU drops or forwards learn frames.	Per port
PORT_CFG.LIMIT_CPU	If set for PPORT, learn frames for which PPORT exceeds the port's limit are copied to the CPU.	Per port
PORT_CFG.LIMIT_DROP	If set for PPORT, learn frames for which PPORT exceeds the port's limit are discarded.	Per port
PORT_CFG. LOCKED_PORTMOVE_CPU	If set for PPORT, frames triggering a port move of a locked entry are copied to the CPU.	Per port
PORT_CFG. LOCKED_PORTMOVE_DROP	If set for PPORT, frames triggering a port move of a locked entry are discarded.	Per port
AGENCTRL.IGNORE_SMAC_FLAGS	Controls the use of the MAC table flags from (SMAC, VID) entry.	None

Three different type of learn frames are identified:

- **Normal learn frames** Frames for which an entry for the (SMAC, VID) is not found in the MAC table or the (SMAC, VID) entry in the MAC table is unlocked and has a DEST_IDX different from LPORT. In addition, the learn limit for the LPORT must not be exceeded (ENTRYLIM).

- **Learn frames exceeding the learn limit** Same condition as for normal learn frames except that the learn limit for the LPORT is exceeded (ENTRYLIM)
- **Learn frames triggering a port move of a locked MAC table entry** Frames for which the (SMAC, VID) entry in the MAC table is locked and has a DEST_IDX different from LPORT.

For all learn frames, the following must apply before learning related processing is applied:

- Learning is enabled by PORT_CFG.LEARN_ENA.
- The LRN_DIS flag from previous processing steps must be cleared, which implies that:
  – Learning is not disabled due to VLAN ingress filtering
  – Learning is enabled for the VLAN (VLAN_LEARN_DISABLED is cleared in the VLAN table)

In addition, learning must not be disabled due to the ingress policer having policed the frame. For more information, see Policers, page 64.

If learning is enabled, learn frames are processed according to the setting of the following configuration parameters.

Normal learn frames:

- Automatic learning. If PORT_CFG.LEARNAUTO is set for PPORT, the (SMAC, VID) entry is automatically added to the MAC table
- Drop learn frames. If PORT_CFG.LEARNDROP is set for PPORT, DEST is cleared for learn frames. Therefore, learn frames are not forwarded on any ports. This is used for secure learning, where the CPU must verify a station before forwarding is allowed.
- Copy learn frames to the CPU. If PORT_CFG.LEARNCPU is set for PPORT, the CPU port is added to DEST for learn frames and CPUQ_CFG.CPUQ_LRN is set in CPUQ. This is used for CPU based learning.

Learn frames exceeding the learn limit:

- Drop learn frames. If PORT_CFG.LIMIT_DROP is set for PPORT, DEST is cleared for learn frames. As a result, learn frames are not forwarded on any ports.
- Copy learn frames to the CPU – If PORT_CFG.LIMIT_CPU is set for PPORT, the CPU port is added to DEST and CPUQ_CFG.CPUQ_LRN is set in CPUQ for learn frames.

Learn frames triggering a port move of a locked MAC table entry:

- Drop learn frames. If PORT_CFG.LOCKED_PORTMOVE_DROP is set for PPORT, DEST is cleared for learn frames. Therefore, learn frames are not forwarded on any ports.
- Copy learn frames to the CPU. If PORT_CFG.LOCKED_PORTMOVE_CPU is set for PPORT, the CPU port is added to DEST and CPUQ_CFG.CPUQ_LOCKED_PORTMOVE is added to CPUQ.

Finally, if a match is found in the MAC table for the (SMAC, VID), adjustments can be made to the forwarding decision.

- If the (SMAC, VID) match in the MAC table has SRC_KILL set, DEST is cleared except the CPU port.
- If the (SMAC, VID) match in the MAC table has MAC_CPU_COPY set, the CPU port is added to DEST and CPUQ_CFG.CPUQ_MAC_COPY is added to CPUQ.

The processing of the MAC table flags from the (SMAC, VID) match can be disabled through AGENCTRL.IGNORE_SMAC_FLAGS.

4.6.3.5 Storm Policers

The storm policers are activated during the storm policers step. The following table lists the registers associated with storm policers.

Table 43 • **Storm Policer Registers**

Register	Description	Replication
STORMLIMIT_CFG	Enable policing of various frame types.	4
STORMLIMIT_BURST	Configure maximum allowed rates of the different frame types.	None

The analyzer contains four storm policers that can limit the maximum allowed forwarding frame rate for various frame types. The storm policers are common to all ports and, as a result, measure the sum of traffic forwarded by the switch. A frame can activate several storm policers, and the frame is discarded if any of the activated storm policers exceed a configured rate. The storm policers work independently of other policers in the system (for example, port policers). As a result, frames policed by other policers are still measured by the storm policers.

Each storm policer can be configured to a frame rate ranging from 1 frame per second to 1 million frames per second.

The following table lists the available storm policers.

Table 44 • **Storm Policers**

Storm Policer	Description
Broadcast	Flooded frames with DMAC = 0xFFFFFFFFFFFF.
Multicast	Flooded frames with DMAC bit 40 set, except broadcasts.
Unicast	Flooded frames with DMAC bit 40 cleared.
Learn	Learn frames copied or redirected to the CPU due to learning (LOCKED_PORTMOVE_CPU, LIMIT_CPU, LEARNCPU).

For each of the storm policers, a maximum rate is configured in STORMLIMIT_CFG and STORMLIMIT_BURST:

- STORM_UNIT chooses between a base unit of 1 frame per second or 1 kiloframes per second.
- STORM_RATE sets the rate to 1, 2, 4, 8, …, 1024 times the base unit (STORM_UNIT).
- STORM_BURST configures the maximum number of frames in a burst.
- STORM_MODE specifies how the policer affects the forwarding decision. The options are:
  When policing, clear the CPU port in DEST.
  When policing, clear DEST except for the CPU port.
  When policing, clear DEST

Note that frames where the DMAC lookup returned a PGID with the CPU port set are always forwarded to the CPU even when the frame is policed by the storm policers. For more information, see DMAC Analysis, page 56.

4.6.3.6 sFlow Sampling

This process step handles sFlow sampling. The following table lists the registers associated with sFlow sampling.

Table 45 • **sFlow Sampling Registers**

Register	Description	Replication
SFLOW_CFG	Configures sFlow samplers (type and rates).	Per port
CPUQ_CFG.CPUQ_SFLOW	CPU extraction queue for sFLow sampled frames.	None

sFlow is a standard for monitoring high-speed switch networks through statistical sampling of incoming and outgoing frames. Each port in the devices can be setup as an sFlow agent monitoring the particular link and generating sFlow data. If a frame is sFlow sampled, it is copied to the sFlow CPU extraction queue (CPUQ_SFLOW).

An sFlow agent is configured through SFLOW_CFG with the following options:

- SF_RATE specifies the probability that the sampler copies a frame to the CPU. Each frame being candidate for the sampler has the same probability of being sampled. The rate is set in steps of 1/4096.
- SF_SAMPLE_RX enables incoming frames on the port as candidates for the sampler.

- SF_SAMPLE_TX enables outgoing frames on the port as candidates for the sampler.

The Rx and Tx can be enabled independently. If both are enabled, all incoming and outgoing traffic on the port is subject to the statistical sampling given by the rate in SF_RATE.

4.6.3.7 Mirroring

This processing step handles mirroring. The following table lists the registers associated with mirroring.

Table 46 • **Mirroring Registers**

Register	Description	Replication
ADVLEARN.LEARN_MIRROR	For learn frames, ports in this mask (mirror ports) are added to DEST.	None
AGENCTRL.MIRROR_CPU	Mirror all frames forwarded to the CPU port module	None
PORT_CFG.SRC_MIRROR_ENA	Mirror all frames received on an ingress port (ingress port mirroring).	Per port
EMIRRORPORTS	Mirror frames that are to be transmitted on any ports set in this mask (egress port mirroring)	None
VLANTIDX.VLAN_MIRROR	Mirror all frames classified to a specific VID.	Per VLAN
MIRRORPORTS	When mirroring a frame, ports in this mask are added to DEST.	None
AGENCTRL.CPU_CPU_KILL_ENA	Clear the CPU port if source port is the CPU port and the CPU port is set in DEST.	None

Frames subject to mirroring are identified based on the following mirror probes:

- Learn mirroring if ADVLEARN.LEARN_MIRROR is set and frame is a learn frame.
- CPU mirroring if AGENCTRL.MIRROR_CPU is set and the CPU port is set in DEST.
- Ingress mirroring if PORT_CFG.SRC_MIRROR_ENA is set.
- Egress mirroring if any port set in EMIRRORPORTS is also set in DEST.
- VLAN mirroring if VLAN_MIRROR set in the VLAN table entry.

The following adjustment is made to the forwarding decision for frames subject to mirroring:

- Ports set in MIRRORPORTS are added to DEST.

If the CPU port is set in the MIRRORPORTS, CPU extraction queue CPUQ_CFG.CPUQ_MIRROR is added to the CPUQ.

For learn frames with learning enabled, all ports in ADVLEARN.LEARN_MIRROR are added to DEST. For more information, see SMAC Analysis, page 60.

For more information about mirroring, see Mirroring, page 156.

Finally, if AGENCTRL.CPU_CPU_KILL_ENA is set, the CPU port is removed if the ingress port is the CPU port itself. This is similar to source port filtering done for front ports and prevents the CPU from sending frames back to itself.

4.6.4 Analyzer Monitoring

Miscellaneous events in the analyzer can be monitored, which can provide an understanding of the events during the processing steps. The following table lists the registers associated with analyzer monitoring.

Table 47 • **Analyzer Monitoring**

Register	Description	Replication
ANMOVED	ANMOVED[n] is set when a known station has moved to port n.	None
ANEVENTS	Sticky bit register for various events.	None
LEARNDISC	The number of learn events that failed due to a lack of storage space in the MAC table.	None

Port moves, defined as a known station moving to a new port, are registered in the ANMOVED register. A port move occurs when an existing MAC table entry for (MAC, VID) is updated with new port information (DEST_IDX). Such an event is registered in ANMOVED by setting the bit corresponding to the new port.

Continuously occurring port moves may indicate a loop in the network or a faulty link aggregation configuration.

A list of 27 events, such as frame flooding or policer drop, can be monitored in ANEVENTS.

The LEARNDISC counter registers every time an entry in the MAC table cannot be made or if an entry is removed due to lack of storage.

4.7 Policers and Ingress Shapers

The devices support a policer per ingress ports and per ingress queues. Each ingress port also has an ingress shaper. Both the policers and the shapers can limit the bandwidth of received frames. When configured bandwidth is exceeded, the policers discard frames, while the ingress shaper holds back the traffic in the queue system. Each frame can hit up to two policers and one ingress shaper.

In addition to the policers and ingress shapers described, the devices also support a number of storm policers and an egress scheduler with per-port and per-egress queue shapers. For more information, see Storm Policers, page 61 and Scheduler and Shaper, page 74.

4.7.1 Policers

This section explains the functions of the policers. The following table lists the registers associated with policer control.

Table 48 • **Policer Control Registers**

Register	Description	Replication
ANA:PORT:POL_CFG	Enables use of port and queue policers.	Per port
SYS:POL:POL_PIR_CFG	Configures the policer's peak information rate.	256
SYS:POL:POL_MODE_CFG	Configures the policer's mode of operation.	256
SYS:POL:POL_PIR_STATE	Current state of the peak information rate bucket.	256
SYS:PORT:POL_FLOWC	Flow control settings	Per port
SYS::POL_HYST	Hysteresis settings.	None

The policers can be assigned to the following two blocks:

- Ingress ports. Port ‘p’ use policer ‘p’.
- Ingress queues. Ingress queue ‘q’ on port ‘p’ use policer 32 + 8x ‘p’ + ‘q’. Each of the eight per-port ingress queues can be assigned to its own policer.

Port and queue policers are enabled through ANA:PORT:POL_CFG.PORT_POL_ENA and ANA:PORT:POL_CFG.QUEUE_POL_ENA.

Each frame can hit a policer from each block; one port policer, one queue policer. The policers are selected as follows:

- The ingress port where the frame was received points to the port policer.
- The QoS class classified to by the classifier points to the queue policer.

Any frame received by the MAC and forwarded to the classifier is applicable to policing. Frames with errors, pause frames, or MAC control frames are not forwarded by the MAC and, as a result, they are not accounted for in the policers. That is, they are not policed and are not adding to the rate measured by the policers.

In addition, the following special frame types can bypass the policers:

- If ANA:PORT:POL_CFG.POL_CPU_REDIR_8021 is set, frames being redirected to the CPU due to the classifier detecting the frames as being BPDU, ALLBRIDGE, GARP, or CCM/Link trace frames are not policed.
- If ANA:PORT:POL_CFG.POL_CPU_REDIR_IP is set, frames being redirected to the CPU due to the classifier detecting the frames as being IGMP or MLD frames are not policed.

These frames are still considered part of the rates being measured so the frames add to the relevant policer buckets but they are never discarded due to policing.

The order in which the policers are executed is controlled through ANA:PORT:POL_CFG.POL_ORDER. The order can take the following main modes:

- **Serial** The policers are checked one after another. If a policer is closed, the frame is discarded and the subsequent policer buckets are not updated with the frame. The serial order is programmable.
- **Parallel with independent bucket updates** The two policers are working in parallel independently of each other. Each frame is added to a policer bucket if the policer is open, otherwise the frame is discarded. A frame may be added to one policer although another policer is closed.
- **Parallel with dependent bucket updates** The two policers are working in parallel but dependent on each other with respect to bucket updates. A frame is only added to the policer buckets if all two policers are open.

Each of the policers contain a leaky bucket with the following configurations:

- Peak Information Rate (PIR) – Specified in POL_PIR_CFG.PIR_RATE in steps of 100 kbps. Maximum is 3.277 Gbps.
- Peak Burst Size (PBS) – Specified in POL_PIR_CFG.PIR_BURST in steps of 4 kilobytes. Maximum is 252 kilobytes.

Additionally, the following parameters can be configured per policer:

- The leaky bucket calculation can be configured to include or exclude preamble and inter-frame gap through configuration of POL_MODE_CFG.IPG_SIZE.
- Each policer can be configured to measure frame rates instead of bit rates (POL_MODE_CFG.FRM_MODE). The rate unit can be configured to 100 frames per second or 1 frame per second.
- POL_MODE_CFG.OVERSHOOT_ENA controls whether a bucket is allowed to use more than the actual number of tokens in the bucket when accepting a frame (overshooting). If POL_MODE_CFG.OVERSHOOT_ENA is cleared, the number of tokens in the bucket must be larger than the number of tokens required to accept the frame.

By default, a policer discards frames while the policer is closed. A discarded frame is neither forwarded to any ports (including the CPU) nor is it learned.

However, each port policer has the option to run in flow control where the policer instructs the MAC to issue flow control pause frames instead of discarding frames. This is enabled in SYS:PORT:POL_FLOWC. Common for all port policers, POL_HYST.POL_FC_HYST specifies a hysteresis, which controls when the policer can re-open after having closed.

To improve fairness between small and large frames being policed by the same policer, POL_HYST.POL_DROP_HYST specifies a hysteresis, which controls when the policer can re-open after being closed. By setting it to a value larger than the maximum transmission unit, it guarantees that when the policer opens again, all frames have the same chance of being accepted. This setting only applies to policers working in drop mode.

The current fill level of the leaky buckets can be read in POL_PIR_STATE. The unit is 0.5 bits.

4.7.2 Ingress Shapers

The following table lists the registers associated with ingress shaper control.

Table 49 • **Ingress Shaper Control Registers**

Register	Description	Replication
SYS:PORT:ISHP_CFG	Configures rate and burst.	Per port
SYS:PORT:ISHP_MODE_CFG	Configures mode of operation.	Per port
SYS:PORT:ISHP_STATE	Current level of leaky bucket.	Per port

In addition to the policers, each port has an ingress shaper that controls the rate at which ingress ports are allowed to transfer data to egress ports. An ingress shaper does not discard any frames when its rate is exceeded, but simply holds back the frames in the ingress queues until the rate is below the configured value again. To ensure proper operation of the ingress shapers, all frames on all ports must be assigned the same QoS class when the ingress shapers are enabled.

The ingress shaper is enabled in ISHP_CFG.ISHP_ENA. Each of the ingress shapers contains a leaky bucket with the following configurations:

- Maximum transfer rate is specified in ISHP_CFG.ISHP_RATE in steps of 100 kbps. Maximum is 3.277 Gbps.
- Maximum burst size is specified in ISHP_CFG.ISHP_BURST in steps of 4 kilobytes. Maximum is 252 kilobytes.

Additionally, the following parameters can be configured per ingress shaper:

- The leaky bucket calculation can be configured to include or exclude preamble and inter-frame gap through configuration of ISHP_MODE_CFG.ISHP_IPG_SIZE.
- Each ingress shaper can be configured to measure frame rates instead of bit rates (ISHP_MODE_CFG.ISHP_FRM_MODE). The rate unit can be configured to 100 frames per second or 1 frame per second.

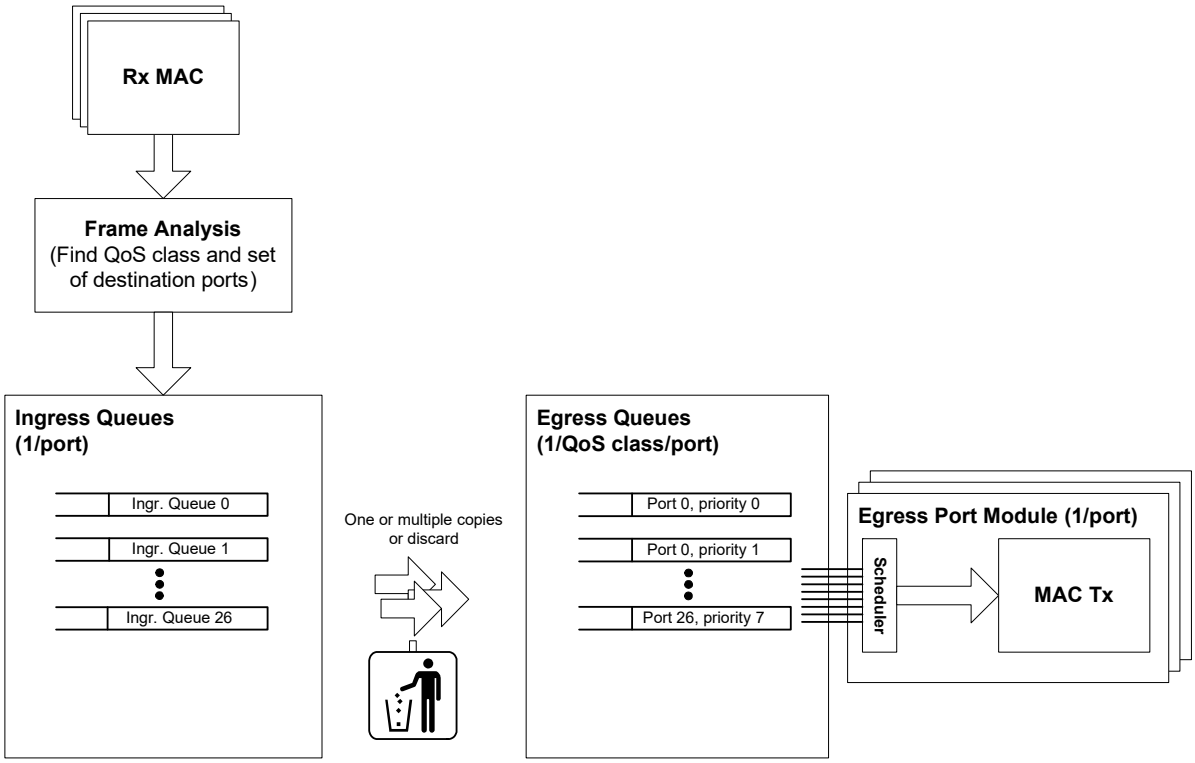
The current fill level of the leaky bucket can be read in ISHP_STATE. The unit is 0.5 bits.

4.8 Shared Queue System

The devices include a shared queue system with one ingress queue and eight egress queues per port. The queue system has 512 kilobytes of buffer.

Frames are stored in the ingress queue after frame analysis. Each egress port module selected by the frame analysis receives a copy of the frame and stores the frame in the appropriate egress queue given by the frame's QoS class. The transfer from ingress to egress is extremely efficient with a transfer time of 8 ns per frame copy (equivalent to a transfer rate of 64 Gbps for 64-byte frames and 1.5 Tbps for 1518-byte frames. Each egress port module has a scheduler, which selects between the egress queues when transmitting frames.

The following illustration shows the shared queue system.



Resource depletion can prevent one or more of the frame copies from the ingress queue to the egress queues. If a frame copy cannot be made due to lack of resources, the ingress port's flow control mode determines the behavior as follows:

- Ingress port is in drop mode: The frame copy is discarded.
- Ingress port is in flow control mode: The frame is held back in the ingress queue and the frame copy is made when the congestion clears.

For more information about special configurations of the shared queue system with respect to flow control, see Ingress Pause Request Generation, page 72.

4.8.1 Buffer Management

A number of watermarks control how much data can be pending in the egress queues before the resources are depleted. There are no watermarks for the ingress queues, except for flow control, because the ingress queues are empty most of the time due to the fast transfer rates from ingress to egress. For more information, see Ingress Pause Request Generation, page 72. When the watermarks are configured properly, congested traffic does not influence the forwarding of non-congested traffic. F

The memory is split into two main areas:

- A reserved memory area. The reserved memory area is subdivided into areas per port per QoS class per direction (ingress/egress).
- A shared memory area, which is shared by all traffic.

For setting up the reserved areas, egress queue watermarks exist per port and per QoS class for both ingress and egress. The following table lists the reservation watermarks.

Table 50 • **Reservation Watermarks**

Register	Description	Replication
BUF_Q_RSRV_E	Configures the reserved amount of egress buffer per egress queue.	Per egress queue

Table 50 • **Reservation Watermarks *(continued)***

Register	Description	Replication
BUF_P_RSRV_E	Configures the reserved amount of egress buffer shared among the eight egress queues.	Per egress port
BUF_Q_RSRV_I	Configures the reserved amount of egress buffer per ingress port per QoS class across all egress ports.	Per ingress port per QoS class
BUF_P_RSRV_I	Configures the reserved amount of egress buffer per ingress port shared among the eight QoS classes.	Per ingress port

All the watermarks, including the ingress watermarks, are compared against the memory consumptions in the egress queues. For example, the ingress watermarks in BUF_Q_RSRV_I compare against the total consumption of frames across all egress queues received on the specific ingress port and classified to the specific QoS class. The ingress watermarks in BUF_P_RSRV_I compare against the total consumption of all frames across all egress queues received on the specific ingress port.

The reserved areas are guaranteed minimum areas. A frame cannot be discarded or held back in the ingress queues if the frame's reserved areas are not yet used.

The shared memory area is the area left when all the reservations are taken out. The shared memory area is shared between all ports, however, it is possible to configure a set of watermarks per QoS class and per drop precedence level (green/yellow) to stop some traffic flows before others. The following table lists the sharing watermarks.

Table 51 • **Sharing Watermarks**

Register	Description	Replication
BUF_PRIO_SHR_E	Configures how much of the shared memory area that egress frames with the given QoS class are allowed to use.	Per QoS class
BUF_COL_SHR_E	Configures how much of the shared memory area that egress frames with the given drop precedence level are allowed to use.	Per drop precedence level
BUF_PRIO_SHR_I	Configures how much of the shared memory area that ingress frames with the given QoS class are allowed to use.	Per QoS class
BUF_COL_SHR_I	Configures how much of the shared memory area that ingress frames with the given drop precedence level are allowed to use.	Per drop precedence level

The sharing watermarks are maximum areas in the shared memory that a given traffic flow can use. They do not guarantee anything.

When a frame is enqueued into the egress queue system, the frame first consumes from the queue's reserved memory area, then from the port's reserved memory area. When all the frame's reserved memory areas are full, it consumes from the shared memory area.

The following provides some simple examples on how to configure the watermarks and how that influences the resource management:

- Setting BUF_Q_RSRV_E(egress port = 17, QoS class = 4) to 2 kilobytes guarantees that traffic destined for port 17 classified to QoS class 4 have room for 2 kilobytes of frame data before frames can get discarded.
- Setting BUF_Q_RSRV_I(ingress port = 17, QoS class = 4) to 2 kilobytes guarantees that traffic received on port 17 classified to QoS class 4 have room for 2 kilobytes of frame data before frames can get discarded.

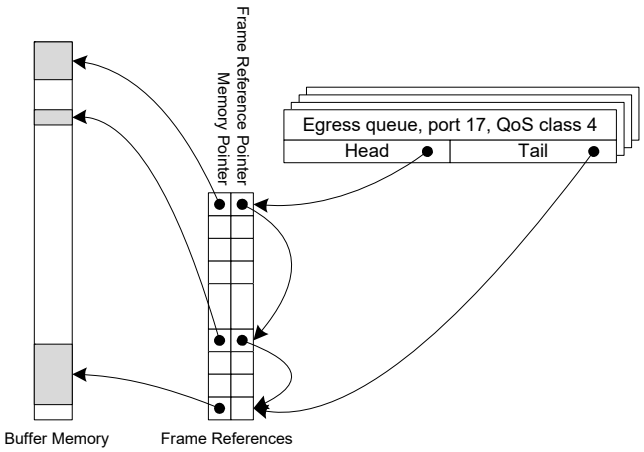
- Setting BUF_P_RSRV_I(ingress port 17) to 10 kilobytes guarantees that traffic received on port 17 have room for 10 kilobytes of data before frames can get discarded.
- The three above reservations reserve in total 14 kilobytes of memory (2 + 2+ 10 kilobytes) for port 17. If the same reservations are made for all ports, there are 512 – 27 × 14 = 134 kilobytes left for sharing. If the sharing watermarks are all set to 134 kilobytes, all traffic groups can consume memory from the shared memory area without restrictions.

  If, instead, setting BUF_PRIO_SHR_E(QoS class = 7) to 100 kilobytes and the other watermarks BUF_PRIO_SHR_E(QoS class = 0:6) to 70 kilobytes guarantees that traffic classified to QoS class 7 has 30 kilobytes extra buffer. The buffer is shared between all ports.

4.8.2 Frame Reference Management

Each frame in an egress queue consumes a frame reference, which is a pointer element that points to the frame's data in the memory and to the pointer element belonging to the next frame in the queue. The following illustrations shows how the frame references are used for creating the queue structure.

Figure 20 • **Frame Reference**



The shared queue system holds a table of 5500 frame references. The consumption of frame references is controlled through a set of watermarks. The set of watermarks is the exact same as for the buffer control. The frame reference watermarks are prefixed REF_. Instead of controlling the amount of consumed memory, they control the number of frame references. Both reservation and sharing watermarks are available. For more information, see Table 50, page 67 and Table 51, page 68.

When a frame is enqueued into the shared queue system, the frame consumes first from the queue's reserved frame reference area, then from the port's reserved frame reference area. When all the frame's reserved frame reference areas are full, it consumes from the shared frame reference area.

4.8.3 Resource Depletion Condition

A frame copy is made from an ingress port to an egress port when both a memory check and a frame reference check succeed. The memory check succeeds when at least one of the following conditions is met:

- Ingress memory is available: BUF_Q_RSRV_I or BUF_P_RSRV_I are not exceeded.
- Egress memory is available: BUF_Q_RSRV_E or BUF_P_RSRV_E are not exceeded.
- Shared memory is available: None of BUF_PRIO_SHR_E or BUF_PRIO_SHR_I are exceeded.

The frame reference check succeeds when at least one of the following conditions is met:

- Ingress frame references are available: REF_Q_RSRV_I or REF_P_RSRV_I are not exceeded.
- Egress frame references are available: REF_Q_RSRV_E or REF_P_RSRV_E are not exceeded.
- Shared frame references are available: None of REF_PRIO_SHR_E or REF_PRIO_SHR_I are exceeded.

4.8.4 Configuration Example

This section provides an example of how the watermarks can be configured for a QoS-aware switch with no color handling and the effects of the settings.

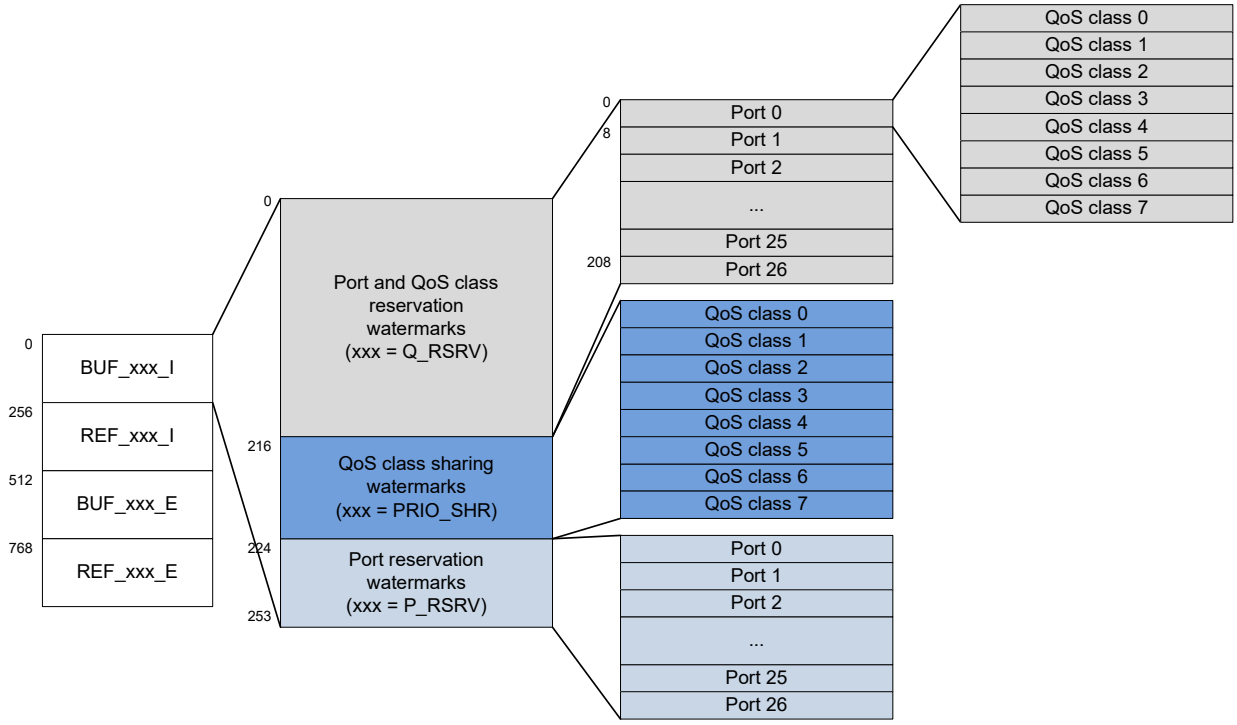
Table 52 • **Watermark Configuration Example**

Watermark	Value	Comment
BUF_Q_RSRV_I	500 bytes	Guarantees that a port is capable of receiving at least one frame in all QoS classes. **Note** It is not necessary to assign a full MTU, because the watermarks are checked before the frame is added to the memory consumption.
BUF_P_RSRV_I	0	No additional guarantees for the ingress port.
BUF_Q_RSRV_E	200 bytes	Guarantees that all QoS classes are capable of sending a non-congested stream of traffic through the switch.
BUF_P_RSRV_E	10 kilobytes	Guarantees that all egress ports have 10 kilobytes of buffer, independently of other traffic in the switch. This is the most demanding reservation in this setup, reserving 270 kilobytes of the total 512 kilobytes.
BUF_COL_SHR_E BUF_COL_SHR_I	Maximum	Effectively disables frame coloring as watermark is never reached.
BUF_PRIO_SHR_E BUF_PRIO_SHR_I	82 kilobytes to 103 kilobytes	The different QoS classes are cut-off with 3 kilobytes distance (82, 85, 88, 91, 94, 97, 100, and 103 kilobytes). This gives frames with higher QoS classes a larger part of the shared buffer area. Effectively, this means that the burst capacity is 92 kilobytes for frames belonging to QoS class 0 and up to 113 kilobytes for frame belonging to QoS class 7.
REF_Q_RSRV_E REF_Q_RSRV_I	4	For both ingress and egress, this guarantees that four frames can be pending from and to each port.
REF_P_RSRV_E REF_P_RSRV_I	20	For both ingress and egress, this guarantees that an extra 20 frames can be pending, shared between all QoS classes within the port.
REF_COL_SHR_E REF_COL_SHR_I	Maximum	Effectively disables frame coloring as watermark is never reached.
REF_PRIO_SHR_E REF_PRIO_SHR_I	2350 - 2700	The different QoS classes are cut-off with a distance of 50 frame references (2350, 2400, 2450, 2500, 2550, 2600, 2650, and 2700). This gives frames with higher QoS classes a larger part of the shared reference area.

4.8.5 Watermark Programming and Consumption Monitoring

The watermarks previously described are all found in the SYS::RES_CFG register. The register is replicated 1024 times. The following illustration the organization.

Figure 21 • **Watermark Layout**



The illustration shows the watermarks available for the BUF_xxx_I group of watermarks. For the other groups of watermarks (BUF_xxx_I, REF_xxx_I, BUF_xxx_E, and REF_xxx_E), the exact same set of watermarks is available.

For monitoring purposes, SYS::RES_STAT provides information about the resource consumption currently in use as well as the maximum consumption for corresponding watermarks. The information is available for each of the watermarks listed, and the layout of the RES_STAT register follows the layout of the watermarks. SYS::MMGT.FREECNT holds the amount of free memory in the shared queue system and SYS::EQ_CTRL.FP_FREE_CNT holds the number of free frame references in the shared queue system.

4.8.6 Advanced Resource Management

A number of additional handles into the resource management system are available for special use of the device. They are described in the following table.

Table 53 • **Resource Management**

Resource Management	Description
Forced drop of egress frames	SYS:PORT:EGR_DROP_FORCE. If an ingress port is in configured in flow control mode, frames received on the port are by default held back if one or more destination ports do not allow more data. However, if forced drop of egress frames is enabled for the egress port, frames are discarded. This could be enabled for the CPU port and for a mirror target port in order not to cause head-of-line blocking of non-congested traffic.
Prevent ingress port from using of the shared resources.	SYS:IGR_NO_SHARING. For frames received on ports set in this mask, the shared watermarks are considered exceeded. This prevents the port from using more resources than allowed by the reservation watermarks.

Table 53 • **Resource Management** ***(continued)***

Resource Management	Description
Prevent egress port from using of the shared resources.	SYS:EGR_NO_SHARING. For frames switched to ports set in this mask the shared watermarks are considered exceeded. This prevents the port from using more resources than allowed by the reservation watermarks.
Preferred sources	SYS::EQ_PREFER_SRC. By default, ingress ports that have frames for transmission of equal QoS class are serviced in round robin. However, ingress ports marked in this mask are preferred over ingress ports not marked.
Truncating	SYS:PORT:EQ_TRUNCATE. Each egress queue can be configured to truncate frames to 92 bytes. Frames shorter than 92 bytes are not changed. This could be the enabled for a specific CPU extraction queue used for learning or a mirror target port where the first segment of the frames is sufficient for further frame processing.
Prevent dequeuing	SYS:PORT:PORT_MODE.DEQUEUE_DIS. Each egress port can disable dequeuing of frames from the egress queues.

4.8.7 Ingress Pause Request Generation

During resource depletion, the shared queue system either discards frames when the ingress port operates in drop mode, or holds back frames when the ingress port operates in flow control mode. The following describes special configuration for the flow control mode.

The shared queue system is enabled for holding back frames during resource depletion in SYS:PORT:PAUSE_CFG.PAUSE_ENA. In addition, this enables the generation of pause requests to the port module based on memory consumptions. The MAC uses the pause request to generate pause frames or create back pressure collisions to halt the link partner. This is done according to the MAC configuration. For more information about MAC configuration, see MAC, page 12.

The shared queue system generates the pause request based on the ingress port's memory consumption and also based on the total memory consumption in the shared queue system. This enables a larger burst capacity for a port operating in flow control while not jeopardizing the non-dropping flow control.

Generating the pause request partially depends on a memory consumption flag, TOT_PAUSE, which is set and cleared under the following conditions:

- The TOT_PAUSE flag is set when the total consumed memory in the shared queue system exceeds the SYS:PORT:PAUSE_TOT_CFG.PAUSE_TOT_START watermark.
- The TOT_PAUSE flag is cleared when the total consumed memory in the shared queue system is below the SYS:PORT:PAUSE_TOT_CFG.PAUSE_TOT_STOP watermark.

The pause request is asserted when both of the following conditions are met:

- The TOT_PAUSE flag is set.
- The ingress port memory consumption exceeds the SYS:PORT:PAUSE_CFG.PAUSE_START watermark.

The pause request is deasserted the following condition is met:

- The ingress port's consumption is below the SYS:PORT:PAUSE_CFG.PAUSE_STOP watermark.

4.8.8 Tail Dropping

The shared queue system implements a tail dropping mechanism where incoming frames are discarded if the port's memory consumption and the total memory consumption exceed certain watermarks. Tail

dropping implies that the frame is discarded unconditionally. All ports in the device are subject to tail dropping. It is independent of whether the port is in flow control mode or drop mode.

Tail dropping can be effective under special conditions. For example, tail dropping can prevent an ingress port from consuming all the shared memory when pause frames are lost or the link partner is not responding to pause frames.

The shared queue system initiates tail dropping by discarding the incoming frame if the following two conditions are met at any point while writing the frame data to the memory:

- The ingress port memory consumption exceeds the SYS:PORT:ATOP_CFG.ATOP watermark.
- The total consumed memory in the shared queue system exceeds the SYS:PORT:ATOP_TOT_CFG.ATOP_TOT watermark.

4.8.9 Test Utilities

This section describes some of test utilities that are built into the shared queue system.

Each egress port can enable a frame repeater (SYS::REPEATER), which means that the head-of-line frames in the egress queues are transmitted but not dequeued after transmission. As a result, the scheduler sees the same frames again and again while the repeater function is active.

The SYS:PORT:PORT_MODE.DEQUEUE_DIS disables both transmission and dequeuing from the egress queues when set.

4.8.10 Energy Efficient Ethernet

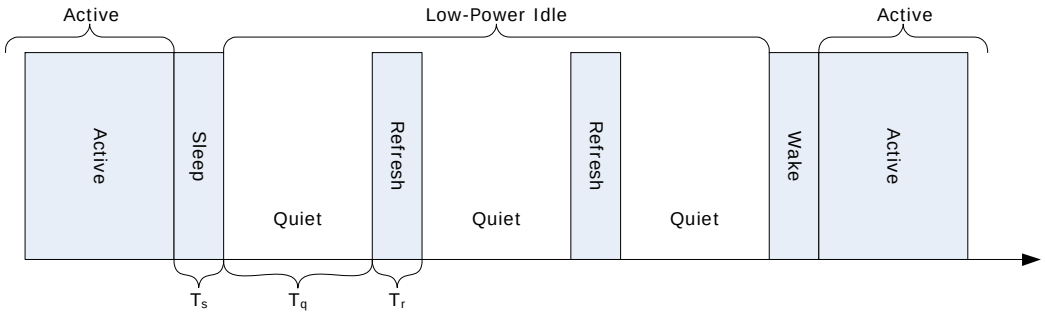
This section provides information about the functions of Energy Efficient Ethernet in the shared queue system. The following tables lists the registers associated with Energy Efficient Ethernet.

Table 54 • **Energy Efficient Ethernet Control Registers**

Register	Description	Replication
SYS:PORT:EEE_CFG	Enabling and configuration of Energy Efficient Ethernet	Per port
SYS:EEE_THRES	Configuration of thresholds (bytes and frames)	None
SYS::SW_STATUS.PORT_LPI	Status bit indicating that egress port is in LPI state	Per port

The shared queue system supports Energy Efficient Ethernet (EEE) as defined by IEEE 802.3az by initiating the Low Power Idle (LPI) mode during periods of low link use. EEE is controlled per port by an egress queue state machine that monitors the queue fillings and ensures correct wake-up and sleep timing. The egress queue state machine is responsible for informing the connected PCS or internal PHY of changes in EEE states (active, sleep, low power idle, and wake up).

Figure 22 • **Low Power Idle Operation**



Energy Efficient Ethernet is enabled per port through SYS:PORT:EEE_CFG.EEE_ENA.

By default, the egress port is transmitting enqueued data. This is the active state. If none of the port's egress queues have enqueued data for the time specified in SYS:PORT:EEE_CFG.EEE_TIMER_HOLDOFF, the egress port instructs the PCS or internal PHY to enter the EEE sleep state.

When data is enqueued in any of the port's egress queues, a timer (SYS:PORT:EEE_CFG.EEE_TIMER_AGE) is started. When one of the following conditions is met, the port enters the wake up state:

- A queue specified as high priority (SYS:PORT:EEE_CFG.EEE_FAST_QUEUES) has any data to transmit.
- The total number of frames in the port's egress queues exceeds SYS::EEE_THRESS.EEE_HIGH_FRAMES.
- The total number of bytes in the port's egress queues exceeds SYS::EEE_THRESS.EEE_HIGH_FRAMES.
- The time specified in SYS:PORT:EEE_CFG.EEE_TIMER_AGE has passed.

PCS and or the internal PHY is instructed to wake up. To ensure that PCS, PHY, and link partner are resynchronized; the egress port holds back transmission of data until the time specified in SYS:PORT:EEE_CFG.EEE_TIMER_WAKEUP has passed. After this time interval, the port resumes transmission of data.

The status bit SYS::SW_STATUS.PORT_LPI is set while the egress port holds back data due to LPI (from the sleep state to the wake up state, both included).

4.9 Scheduler and Shaper

The following table lists the registers associated with the scheduler and egress shaper control.

Table 55 • **Scheduler and Egress Shaper Control Registers**

Register	Description	Replication
SYS::LB_DWRR_FRM_ADJ	Configuration of gap value	Common
SYS::LB_DWRR_CFG	Enabling of gap value adjustment for use in scheduler and shapers	Per port
SYS::SCH_DWRR_CFG	Enabling of DWRR scheduler and configurations of costs	Per port
SYS::SCH_SHAPING_CTRL	Enabling of shaping	Per port
SYS::SCH_LB_CTRL.LB_INIT	Initialization of scheduler and shapers	Common
SYS::LB_THRES	Configuration of shaper threshold	Per shaper
SYS::LB_RATE	Configuration of shaper rate	Per shaper

Each egress port contains a scheduler and a set of egress shapers that control the read out from the egress queuing system to the associated port module.

By default, the scheduler operates in strict priority. The egress queues are searched in the following prioritized order: Queue for QoS class 7 has highest priority followed by 6, 5, 4, 3, 2, 1, and 0.

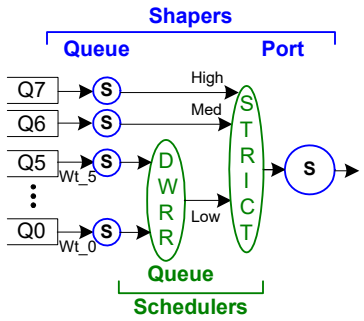
In addition, the scheduler can operate in a mixed mode, where queue 7 and queue 6 are strictly served and queues 5 through 0 operate in a deficit weighted round robin (DWRR) mode. In DWRR mode, QoS class queues 5 through 0 are given a weight and the scheduler selects frames from these queues according to the weights.

Both the egress port and each of the egress queues have an associated leaky-bucket shaper. The egress port shaper is positioned towards the MAC and limits the overall transmission bandwidth on the port. Frames are only scheduled if the port shaper is open. The egress queue shapers control the input to the scheduler for each egress queue. Generally, the scheduler only searches an egress queue if the egress queue's shaper is open.

DWRR is used to guarantee queues a minimum share of the available bandwidth, and shaping is used to configure a maximum rate that cannot be exceeded.

The following illustration shows the egress shapers and scheduler.

Figure 23 • **Egress Scheduler and Shapers**



The overall scheduling algorithm is as follows:

1. If the port shaper is closed, no frames are scheduled. Frames are held back until the port shaper opens.
2. If the port shaper is open, queues with an open queue shaper are candidates for scheduling. Queue 7 has highest priority followed by 6. Queues 5 through 0 may operate in strict mode or in the DWRR mode where each queue is weighted relatively to the other queues. Frames in a queue with a closed queue shaper are held back until the queue shaper opens.
3. If no frames are scheduled during step 2, a second round of scheduling is performed. Queues programmed as work conserving and having a closed queue shaper become candidates for the second round of scheduling.

The following are the configuration options for the shapers and scheduler. Each port is configured independently of other ports. Within a port, the following functionality can be enabled independently:

- DWRR mode (SCH_DWRR_CFG.DWRR_MODE): If set, queues 5 through 0 are scheduled according to the associated weights.
- Port shaping (SCH_SHAPING_CTRL.PORT_SHAPING_ENA): If set, the egress bandwidth is controlled by the port shaper settings.
- Per-queue shaping (SCH_SHAPING_CTRL.PRIO_SHAPING_ENA): If set for a queue, the queue shaper settings control the rate into the scheduler.

4.9.1 Egress Shapers

Each of the egress shapers (port and queues) contains a leaky bucket with the following configurations:

- Maximum rate – Specified in LB_RATE.LB_RATE in steps of 100160 bps. Maximum is 3.282 Gbps.
- Maximum burst size – Specified in LB_THRES.LB_THRES in steps of 4 kilobytes. Maximum is 252 kilobytes.

The frame adjustment value LB_DWRR_FRM_ADJ.FRM_ADJ can be used to program the fixed number of extra bytes to add to each frame transmitted (irrespective of QoS class) in the shaper and DWRR calculations. A value of 20 bytes corresponds to line-rate calculation and accommodates for 12 bytes of inter-frame gap and 8 bytes of preamble. Data-rate based shaping and DWRR calculations are achieved by programming 0 bytes.

Each port can enable the use of the frame adjustment value LB_DWRR_FRM_ADJ.FRM_ADJ through LB_DWRR_CFG.FRM_ADJ_ENA. If enabled on a port, both shapers and scheduler are affected.

By default, while a queue shaper is closed, frames in the queue are not scheduled, even if none of the other queues have frames to transmit. Each queue can enable a work-conserving mode (SCH_SHAPING_CTRL.PRIO_LB_EXS_ENA) in which a second scheduling round is possible. If none of the queues with an open shaper have frames for transmission, work-conserving queues with closed shapers may get a share of the excess bandwidth. The sharing of the excess bandwidth obeys the same configured scheduling rules as for the first round of scheduling.

The queue shapers implement two burst modes. By default, a leaky bucket is continuously assigned new credit according to the configured shaper rate (LB_RATE). This implies that during idle periods, credit is building up, which allows for a burst of data when the queue again has data to transmit. This is not convenient in an Audio/Video Bridging (AVB) environment where this behavior enforces a requirement for larger buffers in end-equipment. To circumvent this, each queue shaper can enable an AVB mode (SCH_SHAPING_CTRLPRIO_LB_AVB_ENA) in which credit is only assigned during periods where the queue shaper has data to transmit and is waiting for another queue to finish a transmission. This AVB mode prevents the accumulation of large amount of credits.

The shapers must be initialized through SCH_LB_CTRL.LB_INIT before use.

4.9.2 Deficit Weighted Round Robin

The DWRR uses a cost-based algorithm compared to a weight-based algorithm. A high cost implies a small share of the bandwidth. When the DWRR is enabled, each of queues 5 through 0 are programmed with a cost (SCH_DWRR_CFG.COST_CFG). A cost is a number between 1 and 32.

The programmable DWRR costs determine the behavior of the DWRR algorithm. The costs result in weights for each queue. The weights are relative to one another, and the resulting share of the egress bandwidth for a particular QoS class is equal to the queue's weight divided by the sum of all the queues' weights.

Costs are easily converted to weights and vice versa given the following two algorithms:

Weights to Costs Given a desired set of weights (W0, W1, W2, W3, W4, W5), the costs can be calculated using the following algorithm:

1. Set the cost of the queue with the smallest weight (Wsmallest) to cost 32.
2. For any other queue Qn with weight Wn, set the corresponding cost Cn to:
   Cn = 32 × Wsmallest/Wn

Costs to Weights Given a set of costs for all queues (C0, C1, C2, C3, C4, C5), the resulting weights can be calculated using the following algorithm:

1. Set the weight of the queue with the highest cost (Chighest) to 1.
2. For any other queue Qn with cost Cn, set the corresponding weight Wn to Wn = Chighest/Cn

Cost and Weight Conversion Examples

The following bandwidth distribution must be implemented:

- Queue 0: 5% (W0 = 5)
- Queue 1: 10% (W1 = 10)
- Queue 2: 15% (W2 = 15)
- Queue 3: 20% (W3 = 20)
- Queue 4: 20% (W4 = 20)
- Queue 5: 30% (W5 = 30)

Given the algorithm to get from weights to costs, the following costs are calculated:

- C0 = 32 (Smallest weight)
- C1 = 32*5/10 = 16
- C2 = 32*5/15 = 10.67 (rounded up to 11)
- C3 = 32*5/20 = 8
- C4 = 32*5/20 = 8
- C5 = 32*5/30 = 5.33 (rounded down to 5)

Due to the rounding off, these costs result in the following bandwidth distribution, which is slightly off compared to the desired distribution:

- Queue 0: 4.92%
- Queue 1: 9.85%
- Queue 2: 14.32%
- Queue 3: 19.70%
- Queue 4: 19.70%
- Queue 5: 31.51%

4.9.3 Shaping and DWRR Scheduling Examples

This section provides examples and additional information about the use of the egress shapers and scheduler.

Mixing DWRR and Shaping Example

- Port is shaped down to 500 Mbps.
- Queues 7 and 6 are strict while queue 5 through 0 are weighted.
- Queue 7 is shaped to 100 Mbps.
- Queue 6 is shaped to 50 Mbps.
- The following traffic distribution is desired for queue 5 through 0:
  Q0: 5%, Q1: 10%, Q2: 15%, Q3: 20%, Q4: 20%, Q5: 30%
- Each queue receives 125 Mbps of incoming traffic.

The following table lists the DWRR configuration and the resulting egress bandwidth for the various queues.

Table 56 • **Example of Mixing DWRR and Shaping**

Queue	Distribution of Weighted Traffic	Configuration Costs/Weights (C*n*/W*n*)	Result: Egress Bandwidth
Q0	5%	32/1	1/(1+2+2.9+4+4+6.4) × (500 – Mbps – 150 Mbps) = 17.2 Mbps
Q1	10%	16/2	2/(1+2+2.9+4+4+6.4) × (500 – Mbps – 150 Mbps) = 34.5 Mbps
Q2	15%	11/2.9	2.9/(1+2+2.9+4+4+6.4) × (500 – Mbps – 50 Mbps) = 50.1 Mbps
Q3	20%	8/4	4/(1+2+2.9+4+4+6.4) × (500 – Mbps – 150 Mbps) = 68.9 Mbps
Q4	20%	8/4	4/(1+2+2.9+4+4+6.4) × (500 – Mbps – 150 Mbps) = 68.9 Mbps
Q5	30%	5/6.4	6.4/(1+2+2.9+4+4+6.4) × (500 – Mbps – 150 Mbps) = 110.3 Mbps
Q6			50 = Mbps
Q7			100 = Mbps
Sum:	100%		**500** = **Mbps**

Strict and Work-Conserving Shaping Example

- Port is shaped down to 500 Mbps.
- All queues are strict.
- All queues are shaped to 50 Mbps.
- Queues 6 and 7 are work-conserving (allowed to use excess bandwidth).
- All queues receive 125 Mbps of traffic each.

The following table lists the resulting egress bandwidth for the various queues.

Table 57 • **Example of Strict and Work-Conserving Shaping**

Queue	Result: Egress Bandwidth
Q0	50 Mbps
Q1	50 Mbps
Q2	50 Mbps
Q3	50 Mbps
Q4	50 Mbps
Q5	50 Mbps
Q6	75 Mbps (Gets the last 25 Mbps of the 100 Mbps in excess not used by queue 7)
Q7	125 Mbps (Gets 75 Mbps of the 100 Mbps in excess limited only by the received rate)

Table 57 • **Example of Strict and Work-Conserving Shaping *(continued)***

Queue	Result: Egress Bandwidth
Sum:	**500 Mbps**

4.10 Rewriter

The switch core includes a rewriter common for all ports that determines how the egress frame is edited before transmitted. The rewriter performs the following editing:

- VLAN editing; tagging of frames and remapping of PCP and DEI.
- DSCP remarking; rewriting the DSCP value in IPv4 and IPv6 frames based on classified DSCP value.
- FCS updating.
- CPU extraction header insertion.

Each port module including the CPU port module has its own set of configuration in the rewriter. Each frame is handled by the rewriter one time per destination port.

4.10.1 VLAN Editing

The following table lists the registers associated with VLAN editing.

Table 58 • **VLAN Editing Registers**

Register	Description	Replication
PORT_VLAN_CFG	Port VLAN for egress port. Used for untagged set.	Per port
TAG_CFG	Tagging rules for port tag	Per port
PCP_DEI_QOS_MAP_CFG	Mapping table. Maps QoS class to new PCP and DEI values.	Per port per QoS

The rewriter initially pops the number of VLAN tags specified by the VLAN_POP_CNT parameter received with the frame from the classifier. One VLAN tag can be popped. The rewriter itself does not influence the number of VLAN tags being popped.

After popping the VLAN tags, the rewriter decides whether to push zero or one new VLAN tag to the outgoing frame according to the port's tagging configuration in register TAG_CFG The following table lists the possible tagging combinations:

Table 59 • **Tagging Combinations**

TAG_CFG.TAG_CFG	Tagging action
0	No tagging.
1	Tag all frames according to the port's tagging configuration. Do not tag if VID=0 or VID=PORT_VLAN.PORT_VID.
2	Tag all frames according to the port's tagging configuration. Do not tag if VID=0.
3	Tag all frames according to the port's tagging configuration.

When adding a VLAN tag, the contents of the tag header, including the TPID, is highly programmable. The starting point is the classified tag header coming from the analyzer containing a PCP, DEI, VID and tag type.

For each of the fields in the resulting tag, it is programmable how the value is determined. For the port tag, the following options are available:

Port tag: PCP and DEI

- Use the classified values.
- Use the egress port's port VLAN (PORT_VLAN.PORT_PCP, PORT_VLAN.PORT_DEI).
- Map the QoS class to a new set of PCP and DEI using the per-port table PCP_DEI_QOS_MAP_CFG.
- Set the DEI to the DP level, independently of the preceding PCP and DEI configurations.

Port Tag: VID

- Use the classified VID.

Port Tag: TPID

- Use Ethernet type 0x8100 (C-tag)
- Use Ethernet type 0x88A8 (S-tag)
- Use custom Ethernet type programmed in PORT_VLAN.PORT_TPID.
- Use custom Ethernet type programmed in PORT_VLAN.PORT_TPID unless the incoming tag was a C-tag.

4.10.2 DSCP Remarking

The following table lists the registers associated with DSCP remarking.

Table 60 • **DSCP Remarking Registers**

Register	Description	Replication
DSCP_CFG	Selects how the DSCP remarking is done	Per port
DSCP_REMAP_CFG	Mapping table from DSCP to DSCP.	None

The rewriter can remark the DSCP value in IPv4 and IPv6 frames, that is, write a new DSCP value to the DSCP field in the frame.

If a port is enabled for DSCP remarking (DSCP_CFG.DSCP_REWR_CFG), the new DSCP value is derived by using the classified DSCP value from the classifier in the ingress port. This DSCP value can be mapped before replacing the existing value in the frame. The following options are available:

- No DSCP remarking - Leave the DSCP value in the frame untouched.
- Update the DSCP value in the frame with the value received from the analyzer
- Update the DSCP value in the frame with the value received from the analyzer remapped through DSCP_REMAP_CFG.

Additionally, the IP checksum is updated for IPv4 frames. Note that the IPv6 header does not contain a checksum. As a result, checksum updating does not apply for IPv6 frames.

4.10.3 FCS Updating

The following table lists the registers associated with FCS updating.

Table 61 • **FCS Updating Registers**

Register	Description	Replication
PORT_CFG.FCS_UPDATE_NONCPU_CFG	FCS update configuration for non-CPU injected frames.	Per port
PORT_CFG.FCS_UPDATE_CPU_ENA	FCS update configuration for CPU injected frames.	Per port

The rewriter updates a frame's FCS when required or instructed to do so. Different handling is available for frames injected by the CPU and for all other frames.

For non-CPU injected frames, the following update options are available:

- Never update the FCS.

- Conditional update - Update the FCS if the frame was modified due to VLAN tagging or DSCP remarking.
- Always update the FCS.

Additionally, the rewriter can update the FCS for all frames injected from the CPU through the CPU injection queues in the CPU port module:

- Never update the FCS.
- Always update the FCS.

4.10.4 CPU Extraction Header Insertion

The following table lists the registers associated with CPU extraction header insertion.

Table 62 • **CPU Extraction Header Insertion Registers**

Register	Description	Replication
PORT_CFG.IFH_INSERT_ENA	Enables insertion of the CPU extraction header.	Per port
PORT_CFG.IFH_INSERT_MODE	Configures the position of the CPU extraction header.	Per port

Any port in the switch core can request the rewriter to insert a CPU extraction header in the frame before transmission. For more information about the contents of the CPU extraction header, see CPU Extraction and Injection, page 162.

The CPU extraction header can be placed before the DMAC or right after the SMAC. When inserting the header, the frame is extended with eight bytes. Note that the FCS is only updated when the header is inserted after the SMAC.

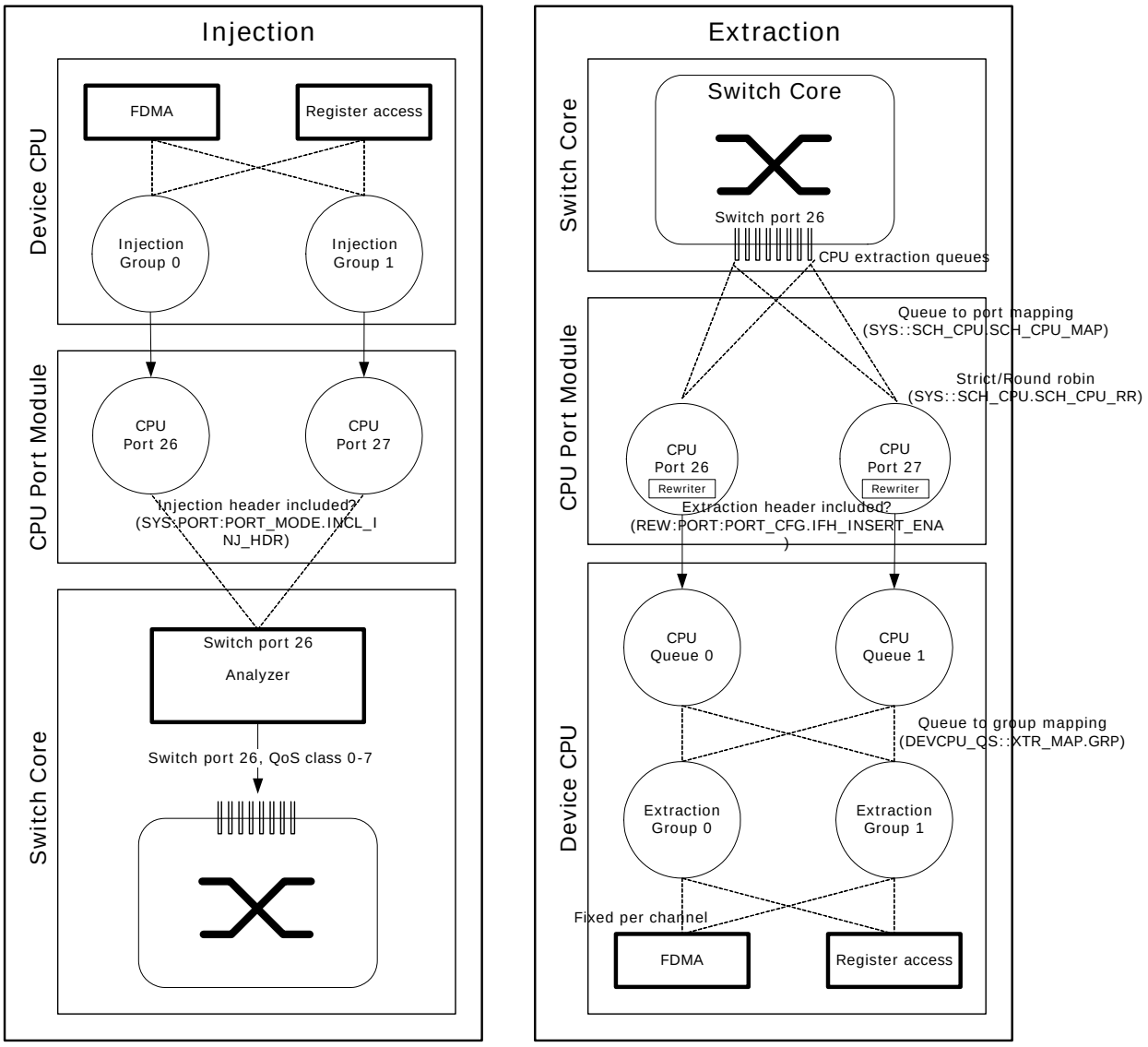
The insertion of the CPU extraction header is the last editing in the rewriter. This implies that any VLAN tags in the frame will appear after the extraction header.

4.11 CPU Port Module

The CPU port module connects the switch core to the CPU system so that frames can be injected from or extracted to the CPU. It is also possible to use a regular front port as a CPU port. This is known as a Network Processor Interface (NPI).

The following illustration shows how the switch core interfaces to the CPU system through the CPU port module for injection and extraction of frames.

Figure 24 • **CPU Injection And Extraction**



4.11.1 Frame Extraction

The following table lists the registers associated with frame extraction.

Table 63 • **Frame Extraction Registers**

Register	Description	Replication
SYS::SCH_CPU.SCH_CPU_MAP	Configuration of mapping of extraction queues to CPU ports	Per CPU port (ports 26 and 27)
SYS::SCH_CPU.SCH_CPU_RR	Configuration of CPU scheduler	Per CPU port (ports 26 and 27)
REW:PORT:PORT_CFG.IFG_INSERT_ENA	Enables insertion of extraction header	Per CPU port (port 26 and 27)

In the switch core, extracted frames are forwarded to one of the eight CPU extraction queues. Each of these queues is mapped to one of two CPU ports (port 26 and port 27) through SYS::SCH_CPU.SCH_CPU_MAP. For each CPU port, there is a scheduler working either in strict mode

or round robin, which selects between the CPU extraction queues mapped to the same CPU port (SYS::SCH_CPU.SCH_CPU_RR). In strict mode, higher queue numbers are preferred over smaller queue numbers. In round robin, all queue are serviced one after another.

The two CPU ports contain the same rewriter as regular front ports. The rewriter modifies the frames before sending them to the CPU. In particular, the rewriter inserts an extraction header (REW::PORT:PORT_CFG.IFH_INSERT_ENA), which contains relevant side band information about the frame such as the frame's classification result (VLAN tag information, DSCP, QoS class) and the reason for sending the frame to the CPU. For more information about the rewriter, see Rewriter, page 78.

The device CPU contains the functionality for reading out the frames. This can be done through the frame DMA or regular register access.

The following table lists the contents of the CPU extraction header.

Table 64 • **CPU Extraction Header**

Field	Bit	Width	Description
SIGNATURE	56	8	Must be 0xFF.
SRC_PORT	51	5	The port number where the frame was received (0-26).
DSCP	45	6	The frame's classified DSCP value.
RESERVED	38	8	Unused.
SFLOW_ID	32	5	sFlow sampling ID. 0-26: Frame was SFlow sampled by a Tx sampler on port given by SFLOW_ID. 27: Frame was SFlow sampled by an RX sampler on port given by SRC_PORT. 28-30: Reserved. 31: Frame was not SFlow sampled.
RESERVED	30	2	Unused.
LRN_FLAGS	28	2	The source MAC address learning action triggered by the frame. 0: No learning. 1: Learning of a new entry. 2: Updating of an already learned unlocked entry. 3: Updating of an already learned locked entry.
CPU_QUEUE	20	8	CPU extraction queue mask (one bit per CPU extraction queue). Each bit set implies the frame was subjected to CPU forwarding to the specific queue.
QOS_CLASS	17	3	The frame's classified QoS class.
TAG_TYPE	16	1	The tag information's associated Tag Protocol Identifier (TPID). The definitions are: 0: C-tag: EtherType = 0x8100. 1: S-tag: EtherType = 0x88A8 or custom value.
PCP	13	3	The frame's classified PCP.
DEI	12	1	The frame's classified DEI.
VID	0	12	The frame's classified VID.

4.11.2 Frame Injection

The following table lists the registers associated with frame injection.

Table 65 • **Frame Injection Registers**

Register	Description	Replication
SYS:PORT:PORT_MODE.INCL_INJ_HDR	Enable parsing of injection header	Per CPU port (ports 26 and 27)
SYS:PORT:EQ_PREFER_SRC	Enable preferred arbitration of the CPU port (port 26) over front ports	CPU port (port 26 only)

The CPU injects frames through the two CPU injection groups independent of each other. The injection groups connect to the two CPU ports (port 26 and port 27) in the CPU port module. In CPU port module, each of the two CPU ports have dedicated access to the switch core. Inside the switch core, all CPU injected frames are seen as coming from CPU port (port 26). This implies that both CPU injection groups consume memory resources from the shared queue system for port 26 and that analyzer configuration for port 26 are applied to all frames.

In the switch core, the CPU port can be preferred over other ingress ports when transferring frames to egress queues by enabling precedence of the CPU port (SYS::EQ_PREFER_SRC).

The first eight bytes of a frame written to a CPU injection group is an injection header containing relevant side band information about how the frame must be processed by the switch core. The CPU ports must be enabled to expect the CPU injection header (SYS:PORT:INCL_INJ_HDR).

On a per-frame basis, the CPU controls whether frames injected through the CPU port module are processed by the analyzer. If the frame is processed by the analyzer, it is sent through the processing steps to calculate the destination ports for the frame. If analyzer processing is not selected, the CPU can specify the destination port set and related information to fully control the forwarding of the frame. For more information about the analyzer's processing steps, see Forwarding Engine, page 55.

The contents of the CPU injection header is listed in the following table.

Table 66 • **CPU Injection Header**

Field	Bit	Width	Description
BYPASS	63	1	When this bit is set, the analyzer processing is skipped for this frame. The destination set is specified in DEST and CPU_QUEUE. Forwarding uses the QOS_CLASS, and the rewriter uses the tag information (POP_CNT, TAG_TYPE, PCP, DEI, VID) for rewriting actions. When this bit is cleared, the analyzer determines the destination set, QoS class, and VLAN classification for the frame through normal frame processing including lookups in the MAC table and VLAN table.
RESERVED	59	4	Unused.
DEST	32	27	This is the destination set for the frame. DEST[26] is the CPU. Used when BYPASS = 1.
RESERVED	30	2	Unused.

Table 66 • **CPU Injection Header *(continued)***

Field	Bit	Width	Description
POP_CNT	28	2	Number of VLAN tags that must be popped in the rewriter before adding new tags. Used when BYPASS = 1. 0: No tags must be popped. 1: One tag must be popped. 2: Two tags must be popped. 3: Disable rewriting of VLAN tags and DSCP value. The FCS is still updated.
CPU_QUEUE	20	8	CPU extraction queue mask (one bit per CPU extraction queue). Each bit set implies the frame must be forwarded by the CPU to the specific queue. Used when BYPASS = 1 and DEST[26] = 1.
QOS_CLASS	17	3	The frame's classified QoS class. Used when BYPASS = 1.
TAG_TYPE	16	1	The tag information's associated Tag Protocol Identifier (TPID). Used when BYPASS = 1. 0: C-tag: EtherType = 0x8100. 1: S-tag: EtherType = 0x88A8 or custom value.
PCP	13	3	The frame's classified PCP. Used when BYPASS = 1.
DEI	12	1	The frame's classified DEI. Used when BYPASS = 1.
VID	0	12	The frame's classified VID. Used when BYPASS = 1.

4.11.3 Network Processor Interface (NPI)

The following table lists the registers associated with the network processor interface.

Table 67 • **Network Processor Interface Registers**

Register	Description	Replication
SYS::EXT_CPU_CFG	Configuration of the NPI port number and configuration of which CPU extraction queues are redirected to the NPI.	None
REW:PORT:PORT_CFG.IFG_INSERT_ENA	Enables insertion of extraction header	Per port
SYS:PORT:PORT_MODE.INCL_INJ_HDR	Configuration of NPI ingress mode.	Per port

Any front port can be configured as a network processor interface through which frames can be injected from and extracted to an external CPU. Only one port can be an NPI at the same time. SYS::EXT_CPU_CFG.EXT_CPU_PORT holds the port number of the NPI.

A dual CPU system is possible where both the internal and the external CPU are active at the same time. Through SYS::EXT_CPU_CFG.EXT_CPUQ_MSK, it is configurable to which of the eight CPU extraction queues are directed to the internal CPU and which are directed to external CPU. A frame can be extracted to both the internal CPU and the external CPU if the frame is extracted for multiple reasons.

A frames being extracted to the external CPU can have the CPU extraction header inserted in front of the frame (REW:PORT:PORT_CFG.IFG_INSERT_ENA), and a frame being injected to the switch core can have the CPU injection header inserted in front of the frame (SYS:PORT:PORT_MODE.INCL_INJ_HDR).

Through the BYPASS field in the CPU injection header, the external CPU can control forwarding of injected frames by either letting the frame analyze and forward accordingly or directly specifying the destination set

4.12 Clocking and Reset

The following table lists the registers associated with clocking and reset.

Table 68 • **Clocking and Reset Registers**

Target:Register_group:Register.field	Description	Replication
HSIO::PLL5G_STATUS0	LCPLL status	None
DEVCPU_GCB:: SOFT_CHIP_RST	Reset of the internal copper PHYs or the entire device	None
DEVCPU_GCB::SOFT_DEVCPU_RST	Reset of the extraction and injection modules	None
CFG::RESET	CPU reset configuration	None

The LCPLL provides the clocks used by the SerDes, the central part of the switch core, and the VCore-Ie CPU system.

The reference clock for the LCPLL (REFCLK_P and REFCLK_N pins) is either differential or single-ended. The frequency can be 25 MHz, 125 MHz, or 156.25 MHz. For more information about the reference clock frequency selections, see the Pins by Function section for the appropriate device.

For more information about reference clock options, see Reference Clock, page 589.

A global software reset is performed with DEVCPU_GCB::SOFT_CHIP_RST.

For more information about the configuration of the CPU frequency and software reset options when using the V-Core-III, see Clocking and Reset, page 88.

For more information about the clock and reset configuration for the Ethernet interfaces in the port modules, see MAC, page 12, and SERDES6G, page 18. The MAC clock domains are not included in the global reset.

5 VCore-Ie System and CPU Interface

This section provides information about the functional aspects of blocks and the interfaces related to the VCore-Ie on-chip microprocessor system.

The VSC7420-02, VSC7421-02, and VSC7422-02 devices contain a fast VCore-Ie CPU system that is based on an embedded 8051-compatible microprocessor. The VCore-Ie system can control the device independently or it can support an external CPU, relieving the external CPU of the otherwise time-consuming tasks of transferring frames, maintaining the switch core, and handling networking protocols.

When the VCore-Ie CPU is enabled, it either boots up independently from Flash or a code-image can be manually loaded and started from an external CPU.

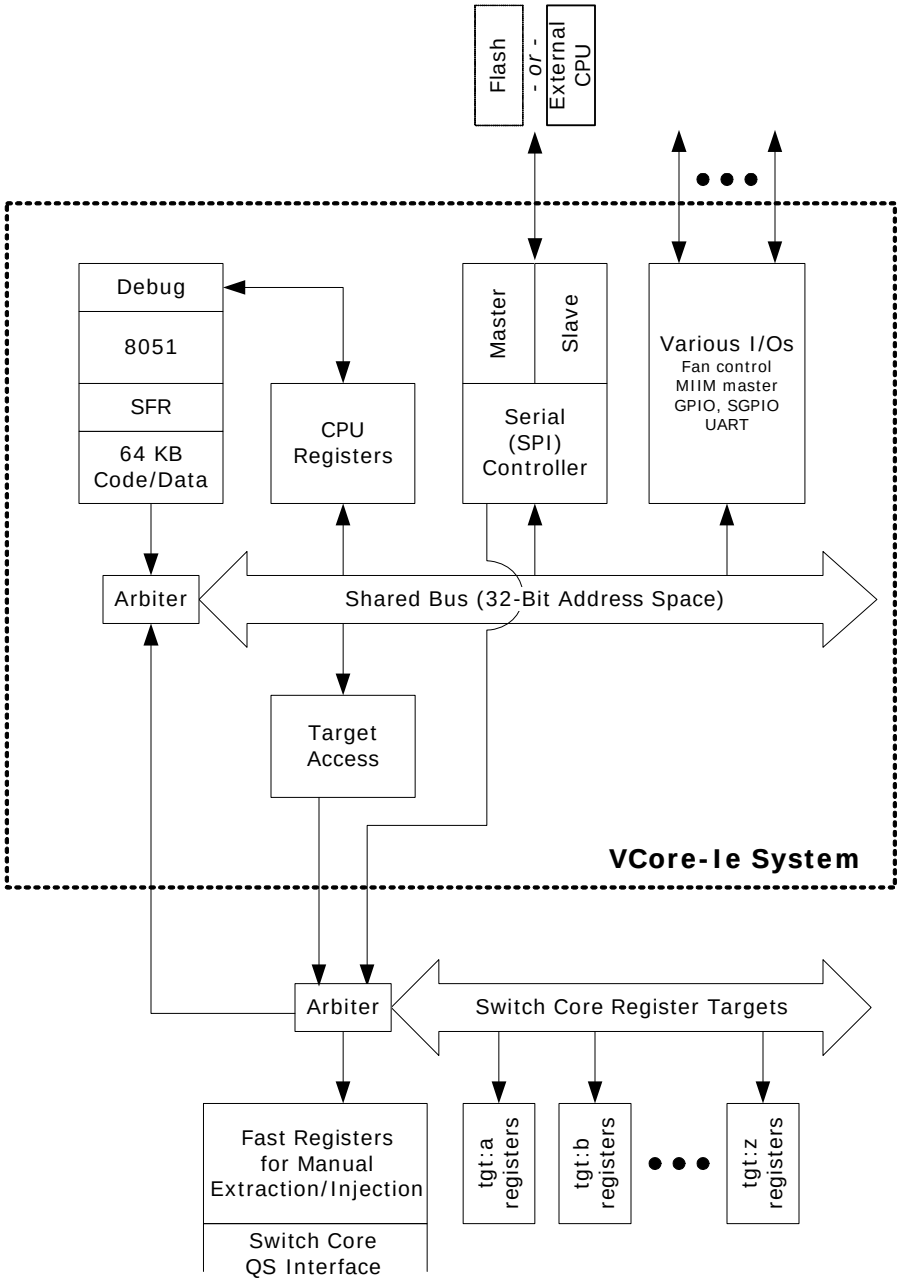
An external CPU can be connected to the VSC7420-02, VSC7421-02, and VSC7422-02 devices through the serial interface (SI) or dedicated MIIM slave interface. When the VCore-Ie CPU is enabled and boots up from Flash, the SI is reserved as boot interface and cannot be used by an external CPU.

The VCore-Ie CPU and the external CPUs can access internal chip registers for configuration, monitoring, and collecting statistics.

The VCore-Ie system includes a number of functional blocks and registers that are tightly coupled to the VCore-Ie CPU. The external CPU can access these blocks and register through an indirect addressing scheme. The registers are available when the VCore-Ie CPU is enabled or disabled.

The following illustration shows how the serial controller operates in either master or slave mode. When the VCore-Ie CPU is enabled, it forces the boot interface to master mode. An interface in slave mode allows an external CPU access to register targets inside the device.

Figure 25 • **VCore-Ie System Block Diagram**



5.1 VCore-Ie Configurations

The following table summarizes the possible VCore-Ie configurations.

Table 69 • **VCore-Ie Configurations**

Level of Strapping Pins			
VCORE_CFG[2]	**VCORE_CFG[1]**	**VCORE_CFG[0]**	**Behavior**
Don't care	0	0	The 8051 is enabled and boots from SI.

Table 69 • **VCore-Ie Configurations *(continued)***

Level of Strapping Pins			
VCORE_CFG[2]	**VCORE_CFG[1]**	**VCORE_CFG[0]**	**Behavior**
Don't care	0	1	Automatic boot is disabled by forcing the 8051 into reset. SI slave mode is enabled. The 8051 can be manually started from the on-chip RAM.
Don't care	1	1	Automatic boot is disabled by forcing the 8051 into reset. MIIM and SI slave modes are enabled. The 8051 can be manually started from the on-chip RAM.

The VCore-Ie CPU can boot up automatically and then hand over ownership of the SI to an external CPU (after it boots up from SI Flash).

5.2 Clocking and Reset

The following table lists the registers associated with clocking and reset.

Table 70 • **Clocking and Reset Configuration Registers**

Register	Description
RESET	VCore-Ie reset configuration and release of specific blocks from reset
SOFT_CHIP_RST	Resets configuration
WDT	Watchdog timer configuration and status

The frequency of the VCore-Ie CPU is 250 MHz, and the frequency of the VCore-Ie system is 125 MHz.

The VCore-Ie CPU (including the VCore-Ie system) can be soft-reset by setting RESET.CORE_RST_FORCE. By default, this resets both the VCore-Ie CPU and the VCore-Ie system. The VCore-Ie system can be excluded from a soft reset by setting RESET.CORE_RST_CPU_ONLY;soft-reset using CORE_RST_FORCE only then resets the VCore-Ie CPU.

The VSC7420-02, VSC7421-02, and VSC7422-02 devices can be soft-reset by using SOFT_CHIP_RST.SOFT_CHIP_RST, which by default, resets the entire device. The VCore-Ie system and CPU can be protected from a chip-level soft reset by configuring RESET.CORE_RST_PROTECT. In this case, a chip-level soft reset is applied to all other blocks except the VCore-Ie system and CPU.

The GPIO alternate modes are reset to the default values when performing chip-level soft reset. This must be taken into account when the VCore-Ie system is protected from chip-level soft reset (by means of RESET.CORE_RST_PROTECT).

When automatic booting of the VCore-Ie CPU is disabled using the VCORE_CFG pins, the VCore-Ie CPU can be manually released through RESET.CPU_RELEASE.

5.2.1 Watchdog Timer

The VCore-Ie system has a built-in watchdog timer (WDT) with a time-out cycle of two seconds. The watchdog timer is enabled, disabled, or reset through the WDT register. The watchdog timer is disabled by default.

After the watchdog timer is enabled, it must be regularly reset by software. Otherwise, it times out and causes a VCore-Ie soft reset equivalent to setting RESET.CORE_RST_FORCE. Improper use of the WDT.WDT_LOCK causes an immediate timeout-reset as if the watchdog timer had run out. The

WDT.WDT_STATUS field shows if the last VCore-Ie CPU reset was caused by WDT timeout (or improper locking sequence). The WDT.WDT_STATUS field is updated only during VCore-Ie CPU reset.

To enable or to reset the watchdog timer, write the locking sequence, as described in WDT.WDT_LOCK, at the same time as setting the WDT.WDT_ENABLE field.

Because watchdog timeout is equivalent to setting RESET.CORE_RST_FORCE, the RESET.CORE_RST_CPU_ONLY field also applies to watchdog initiated soft reset.

5.3 Shared Bus

The following table lists the registers associated with the shared bus.

Table 71 • **Shared Bus Configuration Registers**

Register	Description
PL1, PL2, PL3	Master priorities

The shared bus is a 32-bit address and 32-bit data bus with dedicated master and slave interfaces that interconnect all blocks in the VCore-Ie system. The VCore-Ie CPU and external CPU are masters on the shared bus and only they can start access on the bus.

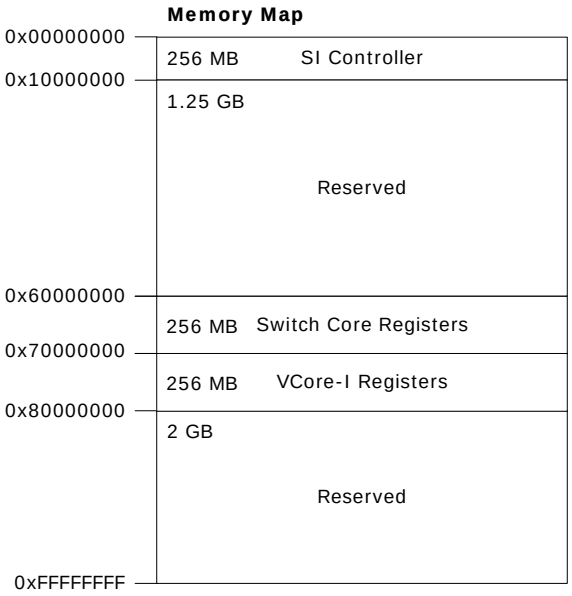
The shared bus uses byte addresses, and transfers of 8, 16, or 32 bits can be made. For 16-bit and 32-bit access, the addresses must be aligned to 16-bit and 32-bit addresses, respectively. To increase performance, bursting of multiple 32-bit words on the shared bus can be performed.

All slaves are mapped into the VCore-Ie system's 32-bit address space and can be accessed directly by masters on the shared bus.

The address space of the shared bus is considerably wider than what the 8051 can access directly. However, by using custom special function registers, which is part of the Microsemi 8051 implementation, reads and writes can be done in the complete VCore-Ie shared bus region. For more information, see VCore-Ie CPU, page 91.

The following illustration shows the mapping of the shared bus memory.

Figure 26 • **Shared Bus Memory Map**



5.3.1 Shared Bus Arbitration

The VCore-Ie shared bus arbitrates between masters that want to access the bus; the default is to use a strict prioritized arbitration scheme where the VCore-Ie CPU has highest priority. Priorities can be changed using registers PL1 though PL3.

5.3.2 SI Memory Region

This section provides information about the functional aspects of the serial interface (SI) in master mode. For information about using an external CPU to access register targets using the serial interface, see Serial Interface in Slave Mode, page 101.

The following table lists the registers associated with the SI controller.

Table 72 • **SI Controller Configuration Registers**

Register	Description
SPI_MST_CFG	Serial interface speed
SW_MODE	Manual control of the serial interface pins

When the VCore-Ie system controls the SI, reading from the SI controller's memory region is automatically converted to read access on the SI. The SI supports one 24-address bit Flash device. The VCore-Ie CPU can execute code directly from Flash by executing from the SI controller's memory region.

The SI controller accepts 8-bit, 16-bit, and 32-bit read access with or without bursting, byte address n in the SI controller's memory region maps directly to byte address n inside the SPI Flash. Writing to the SI requires manual control of the SI pins using software. Setting SW_MODE.SW_PIN_CTRL_MODE places all SI pins under software control. Output enable and the value of SI_Clk, SI_DO, SI_nEn are controlled using the SW_MODE register. The value of the SI_DI pin is available through SW_MODE.SW_SPI_SDI.

Note The VCore-Ie CPU cannot execute code directly from the SI controller's memory region while simultaneously writing to the serial interface.

The following table lists the serial interface pins.

Table 73 • **Serial Interface Pins**

Pin Name	I/O	Description
SI_nEN	O	Active low chip select.
SI_Clk	O	Clock output.
SI_DO	O	Data output (MOSI).
SI_DI	I	Data output (MISO).

The SI controller does speculative perfecting of data. After reading address *n*, the SI controller automatically continues reading address *n* + 1, so that the next value is ready if or when requested by the VCore-Ie CPU. This greatly optimizes reading from sequential addresses in the Flash, such as when copying data from Flash into program memory.

Figure 27 • **SI Read Timing in Normal Mode**

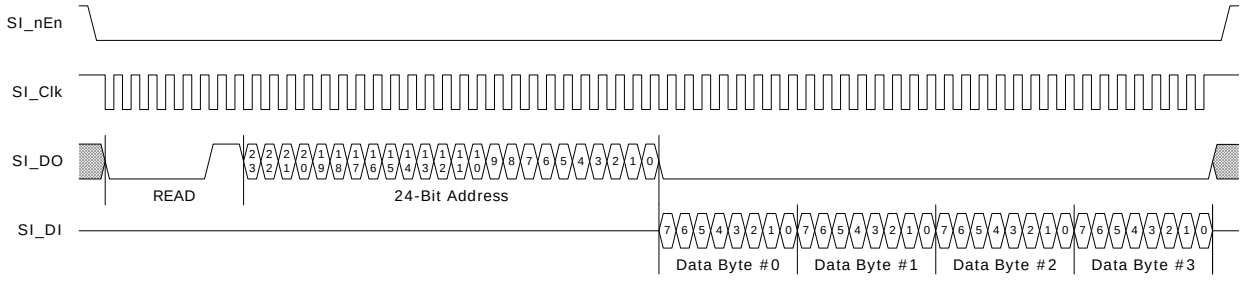
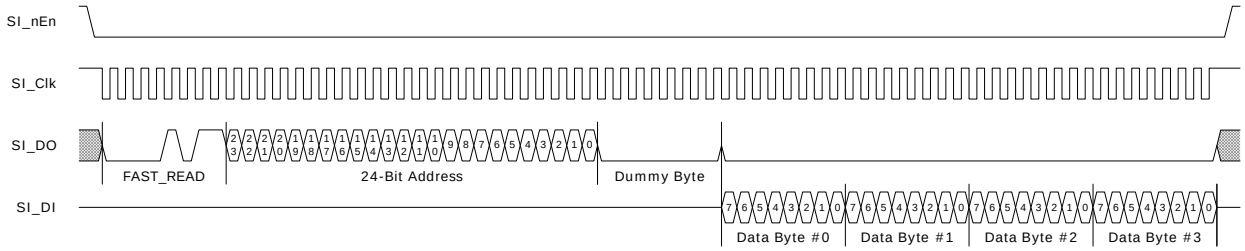


Figure 28 • **SI Read Timing in Fast Mode**



The default timing of the SI controller operates with most serial interface Flash devices. Use the following process to calculate the optimized SI parameters for a specific SI device:

1. Calculate an appropriate frequency divider value as described in SPI_MST_CFG.CLK_DIV. The SI operates at no more than 25 MHz, and the maximum frequency of the SPI device must not be exceeded. For information about the VCore-Ie system frequency, see Clocking and Reset, page 88.
2. The SPI device may require a FAST_READ command rather than normal READ when the SI frequency is increased. Setting SPI_MST_CFG.FAST_READ_ENA makes the SI controller use FAST_READ commands.
3. Calculate SPI_MST_CFG.CS_DESELECT_TIME so that it matches how long the SPI device requires chip-select to be deasserted between accesses. This value depends on the SI clock period that results from the SPI_MST_CFG.CLK_DIV setting.

These parameters must be written to SPI_MST_CFG. The CLK_DIV field must either be written last or at the same time as the other parameters. The SPI_MST_CFG register can be configured while also booting up from the SI.

When the VCore CPU boots from the SI interface, the default values of the SPI_MST_CFG register are used until the SI_MST_CFG is reconfigured with optimized parameters. This implies that SI_Clk is operating at approximately 4 MHz, with normal read instructions, and maximum gap between chip select operations to the Flash.

5.3.3 Switch Core Registers Memory Region

Register targets in the Switch Core are memory-mapped into the Switch Core registers region of the shared bus memory map. All registers are 32-bit wide and must only be accessed using 32-bit reads and writes. Bursts are supported.

Writes to this region are buffered (there is a one-word write buffer). Multiple back-to-back write access pauses the shared bus until the write buffer is freed up (until the previous writes are done). Reads from this region pause the shared bus until read data is available.

Registers in the 0x60000000 though 0x6FFFFFFF region in the 0x6 targets are physically located in other areas of the device rather than the VCore-Ie system; reading from these targets may take up to 1.1 µs in a single master system. For more information, see Register Access and Multimaster Systems, page 101.

5.3.4 VCore-Ie Registers Memory Region

Registers inside the VCore-Ie domain are memory mapped into the VCore-Ie registers region of the shared bus memory map. All registers are 32-bit wide and must only be accessed using 32-bit reads and writes, bursts are supported.

The registers in the 0x70000000 though 0x7FFFFFFF region are all placed inside the VCore-Ie, read and write access to these registers is fast (done in a few clock cycles).

5.4 VCore-Ie CPU

The VCore-Ie CPU system is based on a fast, embedded 8051-compatible microprocessor.

When automatic boot is enabled using the VCORE_CFG strapping pins, the VCore-Ie CPU automatically starts to execute code in the Flash at byte address 0 in the SI controller region.

A typical automatic boot sequence is as follows:

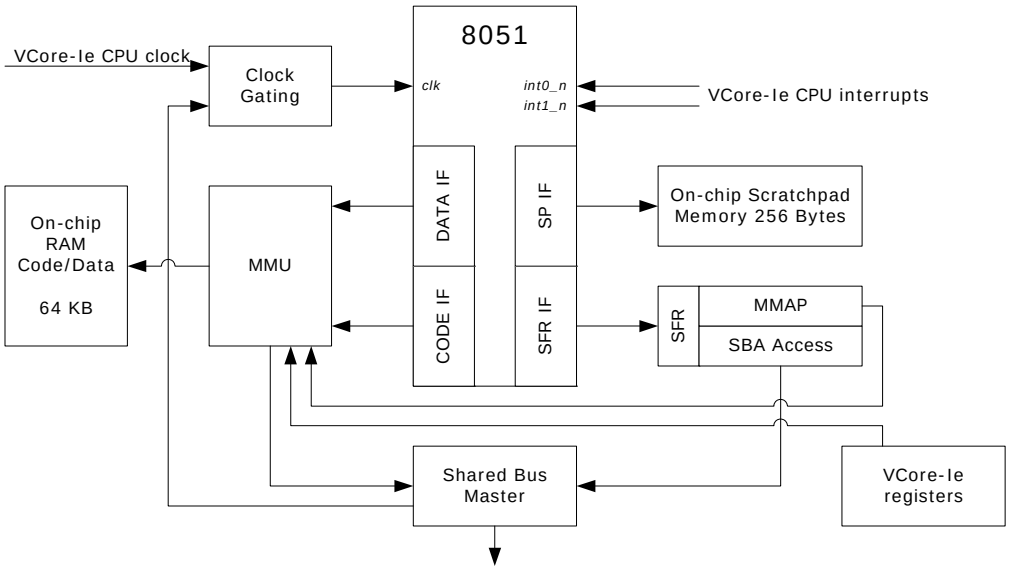
1. Configure the appropriate VCore-Ie CPU frequency the same as for clocking and reset. For more information about supported clock frequencies, see Clocking and Reset, page 88. The maximum frequency for the VCore-Ie CPU is 208.33 MHz.
2. Speed up the boot interface. For more information, see Shared Bus, page 89.
3. Copy code-image from the Flash to on-chip memory. For more information, see Loading On-chip Memory, page 94.
4. Map on-chip memory. For more information, see Mapping On-chip Memory, page 95.

When automatic boot is disabled, an external CPU can start the VCore-Ie CPU through the registers. A typical manual boot-up sequence is as follows:

1. Load on-chip memory with code-image. For more information, see Loading On-chip Memory, page 94.
2. Map on-chip memory. For more information, see Mapping On-chip Memory, page 95.
3. Configure appropriate VCore-Ie CPU frequency and release reset to the VCore-Ie CPU. For more information, see Clocking and Reset, page 88.

Note When manually booting up, the size of the code image is limited by the size of the on-chip memory. However, when automatically booting up from Flash, the VCore-Ie CPU can use paging to access code and data for a total of up to 16 megabytes. For more information, see Paged Access to VCore-Ie Shared Bus, page 96.

Figure 29 • **VCore-Ie Block Diagram**



The preceding illustration shows the basic blocks of the VCore-Ie 8051 implementation. The illustration highlights features such as:

- VCore-Ie CPU frequency of 250 MHz.
- Advanced clock gating control that automatically pauses the 8051 during shared bus access.
- Two independent interrupts from dedicated VCore-Ie interrupt controller allows interrupts from all major VCore-Ie blocks, including timers, UART, and hardware based semaphores (for communication with external CPU).
- On-chip 256-byte scratchpad. The lower 128 bytes are directly and indirectly addressable. The upper 128 bytes are indirectly addressable.
- Simple Memory Management Unit maps 8051's code and data access to either on-chip memory or shared bus (with support for paging).
- Custom SFR registers allows access to the full 32-bit address space of the shared bus, direct control of the MMU, and other features.

- Easy debugging and development of software using an external CPU through dedicated status registers in the VCore-Ie system domain. For more information, Software Debug and Development, page 97.

The UART and three timers have been moved out of the 8051 and into the general VCore-Ie register domain so that they are unaffected by the clock gating of the VCore-Ie CPU. The SFR registers related to timers and UART have been removed from the list of SFR registers. For more information on how to use the VCore-Ie system UART and timers, see UART, page 108 and Timers, page 108.

The following table lists the available VCore-Ie CPU SFR registers and associated register fields. A "-" means that the register field is available for general read and write access, and a 0 or 1 means that the register field is reserved. When writing reserved register fields, these must be set to 0 or 1, as indicated in the table.

Table 74 • **Special Function Registers (SFR)**

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPR(1)	0x80	-	-	-	-	-	-	-	-
SP	0x81	-	-	-	-	-	-	-	-
DPL	0x82	-	-	-	-	-	-	-	-
DPH	0x83	-	-	-	-	-	-	-	-
PCON	0x87	-	-	1	1	GF1	GF0	STOP	IDLE
TCON	0x88	0	0	0	0	IE1	IT1	IE0	IT0
MPAGE(1)	0x92	-	-	-	-	-	-	-	-
PG(1)	0xB0	IFP3	IFP2	IFP1	IFP0	OP3	OP2	OP1	OP0
EPG(1)	0xC0	EIFP3	EIFP2	EIFP1	EIFP0	EOP3	EOP2	EOP1	EOP0
PSW	0xD0	CY	AC	F0	RS1	RS0	0V	F1	P
ACC	0xE0	-	-	-	-	-	-	-	-
B	0xF0	-	-	-	-	-	-	-	-
MMAP(1)	0xF2	ACH	ACL	ADH	ADL	MCH	MCL	MDH	MDL
RA_AD0_RD(1)	0xF6	-	-	-	-	-	-	0	0
RA_AD0_WR(1)	0xF7	-	-	-	-	-	-	0	0
RA_AD1(1)	0xF9	-	-	-	-	-	-	-	-
RA_AD2(1)	0xFA	-	-	-	-	-	-	-	-
RA_AD3(1)	0xFB	-	-	-	-	-	-	-	-
RA_DA0(1)	0xFC	-	-	-	-	-	-	-	-
RA_DA1(1)	0xFD	-	-	-	-	-	-	-	-
RA_DA2(1)	0xFE	-	-	-	-	-	-	-	-
RA_DA3(1)	0xFF	-	-	-	-	-	-	-	-

1. This register is not part of the standard 8051 implementation.

The SFR::GPR register is an 8-bit general-purpose register. The value of this register is available to external CPU through ICPU_CFG::MPU8051_STAT.MPU8051_GPR.

The contents of the SFR::MPAGE register are used for the upper eight address bits during "MOVX A, @Ri" and "MOVX @Ri, A" instructions. For legacy 8051 designs, the MPAGE register replaces the Port-2-Latch. To enable memory access instructions ("MOVX A, @Ri"" and "MOVX @Ri, A"), SFR register 0x8E must be written to 0 ("MOV 0x8E, #0x00").

For more information about the SFR::MMAP register, see Mapping On-chip Memory, page 95.

For more information about the SFR::RA_* registers, see Accessing the VCore-Ie Shared Bus, page 95.

5.4.1 Starting the VCore-Ie CPU

This section provides information about the startup procedures for the VCore-Ie CPU. The procedures apply to both manual and automatic booting.

The following table lists the registers associated with starting up the VCore-Ie CPU.

Table 75 • **VCore-Ie CPU Startup Registers**

Register	Description
RESET	Manual release of VCore-Ie CPU reset
MPU8051_MMAP	Mapping of on-chip memory
MEMACC_CTRL	Starting copy of memory regions
MEMACC	Configuration of on-chip memory address range
MEMACC_SBA	Configuration of SBA start address
GPR	Set of eight general-purpose 32-bit registers

The VCORE_CFG strapping pins determine if the VCore-Ie CPU boots up automatically or if it is kept in reset after startup. For more information, see VCore-Ie Configurations, page 87.

5.4.1.1 Loading On-chip Memory

The basic principle of loading the on-chip memory is the same whether the VCore-Ie CPU is copying from Flash during automatic booting or if an external CPU is manually loading a code-image.

The initial step of loading on-chip memory is to set up a source address in the shared bus domain by writing to MEMACC_SBA.MEMACC_SBA_START. For automatic booting, this is typically address 0x00000000 (the first address in the Flash). When manually loading on-chip memory from an external CPU, a good choice for transferring data is the eight 32-bit general-purpose registers (GPR), starting at address 0x70000000.

The second step is to configure destination-range in the on-chip memory by using MEMACC.MEMACC_START and MEMACC.MEMACC_STOP.

A transfer is started by writing to MEMACC_CTRL.MEMACC_DO. This field is cleared when all (32-bit) words in the range MEMACC_START through MEMACC_STOP are copied. When MEMACC_START is equal to MEMACC_STOP, only one word is copied. Word addresses are incremented for each word that is copied (the registers are not physically changed). This means that the *n*'th word in a given transfer is copied between addresses MEMACC_AHB_START.MEM_ACC_START+*n* and MEMACC.MEMACC_START+*n*.

When loading from Flash, the entire on-chip memory can be filled using one long transfer. When loading from an external CPU using the GPR registers, the external CPU repeat transferring blocks of code until the entire code-image is copied to on-chip memory.

The clock of the VCore-Ie CPU is gated during loading of the on-chip memory, which means that loading of the on-chip memory is instantaneous (from the point of view of the software running on the VCore-Ie CPU).

By setting MEMACC_CTRL.MEMACC_EXAMINE, the direction of the transfer can be changed, which allows an external CPU to examine the contents of the on-chip memory instead of loading it.

Loading of the on-chip memory is not limited to copying code during booting. Whenever code or data must be copied from Flash to on-chip memory, the hardware for loading the on-chip memory can be used. The on-chip memory area can be loaded while the VCore-Ie CPU is operating.

Example: Manually Loading 58 Bytes of Code to On-Chip Memory. This example uses all eight GPR registers for transferring data to on-chip memory. Configure the MEMACC_AHB register to 0x70000000 (the address of the first GPR register). Write the first 32 bytes of code to GRP[0] though GPR[7]. Set the destination range to the first 8 words of on-chip memory by writing 0x001C0000 to the MEMACC register.

Write to MEMACC_CTRL.MEMACC_DO to start the access, make sure that MEMACC_CTRL.MEMACC_EXAMINE is cleared. The MEMACC_DO field is automatically cleared when the transfer is done, when this happens the next 26 bytes can be written to GRP[0] though GPR[6] (only byte addresses 0 and 1 of GPR[6] is used). Update the destination range in on-chip memory by writing 0x00380020 to the MEMACC register. Start the second transfer by writing to MEMACC_CTRL.MEMACC_DO. After this field is cleared, the code is copied. The on-chip memory can then be mapped, and the VCore-Ie CPU can be released from reset.

5.4.1.2 Mapping On-chip Memory

By default, the on-chip memory is transparent to the VCore-Ie CPU. Using the MPU8051_MMAP or the SFR::MMAP registers, the on-chip memory can be mapped into code and data space of the VCore-Ie CPU.

There are two MMAP registers: one that is part of the VCore-Ie registers (MPU8051_MMAP) and one that is a part of the 8051's SFR registers (SFR::MMAP). The mapping of on-chip memory is the result of a bit-wise OR between these two registers. Only one of these registers must be used.

When manually loading a code-image from an external CPU, the MPU8051_MMAP register must be used. When automatically booting up from Flash, use the SFR::MMAP register. The encoding of these two registers are the same, and both registers are commonly referred to as MMAP.

The MPU8051_MMAP register in the VCore-Ie registers can be protected from VCore-Ie soft-reset. When the MPU8051_MMAP register is used, and the VCore-Ie system is protected from reset, the mapping remains active after soft-reset of the VCore-Ie CPU.

The code interface of the 8051 maps to the shared bus by default. Setting MMAP.MAP_CODE_LOW maps access in the low 32 kilobyte region of the code interface to the on-chip memory. Setting MMAP.MAP_CODE_HIGH maps access in the high 32 kilobyte region of the code interface to the on-chip memory.

MMAP.MSADDR_CODE_LOW controls if either the lower or higher half of the on-chip memory is accessed when the low 32 kilobyte region of the code interface maps an access to on-chip memory. MMAP.MSADDR_CODE_HIGH controls if either lower or higher half of the on-chip memory is accessed when the high 32 kilobyte region of the code interface maps an access to the on-chip memory.

The data interface of the 8051 maps to the shared bus by default. Setting MMAP.MAP_DATA_LOW maps access in the low 32 kilobyte region of the data interface to the on-chip memory. Setting MMAP.MAP_DATA_HIGH maps access in the high 32 kilobyte region of the data interface to the on-chip memory.

MMAP.MSADDR_DATA_LOW controls if either the lower or higher half of the on-chip memory is accessed when the low 32 kilobyte region of the data interface maps an access to the on-chip memory.

MMAP.MSADDR_DATA_HIGH controls if either the lower or higher half of the on-chip memory is accessed when the high 32 kilobyte region of the data interface maps an access to the on-chip memory.

Example: Map the Complete On-Chip Memory to Both Code and Data. Some 8051 compilers support using the same physical memory for both code and data. To map the complete 64 kilobyte on-chip memory to both code and data interfaces, set MMAP to 0xAF. Then a code access on address n and a data access on address *n* both maps to an access on address *n* inside the on-chip memory.

Example: Split On-Chip Memory between Code and Data. In some cases, it may be desirable to use non-overlapping memory for code and data. Setting MMAP to 0x15 maps the lower half of the on-chip memory to the code interface and the higher half to the data interface. Code address *n* then maps to address *n* inside the on-chip memory, and data address *n* maps to address *n*+0x8000 inside the on-chip memory.

5.4.2 Accessing the VCore-Ie Shared Bus

Access to the VCore-Ie shared bus is done through registers in the Special Function Registers (SFR) domain of the VCore-Ie CPU.

The following table lists the registers associated with the VCore-Ie shared bus.

Table 76 • **Shared Bus Access (SBA) Registers**

Register	Description
SFR::RA_AD0_RD	SBA address[7:0], and read access initiation
SFR::RA_AD0_WR	SBA address[7:0], and write access initiation
SFR::RA_AD1	SBA address[15:8]
SFR::RA_AD2	SBA address[23:16]
SFR::RA_AD3	SBA address[31:24]
SFR::RA_DA0	SBA data[7:0]
SFR::RA_DA1	SBA data[15:8]
SFR::RA_DA2	SBA data[23:16]
SFR::RA_DA3	SBA data[31:24]

During access to the VCore-Ie shared bus, the clock of the VCore-Ie CPU is gated. This means that from the point of view of the software, access to the shared bus is instantaneous.

Although the shared bus is byte-addressable, the VCore-Ie always does word access (reading or writing 32 bits of data). As a result, the shared bus address must be a word-aligned address, meaning that the two least significant bits of the address must always be 0.

Reading from the VCore-Ie shared bus requires configuration of read-address by writing to RA_AD3, RA_AD2, RA_AD1, followed by write to RA_AD0_RD. The last write initiates the read access. The registers RA_DA3, RA_DA2, RA_DA1, and RA_DA0 are overwritten with the result of the read access.

Note Because shared bus accesses are instantaneous, from software perspective, the data is available to the instruction immediately following the write to RA_AD0_RD.

Writing to the VCore-Ie shared bus requires setting up write-data in RA_DA3, RA_DA2, RA_DA1, and RA_DA0, configuration of write-address by writing to RA_AD3, RA_AD2, RA_AD1, followed by write to RA_AD0_WR. The last write initiates the write access.

The only registers that can be modified by hardware are the RA_DA* registers and these are only changed during read operations.

Example: Copy ICPU_CFG::GPR[1] to ICPU_CFG::GPR[2] with change to 4'th byte. Perform read by setting RA_AD3=0x70, RA_AD2=0x00, RA_AD1=0x00, and RA_AD0_RD=0x04. The RA_DA3, RA_DA2, RA_DA1, and RA_DA0 registers have now been updated with the value of ICPU_CFG::GPR[1]. Modify RA_DA3 (the 4'th byte), and set RA_AD0_WR=0x08 to save to ICPU_CFG::GPR[2].

5.4.3 Paged Access to VCore-Ie Shared Bus

The VCore-Ie CPU supports paged access to the shared bus. Paging extends the address space of the VCore-Ie CPU by 8 bits, thereby increasing the addressable region from 64 kilobytes to 16 megabytes.

The following table lists the registers associated with paged access to the VCore-Ie shared bus.

Table 77 • **Paged Access to VCore-Ie Shared Bus**

Register	Description
SFR::PG	Paging Control
SFR::EPG	Extended Paging Control

The paging mechanism of the VCore-Ie CPU only applies to access to the shared bus; the paging registers (PG and EPG) does not effect code or data access that are mapped to on-chip memory.

The PG register contains two groups: IFP[3:0] and OP[3:0]. The IFP group holds four page bits used for instruction fetches and program memory reads (MOVC instructions). The OP group holds four page bits used for all other types of external memory accesses. The layout of the EPG register is similar to the PG register: EIFP[3:0] and EOP[3:0] hold the four most significant page bits, so that the concatenation of EIFP and IFP provides the eight instruction page bits, and the concatenation of EOP and OP provides the eight other access page bits.

Note The IFP/EIFP and OP/EOP fields are independent, which means that the VCore-Ie CPU can execute code and read data from different pages of the Flash.

The paging function is useful for accessing small seldom used functions or data directly in Flash. However, it is sometimes more sensible to copy code or data from Flash to on-chip memory, by use of the dedicated loader hardware, before accessing it. For more information, seeLoading On-chip Memory, page 94.

5.4.4 Software Debug and Development

This section provides information about methods that use combinations of software and hardware to allow debugging code within VCore-Ie CPU.

The following table lists the registers associated with 8051 status.

Table 78 • **8051 Status Registers**

Register	Description
MPU8051_STAT	Status from the 8051
GENERAL_STAT	Sleep status from the 8051
GPR	Set of 8 general purpose 32-bit registers

The MPU8051_STAT.MPU8051_GPR field is a read-only copy of the 8-bit SFR::GPR register.The MPU8051_STAT.MPU8051_STOP field is set when the 8051 enters stop mode (by setting SFR::PCON.STOP). By using these fields, the 8051 can report up to 256 exit conditions from the 8051 software to the external CPU.

The only way for the VCore-Ie CPU to exit the stop mode is by resetting the VCore-Ie CPU. In a real-life application, the VCore-Ie CPU must not use the stop mode unless it has also enabled the watchdog timer, which would bring the system back online after the unlikely event of an error.

The GENERAL_STAT.CPU_SLEEP field is set when the 8051 enters idle mode after setting SFR::PCON.IDLE. As a result, an external CPU can determine if the 8051 is in IDLE mode by examining the CPU_SLEEP field.

The VCore-Ie registers includes eight 32-bit, general-purpose registers (GPR) that can be used for exchanging information between the 8051 and an external CPU. This can be combined with the software interrupt and semaphore implementation. For more information, see Mailbox and Semaphores, page 107.

The same mechanism that is used for loading code into the on-chip memory can also be used for examining on-chip memory. By setting ICPU_CFG::MEMACC_CTRL.MEMACC_EXAMINE, a portion of the on-chip memory can be extracted and placed in SBA domain for access by an external CPU.

5.5 Manual Frame Injection and Extraction

This section provides information about the manual frame injection and extraction to and from the CPU system. The devices have two injection groups and two extraction groups available.

5.5.1 Manual Frame Extraction

This section provides information about manual frame extraction.

The following table lists the registers associated with manual frame extraction.

Table 79 • **Manual Frame Extraction Registers**

Register	Description	Replication
XTR_FRM_PRUNING	Frame pruning	Per xtr queue
XTR_GRP_CFG	Extraction group configuration	Per xtr group
XTR_MAP	Map extraction queue to group	Per xtr queue
XTR_RD	Extraction read data	Per xtr group
XTR_QU_SEL	Software controlled queue selection	Per xtr group
XTR_QU_FLUSH	Extraction queue flush	None
XTR_DATA_PRESENT	Extraction status	None

The devices have two extraction queues to which data can be redirected. Before data can be extracted each extraction queue must be enabled and mapped to an extraction group. The devices have two extraction groups available, and the mapping between queues and groups can be set arbitrary. A queue is enabled by setting the corresponding XTR_MAP.MAP_ENA field and the mapping to an extraction group is set in XTR_MAP.GRP.

The XTR_DATA_PRESENT register shows if data is present in the extraction queues. It has two fields:

- XTR_DATA_PRESENT.DATA_PRESENT shows the data present status per extraction queue
- XTR_DATA_PRESENT.DATA_PRESENT_GRP shows the data present status per extraction group.

When frame data is available in an extraction group, it can be read from the associated XTR_RD register, which is replicated per extraction group. The XTR_RD register returns the next 4 bytes of the frame data. When the read operation is completed, the register is automatically updated with the next 4 bytes of the frame data. End-of-frame (EOF) and other status indications are indicated by special data words in the data stream (when reading XTR_RD). The following table lists the possible special data words.

Table 80 • **Extraction Data Special Values**

Data Value	Description
0x80000000-0x80000003	EOF. The two LSBs indicate the number of unused bytes.
0x80000004	EOF. Frame was pruned.
0x80000005	EOF. The frame was aborted and is invalid.
0x80000006	Escape. Next data is frame data and not a status word.
0x80000007	Data not ready.

Each read operation on the XTR_RD register must check for the special values listed above and act accordingly. The escape data word (0x80000006) is inserted into the data stream when the frame data matches one of the special data words. When the escape data word is read it means that the next data word to be read is actual frame data and not a status word.

The position of the EOF data word in the data stream can be configured in XTR_GRP_CFG.STATUS_WORD_POS. The possibilities are to have the EOF status word after the last frame data word or to have EOF status word just before the last frame data word. The default is to have the EOF status word after the last frame data word.

The byte order of the XTR_RD register can be configured in XTR_GRP_CFG.BYTE_SWAP. The default is to have the byte order in little-endian. By clearing XTR_GRP_CFG.BYTE_SWAP, the byte order is changed to big-endian (network order). The byte order of the status words listed in Table 80, page 98 is not affected by the value of XTR_GRP_CFG.BYTE_SWAP.

It is possible to configure a prune size for all extracted frames from an extraction queue using XTR_FRM_PRUNING. When pruning is enabled, all frames that are larger than the specified prune size

is pruned to the prune size. When a frame is pruned, the EOF status word is set to 0x80000004. The maximum prune size is 1024 bytes, and the prune size is defined in whole 32-bit words only.

Frames in individual extraction queues can be flushed by setting the corresponding bit in XTR_QU_FLUSH.FLUSH. Flushing is disabled by clearing XTR_QU_FLUSH.FLUSH.

Note Flushing does not affect the queues in the OQS so it may be needed to make the OQS stop sending data to the CPU extraction queues before flushing.

When a frame is extracted, it can be prefixed with an 8-byte CPU extraction header (EH). The option to prefix an EH to the frame data is set in the rewriter. For more information about the extraction header format, see CPU Extraction Header, page 82.

The extraction queue from which the frame originates is available through the CPU_QUEUE field in the CPU extraction header.

The following table shows an example of reading a 65-byte frame, followed by a 64-byte frame. In the example, it is assumed that each frame is prefixed with an EH. Data is read big endian, and the EOF status word is configured to come just before the last frame data word. Undefined bytes cannot be assumed to be zero.

Table 81 • **Frame Extraction Example**

Read Number	INJ_WR Bits 31:24	INJ_WR Bits 23:16	INJ_WR Bits 15:8	INJ_WR Bits 7:0
1	EH bit 63:56	EH bit 55:48	EH bit 47:40	EH bit 39:32
2	EH bit 31:24	EH bit 23:16	EH bit 15:8	EH bit 7:0
3	Frame byte 1 (DMAC)	Frame byte 2 (DMAC)	Frame byte 3 (DMAC)	Frame byte 4 (DMAC)
4	Frame byte 5 (DMAC)	Frame byte 6 (DMAC)	Frame byte 7 (SMAC)	Frame byte 8 (SMAC)
…				
19	0x80 (EOF)	0x00 (EOF)	0x00 (EOF)	0x03 (EOF)
20	Frame byte 65 (FCS)	Undefined	Undefined	Undefined
21	EH bit 63:56	EH bit 55:48	EH bit 47:40	EH bit 39:32
…				
38	0x80 (EOF)	0x00 (EOF)	0x00 (EOF)	0x00 (EOF)
39	Frame byte 61	Frame byte 62	Frame byte 63	Frame byte 64

5.5.2 Manual Frame Injection

This section provides information about manual frame injection on the devices.

The following table lists the register associated with manual frame injection.

Table 82 • **Manual Frame Injection Registers**

Register	Description	Replication
INJ_GRP_CFG	Injection group configuration	Per injection group
INJ_WR	Injection write data	Per injection group
INJ_CTRL	Injection control	Per injection group
INJ_STATUS	Injection status	None
INJ_ERR	Injection errors	Per injection group

The devices have two injection groups available. Frames can be injected from the CPU injection groups using register writes. There are two ways of injecting frames:

- Directly forwarding to a specific port, bypassing the analyzer.
- Normal forwarding of a frame through the analyzer.

To control the injection mode, an 8-byte injection header (IH) must be prefixed to the frame data. For more information about the injection modes and the injection header, see Frame Injection, page 83.

Frame data is injected by doing consecutive writes of 4 bytes to the INJ_WR register, which is replicated per injection group. Endianess of the INJ_WR register is configured in INJ_GRP_CFG.BYTE_SWAP. Start-of-frame (SOF) and end-of-frame (EOF) indications are set in INJ_CTRL. INJ_CTRL must be written prior to INJ_WR. SOF and EOF is indicated in INJ_CTRL.SOF and INJ_CTRL.EOF respectively. In INJ_CTRL.VLD_BYTES the number of valid bytes of the last write to INJ_WR is indicated and VLD_BYTES must be set together with the EOF indication. The frame data must include the 4-byte FCS, but it does not have to be correct, because it is recalculated by the egress port module. While a frame is being injected it can be aborted by setting INJ_CTRL.ABORT. The SOF, EOF, and ABORT fields of INJ_CTRL are automatically cleared by hardware.

Dummy bytes can be injected in front of a frame before the actual frame data (including injection header). The dummy bytes are discarded before the frame data is transmitted by the CPU system. The number of bytes to discard from the frame data is set in INJ_CTRL.GAP_SIZE. The GAP_SIZE field must be set together with SOF.

Before each write to INJ_WR, the status fields INJ_STATUS.WMARK_REACHED and INJ_STATUS.FIFO_RDY must be checked to ensure successful injection. The INJ_ERR register shows if an error occurred during frame injection.

The following table shows an example of injecting a 65-byte frame followed by a 64-byte frame. Both frames are prefixed by a CPU injection header and big-endian mode is used for the INJ_WR register. The “don’t care” bytes can be any value.

Table 83 • **Frame Injection Example**

Register Access	INJ_WR Bits 31:24	INJ_WR Bits 23:16	INJ_WR Bits 15:8	INJ_WR Bits 7:0
INJ_CTRL #1	GAP_SIZE = 0, ABORT = 0, EOF = 0, SOF = 1, VLD_BYTES = 0			
INJ_WR #1	IH bit 63:56	IH bit 55:48	IH bit 47:40	IH bit 39:32
INJ_WR #2	IH bit 31:24	IH bit 23:16	IH bit 15:8	IH bit 7:0
INJ_WR #3	Frame byte 1 (DMAC)	Frame byte 2 (DMAC)	Frame byte 3 (DMAC)	Frame byte 4 (DMAC)
INJ_WR #4	Frame byte 5 (DMAC)	Frame byte 6 (DMAC)	Frame byte 7 (SMAC)	Frame byte 8 (SMAC)
…				
INJ_CTRL #2	GAP_SIZE = 0, ABORT = 0, EOF = 1, SOF = 0, VLD_BYTES = 1			
INJ_WR #19	Frame byte 65 (FCS)	Don’t care	Don’t care	Don’t care
INJ_CTRL #3	GAP_SIZE = 0, ABORT = 0, EOF = 0, SOF = 1, VLD_BYTES = 0			
INJ_WR #20	IH bit 63:56	IH bit 55:48	IH bit 47:40	IH bit 39:32
…				
INJ_CTRL #4	GAP_SIZE = 0, ABORT = 0, EOF = 1, SOF = 0, VLD_BYTES = 0			
INJ_WR #37	Frame byte 61	Frame byte 62	Frame byte 63	Frame byte 64

5.5.3 Frame Interrupts

Software can be interrupted when frame data is available for extraction or when there is room for frames to be injected.

The value of DEVCPU_QS::XTR_DATA_PRESENT.DATA_PRESENT_GRP is provided directly as interrupt inputs to the VCore-Ie system's interrupt controller (the XTR_RDY interrupts), so that software can be interrupted when frame data is available for extraction. Using the interrupt controller, these interrupts can be mapped independently to the VCore-Ie CPU interrupt inputs.

The negated value of DEVCPU_QS::INJ_STATUS.WMARK_REACHED is provided as interrupt inputs to the VCore-Ie system's interrupt controller (the INJ_RDY interrupts), so that software can be interrupted when there is room in the IQS. Using the interrupt controller, these can be mapped independently to the VCore-Ie CPU interrupt inputs.

5.6 External CPU Support

This section describes the handles of the device, which is dedicated to supporting external CPU systems. In addition to the dedicated logic, an external CPU can interact with most of the VCore-Ie system.

An external CPU attaches to the device through the SI or MIIM and has access to register targets in the switch core domain. Through these register targets, indirect access into the VCore-Ie system on the VCore-Ie SBA is possible. For more information, Access to the VCore-Ie Shared Bus, page 106. The external CPU can coexist with the internal VCore-Ie CPU and hardware-semaphores and interrupts are implemented for inter-CPU communication. For more information, see Mailbox and Semaphores, page 107.

5.6.1 Register Access and Multimaster Systems

The access time is the time it takes for a CPU interface to read or write a register inside a register target. The access time depends on the target and the number of CPU interfaces that are attempting to access the target. There are two types of targets:

- Fast Register Targets have dedicated logic for each CPU interface, and the interfaces have guaranteed access to the fast targets; the access time is no more than 35 ns.
- Normal Register Targets are accessible by all CPU interfaces. When different interfaces access the same target, each interface competes for access. When a target is accessed by only one CPU interface, the maximum access time is 1.1 µs. When a target is accessed by more than one CPU interface, the access time is increased to no more than 2.2 µs.

Fast Targets are DEVCPU_QS, DEVCPU_ORG, and the VCore-Ie registers (ICPU_CFG, UART, and so on). All other register targets in the device are considered Normal Targets.

The VCore-Ie registers are placed on the VCore-Ie shared bus and are indirectly accessible to an external CPU through the DEVCPU_GCB register target.

5.6.2 Serial Interface in Slave Mode

This section provides information about the function of the serial interface (SI) in slave mode.

The following table lists the registers associated with SI slave mode.

Table 84 • **SI Slave Mode Register**

Register	Description
SI	Configuration of endianess, bit order, and padding

The serial interface implements a SPI-compatible protocol that allows an external CPU to perform read and write accesses to register targets inside the device. Endianess and bit order is configurable, and several options for high frequencies are supported.

The serial interface is available to an external CPU when the VCore-Ie CPU does not own the SI. For more information, VCore-Ie System and CPU Interface, page 86.

The following table lists the pins of the SI interface.

Table 85 • **SI Slave Mode Pins**

Pin Name	Direction	Description
SI_nEn	I	Active low chip select
SI_Clk	I	Clock input
SI_DI	I	Data input (MOSI)
SI_DO	O	Data output (MISO)

SI_DI is sampled on rising edge of SI_Clk. SI_DO is changed on falling edge of SI_Clk. There are no requirements on the logical values of the SI_Clk and SI_DI inputs when SI_nEn is asserted or deasserted, they can be either 0 or 1. SI_DO is only driven during reading when read-data is shifted out of the device.

The external CPU initiates access by asserting chip select and then transmitting one bit read/write indication, one don't care bit, and 22 address bits. For write access, an additional 32 data bits are transmitted. For read access, the external CPU continues to clock the interface while reading out the result.

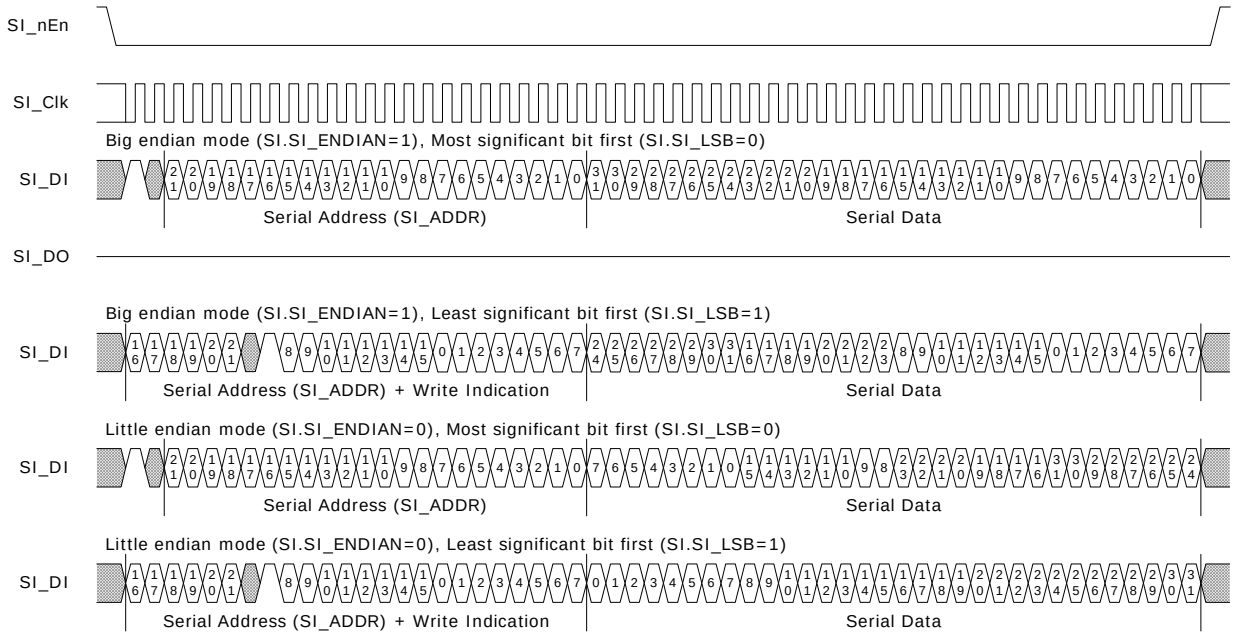
With the register address of a specific register (REG_ADDR), the SI address (SI_ADDR) is calculated:

```
SI_ADDR = (REG_ADDR) – 0×60000000)>>2
```

Data word endianess is configured through SI.SI_ENDIAN. The order of the data bits is configured using SI.SI_LSB. Setting SI.SI_LSB affects both the first 24 bits of the SI command and the 32 bits of data.

The following illustration shows various configurations for write access. The data format during writing, as depicted, is also used when the device is transmitting data during read operations.

Figure 30 • **Write Sequence for SI**



When reading registers using the SI interface, the device needs to prepare read data after receiving the last address bit. The access time of the register that is read must be satisfied before shifting out the first bit of read data. For information about access time, see Register Access and Multimaster Systems, page 101. The external CPU must apply one of the following solutions to satisfy access time:

- Use SI_Clk with a period that is a minimum of twice the access time for the register target. For example, for Normal Targets (single master): 1/(2 × 1.1 µs) = 450 kHz.
- Pause the SI_Clk between shifting of serial address bit 0 and the first data bit with enough time to satisfy the access time for the register target.
- Configure the device to send out enough padding (dummy) bytes before transmitting the read data to satisfy the access time for the register target.

Inserting padding (dummy) bytes is configured in SI.SI_WAIT_STATES. The required number of padding bytes depends on the SI frequency. The SI_DO output is not driven while shifting though padding bytes.

Note When using padding bytes, it is usually cumbersome to change the padding configuration on the fly. Then it makes sense to use enough padding to support the worst case access time.

Example: The required number of padding bytes for 20 MHz SI. The clock period at 20 MHz is 50 ns; it will take 50 ns × 8 = 400 ns to shift through one padding byte. For a single master system, the worst-case access time to any register target is 1.1 µs. To satisfy this delay, SI.SI_WAIT_STATES must be configured to at least three. This means that the external CPU must shift a total of 56 bits when reading from the device (the last 32 bits are the read data).

The following illustrations show the options for serial read access. The illustrations show only one mapping of read data, little endian with most significant bit first. Any of the mappings can be configured and apply to read data in the same way as for write data.

Figure 31 • **Read Sequence for SI_Clk Slow**

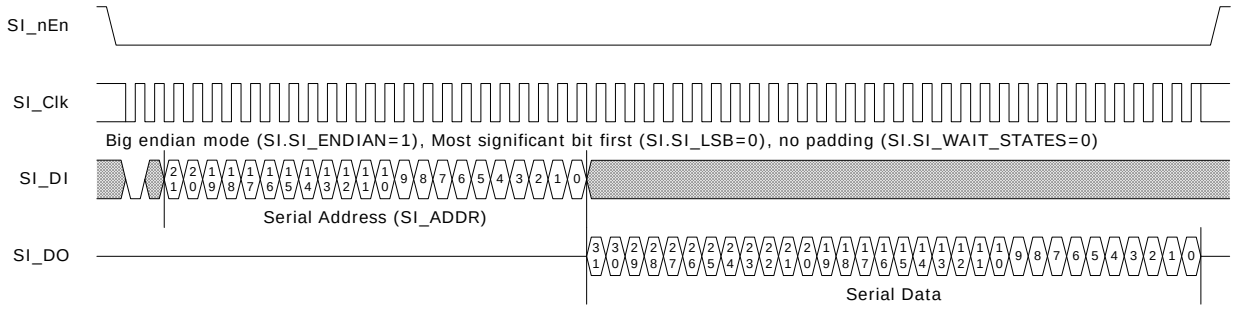


Figure 32 • **Read Sequence for SI_Clk Pause**

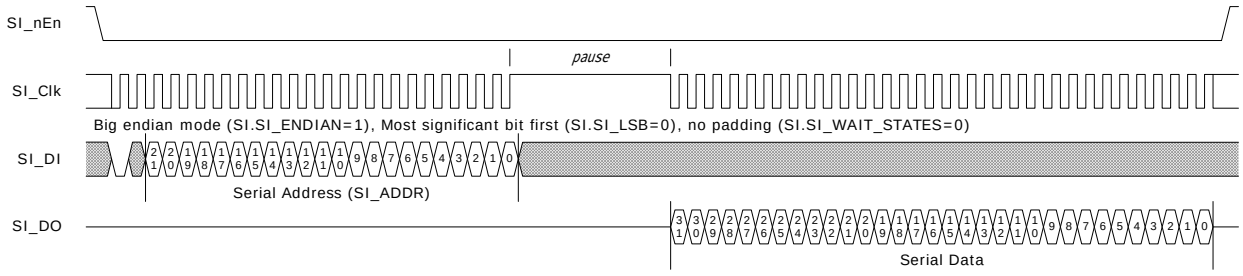
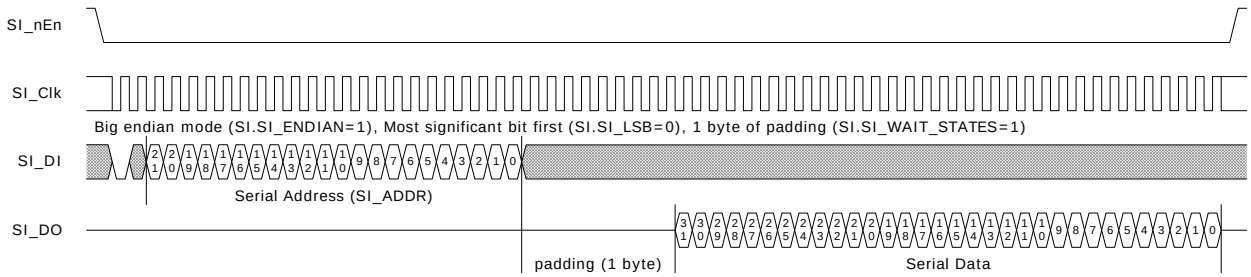


Figure 33 • **Read Sequence for One-Byte Padding**



When using SI, the external CPU must first configure the SI register after power-up, reset, or chip-level soft reset. To configure the device into a known state

1. Write 0 to the SI register.
2. Write the desired configuration using data formatted as little endian with most significant bit first.

5.6.3 MIIM Interface in Slave Mode

This section provides the functional aspects of the MIIM slave interface.

Note: The MIIM slave I/F, due to its low bandwidth, is not aimed at supporting or recommended for managed switch applications.

The MIIM slave interface allows an external CPU to perform read and write access to the register targets inside the device. Register access is done indirectly, because the address and data fields of the MIIM protocol is less than those used by the register targets. Transfers on the MIIM interface are using the Management Frame Format protocol specified in IEEE 802.3, Clause 22.

The MIIM slave pins on the device are overlaid functions on the GPIO interface. MIIM slave mode is enabled by configuring the appropriate VCORE_CFG strapping pins. For more information, see VCore-Ie System and CPU Interface, page 86. When MIIM slave mode is enabled, the appropriate GPIO pins are automatically overtaken. For more information, see Overlaid Functions on the GPIOs, page 115.

The following table lists the pins of the MIIM slave interface.

Table 86 • **MIIM Slave Pins**

Pin Name	I/O	Description
MDC_SLV, GPIO	I	MIIM slave clock input
MDIO_SLV, GPIO	I/O	MIIM slave data input/output

MDIO_SLV is sampled or changed on the rising edge of MDC_SLV by the MIIM slave interface.

The MIIM slave mode uses PHY address 31.

The MIIM slave has seven 16-bit MIIM registers defined as listed in the following table.

Table 87 • **MIIM Registers**

Register Address	Register Name	Description
0	ADDR_REG0	Bit 15:0 of the address to read or write. The address field must be formatted as a word address.
1	ADDR_REG1	Bit 31:16 of the address to read or write.
2	DATA_REG0	Bit 15:0 of the data to read or write. Returns 0x0000 if a register read error occurred.
3	DATA_REG1	Bit 31:16 of the data to read or write. The read or write operation is initiated after this register is read or written. Returns 0x8000 if read while busy or a register read error occurred.
4	DATA_REG1_INCR	Bit 31:16 of data to read or write. The read or write operation is initiated after this register is read or written. When the operation is complete, the address register is incremented by one. Returns 0x8000 if read while busy or if a register read error occurred.

Table 87 • **MIIM Registers *(continued)***

Register Address	Register Name	Description
5	DATA_REG1_INERT	Bit 31:16 of data to read or write. Reading or writing to this register will not cause a register access to be initiated. Returns 0x8000 if a register read error occurred.
6	STAT_REG	The status register gives the status of any ongoing operations. Bit 0: Busy - Is set while a register read/write operation is in progress. Bit 1: Busy_rd - the busy status during the last read or write operation. Bit 2: Err - Is set if a register access error occurred. Others: Reserved.

A 32-bit register read or write transaction over the MIIM interface is done indirectly due to the limited data width of the MIIM frame. First, the address of the register inside the device must be set in the two 16-bit address registers of the MIIM slave using two MIIM write transactions. Afterwards the two 16-bit data registers can be read/written to access the data value of the register inside the device. Thus, it requires up to four MIIM transactions to perform a single read or write operation on a register target.

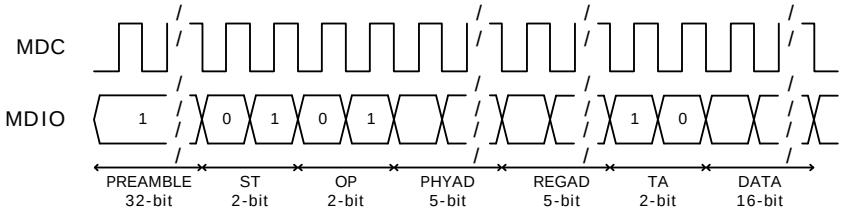
The address of the register to read/write is set in registers ADDR_REG0 and ADDR_REG1. The data to write to the register pointed to by the address in ADDR_REG0 and addr_reg1 is first written to DATA_REG0 and then to DATA_REG1. When the write transaction to DATA_REG1 is completed, the MIIM slave initiates the register transaction.

With the register address of a specific register (REG_ADDR), the MIIM address (MIIM_ADDR) is calculated as:

```
MIIM_ADDR = (REG_ADDR - 0x60000000)>>2
```

The following illustration shows a single MIIM write transaction on the MIIM interface.

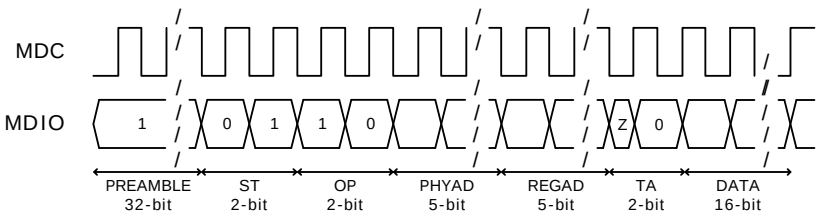
Figure 34 • **MIIM Slave Write Sequence**



A reading transaction is done in a similar way. First, read the DATA_REG0 and then read the DATA_REG1. As with a write operation. The register transaction is not initiated before the DATA_REG1 register is read. In other words, the returned read value is from the previous read transaction.

The following illustration shows a single MIIM read transaction on the MIIM interface.

Figure 35 • **MIIM Slave Read Sequence**



5.6.4 Access to the VCore-Ie Shared Bus

This section provides information about how to access the VCore-Ie shared bus (SBA) from an external CPU. The following table lists the registers associated with the VCore-Ie shared bus access.

Table 88 • **VCore-Ie Shared Bus Access Registers**

Register	Description
VA_CTRL	Status for ongoing accesses
VA_ADDR	Configuration of shared bus address
VA_DATA	Data register
VA_DATA_INCR	Data register, access increments VA_ADDR
VA_DATA_INERT	Data register, access does not start new accesses

An external CPU perform 32-bit reads and writes to the SBA through the VCore Access (VA) registers. In the VCore-Ie system, there is a dedicated master on the shared bus that handles VA accesses. For information about arbitration between masters on the shared bus, see Shared Bus Arbitration, page 89.

The SBA address is configured in VA_ADDR. Accessing the VA_DATA register starts an SBA access. Writing to VA_DATA starts a write with the 32-bit value that was written to VA_DATA. Reading from VA_DATA returns the current value of the register and starts a read access, when the read-access completes the result will automatically be stored in the VA_DATA register.

The VA_DATA_INCR register behaves like VA_DATA, except that after starting an access the VA_ADDR register is incremented by 4 (so that it points to the next word address in the SBA domain). Reading from the VA_DATA_INCR register returns the value of VA_DATA, writing to VA_DATA_INCR overwrites the value of VA_DATA.

Note By using VA_DATA_INCR, sequential addresses can be accessed without having to manually increment the VA_ADDR register between each access.

The VA_DATA_INERT register provides direct access to the VA_DATA value without starting accesses on the SBA. Reading from the VA_DATA_INERT register returns the value of VA_DATA, writing to VA_DATA_INERT overwrites the value of VA_DATA.

The VCore-Ie shared bus is capable of returning error-indication when illegal register regions are accessed. If a VA access result in an error-indication from the SBA, the VA_CTRL.VA_ERR field is set, and the VA_DATA is set to 0x80000000.

Note SBA error indications only occur when non-existing memory regions or illegal registers are accessed. It does not occur during normal operation, so the VA_CTRL.VA_ERR indication is useful during debugging only.

Example: Reading from ICPU_CFG::GRP[1] through the VA registers. The ICPU_GPR register is the second register in the SBA VCore-Ie Registers region. Set VA_ADDR to 0x70000004, read once from VA_DATA (and discard the read-value). Wait until VA_CTRL.VA_BUSY is cleared, then VA_DATA contains the value of the ICPU_CFG::GRP[1] register. Using VA_DATA_INERT (instead of VA_DATA) to read the data is appropriate because this does not start a new SBA access.

5.6.4.1 Optimized Reading

SBA access is typically much faster than the CPU interface, which is used to access the VA registers. The VA_DATA register (VA_DATA_INCR and VA_DATA_INERT) return 0x80000000 while VA_CTRL.VA_BUSY is set. This means that it is possible to skip checking for busy between read access to SBA.

For example, after initiating a read access from SBA, software can proceed directly to reading from VA_DATA, VA_DATA_INCR, or VA_DATA_INERT.

- If the second read is different from 0x80000000; then the second read returned valid read data (the SBA access was done before the second read was performed).

- If the second read is equal to 0x80000000; VA_CTRL must be read.

  If VA_CTRL.VA_BUSY_RD is cleared (and VA_CTRL.VA_ERR_RD is also cleared), then 0x80000000 is the actual read data

  If VA_CTRL.VA_BUSY_RD is set, the SBA access was not yet done at the time of the second read. Start over again by repeating the read from VA_DATA.

Optimized reading can be used for single-read access (reading VA_DATA and then VA_DATA_INERT). For sequential reads (reading VA_DATA_INCR several times), the VA_ADDR is only incremented on successful (non-busy) reads.

5.6.5 Mailbox and Semaphores

This section provides information about the semaphores and mailbox features for CPU to CPU communication. The following table lists the registers associated with mailbox and semaphore.

Table 89 • **Mailbox and Semaphore Registers**

Register	Description
SEMA	Taking of semaphores, replicated per semaphore.
SEMA_FREE	Current status for all semaphores.
SEMA_INTR_ENA	Enable software interrupt on free semaphores.
SEMA_INTR_ENA_CLR	Atomic clear of the SEMA_INTR_ENA register.
SEMA_INTR_ENA_SET	Atomic set of the SEMA_INTR_ENA register.
SW_INTR	Asserting of software interrupts.
MAILBOX	Mailbox.
MAILBOX_CLR	Atomic clear of bits in the mailbox register.
MAILBOX_SET	Atomic set of bits in the mailbox register.

The devices implements eight independent semaphores. The semaphores are controlled through the SEMA register. The SEMA register is replicated once per semaphore; SEMA[0] corresponds to the first semaphore, SEMA[1] the second semaphore, and so on.

Any CPU can attempt to take a semaphore n by reading SEMA[n].SEMA. If the result is 1, the semaphore was successfully taken and is now owned by the CPU. If the result is 0, the semaphore was not free. After a CPU successfully takes a semaphore, all additional reads from the corresponding SEMA register will return 0. To release semaphore *n*, a CPU must write 1 to SEMA[n].SEMA.

Note Any CPU can release semaphores; it does not have to the one that has taken the semaphore, this allows implementation of handshaking protocols.

The current status for all semaphores is available in SEMA_FREE.SEMA_FREE.

A software interrupt can be generated when one or more semaphores are free. Interrupt is enabled in SEMA_INTR_ENA.SEMA_INTR_ENA, atomic set and clear are possible through SEMA_INTR_ENA_CLR and SEMA_INTR_ENA_SET. Semaphores [3:0] can trigger SW0 interrupt when enabled and semaphores [7:4] can trigger SW1 interrupt.

The currently interrupting semaphores are available through SEMA_INTR_ENA.SEMA_INTR_IDENT; this field is the result of a logical AND between SEMA_INTR_ENA.SEMA_INTR_ENA and SEMA_FREE.SEMA_FREE.

In addition to interrupting on free semaphores, a software interrupt can be manually set by writing to SW_INTR.SW0_INTR or SW_INTR.SW1_INTR, these fields are self-clearing.

The mailbox is a 32-bit register that can be set and cleared atomically using any CPU interface (including the VCore-Ie CPU). The MAILBOX register allows reading (and writing) of the current mailbox value.

Atomic clear of specific bits in the mailbox register is done by writing a mask to MAILBOX_CLR. Atomic setting of specific bits in the mailbox register is done by writing a mask to MAILBOX_SET.

5.7 VCore-Ie System Peripherals

This section describes the subblocks of the VCore-Ie system. They are primarily intended to be used by the VCore-Ie CPU. However, an external CPU can access and control these through the shared bus.

5.7.1 Timers

This section provides information about the timers. The following table lists the registers associated with timers.

Table 90 • **Timer Registers**

Register	Description	Replication
TIMER_CTRL	Enable/disable timer	Per timer
TIMER_VALUE	Current timer value	Per timer
TIMER_RELOAD_VALUE	Value to load when wrapping	Per timer
TIMER_TICK_DIV	Common timer-tick divider	None

There are three decrementing 32-bit timers in the VCore-Ie system that run from a common divider. The common divider is driven by a fixed 250 MHz clock and can generate timer ticks in the range of 0.1 µs (10 MHz) to 1 ms (1 kHz), configurable through TIMER_TICK_DIV. The default timer tick is 100 µs (10 kHz).

Note The timers are independent of the VCore-Ie CPU frequency, because the common divider uses a fixed clock.

Software can access each timer value through the TIMER_VALUE registers. These can be read or written at any time, even when the timers are active.

When a timer is enabled through TIMER_CTRL.TIMER_ENA, it decrements from the current value until it reaches zero. An attempt to decrement a TIMER_VALUE of zero generates interrupt and assigns TIMER_VALUE to the contents of TIMER_RELOAD_VALUE. Interrupts generated by the timers are send to the VCore-Ie interrupt controller. From here, interrupts can be forwarded to the VCore-Ie CPU or to an external CPU. For more information, see Interrupt Controller, page 121.

By setting TIMER_CTRL.ONE_SHOT_ENA the timer disables itself after generating one interrupt. When this field is cleared, timers will decrement, interrupt, and reload indefinitely (or until disabled by software, that is, by clearing of TIMER_CTRL.TIMER_ENA).

A timer can be reloaded from TIMER_RELOAD_VALUE at the same time as it is enabled by setting both TIMER_CTRL.FORCE_RELOAD and TIMER_CTRL.TIMER_ENA.

Example: Configure Timer0 So That It Interrupts Every 1 ms. With the default timer tick of 100 µs ten timer ticks are needed for a timer that wraps every 1 ms. Configure TIMER_RELOAD_VALUE[0] to 0x9. Then enable the timer and force a reload by setting TIMER_CTRL[0].TIMER_ENA and TIMER_CTRL[0].FORCE_RELOAD at the same time.

5.7.2 UART

This section provides information about the UART (Universal Asynchronous Receiver/Transmitter) controller.

The following table lists the registers associated with the UART.

Table 91 • **UART Registers**

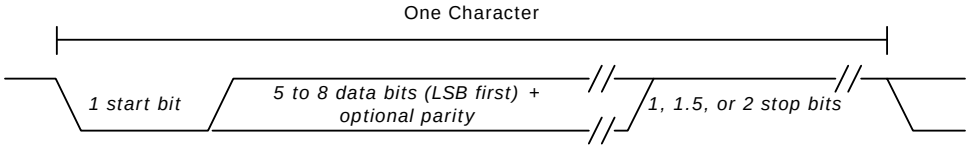
Register	Description
RBR_THR	Receive buffer/transmit buffer/Divisor (low)

Table 91 • **UART Registers *(continued)***

Register	Description
IER	Interrupt enable/Divisor (high)
IIR_FCR	Interrupt identification/FIFO control
LCR	Line control
MCR	Modem control
LSR	Line status
MSR	Modem status
SCR	Scratchpad
USR	UART status

The VCore-Ie system UART is functionally based on the industry-standard 16550 UART (RS232 protocol). This implementation features a 16-byte receive and a 16-byte transmit FIFO.

Figure 36 • **UART Timing**



The number of data-bits, parity, parity-polarity, and stop-bit length are all programmable using LCR.

The UART pins on the devices are overlaid functions on the GPIO interface. Before enabling the UART, the VCore-Ie CPU must enable overlaid modes for the appropriate GPIO pins. For more information, see For more information about enabling the overlaid functionality of the GPIOs, see Overlaid Functions on the GPIOs, page 115.

The following table lists the pins of the UART interface.

Table 92 • **UART Interface Pins**

Pin Name	I/O	Description
UART_RX/ GPIO_31	I	UART receive data
UART_TX/GPIO_30	O	UART transmit data

The baud rate of the UART is derived from the VCore-Ie system frequency. The divider value is indirectly set through the RBR_THR and IER registers. The baud rate is equal to the VCore-Ie system clock frequency divided by sixteen multiplied by the value of the baud rate divisor. A divider of zero disables the baud rate generator and no serial communications occur. The default value for the divisor register is zero.

Example: Configure a baud rate of 9600 in a 125 MHz system. To generate a baud rate of 9600, the divisor register must be set to 0x32E (125 MHz/(16 × 9600 Hz)). Set LCR.DLAB and write 0x2E to RBR_THR and 0x03 to IER (this assumes that the UART is not in use). Finally, clear LCR.DLAB to change the RBR_THR and IER registers back to the normal mode.

By default, the FIFO mode of the UART is disabled. Enabling the 16-byte receive and 16-byte transmit FIFOs (through IIR_FCR) is recommended.

Note Although the UART itself supports RTS and CTS, these signals are not available on the pins of the device.

5.7.2.1 UART Interrupt

The UART can generate interrupt whenever any of the following prioritized events are enabled (through IER):

- Receiver error
- Receiver data available
- Character timeout (in FIFO mode only)
- Transmit FIFO empty or at or below threshold (in programmable THRE interrupt mode)

When an interrupt occurs, the IIR_FCR register can be accessed to determine the source of the interrupt. Note that the IIR_FCR register has different purposes when reading or writing. When reading, the interrupt status is available in bits 0 through 3. For more information about interrupts and how to handle them, see the IIR_FCR register description.

Example: Enable Interrupt When Transmit FIFO is Below One-Quarter Full. To get this type of interrupt, the THRE interrupt must be used. First, configure TX FIFO interrupt level to one-quarter full by setting IIR_FCR.TET to 10; at the same time, ensure that the IIR_FCR.FIFOE field is also set. Set IER.PTIME to enable the THRE interrupt in the UART. In addition, the VCore-Ie interrupt controller must be configured for the CPU to be interrupted. For more information, see Interrupt Controller, page 121.

5.7.3 Two-Wire Serial Interface

This section provides information about the functions of the two-wire serial interface controller.

The following table lists the registers associated with the two-wire serial interface.

Table 93 • **Two-Wire Serial Interface Registers**

Register	Description
CFG	General configuration
TAR	Target address
SAR	Slave address
DATA_CMD	Receive/transmit buffer and command
SS_SCL_HCNT	Standard speed high time clock divider
SS_SCL_LCNT	Standard speed low time clock divider
FS_SCL_HCNT	Fast speed high time clock divider
FS_SCL_LCNT	Fast speed low time clock divider
INTR_STAT	Masked interrupt status
INTR_MASK	Interrupt mask register
RAW_INTR_STAT	Unmasked interrupt status
RX_TL	Receive FIFO threshold for RX_FULL interrupt
TX_TL	Transmit FIFO threshold for TX_EMPTY interrupt
CLR_*	Individual CLR_* registers are used for clearing specific interrupts. See register descriptions for corresponding interrupt.
CTRL	Control register
STAT	Status register
TXFLR	Current transmit FIFO level
RXFLR	Current receive FIFO level
TX_ABRT_SOURCE	Arbitration sources
SDA_SETUP	Data delay clock divider
ACK_GEN_CALL	Acknowledge of general call
ENABLE_STATUS	General two-wire serial controller status
TWI_CONFIG	Configuration of SDA hold-delay

The two-wire serial interface controller is compatible with the industry standard two-wire serial interface protocol. The controller supports standard speed up to 100 kbps and fast speed up to 400 kbps. Multiple bus masters, as well as both 7-bit and 10-bit addressing are also supported.

By default, the two-wire serial interface controller operates as master only (CFG.MASTER_ENA), however, slave mode can be enabled (CFG.SLAVE_DIS). In slave mode, the controller generates an interrupt when addressed by an external master. For read requests, the controller then halts the two-wire serial bus until the VCore-Ie CPU has processed the request and provided a response (reply-data) to the controller. The slave addresses (SAR) of the two-wire serial interface controller must be unique on the two-wire serial interface bus. This must be configured before enabling slave mode. For information about addresses that have a special meaning on the bus, see Two-Wire Serial Interface Addressing, page 111.

The two-wire serial interface pins on the devices are overlaid functions on the GPIO interface. Before enabling the two-wire serial interface, the VCore-Ie CPU must enable overlaid functions for the appropriate GPIO pins. For more information, see Overlaid Functions on the GPIOs, page 115.

The following table lists the pins of the two-wire serial interface.

Table 94 • **Two-Wire Serial Interface Pins**

Pin Name	I/O	Description
TWI_SCL, GPIO	O	Two-wire serial interface clock, open-collector output.
TWI_SDA, GPIO	I/O	Two-wire serial interface data, open-collector output.

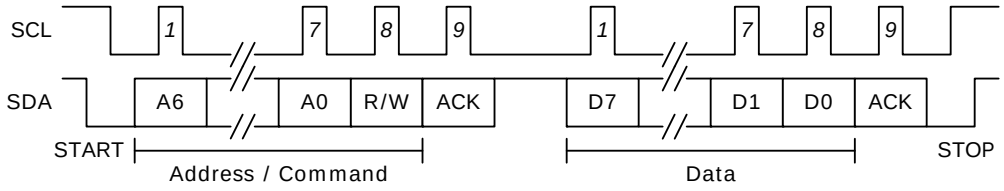
Setting CTRL.ENABLE enables the controller. The controller can be disabled by clearing the CTRL.ENABLE field, there is a chance that disabling is not allowed (at the time when it is attempted); the ENABLE_STATUS register shows if the controller was successful disabled.

Before enabling the controller, the user must decide on either standard or fast mode (CFG.SPEED) and configure clock dividers for generating the correct timing (SS_SCL_HCNT, SS_SCL_LCNT, FS_SCL_HCNT, FS_SCL_LCNT, and SDA_SETUP). The configuration of the divider registers depends on the VCore-Ie system clock frequency. The register descriptions explain how to calculate the required values.

Some two-wire serial devices requires a hold time on SDA after SCK when transmitting from the two-wire serial interface controller. The device supports a configurable hold delay through the TWI_CONFIG register.

The two-wire serial interface controller has an 8-byte combined receive and transmit FIFO.

Figure 37 • **Two-Wire Serial Interface Timing for 7-bit Address Access**



During normal operation of the two-wire serial interface controller, the STATUS register shows the activity and FIFO states.

5.7.3.1 Two-Wire Serial Interface Addressing

Use CFG.MASTER_10BITADDR and CFG.SLAVE_10BITADDR to configure either 7 or 10 bit addressing for master and slave modes respectively.

There are a number of reserved two-wire serial interface addresses. The two-wire serial interface controller does not restrict the use of these. However, if they are used out of context, there may be

compatibility issues with other two-wire serial devices. The following table lists the two-wire serial interface reserved addresses.

Table 95 • **Reserved Two-Wire Serial Interface Addresses**

Register Address	Description
0000 000	General Call address/START Byte If the slave is enabled the two-wire serial interface controller places the data in the receive buffer and issues a general call interrupt. The acknowledge response is configurable (through ACK_GEN_CALL).
0000 001	CBUS address. The two-wire serial interface controller ignores this address.
0000 01X	Reserved, do not use.
0000 1XX	Reserved, do not use.
1111 1XX	Reserved, do not use.
1111 0XX	10-bit addressing indication, 7-bit address devices must not use this.

The two-wire serial interface controller can general both General Call and START Byte. Initiate this through TAR.GC_OR_START_ENA or TAR.GC_OR_START. When operating as master, the target/slave address is configured using the TAR register.

5.7.3.2 Two-Wire Serial Interface Interrupt

The two-wire serial interface controller can generate a multitude of interrupts. All of these are described in the RAW_INTR_STAT register. The RAW_INTR_STAT register contains interrupt fields that are always set when their “trigger” conditions occur. The INTR_MASK register is used for masking interrupts and allowing interrupts to propagate to the INTR_STAT register. When set in the INTR_STAT register, the two-wire serial interface controller asserts interrupt toward the VCore-Ie interrupt controller.

The RAW_INTR_STAT register also specifies what is required to clear the specific interrupts. When the source of the interrupt is removed, reading the appropriate CLR_* register (for example, CLR_RX_OVER) clears the interrupt.

5.7.4 MII Management Controller

This section provides information about the MII Management controllers. The following table lists the registers associated with the MII Management controllers.

Table 96 • **MIIM Registers**

Register	Description
MII_STATUS	General configuration
MII_CMD	Target address
MII_DATA	Slave address
MII_CFG	Receive/transmit buffer and command
MII_SCAN_0	Standard speed high time clock divider
MII_SCAN_1	Standard speed low time clock divider
MII_SCAN_LAST_RSLTS	Fast speed high time clock divider
MII_SCAN_LAST_RSLTS_VLD	Fast speed low time clock divider

The devices contain two MIIM controllers with equal functionality. Controller 0 is connected to the internal PHY, and controller 1 is used to manage external PHYs. Only the interface of controller 1 is available as pins on the device. Data is transferred on the MIIM interface using the Management Frame Format protocol specified in IEEE 802.3, Clause 22 or the MDIO Manageable Device protocol defined in

IEEE 802.3, Clause 45. The clause 45 protocol differs from the clause 22 protocol by using indirect register accesses to increase the address range. The controller supports both Clause 22 and 45.

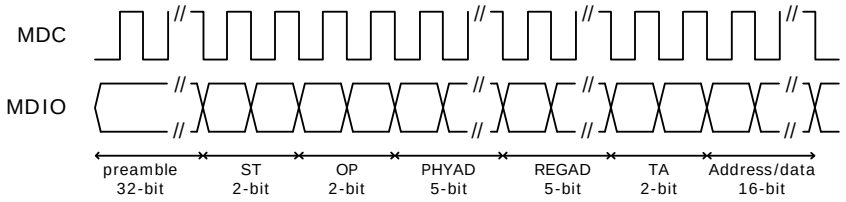
The following table lists the pins of the MIIM interface for controller 1.

Table 97 • **MIIM Management Controller Pins**

Pin Name	I/O	Description
MDC	O	MIIM clock
MDIO	I/O	MIIM data input/output

The MDIO signal is changed or sampled on the falling edge of the MDC clock by the controller. When the controller does not drive the MDIO pin it is tri-stated.

Figure 38 • **MII Management Timing**



5.7.4.1 Clock Configuration

The frequency of the management interface clock generated by the MIIM controller is derived from the VCore-Ie system frequency. The MIIM clock frequency is configurable and is selected with MII_CFG.MIIM_CFG_PRESCALE. The calculation of the resulting frequency is explained in the register description for MII_CFG.MIIM_CFG_PRESCALE. The maximum frequency of the MIIM clock is 25 MHz.

5.7.4.2 MII Management PHY Access

Reads and writes across the MII management interface are performed through the MII_CMD register. Details of the operation, such as the PHY address, the register address of the PHY to be accessed, the operation to perform on the register (for example, read or write), and write data (for write operations) are set in the MII_CMD register. When the appropriate fields of MII_CMD are set, the operation is initiated by writing 0x1 to MII_CMD.MIIM_CMD_VLD. The register is automatically cleared when the MIIM command is initiated. When initiating single MIIM commands, MII_CMD.MIIM_CMD_SCAN must be set to 0x0.

When an operation is initiated, the current status of the operation can be read in MII_STATUS. The fields MII_STATUS.MIIM_STAT_PENDING_RD and MII_STATUS.MIIM_STAT_PENDING_WR can be used to poll for completion of the operation. For a read operation, the read data is available in MII_DATA.MIIM_DATA_RDDATA after completion of the operation. The value of MII_DATA.MIIM_DATA_RDDATA is only valid if MII_DATA.MIIM_DATA_SUCCESS indicates no read errors.

The MIIM controller contains a small command FIFO. Additional MIIM commands can be queued as long as MII_STATUS.MIIM_STAT_OPR_PEND is cleared. Care must be taken with read operations, because multiple queued read operations will overwrite MII_DATA.MIIM_DATA_RDDATA.

Note A typical software implementation will never queue read operations, because the software needs read data before progressing the state of the software. In this case MIIM_STATUS.MIIM_STAT_OPR_PEND is checked before issuing MIIM read or write commands, for read-operations MII_STATUS.MIIM_STAT_BUSY is checked before returning read result.

By default, the MIIM controller operates in clause 22 mode. To access clause 45 compatible PHYs, MII_CFG.MIIM_ST_CFG_FIELD and MII_CMD.MIIM_CMD_OPR_FIELD must be set according to clause 45 mode of operation.

5.7.4.3 PHY Scanning

The MIIM controller can be configured to continuously read certain PHY registers and detect if the read value is different from an expected value. If a difference is detected, a special sticky bit register is set or a CPU interrupt is generated, or both. For example, the controller can be programmed to read the status registers of one or more PHYs and detect whether the Link Status changed since the sticky register was last read.

The reading of the PHYs is performed sequentially with the low and high PHY numbers specified in MII_SCAN_0 as range bounds. The accessed address within each of the PHYs is specified in MII_CMD.MIIM_CMD_REGAD. The scanning begins when a 0x1 is written to MII_CMD.MIIM_CMD_SCAN and a read operation is specified in MII_CMD.MIIM_CMD_OPR_FIELD. Setting MII_CMD.MIIM_CMD_SINGLE_SCAN stops the scanning after all PHYs have been scanned one time. The remaining fields of MII_CMD register is not used when scanning is enabled.

In MII_SCAN_1.MIIM_SCAN_EXPECT the expected value for the PHY register is set. The expected value is compared to the read value after applying the mask set in MII_SCAN_1.MIIM_SCAN_MASK. To “don’t care” a bit-position, write a 0 to the mask. If the expected value for a bit position differs from the read value during scanning, and the mask register has a 1 for the corresponding bit, a mismatch for the PHY is registered.

The scan results from the most recent scan can be read in MII_SCAN_LAST_RSLTS. The register contains one bit for each of the possible 32 PHYs. A mismatch during scanning is indicated by a 0. MII_SCAN_LAST_RSLTS_VLD will indicate for each PHY if the read operation performed during the scan was successful. The sticky-bit register MII_SCAN_RSLTS_STICKY has the mismatch bit set for all PHYs that had a mismatch during scanning since the last read of the sticky-bit register. When the register is read, its value is reset to all-ones (no mismatches).

5.7.4.4 MII Management Interrupt

The MII management controllers can generate interrupts during PHY scanning. Each MII management controller has a separate interrupt signal to the interrupt controller. Interrupt is asserted when one or more PHYs have a mismatch during scan. The interrupt is cleared by reading the MII_SCAN_RSLTS_STICKY register, which resets all MII_SCAN_RSLTS_STICKY indications.

5.7.5 GPIO Controller

This section provides information about the use of GPIO pins.

The following table lists the registers associated with GPIO.

Table 98 • **GPIO Registers**

Register	Description
GPIO_OUT	Value to drive on GPIO outputs
GPIO_OUT_SET	Atomic set of bits in GPIO_OUT
GPIO_OUT_CLR	Atomic clear of bits in GPIO_OUT
GPIO_IN	Current value on the GPIO pins
GPIO_OE	Enable of GPIO output mode (drive GPIOs)
GPIO_ALT	Enable of overlaid GPIO functions
GPIO_INTR	Interrupt on changed GPIO value
GPIO_INTR_ENA	Enable interrupt on changed GPIO value
GPIO_INTR_IDENT	Currently interrupting sources

The GPIO pins are individually programmable. By default, GPIOs are inputs, however, they can be individually changed to outputs through GPIO_OE. For GPIOs that are in input mode, the value of the GPIO pin is reflected in the GPIO_IN register. GPIOs that are in output mode are driven to the value specified in GPIO_OUT.

In a system where multiple different CPU threads (or different CPUs) may work on the GPIOs at the same time, the GPIO_OUT_SET and GPIO_OUT_CLR registers provide a way for each thread to safely control the output value of GPIOs that are under their control, without having to implement locked regions and semaphores.

5.7.5.1 Overlaid Functions on the GPIOs

Most of the GPIO pins have overlaid (alternative) functions that can be enabled through the replicated GPIO_ALT register. For a particular GPIO *n*: Enable overlaid mode 1 by setting GPIO_ALT[0][n] and clearing GPIO_ALT[1][n]. Overlaid mode 2 is enabled by clearing GPIO_ALT[0][n] and setting GPIO_ALT[1][n]. For normal GPIO mode, clear both GPIO_ALT[0][n] and GPIO_ALT[1][n].

The GPIOs that are not included in the following table do not have overlaid functions; the GPIO_ALT bits corresponding to these GPIOs must not be set.

Table 99 • **GPIO Mapping**

GPIO Pin	Overlaid Function 1	Description
GPIO_0 GPIO_1 GPIO_2 GPIO_3	SIO_CLK SIO_LD SIO_DO SIO_DI	Serial GPIO controller connections. See Serial GPIO Controller, page 115.
GPIO_4	TACHO	Fan controller TACHO input. See FAN Controller, page 120.
GPIO_5 GPIO_6 GPIO_7	TWI_SCK TWI_SDA None	Two-wire serial interface connections. See Two-Wire Serial Interface, page 110.
GPIO_8	EXT_IRQ0	External interrupt. See Interrupt Controller, page 121.
GPIO_15 GPIO_16	None	MIIM slave interface connections. GPIO_15 is MDC_SLV, and GPIO_16 is MDIO_SLV. See MIIM Interface in Slave Mode, page 104.
GPIO_29	PWM	Fan controller PWM output. See FAN Controller, page 120.
GPIO_30 GPIO_31	UART_TX UART_RX	UART connections. See UART, page 108.

For example, to enable the UART_RX and UART_TX overlaid functions, set bits 30 (enable UART_TX) and 31 (enable UART_RX) in the GPIO_ALT[0] register. The UART now has control of the GPIO pins.

5.7.5.2 GPIO Interrupt

The GPIO controller continually monitors all inputs and set bits in the GPIO_INTR register whenever a GPIO changes its input value. By enabling specific GPIO pins in the GPIO_INTR_ENA register, a change indication from GPIO_INTR is allowed to propagate (as GPIO interrupt) from the GPIO controller to the VCore-Ie Interrupt Controller.

The currently interrupting sources can be read from GPIO_INTR_IDENT, this register is the result of a binary AND between the GPIO_INTR and GPIO_INTR_ENA registers.

Note When the GPIO_INTR_IDENT register is different from zero, the GPIO controller is indicating an interrupt.

5.7.6 Serial GPIO Controller

The VSC7420-02, VSC7421-02, and VSC7422-02 devices feature a serial GPIO controller (SIO). By using a serial interface, the SIO controller significantly extends the number of available GPIOs with a minimum number of additional pins on the device. The main purpose of the SIO controller is to connect control signals from SFP modules; however, it can also act as an LED controller.

The SIO controller supports up to 128 serial GPIOs (SGPIOs) organized into 32 ports, with four SGPIOs per port. The following table lists the registers associated with the serial GPIO.

Table 100 • **SIO Registers**

Register	Description	Replication
SIO_INPUT_DATA	Input data	SGPIOs per port (4)
SIO_INT_POL	Interrupt polarity	SGPIOs per port (4)
SIO_PORT_INT_ENA	Interrupt enable	None
SIO_PORT_CONFIG	Output port configuration	Per port (32)
SIO_PORT_ENABLE	Port enable	None
SIO_CONFIG	General configuration	None
SIO_CLOCK	Clock configuration	None
SIO_INT_REG	Interrupt register	SGPIOs per port (4)

The following table lists the pins of the SIO controller. The pins of the SIO controller are overlaid on GPIOs. For more information about enabling the overlaid functionality of the GPIOs, see Overlaid Functions on the GPIOs, page 115.

Table 101 • **SIO Controller Pins**

Pin Name	I/O	Description
SIO_CLK/GPIO_0	O	SIO clock output, frequency is configurable using SIO_CLOCK.SIO_CLK_FREQ.
SIO_LD/GPIO_1	O	SIO load data, polarity is configurable using SIO_CONFIG.SIO_LD_POLARITY.
SIO_DO/GPIO_2	O	SIO data output.
SIO_DI/GPIO_3	I	SIO data input.

The SIO controller works by shifting SGPIO values out on SIO_DO though a chain of shift registers on the PCB. After shifting a configurable number of SGPIO bits, the SIO controller asserts SIO_LD, which causes the shift registers to apply the values of the shifted bits to outputs. The SIO controller is also capable of reading inputs, at the same time as shifting out SGPIO values on SIO_DO, it also samples the SIO_DI input. The values sampled on SIO_DI are made available to software.

If the SIO controller is only used for outputs, the use of the load signal is optional. If the load signal is omitted, simpler shift registers (without load) can be used, however, the outputs of these registers will toggle during shifting.

When driving LED outputs, it is acceptable that the outputs will toggle when SGPIO values are updated (shifted through the chain). When the shift frequency is fast, the human eye is not able to see the shifting though the LEDs.

The number of shift registers in the chain is configurable. The SIO controller allows enabling of individual ports through SIO_PORT_ENABLE; only enabled ports are shifted out on SI_DO. Ports that are not enabled are skipped during shifting of GPIO values.

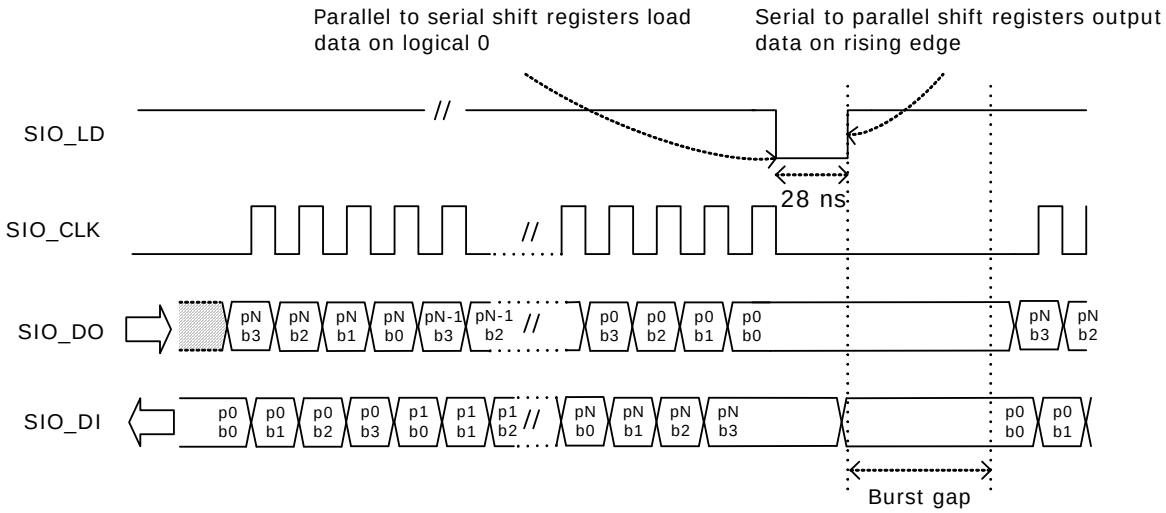
Note SIO_PORT_ENABLE allows skipping of ports in the SGPIO output stream that are not in use. The number of GPIOs per (enabled) port is configurable as well, through SIO_CONFIG.SIO_PORT_WIDTH this can be set to 1,2,3, or 4 bits. The number of bits per port is common for all enabled ports, so the number of shift registers on the PCB must be equal to the number of enabled ports times the number of SGPIOs per port.

Enabling of ports and configuration of SGPIOs per port applies to both output mode and input mode. Unlike a regular GPIO port, a single SGPIO position can be used both as output and input. That is,

software can control the output of the shift register AND read the input value at the same time. Using SGPIOs as inputs requires load-capable shift registers.

Regular shift registers and load-capable shift-registers can be mixed, which is useful when driving LED indications for integrated PHYs at the same time as supporting reading of link status from SFP modules, for example.

Figure 39 • **SIO Timing**



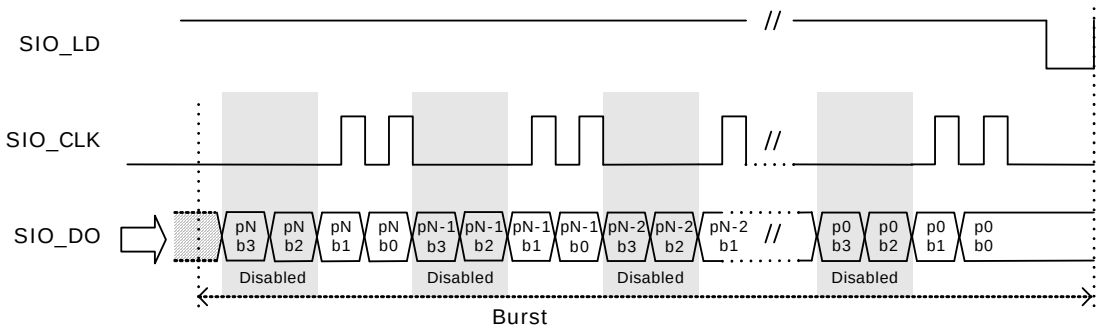
The SGPIO values are output in bursts followed by assertion of the SIO_LD signal. Values can be output as a single burst, or as continuous bursts separated by a configurable burst gap. The maximum length of a burst is 32 × 4 data cycles. The burst gap is configurable in steps of approximately 1 ms between 0 ms and 33 ms through SIO_CONFIG.SIO_BURST_GAP_DIS and SIO_CONFIG.SIO_BURST_GAP.

A single burst is issued by setting SIO_CONFIG.SIO_SINGLE_SHOT. The field is automatically cleared by hardware when the burst is finished. To issue continuous bursts, set SIO_CONFIG.SIO_AUTO_REPEAT. The SIO controller continues to issue bursts until SIO_CONFIG.SIO_AUTO_REPEAT is cleared.

SGPIO output values are configured in SIO_PORT_CONFIG.BIT_SOURCE. The input value is available in SIO_INPUT_DATA.S_IN.

The following illustration shows what happens when the number of SGPIOs per port is configured to 2 (through SIO_CONFIG.SIO_PORT_WIDTH). Disabling of ports (through SIO_PORT_ENABLE) is handled in the same way as disabling the SGPIO ports.

Figure 40 • **SIO Timing with SGPIOs Disabled**



The frequency of the SIO_CLK clock output is configured through SIO_CLOCK.SIO_CLK_FREQ. The SIO_LD output is asserted after each burst, this output is asserted for 28 ns. The polarity of SIO_LD is configurable through SIO_CONFIG.SIO_LD_POLARITY.

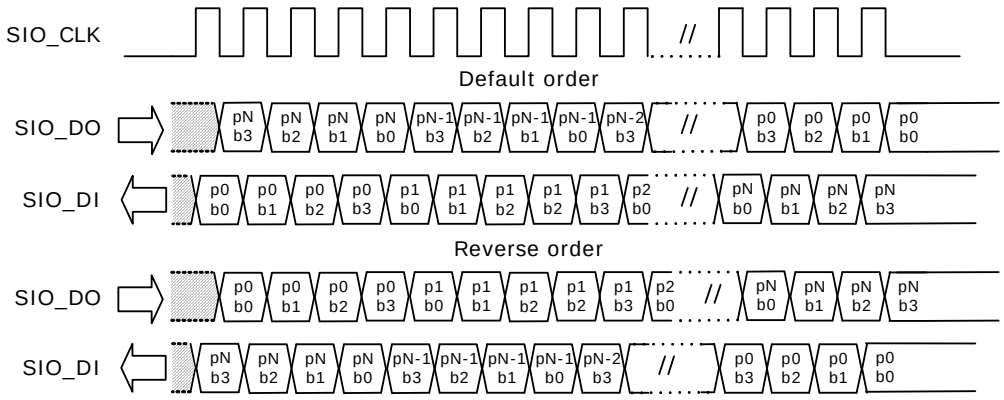
The SIO_LD output can be used to ensure that outputs are stable when serial data is being shifted through the registers. This can be done by using the SIO_LD output to shift the output values into serial-to-parallel registers after the burst is completed. If serial-to-parallel registers are not used, the outputs will toggle while the burst is being shifted through the chain of shift registers. A universal serial-to-parallel shift register outputs the data on a positive-edge load signal, and a universal parallel-to-serial shift register shifts data when the load pin is high, so one common load signal can be used for both input and output serial <-> parallel conversion.

The assertion of SIO_LD happens after the burst to ensure that after power up, the single burst will result in well-defined output registers. Consequently, to sample input values one time, two consecutive bursts must be issued. The first burst results in the input values being sampled by the serial-to-parallel registers, and the second burst shifts the input values into the SIO controller.

The required port order in the serial bitstream depends on the physical layout of the shift register chain. Often the input and output port orders must be opposite in the serial streams. The port order of the input and output bitstream is independently configurable in SIO_CONFIG.SIO_REVERSE_INPUT and SIO_CONFIG.SIO_REVERSE_OUTPUT.

The following illustration shows the port order.

Figure 41 • **SIO Output Order**



5.7.6.1 Output Modes

The output mode of each SGPIO can be individually configured in SIO_PORT_CONFIG.BIT_SOURCE. The SIO controller features three output modes:

- Static
- Blink
- Link activity

Static Mode The static mode is used to assign a fixed value to the SGPIO, for example, fixed 0 or fixed 1.

Blink Mode The blink mode makes the SGPIO blink at a fixed rate. The SIO controller features two blink modes that can be set independently. A SGPIO can then be configured to use either blink mode 0 or blink mode 1. The blink outputs are configured in SIO_CONFIG.SIO_BMODE_0 and SIO_CONFIG.SIO_BMODE_1. To synchronize the blink modes between different devices, reset the blink

counter using SIO_CONFIG.SIO_BLINK_RESET. The “burst toggle” mode of blink mode 1 toggles the output with every burst.

Table 102 • **Blink Modes**

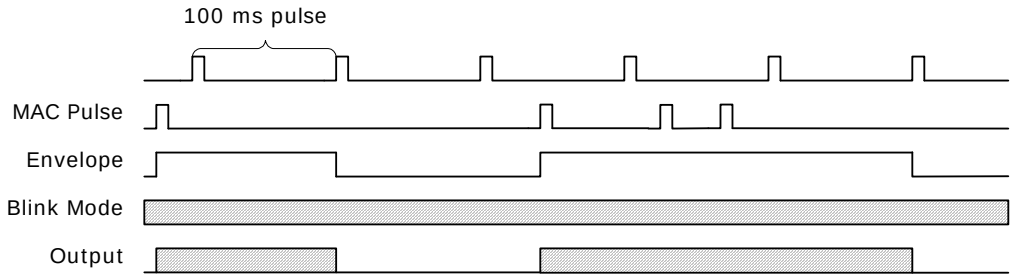
Mode	Description
Blink mode 0	0: 20 Hz blink frequency 1: 10 Hz blink frequency 2: 5 Hz blink frequency 3: 2.5 Hz blink frequency
Blink mode 1	0: 20 Hz blink frequency 1: 10 Hz blink frequency 2: 5 Hz blink frequency 3: Burst toggle

Link Activity Mode The link activity mode makes the output blink when there is activity on the port module (Rx or Tx). The mapping between SIO port number port module number is 1:1, For example, port 0 is connected to port module 0, port 1 is connected to port module 1, and so on.

The link activity mode uses an envelope signal to gate the selected blinking pattern (blink mode 0 or blink mode 1). When the envelope signal is asserted, the output blinks, and when the envelope pattern is de-asserted, the output is turned off. To ensure that even a single packet makes a visual blink, an activity pulse from the port module is extended to minimum 100 ms. If another packet is sent while the envelope signal is asserted, the activity pulse is extended by another 100 ms. The polarity of the link activity modes can be set in SIO_PORT_CONFIG.BIT_SOURCE.

The following illustration shows the link activity timing.

Figure 42 • **Link Activity Timing**



5.7.6.2 SIO Interrupt

The SIO controller can generate interrupts based on the value of the input value of the SGPIOs. All interrupts are level sensitive.

Interrupts are enabled using the two registers. Interrupts can be individually enabled for each port in SIO_PORT_INT_ENA.INT_ENA (32 bits) and in SIO_CONFIG.SIO_INT_ENA (4 bits) interrupts are enabled for the four inputs per port. In other words, SIO_CONFIG.SIO_INT_ENA is common for all 32 ports. The polarity of interrupts is configured for each SGPIO in SIO_INT_POL.

The SIO controller has one interrupt output connected to the main interrupt controller, which is asserted when one or more interrupts are active. To determine which SGPIO is causing the interrupt, the CPU must read the sticky bit interrupt register SIO_INT_REG. The register has one bit per SGPIO and can only be cleared by software. A bit is cleared by writing a 1 to the bit position. The interrupt output remains high until all interrupts in SIO_INT_REG are cleared.

5.7.6.3 Loss of Signal Detection

The SIO controller can propagate loss of signal detection inputs directly to the signal detection input of the port modules. This is useful when, for example, SFP modules are connected to the device. The mapping between SIO ports and port modules is the same as for the link activity inputs; port 0 is connected to port module 0, port1 is connected to port module 1, and so on.

The value of SGPIO bit 0 of each SIO port is forwarded directly to the loss of signal input on the corresponding device. The device must enable the loss of signal input locally in the device.

The polarity of the loss of signal input is configured using SIO_INT_POL, meaning the same polarity must be used for loss of signal detect and interrupt.

5.7.7 FAN Controller

The VSC7420-02, VSC7421-02, and VSC7422-02 devices include a fan controller that can be used to control and monitor a system fan. The fan speed is regulated using a pulse-width-modulation (PWM) output. The fan speed is monitored using a TACHO input. This is especially powerful when combined with the internal temperature sensor (in the PHY).

The following table lists the registers associated with the fan controller.

Table 103 • **Fan Controller Registers**

Register	Description
FAN_CFG	General configuration
FAN_CNT	Fan revolutions counter

The following table lists the pins of the fan controller. The pins of the fan controller are overlaid on GPIOs. For more information about enabling the overlaid functionality of GPIOs, see Overlaid Functions on the GPIOs, page 115.

Table 104 • **Fan Controller Pins**

Pin Name	I/O	Description
TACHO/GPIO_4	I	TACHO input for counting revolutions.
PWM/GPIO_29	O	PWM fan output.

The PWM output can be configured to any of the following frequencies in FAN_CFG.PWM_FREQ:

- 10 Hz
- 20 Hz
- 40 Hz
- 60 Hz
- 80 Hz
- 100 Hz
- 120 Hz
- 25 kHz

The low frequencies can be used for driving three-wire fans using a FET/transistor. The 25 kHz frequency can be used for four-wire fans that use the PWM input internally to control the fan. The duty cycle of the PWM output is programmable from 0% to 100%, with 8-bit accuracy. The polarity of the output can be controlled by FAN_CFG.INV_POL, so a duty-cycle of 100%, for example, can be either always low or always high.

The PWM output pin can be configured to act as a normal output or as an open-collector output, where the output value of the pin is kept low, but the output enable is toggled. The open-collector output mode is enabled by setting FAN_CFG.PWM_OPEN_COL_ENA.

Note By using open-collector mode, it is possible to do external pull-up to higher voltage than the maximum GPIO I/O supply. The GPIOs are 5V-tolerable.

The speed of the fan can be measured using a 16-bit wrapping counter that counts the rising edges on the TACHO-input. A fan usually gives 1-4 pulses per revolution depending on the fan type. Optionally, the TACHO-input can be gated by the polarity-corrected PWM output by setting FAN_CFG.GATE_ENA, so that only TACHO pulses received while the polarity corrected PWM output is high are counted. Glitches on the TACHO-input can occur right after the PWM output goes high, therefore the gate signal is delayed

by 10 µs when PWM goes high. There is no delay when PWM goes low, and the length of the delay is not configurable. Software reads the counter value in FAN_CNT and calculates the RPM of the fan.

The following is an example of how to calculate the RPM of the fan: If the fan controller is configured to 100 Hz and a 20% duty cycle, each PWM pulse is high in 2 ms and low in 8 ms. If gating is enabled the gating of the TACHO-input is “open” in 1.99 ms and “closed” in 8.01 ms. If the fan is turning with 100 RPM and gives two TACHO pulses per revolution, it will ideally give 200 pulses per minute. TACHO pulses are only counted in 19.99% of the time, so it will give 200× 0.1999 = 39.98 pulses per minute. If the additional 10 µs gating time is ignored, the counter value is multiplied by 5/2 to get the RPM value, because there is a 20% duty cycle with two TACHO pulses per revolution. By multiplying with 5/2, the RPM value is calculated to 99.95, which is 0.05% off the correct value (due to the 10 µs gating time).

5.7.8 Interrupt Controller

This section provides information about the VCore-Ie interrupt controller.

The following table lists the registers associated with the interrupt controller.

Table 105 • **Interrupt Controller Registers**

Register	Description
Configuration and status for interrupts	
ICPU_IRQ0_ENA	Global enable of ICPU_IRQ0 interrupt
ICPU_IRQ0_IDENT	Currently interrupting ICPU_IRQ0 sources
ICPU_IRQ1_ENA	Global enable of ICPU_IRQ1 interrupt
ICPU_IRQ1_IDENT	Currently interrupting ICPU_IRQ1 sources
EXT_IRQ0_ENA	Global enable of EXT_IRQ0 interrupt
EXT_IRQ0_IDENT	Currently interrupting EXT_IRQ0 sources
Configuration of individual interrupt sources	
EXT_IRQ0_INTR_CFG	EXT_IRQ0 source configuration
SW0_INTR_CFG	SW0 source configuration
SW1_INTR_CFG	SW1 source configuration
UART_INTR_CFG	UART source configuration
TIMER0_INTR_CFG	TIMER0 source configuration
TIMER1_INTR_CFG	TIMER1 source configuration
TIMER2_INTR_CFG	TIMER2 source configuration
TWI_INTR_CFG	TWI source configuration
GPIO_INTR_CFG	GPIO source configuration
SGPIO_INTR_CFG	SGPIO source configuration
DEV_ALL_INTR_CFG	DEV_ALL source configuration
XTR_RDY0_INTR_CFG	XTR_RDY0 source configuration
XTR_RDY1_INTR_CFG	XTR_RDY1 source configuration
INJ_RDY0_INTR_CFG	INJ_RDY0 source configuration
INJ_RDY1_INTR_CFG	INJ_RDY1 source configuration
MIIM0_INTR_CFG	MIIM0 source configuration
MIIM1_INTR_CFG	MIIM1 source configuration
General enable/disable and status for all interrupt sources	
INTR	Interrupt sticky bits

Table 105 • **Interrupt Controller Registers *(continued)***

Register	Description
INTR_ENA	Interrupt enable
INTR_ENA_SET	Atomic set of bits in INTR_ENA
INTR_ENA_CLR	Atomic clear of bits in INTR_ENA
INTR_RAW	Raw value of interrupt from sources
DEV_IDENT	Currently interrupting DEV_ALL sources

Possible sources of the DEV_ALL interrupt are:

- Fast link status from the PHYs for port 0 through 11 (DEV_IDENT[11:0])
- PCS link status from the PCS for port 12 through 25 (DEV_IDENT[25:12])
- PCS link status from the PCS for port 10 (DEV_IDENT[26])
- PCS link status from the PCS for port 11 (DEV_IDENT[27])
- Global PHY interrupt (DEV_IDENT[28])

Each of the interrupt sources in the VCore-Ie system can be individually assigned to one of three possible interrupt outputs: Two ICPU_IRQ interrupt outputs go directly to the VCore-Ie CPU, and one EXT_IRQ interrupt allows interrupting external devices.

Each interrupt output has a global enable register, ICPU_IRQ0_ENA, ICPU_IRQ1_ENA, and EXT_IRQ0_ENA. This register must be set in order for the interrupt outputs to propagate interrupts. When there is an active interrupt on any interrupt output, the ICPU_IRQ0_IDENT, ICPU_IRQ1_IDENT, and EXT_IRQ0_IDENT registers show the active interrupt sources for each individual interrupt.

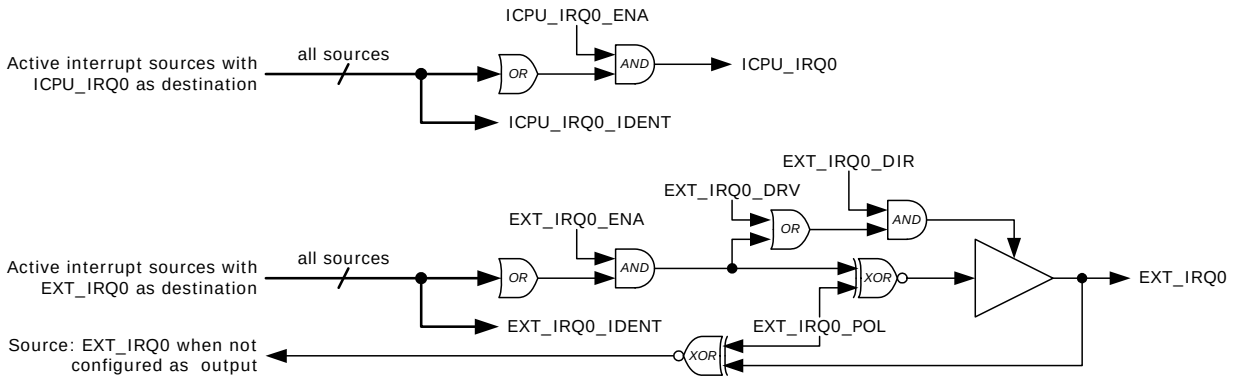
The EXT_IRQ0 pin is special, because it is an overlaid function on the GPIO interface. The active level of the EXT_IRQ0 pin is configured individually through the INTR_POL field of EXT_IRQ0_INTR_CFG. Additionally, the EXT_IRQ0 pin operates as an either interrupt output or as an interrupt source. This is individually configured through the INTR_DIR field of EXT_IRQ0_INTR_CFG. When operating as an output, the EXT_IRQ0 pin can be tri-stated when there is no interrupt. This is configured through the field INTR_DRV in EXT_IRQ0_INTR_CFG field.

For more information about the location on the GPIOs and how to enable the overlaid function, see GPIO Controller, page 114.

When an interrupt output is configured to drive only during interrupt, interrupt outputs from multiple devices can be connected in parallel with a pull-resistor to make wired-or/and interrupts. EXT_IRQ0_INTR_CFG must be configured before enabling the overlaid GPIO function.

The following illustration depicts ICPU_IRQ0 and EXT_IRQ0.

Figure 43 • **Logical Equivalent for Interrupt Outputs**



Note Internally in the device, all interrupt sources are active high.

Each interrupt source has its own configuration register (*_INTR_CFG). The sticky functionality can be bypassed by means of the INTR_BYPASS field. For software development, an interrupt event can be emulated by setting the one-shot INTR_FORCE field. The destination interrupt output is configured through the INTR_SEL field. Interrupt outputs can have many sources, but each source can only have one destination.

The bypass feature can be useful when only a single, or just a few, interrupt source is enabled for a specific interrupt output. When stickiness in the interrupt controller is bypassed, clearing the interrupt indication at its source also clears the associated interrupt.

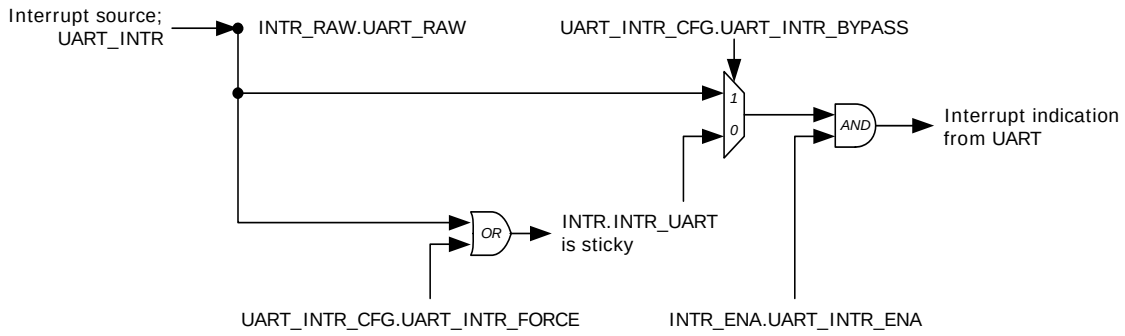
If an interrupt source indicates an interrupt, the associated field in the INTR register is set, this is a sticky indication. The current interrupt inputs from the sources are available through INTR_RAW.

For an interrupt to propagate to its destination, it must be enabled by setting the associated INTR_ENA field. In a system where multiple different CPU threads (or different CPUs) may work on the interrupts at the same time, the INTR_ENA_SET and INTR_ENA_CLR registers provide a method for each thread to safely control enabling and disabling of the interrupts that are under their control, without having to implement locked regions and semaphores.

The following illustration shows an example of the UART interrupt; however, it is representative to any other interrupt by substituting UART for the interrupt name.

The timer interrupt sources are only asserted for a single clock cycle (when the timer wraps). As a result, the trigger and bypass functions (as depicted) are not needed (nor implemented) for the timer interrupt sources.

Figure 44 • **Logical Equivalent for Interrupt Sources**



6 Features

This section provides information about specific features supported by individual blocks in the VSC7420-02, VSC7421-02, and VSC7422-02 devices and describes how these features are administrated by configurations across the entire device. Examples of various standard features are described such as the support for different spanning tree versions and VLAN operations, and more advanced features, such as QoS.

6.1 Port Mapping

This section provides information about the mapping from switch core port modules to SerDes type to physical interface pins on the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

When accessing port module registers (PORT::), port masks in the analyzer, or in general, whenever a switch core register refers to a port, the internal switch port module number must be used.

6.1.1 VSC7420-02 Port Mapping

The internal port modules in the switch core maps to external pins on the VSC7420-02 device according to the following table.

Table 106 • **VSC7420-02: Mapping from Port Modules to Physical Interface Pins**

Port Number	Switch Port Module	Interface Type	SerDes Type	Interface Pins
0 – 7	0 – 7	Internal PHY		P*x*_D[3:0]N, P*x*_D[3:0]P, where *x* is 0 through 7
8	24	2.5G SGMII	SERDES6G	SerDes_E1_TxP, SerDes_E1_TxN, SerDes_E1_RxP, SerDes_E1_RxN
9	25	2.5G SGMII	SERDES6G	SerDes_E0_TxP, SerDes_E0_TxN, SerDes_E0_RxP, SerDes_E0_RxN
	26	CPU port		

6.1.2 VSC7421-02 Port Mapping

The VSC7421-02 device has the option to run in one of two switch modes controlling the type and number of external Ethernet interfaces:

- Switch mode 0 enables 12× CuPHY + 1× QSGMI + 1× 2.5G SGMII
- Switch mode 1 enables 12× CuPHY + 2× 1G SGMII + 2× 2.5G SGMII

The switch mode is controlled through DEVCPU_GCB::MISC_CFG.SW_MODE.

The internal port modules in the switch core maps to the external pins on the VSC7421-02 device as shown in the following tables.

Table 107 • **VSC7421-02 in Switch Mode 0: Mapping from Port Modules to Physical Interface Pins**

Port Number	Switch Port Module	Interface Type	SerDes Type	Interface Pins
0 – 11	0 – 11	Internal PHY		P*x*_D[3:0]N, P*x*_D[3:0]P, where *x* is 0 through 11
12 – 15	12 – 15	QSGMII	SERDES6G	SerDes_E3_TxP, SerDes_E3_TxN, SerDes_E3_RxP, SerDes_E3_RxN
16	25	2.5G SGMII	SERDES6G	SerDes_E0_TxP, SerDes_E0_TxN, SerDes_E0_RxP, SerDes_E0_RxN

Table 107 • **VSC7421-02 in Switch Mode 0: Mapping from Port Modules to Physical Interface Pins**

Port Number	Switch Port Module	Interface Type	SerDes Type	Interface Pins
	26	CPU port		

Table 108 • **VSC7421-02 in Switch Mode 1: Mapping from Port Modules to Physical Interface Pins**

Port Number	Switch Port Module	Interface Type	SerDes Type	Interface Pins
0 – 11	0 – 11	Internal PHY		P*x*_D[3:0]N, P*x*_D[3:0]P, where *x* is 0 through 11
12	16	1G SGMII	SERDES6G	SerDes_E3_TxP, SerDes_E3_TxN, SerDes_E3_RxP, SerDes_E3_RxN
13	19	1G SGMII	SERDES6G	SerDes_E2_TxP, SerDes_E1_TxN, SerDes_E2_RxP, SerDes_E1_RxN
14	24	2.5G SGMII	SERDES6G	SerDes_E1_TxP, SerDes_E1_TxN, SerDes_E1_RxP, SerDes_E1_RxN
15	25	2.5G SGMII	SERDES6G	SerDes_E0_TxP, SerDes_E0_TxN, SerDes_E0_RxP, SerDes_E0_RxN
	26	CPU port		

6.1.3 VSC7422-02 Port Mapping

The internal port modules in the switch core maps to external pins on the VSC7422-02 device as shown in the following table.

Table 109 • **VSC7422-02: Mapping from Port Modules to Physical Interface Pins**

Port Number	Switch Port Module	Interface Type	SerDes Type	Interface Pins
0 – 11	0 – 11	Internal PHY		P*x*_D[3:0]N, P*x*_D[3:0]P, where *x* is 0 through 11
12 – 15	12 – 15	QSGMII	SERDES6G	SerDes_E3_TxP, SerDes_E3_TxN, SerDes_E3_RxP, SerDes_E3_RxN
16 – 19	16 – 19	QSGMII	SERDES6G	SerDes_E2_TxP, SerDes_E2_TxN, SerDes_E2_RxP, SerDes_E2_RxN
20-23	20-23	QSGMII	SERDES6G	SerDes_E1_TxP, SerDes_E1_TxN, SerDes_E1_RxP, SerDes_E1_RxN
24	25	2.5G SGMII	SERDES6G	SerDes_E0_TxP, SerDes_E0_TxN, SerDes_E0_RxP, SerDes_E0_RxN
	26	CPU port		

6.2 Switch Control

This section provides information about the minimum requirements for switch operation.

6.2.1 Switch Initialization

The following initialization sequence is required to ensure proper operation of the switch:

1. Configure the desired switch mode in DEVCPU_GCB::MISC_CFG.SW_MODE.
2. Initialize memories:
   SYS.RESET_CFG.MEM_ENA = 1.
   SYS.RESET_CFG.MEM_INIT = 1.
3. Wait 100 µs for memories to initialize (SYS.RESET_CFG.MEM_INIT cleared).
4. Enable the switch core:
   SYS.RESET_CFG.CORE_ENA = 1.
5. Release reset of the internal PHYs:
   DEVCPU_GCB.SOFT_CHIP_RST.SOFT_PHY_RST = 0.
6. Enable each port module through SYS.PORT.SWITCH_PORT_MODE.PORT_ENA = 1.

6.3 Port Module Control

This section provides information about the features and configurations for port control, port reset procedures, and port counters.

6.3.1 MAC Configuration Port Mode Control

All port modules can be configured independently to the speed and duplex modes listed in the following tables.

Table 110 • **MAC Configuration of Port Modes for Ports with Internal PHYs**

Configuration	10 Mbps, Half Duplex	10 Mbps, Full Duplex	100 Mbps, Half Duplex	100 Mbps, Full Duplex	1 Gbps, Full Duplex
PORT::CLOCK_CFG.LINK_SPEED					
PORT::MAC_MODE_CFG.FDX_ENA	0	1	0	1	1
PORT::MAC_MODE_CFG.GIGA_MODE_ENA	0	0	0	0	1
SYS:PORT:FRONT_PORT_MODE.HDX_MODE	1	0	1	0	0
PORT::MAC_IFG_CFG.TX_IFG	17	17	17	17	5
PORT::MAC_IFG_CFG.RX_IFG1	11		11		
PORT::MAC_IFG_CFG.RX_IFG2	9		9		
PORT::MAC_HDX_CFG.LATE_COL_POS	64		64		
SYS:PORT:FRONT_PORT_MODE.HDX_MODE	1	0	1	0	0

Table 111 • **MAC Configuration of Port Modes for Ports with SerDes**

Configuration	10 Mbps, Half Duplex	10 Mbps, Full Duplex	100 Mbps, Half Duplex	100 Mbps, Full Duplex	1 Gbps, Full Duplex	2.5 Gbps, Full Duplex
PORT::CLOCK_CFG.LINK_SPEED	3	3	2	2	1	1
PORT::MAC_MODE_CFG.FDX_ENA	0	1	0	1	1	1
PORT::MAC_MODE_CFG.GIGA_MODE_ENA	0	0	0	0	1	1
SYS:FRONT_PORT_MODE.HDX_MODE	1	0	1	0	0	0
PORT::MAC_IFG_CFG.TX_IFG	15	15	15	15	5	5
PORT::MAC_IFG_CFG.RX_IFG1	11		7			

Table 111 • **MAC Configuration of Port Modes for Ports with SerDes *(continued)***

Configuration	10 Mbps, Half Duplex	10 Mbps, Full Duplex	100 Mbps, Half Duplex	100 Mbps, Full Duplex	1 Gbps, Full Duplex	2.5 Gbps, Full Duplex
PORT::MAC_IFG_CFG.RX_IFG2	9		9			
PORT::MAC_HDX_CFG.LATE_COL_POS	67		67			
SYS::FRONT_PORT_MODE.HDX_MODE	1	0	1	0	0	0

6.3.2 SerDes Configuration Port Mode Control

The SerDes ports are configured according to the following table.

Table 112 • **SERDES6G Configuration**

Configuration	SGMII Mode	2.5G Mode	QSGMII Mode
hsio::serdes6g_pll_cfg.pll_rot_frq	0	1	0
hsio::serdes6g_pll_cfg.pll_rot_dir	1	0	0
hsio::serdes6g_pll_cfg.pll_ena_rot	0	1	0
hsio::serdes6g_common_cfg.ena_lane	1	1	1
hsio::serdes6g_common_cfg.if_mode	1	1	3
hsio::serdes6g_common_cfg.qrate	1	0	0
hsio::serdes6g_common_cfg.hrate	0	1	0
hsio::serdes6g_ib_cfg1.ib_reserved	1	1	1

6.3.3 Port Reset Procedure

When changing a switch port's mode of operation or restarting a switch port, the following port reset procedure must be followed:

1. Disable the MAC frame reception in the switch port:
   PORT::MAC_ENA_CFG.RX_ENA = 0.
2. Disable traffic being sent to or from the switch port:
   SYS:PORT:SWITCH_PORT_MODE_ENA = 0
   SYS:PORT:FRONT_PORT_MODE_HDX_MODE = 0.
3. Disable shaping to speed up flushing of frames
   SYS:SCH_SHAPING_CTRL.PORT_SHAPING_ENA = 0,
   SYS:SCH_SHAPING_CTRL.PRIO_SHAPING_ENA = 0.
4. Flush the queues associated with the port:
   REW:PORT:PORT_CFG.FLUSH_ENA = 1.
5. Wait at least the time it takes to receive a frame of maximum length on the port Worst-case delays for 10 kilobyte jumbo frames are:
   8 ms on a 10M port
   800 µs on a 100M port
   80 µs on a 1G port, 32 µs on a 2.5G port.
6. Reset the switch port by setting the following reset bits in CLOCK_CFG:
   PORT::CLOCK_CFG.MAC_TX_RST = 1,
   PORT::CLOCK_CFG.MAC_RX_RST = 1,
   PORT::CLOCK_CFG.PORT_RST = 1,
   PORT::CLOCK_CFG.PHY_RST = 1 (if port is connected to an internal PHY).
7. Wait until flushing is complete:
   SYS:PORT:SW_STATUS.EQ_AVAIL must return 0.

8. Clear flushing again:
   REW:PORT:PORT_CFG.FLUSH_ENA = 0.
9. Re-enable traffic being sent to or from the switch port:
   SYS:PORT:SWITCH_PORT_MODE.PORT_ENA = 1.
10. Set up the switch port to the new mode of operation. Keep the reset bits in CLOCK_CFG set. For more information about port mode configurations, see Table 110, page 126 or Table 111, page 126.
11. Release the switch port from reset by clearing the reset bits in CLOCK_CFG.

It is not necessary to reset the SerDes macros.

6.3.4 Port Counters

The statistics collected in each port module provide monitoring of various events. This section describes how industry-standard Management Information Bases (MIBs) can be implemented using the counter set in this device. The following MIBs are considered:

- RMON statistics group (RFC 2819)
- IEEE 802.3-2005 Annex 30A counters
- SNMP interfaces group (RFC 2863)
- SNMP Ethernet-like group (RFC 3536)

6.3.4.1 RMON Statistics Group (RFC 2819)

The following table provides the mapping of RMON counters to port counters.

Table 113 • **Mapping of RMON Counters to Port Counters**

RMON Counter	Rx/Tx	Switch Core Implementation
EtherStatsDropEvents	Rx	C_RX_CAT_DROP + C_DR_TAIL + sum of C_DR_GREEN_PRIO_x, where x is 0 through 7.
EtherStatsOctets	Rx	C_RX_OCT
EtherStatsPkts	Rx	C_RX_SHORT + C_RX_FRAG + C_RX_JABBER + C_RX_LONG + C_RX_SZ_64 + C_RX_SZ_65_127 + C_RX_SZ_128_255 + C_RX_SZ_256_511 + C_RX_SZ_512_1023 + C_RX_SZ_1024_1526 + C_RX_SZ_JUMBO
EtherStatsBroadcastPkts	Rx	C_RX_BC
EtherStatsMulticastPkts	Rx	C_RX_MC
EtherStatsCRCAlignErrors	Rx	C_RX_CRC
EtherStatsUndersizePkts	Rx	C_RX_SHORT
EtherStatsOversizePkts	Rx	C_RX_LONG
EtherStatsFragments	Rx	C_RX_FRAG
EtherStatsJabbers	Rx	C_RX_JABBER
EtherStatsPkts64Octets	Rx	C_RX_SZ_64
EtherStatsPkts65to127Octets	Rx	C_RX_SZ_65_127
EtherStatsPkts128to255Octets	Rx	C_RX_SZ_128_255
EtherStatsPkts256to511Octets	Rx	C_RX_SZ_256_511
EtherStatsPkts512to1023Octets	Rx	C_RX_SZ_512_1023
EtherStatsPkts1024to1518Octets	Rx	C_RX_SZ_1024_1526
EtherStatsDropEvents	Tx	C_TX_DROP + C_TX_AGE
EtherStatsOctets	Tx	C_TX_OCT

Table 113 • **Mapping of RMON Counters to Port Counters *(continued)***

RMON Counter	Rx/Tx	Switch Core Implementation
EtherStatsPkts	Tx	C_TX_SZ_64 + C_TX_SZ_65_127 + C_TX_SZ_128_255 + C_TX_SZ_256_511 + C_TX_SZ_512_1023 + C_TX_SZ_1024_1526 + C_TX_SZ_JUMBO
EtherStatsBroadcastPkts	Tx	C_TX_BC
EtherStatsMulticastPkts	Tx	C_TX_MC
EtherStatsCollisions	Tx	C_TX_COL
EtherStatsPkts64Octets	Tx	C_TX_SZ_64
EtherStatsPkts65to127Octets	Tx	C_TX_SZ_65_127
EtherStatsPkts128to255Octets	Tx	C_TX_SZ_128_255
EtherStatsPkts256to511Octets	Tx	C_TX_SZ_256_511
EtherStatsPkts512to1023Octets	Tx	C_TX_SZ_512_1023
EtherStatsPkts1024to1518Octets	Tx	C_TX_SZ_1024_1526

6.3.4.2 IEEE 802.3-2005 Annex 30A Counters

This section provides the mapping of IEEE 802.3-2005 Annex 30A counters to port counters. Only counter groups with supported counters are listed.

Table 114 • **Mandatory Counters**

Counter	Rx/Tx	Switch Core Implementation
aFramesTransmittedOK	Tx	C_TX_SZ_64 + C_TX_SZ_65_127 + C_TX_SZ_128_255 + C_TX_SZ_256_511 + C_TX_SZ_512_1023 + C_TX_SZ_1024_1526 + C_TX_SZ_JUMBO
aSingleCollisionFrames	Tx	Does not apply
aMultipleCollisionFrames	Tx	Does not apply
aFramesReceivedOK	Rx	Sum of C_RX_GREEN_PRIO_x, where x is 0 through 7.
aFrameCheckSequenceErrors	Rx	Not available. C_RX_CRC is the sum of FCS and alignment errors.
aAlignmentErrors	Rx	Not available. C_RX_CRC is the sum of FCS and alignment errors.

Table 115 • **Optional Counters**

Counter	Rx/Tx	Switch Core Implementation
aMulticastFramesXmittedOK	Tx	C_TX_MC
aBroadcastFramesXmittedOK	Tx	C_TX_BC
aMulticastFramesReceivedOK	Rx	C_RX_MC
aBroadcastFramesReceivedOK	Rx	C_RX_BC
aInRangeLengthErrors	Rx	Not available
aOutOfRangeLengthField	Rx	Not available

Table 115 • **Optional Counters *(continued)***

Counter	Rx/Tx	Switch Core Implementation
aFrameTooLongErrors	Rx	C_RX_LONG

Table 116 • **Recommended MAC Control Counters**

Counter	Rx/Tx	Switch Core Implementation
aMACControlFramesTransmitted	Tx	Not available
aMACControlFramesReceived	Rx	C_RX_CONTROL
aUnsupportedOpcodesReceived	Rx	Not available

Table 117 • **Pause MAC Control Recommended Counters**

Counter	Rx/Tx	Switch Core Implementation
aPauseMACControlFramesTransmitted	Tx	C_TX_PAUSE. Transmitted pause frames in 10/100 Mbps full-duplex are not counted.
aPauseMACControlFramesReceived	Rx	C_RX_PAUSE

6.3.4.3 SNMP Interfaces Group (RFC 2863)

The following table provides the mapping of SNMP interfaces group counters to port counters.

Table 118 • **Mapping of SNMP Interfaces Group Counters to Port Counters**

Counter	Rx/Tx	Switch Core Implementation
IfInOctets	Rx	C_RX_OCT
IfInUcastPkts	Rx	C_RX_UC
IfInNUcastPkts	Rx	C_RX_BC + C_RX_MC
IfInBroadcast (RFC 1573)	Rx	C_RX_BC
IfInMulticast (RFC 1573)	Rx	C_RX_MC
IfInDiscards	Rx	C_DR_TAIL + C_RX_CAT_DROP
IfInErrors	Rx	C_RX_CRC + C_RX_SHORT + C_RX_FRAG + C_RX_JABBER + C_RX_LONG
IfInUnknownProtos	Rx	Always zero.
IfOutOctets	Tx	C_TX_OCT
IfOutUcastPkts	Tx	C_TX_UC
IfOutNUcastPkts	Tx	C_TX_BC + C_TX_MC
ifOutMulticast (RFC 1573)	Tx	C_TX_MC
ifOutBroadcast (RFC 1573)	Tx	C_TX_BC
IfOutDiscards	Tx	Always zero.
IfOutErrors	Tx	C_TX_DROP + C_TX_AGE

6.3.4.4 SNMP Ethernet-Like Group (RFC 3536)

The following table provides the mapping of SNMP Ethernet-like group counters to port counters.

Table 119 • **Mapping of SNMP Ethernet-Like Group Counters to Port Counters**

Counter	Rx/Tx	Switch Core Implementation
dot3StatsAlignmentErrors	Rx	Not available. C_RX_CRC is the sum of FCS and alignment errors.
dot3StatsFCSErrors	Rx	Not available. C_RX_CRC is the sum of FCS and alignment errors.
dot3StatsSingleCollisionFrames	Tx	Not available.
dot3StatsMultipleCollisionFrames	Tx	Not available.
dot3StatsSQETestErrors	Rx	Not applicable.
dot3StatsDeferredTransmissions	Tx	Not available.
dot3StatsLateCollisions	Tx	Not available. C_TX_DROP is the sum of Late collisions and Excessive collisions.
dot3StatsExcessiveCollisions	Tx	Not available. C_TX_DROP is the sum of Late collisions and Excessive collisions.
dot3StatsInternalMacTransmitErrors	Tx	Not applicable. Always 0.
dot3StatsCarrierSenseErrors	Tx	Not available.
dot3StatsFrameTooLongs	Rx	C_RX_LONG.
dot3StatsInternalMacReceiveErrors	Rx	Not applicable. Always 0.
dot3InPauseFrames	Rx	C_RX_PAUSE.
dot3OutPauseFrames	Tx	C_TX_PAUSE. Transmitted pause frames in 10/100 Mbps full-duplex are not counted.

6.4 Layer-2 Switch

This section describes the Layer-2 switch features:

- Switching
- VLAN and GVRP
- Rapid Spanning Tree
- Link aggregation
- Port-based access control
- Mirroring
- SNMP support

6.4.1 Basic Switching

Basic switching covers forwarding, address learning, and address aging.

6.4.1.1 Forwarding

The devices contain a Layer-2 switch and frames are forwarded using Layer-2 information only.

The switch is designed to comply with the IEEE Bridging standard in IEEE 802.1D and the IEEE VLAN standard in IEEE 802.1Q:

- Unicast frames are forwarded to a single destination port that corresponds to the DMAC.
- Multicast frames are forwarded to multiple ports determined by the DMAC multicast group. The CPU configures multicast groups in the MAC table and the port group identifier (PGID) table. A multicast group can span across any set of ports.
- Broadcast frames (DMAC = FF-FF-FF-FF-FF-FF) are, by default, flooded to all ports except the ingress port. Also, in compliance with the standard, a unicast or multicast frame with unknown

DMAC is flooded to all ports except the ingress port. It is possible to configure flood masks to restrict the flooding of frames. There are separate flood masks for the following frame types:

Unicast (ANA::FLOODING.FLD_UNICAST)
Layer 2 multicast (ANA::FLOODING.FLD_MULTICAST)
Layer 2 broadcast (ANA::FLOODING.FLD_BROADCAST)
IPv4 multicast data (ANA::FLOODING_IPMC.FLD_MC4_DATA)
IPv4 multicast control (ANA::FLOODING_IPMC.FLD_MC4_CTRL)
IPv6 multicast data (ANA::FLOODING_IPMC.FLD_MC6_DATA)
IPv6 multicast control (ANA::FLOODING_IPMC.FLD_MC6_CTRL)

For frames with a known destination MAC address, the destination mask comes from an entry in the port group identifier table (ANA::PGID). The PGID table contains 107 entries (entry 0 through 106), where entry 0 through 63 are used for destination masks. The remaining PGID entries are used for other parts of the forwarding and are described below.

The following table shows the PGID table organization.

Table 120 • **Port Group Identifier Table Organization**

Entry Type	Number
Unicast entries	0 – 26 (including CPU)
Multicast entries	27 – 63
Aggregation Masks	64 – 79
Source Masks	80 – 106

The unicast entries contains only the port number corresponding to the entry number.

Destination masks for multicast groups must be manually entered through the CPU into the destination masks table. IPv4 and IPv6 multicast entries can also be entered using direct encoding in the MAC table, where the destination masks table is not used. For information about forwarding and configuring destination masks, see MAC Table, page 48.

The aggregation masks ensures that a frame is forwarded to exactly one member of an aggregation group.

For all forwarding decisions, a source mask prevents frames from being sent back to the ingress port. The source mask removes the ingress port from the destination mask.

All ports are enabled for receiving frames by default. This can be disabled by clearing ANA:PORT:PORT_CFG.RECV_ENA.

6.4.1.2 Address Learning

The learning process minimizes the flooding of frames. A frame's source MAC address is learned together with its VID. Each entry in the MAC table is uniquely identified by a (MAC,VID) pair. In the forwarding process, a frame's (DMAC,VID) pair is used as the key for the MAC table lookup.

The learning of unknown SMAC addresses can be either hardware-based or CPU-based. The following list shows the available learn schemes, which can be configured per port:

- **Hardware-based learning** autonomously adds entries to the MAC table without interaction from the CPU. Use the following configuration:
  ANA:PORT:PORT_CFG.LEARN_ENA = 1
  ANA:PORT:PORT_CFG.LEARNCPU = 0
  ANA:PORT:PORT_CFG.LEARNDROP = 0
  ANA:PORT:PORT_CFG.LEARNAUTO = 1
- **CPU-based learning** copies frames with unknown SMACs, or when the SMAC appears on a different port, to the CPU. These frames are forwarded as usual. Use the following configuration.
  ANA:PORT:PORT_CFG.LEARN_ENA = 1
  ANA:PORT:PORT_CFG.LEARNCPU = 1

ANA:PORT:PORT_CFG.LEARNDROP = 0
ANA:PORT:PORT_CFG.LEARNAUTO = 0

- **Secure CPU-based learning** is similar to CPU-based learning, except that it allows the CPU to verify the SMAC addresses before both learning and forwarding. Secure CPU-based learning redirects frames with unknown SMACs, or when the SMAC appears on a different port, to the CPU. These frames are not forwarded by hardware. Use the following configuration.
  ANA::PORT_CFG.LEARN_ENA = 1
  ANA::PORT_CFG.LEARNCPU = 1
  ANA::PORT_CFG.LEARNDROP = 1
  ANA::PORT_CFG.LEARNAUTO = 0
- **No learning** where all learn frames are discarded. Frames with known SMAC in the MAC table are forwarded by hardware. Use the following configuration.
  ANA:PORT:PORT_CFG.LEARN_ENA = 1
  ANA:PORT:PORT_CFG.LEARNCPU = 0
  ANA:PORT:PORT_CFG.LEARNDROP = 1
  ANA:PORT:PORT_CFG.LEARNAUTO = 0

Frames forwarded to the CPU for learning can be extracted from the CPU extraction queue configured in ANA:PORT:CPUQ_CFG.CPUQ_LRN.

During CPU-based learning, the rate of frames subject to learning being copied or redirected to the CPU can be controlled with the learn storm policer (ANA::STORMLIMIT_CFG[3]). This policer puts a limit on the number of frames per second that are subject to learning being copied or redirected to the CPU. The learn frames storm policer can help prevent a CPU from being overloaded when performing CPU based learning.

6.4.1.3 MAC Table Address Aging

To keep the MAC table updated, an aging scan is conducted to remove entries that were not recently accessed. This ensures that stations that have moved to a new location are not permanently prevented from receiving frames in their new location. It also frees up MAC table entries occupied by obsolete stations to give room for new stations.

In IEEE 802.1D, the recommended period for aging-out entries in the MAC address table is 300 seconds per entry. The device aging implementation checks for the aging-out of all the entries in the table. The first age scan sets the age bit for every entry in the table. The second age scan removes entries where the age bit has not been cleared since the first age scan. An entry's age bit is cleared when a received frame's (SMAC, VID) matches an entry's (MAC, VID); that is, the station is active and transmits frames. To ensure that 300 seconds is the longest an entry can reside not accessed (and unchanged) in the table, the maximum time between age scans is 150 seconds.

The device can conduct age scans in two ways:

- Automatic age scans
- CPU initiated age scans

When using automatic aging, the time between age scans is set in the ANA::AUTOAGE register in steps of 1 second, in the range from 1 second to 12 days.

When using CPU-initiated aging, the CPU implements the timing between age scans. A scan is initiated by sending an aging command to the MAC address table (ANA::MACACCESS. MAC_TABLE_CMD).

The CPU-controlled age scan process can conveniently be used to flush the entire MAC table by conducting two age scans, one immediately after the other.

Flushing selective MAC table entries is also possible. Incidents that require MAC table flushing are:

- Reconfiguration of Spanning Tree protocol port states, which may cause station moves to occur.
- If there is a link failure notification (identified by a PHY layer device), flush the MAC table on the specific port where the link failed.

To deal with these incidents, the age scan process is configurable to run only for entries learned on a specified port or for a specified VLAN (ANA:: ANAGEFIL.VID_VAL). The filters can also be combined to do aging on entries that match both the specific port and the specific VLAN.

Single entries can be flushed from the MAC table by sending the FORGET command to the MAC address table.

6.4.2 Standard VLAN Operation

This section provides information about configuring and operating the devices as a standard VLAN-aware switch. For more information about using the switch as a Q-in-Q enabled provider bridge, see Provider Bridges and Q-in-Q Operation, page 137. For information about the use of private VLANs and asymmetric VLANs, see Private VLANs, page 141 and Asymmetric VLANs, page 145.

The following table lists the port module registers for standard VLAN operation.

Table 121 • **Port Module Registers for Standard VLAN Operation**

Register/Register Field	Description	Replication
MAC_TAGS_CFG	Allows tagged frames to be 4 bytes longer than the length configured in MAC_MAXLEN_CFG.	Per port

The following table lists the analyzer configurations and status bits for standard VLAN operation.

Table 122 • **Analyzer Registers for Standard VLAN Operation**

Register/Register Field	Description	Replication
DROP_CFG.DROP_UNTAGGED_ENA	Discard untagged frames.	Per port
DROP_CFG.DROP_C_TAGGED_ENA	Discard VLAN tagged frames.	Per port
DROP_CFG.DROP_PRIO_C_TAGGED_ENA	Discard priority tagged frames.	Per port
VLAN_CFG.VLAN_AWARE_ENA	Use incoming VLAN tags in VLAN classification.	Per port
VLAN_CFG.VLAN_POP_CNT	Remove VLAN tags from frames in the rewriter.	Per port
VLAN_CFG.VLAN_DEI VLAN_CFG.VLAN_PCP VLAN_CFG.VLAN_VID	Ingress port VLAN configuration.	Per port
VLANMASK	Per-port VLAN ingress filtering enable.	None
ANEVENTS.VLAN_DISCARD	A sticky bit indicating that a frame was dropped due to lack of VLAN membership of source port.	None
ADVLEARN.VLAN_CHK	Disable learning for frames discarded due to source port VLAN membership check.	None
VLANACCESS	VLAN table command. For indirect access to configuration of the 4096 VLANs.	None
VLANTIDX	VLAN table index. For indirect access to configuration of the 4096 VLANs.	None
AGENCTRL.FID_MASK	Enable shared VLAN learning.	None
CPU_FWD_GARP_CFG	Enable capture of frames with reserved GARP DMAC addresses, including GVRP for VLAN registration. Per-address configuration.	Per port
CPUQ_8021_CFG.CPUQ_GARP_VAL	CPU queue for captured GARP frames.	Per GARP address

The following table lists the rewriter registers for standard VLAN operation.

Table 123 • **Rewriter Registers for Standard VLAN Operation**

Register/Register Field	Description	Replication
TAG_CFG	Egress VLAN tagging configuration	Per port
PORT_VLAN_CFG	Egress port VLAN configuration	Per port

In a VLAN-aware switch, each port is a member of one or more virtual LANs. Each incoming frame must be assigned a VLAN membership and forwarded according to the assigned VID. The following information draws on the definitions and principles of operations in IEEE 802.1Q. Note that the switch supports more features than mentioned in the following section, which only describes the basic requirements for a VLAN aware switch.

Standard VLAN operation is configured individually per switch port using the following configuration:

- MAC_TAGS_CFG.VLAN_AWR_ENA = 1
  MAC_TAGS_CFG.VLAN_LEN_AWR_ENA = 1
- VLAN_CFG.VLAN_AWARE_ENA = 1,
  VLAN_CFG.VLAN_POP_CNT = 1.

Each switch port has an Acceptable Frame Type parameter, which is set to Admit Only VLAN tagged frames or Admit All Frames:

- Admit Only VLAN-tagged frames:
  DROP_CFG.DROP_UNTAGGED_ENA = 1,
  DROP_CFG.DROP_PRIO_C_TAGGED_ENA = 1,
  DROP_CFG.DROP_C_TAGGED = 0.
- Admit All Frames:
  DROP_CFG.DROP_UNTAGGED_ENA = 0,
  DROP_CFG.DROP_PRIO_C_TAGGED_ENA = 0,
  DROP_CFG.DROP_C_TAGGED = 0.

Frames that are not discarded are subject to the VLAN classification. Untagged and priority-tagged frames are classified to a Port VLAN Identifier (PVID). The PVID is configured per port in VLAN_CFG.VLAN_VID. Tagged frames are classified to the VID given in the frame's tag. For more information about VLAN classification, see VLAN Classification, page 44.

6.4.2.1 Forwarding

Forwarding is always based on the combination of the classified VID and the destination MAC address. By default, all switch ports are members of all VLANs. This can be changed in VLANACCESS and VLANTIDX where port masks per VLAN are set up.

6.4.2.2 Ingress Filtering

VLAN ingress filtering can be enabled per switch port with the register VLANMASK and per router port with MACx_CFG.INGRESS_CHK.

The filter checks for all incoming frames to determine if the ingress port is a member of the VLAN to which the frame is classified. If the port is not a member, the frame is discarded. Whenever a frame is discarded due to lack of VLAN membership, the ANEVENTS.VLAN_DISCARD sticky bit is set. To ensure that VLAN ingress filtered frames are not learned, ADVLEARN.VLAN_CHK must be set.

6.4.2.3 GARP VLAN Registration Protocol (GVRP)

GARP VLAN Registration Protocol (GVRP) is used to propagate VLAN configurations between bridges. On a GVRP-enabled switch, all GVRP frames must be redirected to the CPU for further processing. The GVRP frames use a reserved GARP MAC address (01-80-C2-00-00-21) and can be redirected to the CPU by setting bit 1 in the analyzer register CPU_FWD_GARP_CFG.

6.4.2.4 Shared VLAN Learning

The devices can be configured for either Independent VLAN learning or Shared VLAN learning. Independent VLAN learning is the default.

Shared VLAN learning, where multiple VLANs map to the same filtering database, is enabled through Filter Identifiers (FIDs). Basically, this means that learning is unique for a (MAC, FID) set and that a learned MAC address is learned for all VIDs that map to the FID. Shared VLAN learning is enabled in AGENCTRL.FID_MASK.

The 12-bit FID mask sets which bits in the VID are indifferent to the learning. For example, if the least significant two bits are set in the FID mask, the following VID sets are sharing learning, where X and Y are any hexadecimal digits:

- VID set 1: 0xXY0, 0xXY1, 0xXY2, 0xXY3
- VID set 2: 0xXY4, 0xXY5, 0xXY6, 0xXY7
- VID set 3: 0xXY8, 0xXY9, 0xXYA, 0xXYB
- VID set 4: 0xXYC, 0xXYD, 0xXYE, 0xXYF

6.4.2.5 Untagging

An untagged set can be configured for each egress port, which defines the VIDs for which frames are transmitted untagged. The untagged set can consist of zero, one, or all VIDs. For all VIDs not in the untagged set, frames are transmitted tagged. The available configurations are:

- The untagged set is empty:
  TAG_CFG.TAG_CFG = 3.
- The untagged set consists of all VIDs:
  TAG_CFG.TAG_CFG = 0.
- The untagged set consists of one VID <VID>:
  TAG_CFG.TAG_CFG = 1.
  PORT_VLAN_CFG.PORT_VID = <VID>.

Optionally, frames received as priority-tagged frames (VID = 0) can also be transmitted as untagged (TAG_CFG.TAG_CFG=2).

6.4.2.5.1 Port-Based VLAN Example

Situation:

Ports 0 and 1 are isolated from ports 2 and 3 using port-based VLANs. Ports 0 and 1 are assigned port VID 1 and ports 2 and 3 port VID 2. All frames in the network are untagged.

Resolution:

```
# Port module configuration of ports 0 – 1.
# Configure the ports to always use the port VID.
VLAN_CFG.VLAN_AWARE_ENA = 0
# Allow only untagged frames.
DROP_CFG.DROP_UNTAGGED_ENA = 0
DROP_CFG.DROP_PRIO_C_TAGGED = 1
DROP_CFG.DROP_C_TAGGED = 1
# Configure the port VID to 1.
VLAN_CFG.VLAN_VID = 1

# Port module configuration of ports 2 – 3.
# Same as for ports 0-1, except that the port VID is set to 2.
VLAN_CFG.VLAN_VID = 2
# Analyzer configuration.
# Configure VLAN 1 to contain ports 0-1.
VLANTIDX.INDEX = 1
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 1
VLANACCESS.VLAN_PORT_MASK = 0x03
VLANACCESS.VLAN_TBL_CMD = 2
# Configure VLAN 2 to contain ports 2-3.
VLANTIDX.INDEX = 2
```

```
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 1
VLANACCESS.VLAN_PORT_MASK = 0x0C
VLANACCESS.VLAN_TBL_CMD = 2
```

6.4.3 Provider Bridges and Q-in-Q Operation

The following table lists the port module configurations for provider bridge VLAN operation.

Table 124 • **Port Module Configurations for Provider Bridge VLAN Operation**

Register/Register Field	Description	Replication
MAC_TAGS_CFG	Allow single tagged frames to be 4 bytes longer and double-tagged frames to be 8 bytes longer than the length configured in MAC_MAXLEN_CFG.	Per port

The following table lists the port module configurations for provider bridge VLAN operation.

Table 125 • **System Configurations for Provider Bridge VLAN Operation**

Register/Register Field	Description	Replication
VLAN_ETYPE_CFG.VLAN_S_TAG_ETYPE_VAL	TPID for S-tagged frames. EtherType 0x88A8 and the configurable value VLAN_ETYPE_CFG.VLAN_S_TAG_ETYPE_VAL are identified as the S-tag identifier.	Per port

The following table lists the analyzer configurations for provider bridge VLAN operation.

Table 126 • **Analyzer Configurations for Provider Bridge VLAN Operation**

Register/Register Field	Description	Replication
DROP_CFG.DROP_UNTAGGED_ENA	Discard untagged frames.	Per port
DROP_CFG.DROP_S_TAGGED_ENA	Discard VLAN S-tagged frames.	Per port
DROP_CFG.DROP_PRIO_S_TAGGED_ENA	Discard priority S-tagged frames.	Per port
VLAN_CFG.VLAN_AWARE_ENA	Use incoming VLAN tags in VLAN classification.	Per port
VLAN_CFG.VLAN_POP_CNT	Remove VLAN tags from frames in the rewriter.	Per port
VLAN_CFG.VLAN_TAG_TYPE	Tag type for untagged frames (Customer tag or service tag).	Per port
VLAN_CFG.VLAN_INNER_TAG_ENA	Use inner tag for VLAN classification instead of outer tag.	Per port
VLAN_CFG.VLAN_DEI VLAN_CFG.VLAN_PCP VLAN_CFG.VLAN_VID	Ingress port VLAN configuration.	Per port

Table 126 • **Analyzer Configurations for Provider Bridge VLAN Operation *(continued)***

Register/Register Field	Description	Replication
VLANACCESS	VLAN table command. For indirect access to configuration of the 4096 VLANs.	None
VLANTIDX	VLAN table index. For indirect access to configuration of the 4096 VLANs.	None

The devices support the standard provider bridge features in IEEE 802.1ad (Provider Bridges). The features related to provider bridges are:

- Support for multiple tag headers (EtherTypes 0x8100, 0x88A8, and a programmable value are recognized as tag header EtherTypes)
- Pushing and popping of one VLAN tag
- Selective VLAN classification using either inner or outer VLAN tag
- Enabling or disabling learning per VLAN

The following section discusses briefly how to configure these different features in the switch.

The devices support multiple VLAN tags. They can be used in MAN applications as a provider bridge, aggregating traffic from numerous independent customer LANs into the MAN space. One of the purposes of the provider bridge is to recognize and use VLAN tags so that the VLANs in the MAN space can be used independent of the customers' VLANs. This is accomplished by adding a VLAN tag with a MAN-related VID for frames entering the MAN. When leaving the MAN, the tag is stripped, and the original VLAN tag with the customer-related VID is again available. This provides a tunneling mechanism to connect remote customer VLANs through a common MAN space without interfering with the VLAN tags. All tags use EtherType 0x8100 for customer tags and EtherType 0x88A8, or a programmable value, for service provider tags.

If a given service VLAN only has two member ports on the switch, the learning can be disabled for the particular VLAN (VLANTIDX.VLAN_LEARN_DISABLE) and can rely on flooding as the forwarding mechanism between the two ports. This way, the MAC table requirements are reduced.

6.4.3.0.1 MAN Access Switch Example

Situation:

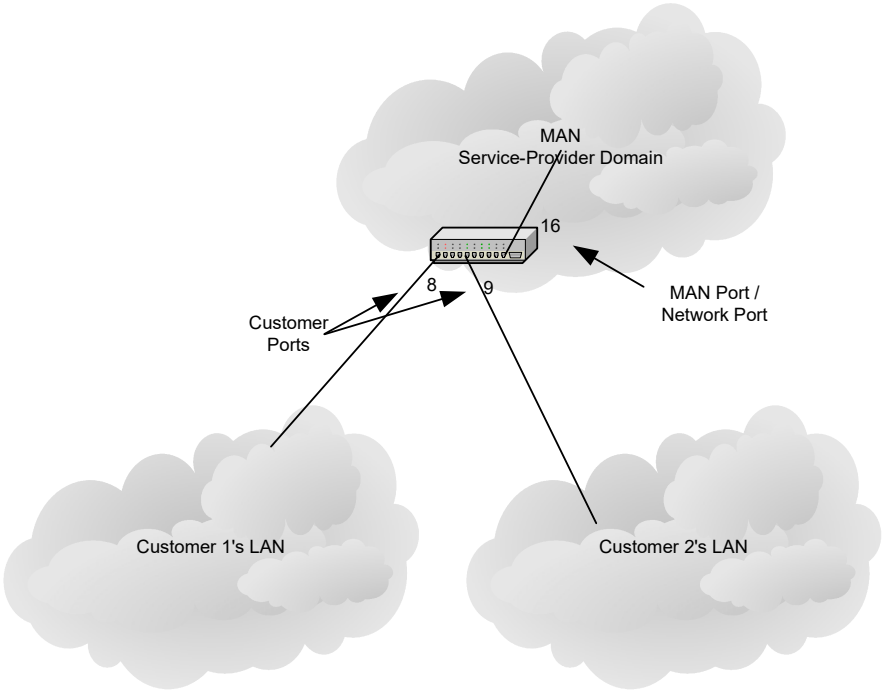
The following is an example of setting up the device as a MAN access switch with these requirements:

- Customer ports are aggregated into a network port for tunneling through the MAN to access remote VLANs.
- Local switching between ports of the different customers must be eliminated.
- Frames must be label-switched from network port to correct customer port without need for MAC address learning.

Figure 45 • **MAN Access Switch Setup**

Frames in This Segment

Service Provider Tag (Outer Tag)		Customer Tag (Inner Tag)		
EtherType	VID	EtherType	VID	Description
0x88A8	1	0x8100	1	Frames to/from customer 1's VLAN 1
0x88A8	1	0x8100	118	Frames to/from customer 1's VLAN 118
0x88A8	1	0x8100	0	Priority-tagged frames to/from customer 1
0x88A8	2	0x8100	1	Frames to/from customer 2's VLAN 1
0x88A8	2	0x8100	4	Frames to/from customer 2's VLAN 4
0x88A8	2	N/A	N/A	Untagged frames to/from customer 2



Frames in This Segment

Customer Tag		
EtherType	VID	Description
0x8100	1	Frames in Customer 1's VLAN 1
0x8100	118	Frames in Customer 1's VLAN 118
0x8100	0	Customer 1's Priority-Tagged Frames

Frames in This Segment

Customer Tag		
EtherType	VID	Description
0x8100	1	Frames in Customer 2's VLAN 1
0x8100	4	Frames in Customer 2's VLAN 4
N/A	N/A	Customer 2's Untagged Frames

This example is typically accomplished by letting each customer port have a unique port VID (PVID), which is used in the outer VLAN tag (the service provider tag). In the MAN, the VID directly indicates the customer port from which the frame is received or the customer port to which the frame is going.

A customer port is VLAN-unaware and classifies to a port-based VLAN. In the egress direction of the customer port, frames are transmitted untagged, which facilitates the stripping of the outer tag. That is, the provider tag is stripped, but the customer tag is kept. The port must allow frames with a maximum size of 1522 bytes.

Resolution:

```
# Configuration of customer 1’s port (port 8).
# Allow for a single VLAN tag in the length check and set the maximum length
without VLAN
# tag to 1518 bytes.
MAC_TAGS_CFG.VLAN_LEN_AWR_ENA = 1
MAC_TAGS_CFG.VLAN_AWAR_ENA = 1
MAC_MAXLEN_CFG.MAX_LEN = 1518
# Configure the port to leave any incoming tags in the frame and to ignore any
# incoming VLAN tags in the VLAN classification. The port VID is always used
in the
# VLAN classification.
VLAN_CFG.VLAN_POP_CNT = 0
VLAN_CFG.VLAN_AWARE_ENA = 0
# Allow both C-tagged and untagged frames coming in to the device to also
support customer traffic not using VLANs to be carried across the MAN.
DROP_CFG.DROP_UNTAGGED_ENA = 0
DROP_CFG.DROP_C_TAGGED = 0
DROP_CFG.DROP_PRIO_C_TAGGED = 0
DROP_CFG.DROP_S_TAGGED = 1
DROP_CFG.DROP_PRIO_S_TAGGED = 1
# Use service provider tagging when frames from this port exit the switch.
# (EtherType 0x88A8).
VLAN_CFG.VLANTAG_TYPE = 1
# Configure the port VID to 1.
VLAN_CFG.VLAN_VID = 1
# Configure the egress side of the port to not insert tags.
# (The service provider tags are stripped in the ingress side of the MAN port).
TAG_CFG.TAG_CFG = 0
# Configuration of customer 2's port (port 9).
# Same as for customer 1’s port (port 8), except that the port VID is set to 2.
VLAN_CFG.VLAN_VID = 2
# Configuration of the network port (port 16).
# MAN traffic in transit between network ports is supported by configuring all
network
# ports as follows:
# Allow for two VLAN tags in the length check and set the max length without
# VLAN tags to 1518 bytes.
MAC_TAGS_CFG.VLAN_LEN_AWR_ENA = 1
MAC_TAGS_CFG.VLAN_AWAR_ENA = 1
MAC_TAGS_CFG.PB_ENA =1
MAC_MAXLEN_CFG.MAX_LEN = 1518
# Configure the port to use incoming VLAN tags in the VLAN classification,
# and to remove the first (outer) VLAN tag (the service tag) from incoming
frames.
VLAN_CFG.VLAN_POP_CNT = 1
VLAN_CFG.VLAN_AWARE_ENA = 1
# Allow only S-tagged frames.
DROP_CFG.DROP_UNTAGGED_ENA = 1
DROP_CFG.DROP_C_TAGGED = 1
DROP_CFG.DROP_PRIO_C_TAGGED = 1
DROP_CFG.DROP_S_TAGGED = 0
DROP_CFG.DROP_PRIO_S_TAGGED = 0
# The tag type is unused on the network port
VLAN_CFG.VLANTAG_TYPE = 0
# Configure the egress side of the port to insert tags.
TAG_CFG.TAG_CFG = 1
# Common configuration in the analyzer.
```

```
# Configure VLAN 1 to contain customer 1’s port (port 8) and the network port
# (port 16). Disable learning in VLAN 1. Ingress filtering is don’t care for
port
# based VLANs.
VLANTIDX.INDEX = 1
VLANTIDX.VLAN_PRIV_VLAN = 0 (don’t care, for this example)
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 1
VLANTIDX.VLAN_SRC_CHK = 0 (don’t care, for this example)
VLANACCESS.VLAN_PORT_MASK = 0x00010100
VLANACCESS.VLAN_TBL_CMD = 2
# Configure VLAN 2 to contain customer 2's port (port 9) and the network port
# (port 16). Disable learning in VLAN 2. Ingress filtering is don’t-care for
port
# based VLANs.
VLANTIDX.INDEX = 2
VLANTIDX.VLAN_PRIV_VLAN = 0 (don’t care, for this example)
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 1
VLANTIDX.VLAN_SRC_CHK = 0 (don’t care, for this example)
VLANACCESS.VLAN_PORT_MASK = 0x00010200
VLANACCESS.VLAN_TBL_CMD = 2
```

6.4.4 Private VLANs

The following table lists the analyzer configuration registers for private VLAN support.

Table 127 • **Private VLAN Configuration Registers**

Register	Description	Replication
VLANACCESS	VLAN table command. For indirect access to configuration of the 4096 VLANs.	None
VLANTIDX	VLAN table index. For indirect access to configuration of the 4096 VLANs.	None
ISOLATED_PORTS	VLAN port mask indicating isolated ports in private VLANs.	None
COMMUNITY_PORTS	VLAN port mask indicating community ports in private VLANs.	None

When a VLAN is configured to be a private VLAN, communication between ports within that VLAN can be prevented. Two application examples are:

- Customers connected to an ISP can be members of the same VLAN, but they are not allowed to communicate with each other within that VLAN.
- Servers in a farm of web servers in a Demilitarized Zone (DMZ) are allowed to communicate with the outside world and with database servers on the inside segment, but are not allowed to communicate with each other

For private VLANs to be applied, the switch must first be configured for standard VLAN operation. For more information, see Standard VLAN Operation, page 134. When this is in place, one or more of the configured VLANs can be configured as private VLANs. Ports in a private VLAN fall into one of three groups:

- Promiscuous ports
  Ports from which traffic can be forwarded to all ports in the private VLAN

  Ports that can receive traffic from all ports in the private VLAN
- Community Ports
  Ports from which traffic can only be forwarded to community and promiscuous ports in the private

VLAN

Ports that can receive traffic from only community and promiscuous ports in the private VLAN

- Isolated ports
  Ports from which traffic can only be forwarded to promiscuous ports in the private VLAN

  Ports that can receive traffic from only promiscuous ports in the private VLAN

The configuration of promiscuous, community, and isolated ports applies to all private VLANs.

The forwarding of frames classified to a private VLAN happens:

- When traffic comes in on a promiscuous port in a private VLAN, the VLAN mask from the VLAN table is applied.
- When traffic comes in on a community port, the ISOLATED_PORT mask is applied in addition to the VLAN mask from the VLAN table.
- When traffic comes in on an isolated port, the ISOLATED_PORT mask and the COMMUNITY_PORT mask are applied in addition to the VLAN mask from the VLAN table.

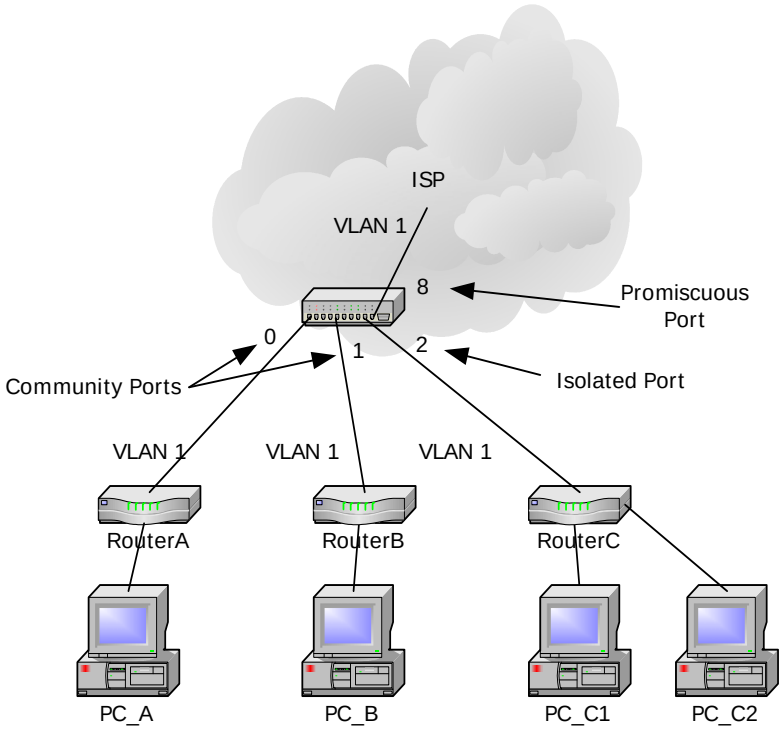
6.4.4.0.1 ISP Example

Situation:

Customers A, B, and C are connected to the same switch at the ISP. Customers A and B are allowed to communicate with each other, as well as the ISP. Customer C can only communicate with the ISP. VLAN 1 is the private VLAN that isolates Customers A, B from C. Traffic on VLAN 1 coming in from the ISP (port 8) uses the VLAN mask in the VLAN table. Traffic on VLAN 1 from customer A or B has the ISOLATED_PORTS mask applied in addition to the mask from the VLAN table, with the result that traffic from customer A and B is not forwarded to customers C. Traffic on VLAN 1 from customer C has the ISOLATED_PORTS mask and the COMMUNITY_PORTS mask applied in addition to the mask from the VLAN table, with the result that traffic from customer C is not forwarded to customers A and B.

The following illustration shows the desired setup.

Figure 46 • **ISP Example for Private VLAN**



VLAN Table

VID	Ports in Mask	Private
⋮	⋮	⋮
1	0, 1, 2, 8	1
⋮	⋮	⋮

ISOLATED_PORTS
(Isolated ports set to 0)

Bit	Value
0	1
1	1
2	0
⋮	⋮
8	1
⋮	⋮

COMMUNITY_PORTS
(Community ports set to 0)

Bit	Value
0	0
1	0
2	1
⋮	⋮
8	1
⋮	⋮

Resolution:

```
# It is assumed that Port VID and tag handling for VLAN 1 is already
# configured according to the description in Standard VLAN Operation.
# Configure VLAN 1 as a private VLAN in the VLAN table by performing these
steps:
# - Point to VLAN 1.
# - Set it as private.
# - Disable mirroring of the VLAN (not important for the example).
# - Enable learning within the VLAN (not important for the example).
# - Disable source check within the VLAN (not important for the example).
# - Include ports 0, 1, 2, and 8 in the VLAN mask.
# Insert the entry into the VLAN table.
VLANTIDX.INDEX = 1
VLANTIDX.VLAN_PRIV_VLAN = 1
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0 (don’t care, for this example)
VLANTIDX.VLAN_SRC_CHK = 0 (don't care, for this example)
VLANACCESS.VLAN_PORT_MASK = 0x00000107
VLANACCESS.VLAN_TBL_CMD = 2
```

```
# Configure the private VLAN mask so that port 8 is a promiscuous
# port, ports 0 and 1 are community ports, and port 2 is an isolated port.
ISOLATED_PORTS.ISOL_PORTS = 0x00000103
COMMUNITY_PORTS.COMM_PORTS = 0x00000104
```

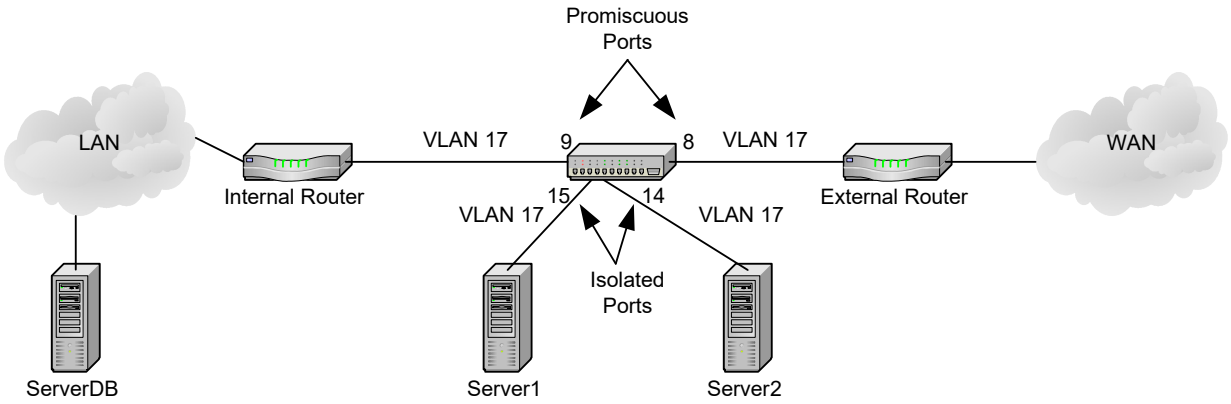
6.4.4.0.2 DMZ Example

Situation:

VLAN 17 is a private VLAN that isolates Server1 and Server2. Traffic on VLAN 17 coming from the internal or the external router (ports 8 and 9) uses the VLAN mask in the VLAN table. Traffic on VLAN 17 from Server1 and Server2 (ports 14 and 15) has the ISOLATED_PORTS applied in addition to the mask from the VLAN table, with the result that traffic from Server1 is not forwarded to Server2 and visa versa.

The following illustration shows the desired setup.

Figure 47 • **DMZ Example for Private VLAN**



VLAN Table

VID	Ports in Mask	Private
⋮	⋮	⋮
17	8, 9, 14, 15	1
⋮	⋮	⋮

ISOLATED_PORTS
(Promiscuous Ports Set to 1)

Bit	Value
⋮	⋮
8	1
9	1
⋮	⋮
14	0
15	0
⋮	⋮

Resolution:

```
# It is assumed that Port VID and tag handling for VLAN 17 is already
# configured according to the description in Standard VLAN Operation.
# Configure VLAN 17 as a private VLAN in the VLAN table by performing these
steps:
# - Point to VLAN 17.
# - Set it as private.
# - Disable mirroring of the VLAN (not important for the example).
# - Enable learning within the VLAN (not important for the example).
# - Disable source check within the VLAN (not important for the example).
# - Include ports 8, 9, 14, and 15 in the VLAN mask.
# - Insert the entry into the VLAN table.
VLANTIDX.INDEX = 17
VLANTIDX.VLAN_PRIV_VLAN = 1
```

```
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0 (don’t care, for this example)
VLANTIDX.VLAN_SRC_CHK = 0 (don’t care, for this example)
VLANACCESS.VLAN_PORT_MASK = 0x0000C300
VLANACCESS.VLAN_TBL_CMD = 2
# Configure the private VLAN mask so that ports 8 and 9 are promiscuous
# ports.
ISOLATED_PORTS.ISOL_PORTS = 0x00000300
```

6.4.5 Asymmetric VLANs

Asymmetric VLANs use the same configuration registers as for standard VLAN operation. For more information about standard VLAN operation, see Standard VLAN Operation, page 134.

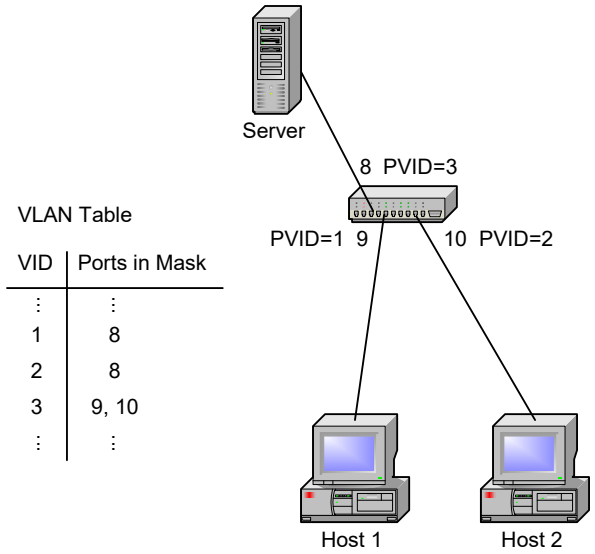
Asymmetric VLANs can be used to prevent communication between hosts in a network. This behavior is similar to what can be obtained by using private VLANs. For more information, seePrivate VLANs, page 141.

Situation:

A server and two hosts are connected to a switch. Communication between the hosts and the server should be allowed, but the hosts are not allowed to communicate directly. All traffic between the server and the hosts is untagged. Host 1 is connected to port 9, host 2 to port 10, and the server to port 8.

The host-1 port gets port VID 1 and the host-2 port gets port VID 2. The server port is a member of both VLANs 1 and 2. The server port gets port VID 3, and the two host ports are members of VLAN 3, as shown in the following illustration.

Figure 48 • **Asymmetric VLANs**



Resolution:

```
# Analyzer configurations common for ports 8, 9, and 10.
# Allow only untagged frames.
DROP_CFG.DROP_UNTAGGED_ENA = 0
DROP_CFG.DROP_C_TAGGED_ENA = 1
DROP_CFG.DROP_PRIO_C_TAGGED_ENA = 1
# As tagged frames are dropped all frames are classified to the port VID.
VLAN_CFG.VLAN_AWARE_ENA = 0 (don’t care, for this example)
# Configure the egress side of the port to not insert tags.
TAG_CFG.TAG_CFG = 0
```

```
# Analyzer configuration specific for port 8. Set the port VID to 3.
VLAN_CFG.VLAN_VID = 3
VLAN_CFG.VLAN_DEI = 0 (don’t care, for this example)
# Analyzer configuration specific for port 9. Set the port VID to 1.
VLAN_CFG.VLAN_VID = 1
VLAN_CFG.VLAN_DEI = 0 (don’t care, for this example)


# Analyzer configuration specific for port 10. Set the port VID to 2.
VLAN_CFG.VLAN_VID = 2
VLAN_CFG.VLAN_DEI = 0 (don’t care, for this example)
# Analyzer configuration common to all ports.
# Configure VLAN 1 to contain port 8.
VLANTIDX.INDEX = 1
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 0
VLANACCESS.VLAN_PORT_MASK = 0x00000100
VLANACCESS.VLAN_TBL_CMD = 2
# Configure VLAN 2 to contain port 8.
VLANTIDX.INDEX = 2
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 0
VLANACCESS.VLAN_PORT_MASK = 0x00000100
VLANACCESS.VLAN_TBL_CMD = 2
# Configure VLAN 3 to contain ports 9 and 10.
VLANTIDX.INDEX = 3
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 0
VLANACCESS.VLAN_PORT_MASK = 0x00000600
VLANACCESS.VLAN_TBL_CMD = 2
```

6.4.6 Spanning Tree Protocol

This section provides information about Rapid Spanning Tree Protocol (RSTP) support. The devices also support legacy Spanning Tree Protocol (STP). STP was obsoleted by RSTP in IEEE 802.1D and is not described in this document.

It is assumed that only LAN ports connected to the switch core participate in the spanning tree protocol. This implies that BPDUs are terminated by the switch core.

6.4.6.1 Rapid Spanning Tree Protocol

The following table lists the analyzer configuration registers for Rapid Spanning Tree Protocol (RSTP) operation.

Table 128 • **Analyzer Configurations for RSTP Support**

Register/Register Field	Description	Replication
PGID[80-106]	Source masks used for ingress filtering	Per port
PGID[64-79]	Aggregation masks that can be used for egress filtering for RSTP	16
PORT_CFG.LEARN_ENA	Enable learning per port	Per port

Table 128 • **Analyzer Configurations for RSTP Support *(continued)***

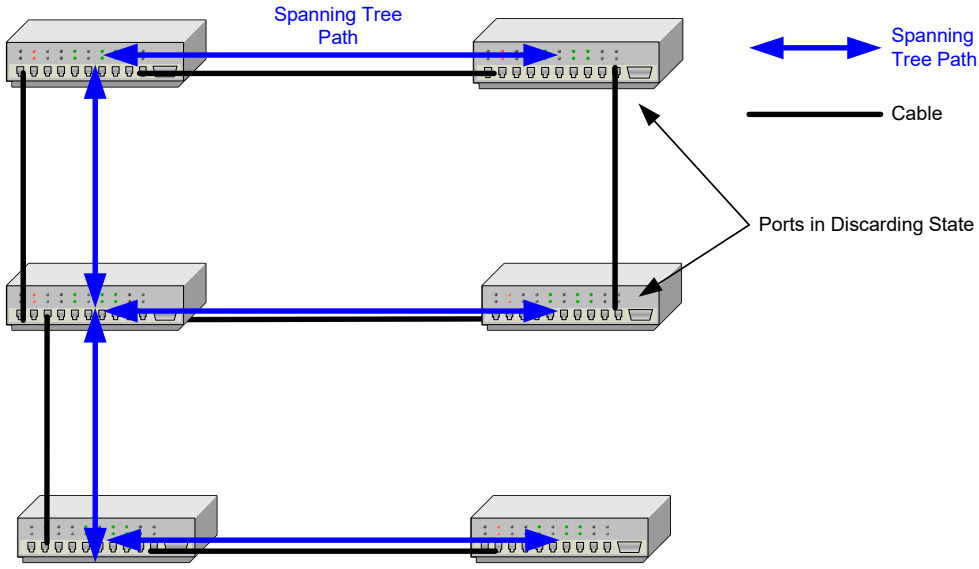
Register/Register Field	Description	Replication
CPU_FWD_BPDU_CFG	Enable redirection of frames with reserved BPDU DMAC addresses	Per port per address
CPUQ_8021_CFG.CPUQ_BPDU_VAL	CPU extraction queue for redirected BPDU frames	Per address

To eliminate potential loops in a network, the Rapid Spanning Tree Protocol in IEEE 802.1D creates a single path between any two bridges in a network, adding stability and predictability to the network. The protocol is implemented by assigning states to all ports. Each state controls a port's functionality, limiting its ability to receive and transmit frames and learn addresses.

Establishing a spanning tree is done through the exchange of BPDUs between bridge entities. BPDUs are frequently exchanged between neighboring bridges. These frames are identified by the Bridge protocol address range (DMAC = 01-80-C2-00-00-0x).

When there is a change in the network topology, the protocol reconfigures the port states.

Figure 49 • **Spanning Tree Example**



The following table lists the Rapid Spanning Tree port state properties.

Table 129 • **RSTP Port State Properties**

State	BPDU Reception	BPDU Generation	Frame Forwarding	SMAC Learning
Discarding	Yes	Yes	No	No
Learning	Yes	Yes	No	Yes
Forwarding	Yes	Yes	Yes	Yes

The legacy STP states disabled, blocking, and listening correspond to the discarding state of RSTP.

All frames with a Bridge protocol address must be redirected to the CPU. This is configured in CPU_FWD_BPDU_CFG. BPDUs are forwarded to the CPU irrespective of the port's RSTP state. CPUQ_8021_CFG.CPUQ_BPDU_VAL can be used to configure in which CPU extraction queue the BPDUs are placed. BPDU generation is done through frame injection from the CPU.

Frame forwarding is controlled through ingress filtering and egress filtering. Ingress filtering can be done by using the source masks (PGID[80-106]), and egress filtering can be done by using the aggregation masks (PGID[64-79]). Forwarding can be disabled for ports not in the Forwarding state by clearing their source masks and excluding them from all aggregation masks. The use of the aggregation masks for egress filtering does not preclude the combination of link aggregation and RSTP support. All ports in a link aggregation group that are not in the Forwarding state must be disabled in all aggregation masks. For link aggregated ports in the Forwarding state, the aggregation masks must be configured for link aggregation (such as when RSTP is not supported.)

Learning can be enabled per port with the PORT_CFG.LEARN_ENA.

The following table provides an overview of the port state configurations for port p.

Table 130 • **RSTP Port State Configuration for Port p**

State	CPU_FWD_BPDU_CFG[p].BPDU_REDIR_ENA[0]	PGID[80+p]	PGID[64-79], All 16 Masks, Bit p	PORT_CFG[p].LEARN_ENA
Discarding	1	0	0	0
Learning	1	0	0	1
Forwarding	1	1 except for bit p	1	1

6.4.6.1.1 RSTP Example

Situation:

Port 0 is in the RSTP Discarding state. Port 2 is in the RSTP Learning state. Port 3 is in the RSTP Forwarding state. All other ports on the switch are unused.

Resolution:

```
# Get Spanning Tree Protocol BDPUs to CPU extraction queue 0 for port 0, 2,
and 3.
CPU_FWD_BPDU_CFG[0].BPDU_REDIR_ENA[0] = 1
CPU_FWD_BPDU_CFG[2].BPDU_REDIR_ENA[0] = 1
CPU_FWD_BPDU_CFG[3].BPDU_REDIR_ENA[0] = 1
CPUQ_8021_CFG.CPUQ_BPDU_VAL[0] = 0
# Configure the source mask for port 0 (Discarding state).
PGID[80] = 0x00
# Configure the source mask for port 2 (Learning state).
PGID[82] = 0x00
# Configure the source mask for port 3 (Forwarding state).
PGID[83] = 0x77
# Configure the aggregation masks to only allow forwarding to port 3
# (Forwarding state).
PGID[64-79] = 0x08
# Configure the learn mask to only allow learning on ports
# 2 (Learning state) and 3 (Forwarding state).
PORT_CFG[0].LEARN_ENA = 0
PORT_CFG[2].LEARN_ENA = 1
PORT_CFG[3].LEARN_ENA = 1
```

6.4.6.2 Multiple Spanning Tree Protocol

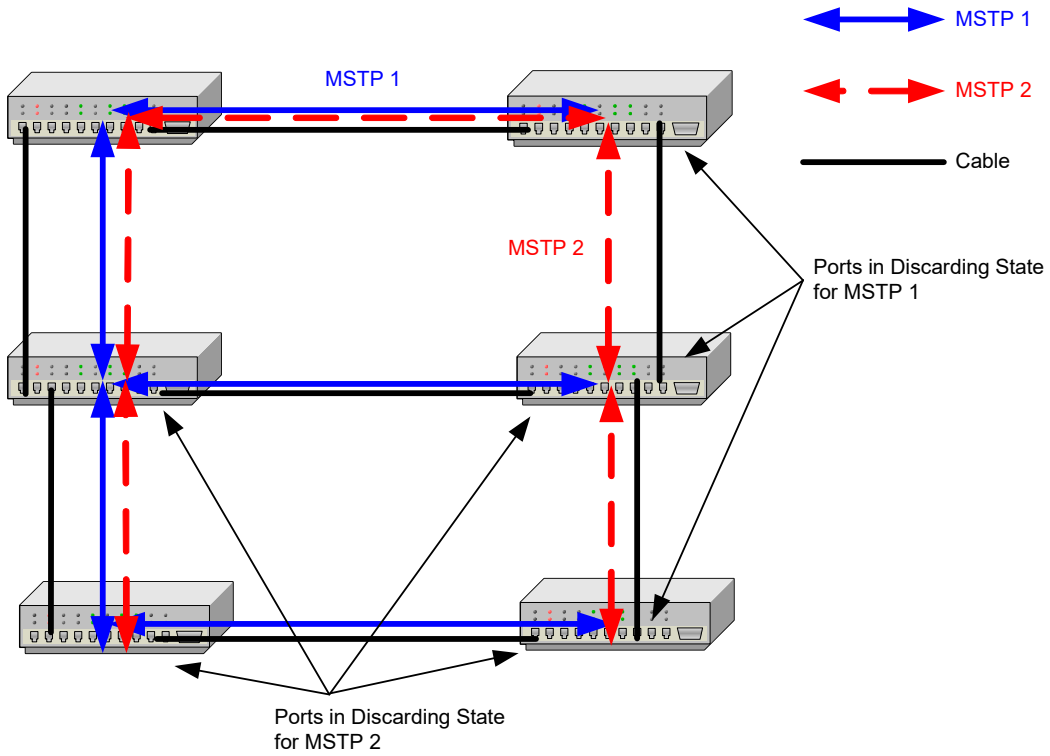
The following table lists the analyzer configuration registers for Multiple Spanning Tree Protocol (MSTP) operation.

Table 131 • **Analyzer Configurations for MSTP Support**

Register/Register Field	Description	Replication
VLANACCESS.VLAN_SRC_CHK	Per-VLAN ingress filtering enable. Part of VLAN table command for indirect access to configuration of the 4095 VLANs	None
VLANMASK	Per-port VLAN ingress filtering enable	None
ADVLEARN.VLAN_CHK	Disable learning for frames discarded due to VLAN membership source port filtering	None
PORT_CFG.LEARN_ENA	Enable learning per port	Per port
CPU_FWD_BPDU_CFG	Enable redirection of frames with reserved BPDU DMAC addresses	Per port per address
CPUQ_8021_CFG.CPUQ_BPDU_VAL	CPU extraction queue for redirected BPDU frames	Per address

The Multiple Spanning Tree Protocol (MSTP) in IEEE 802.1Q increases network use, relative to RSTP, by creating multiple spanning trees that VLANs can map to independently, rather than having only one path between bridges common for all VLANs. The multiple spanning trees are created by assigning different bridge identifiers for each spanning tree. Mapping the VLANs to spanning trees is done arbitrarily.

Figure 50 • **Multiple Spanning Tree Example**



The Learning state is not supported for MSTP. However, this has limited impact, because when the port is taken to the Forwarding state, learning is done at wire-speed, and, as a result, the SMAC learn delay is less important. MSTP is supported for all VLANs.

The following table lists the multiple spanning tree port state properties.

Table 132 • **MSTP Port State Properties**

State per VLAN	BPDU Reception	BPDU Generation	Frame Forwarding	SMAC Learning
Discarding	Yes	Yes	No	No
Learning (not supported)	Yes	Yes	No	Yes
Forwarding	Yes	Yes	Yes	Yes

To enable the MSTP port states:

- Ensure that the switch is VLAN-aware. For more information, see Standard VLAN Operation, page 134.
- Set the ADVLEARN.VLAN_CHK bit to prevent learning of frames discarded due to VLAN ingress filtering.
- Configure all ports as defined for the forwarding state of the RSTP port. For more information, see Table 130, page 148.

Port states per VLAN are hereafter solely configured through the VLAN masks as listed in the following table for port p and VLAN v.

Table 133 • **MSTP Port State Configuration for Port p and VLAN v**

State	VLAN_ACCESS. VLAN_SRC_CHKVLAN v	VLAN_ACCESS. VLAN_PORT_MASK Bit p, VLAN v
Discarding	1	0
Learning	Not supported	Not supported
Forwarding	1	1

As an alternative to setting the VLANACCESS.VLAN_SRC_CHK bit in all VLAN entries in the VLAN table, VLAN ingress filtering can be enabled globally for all VLANs on a per port basis through VLANMASK.

For all multiple spanning tree instances, BPDUs are forwarded to the CPU irrespective of the port states.

6.4.6.2.1 MSTP Example

Situation:

Ports 10 and 11 are both members of VLANs 20 and 21. Two spanning trees are used:

- Spanning tree for VLAN 20, where both ports 10 and 11 are in the Forwarding state
- Spanning tree for VLAN 21, where port 10 is in the Discarding state and port 11 is in the Forwarding state

All other ports on the switch are unused.

Resolution:

```
# Get all BDPUs to CPU queue 0.
CPU_FWD_BPDU_CFG[*].BPDU_REDIR_ENA[0] = 1
CPUQ_8021_CFG.CPUQ_BPDU_VAL[0] = 0
# Enable learning on all ports. The VLAN table controls forwarding and
learning.
PORT::PORT_CFG.LEARN_ENA = 1
# Disable learning of VLAN membership source port filtered frames.
ADVLEARN.VLAN_CHK = 1
```

```
# Configure VLAN 20 for ports 10 and 11 in Forwarding state.
VLANTIDX.INDEX = 20
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 1
VLANACCESS.VLAN_PORT_MASK = 0x00000C00
VLANACCESS.VLAN_TBL_CMD = 2
# Configure VLAN 21 for port 10 in Discarding state and port 11 in Forwarding
state.
VLANTIDX.INDEX = 21
VLANTIDX.VLAN_PRIV_VLAN = 0
VLANTIDX.VLAN_MIRROR = 0 (don’t care, for this example)
VLANTIDX.VLAN_LEARN_DISABLE = 0
VLANTIDX.VLAN_SRC_CHK = 1
VLANACCESS.VLAN_PORT_MASK = 0x00000800
VLANACCESS.VLAN_TBL_CMD = 2
```

6.4.7 IEEE 802.1X: Network Access Control

IEEE 802.1X Port-Based Network Access Control provides a standard for authenticating and authorizing devices attached to a LAN port.

Generally, IEEE 802.1X is port-based; however, the devices also support MAC-based network access control.

This section provides information about the configuration settings for port-based and MAC-based network access control.

6.4.7.1 Port-Based Network Access Control

The following table lists the configuration settings that are required for port-based network access control.

Table 134 • **Configurations for Port-Based Network Access Control**

Register/Register Field	Description/Value	Replication
ANA::CPU_FWD_BPDU_CFG.BPDU_REDIR_ENA[3]	Must be set to 1 to redirect frames with destination MAC addresses 01-80-C2-00-00-03 to the CPU Port Module. IEEE 802.1X uses MAC address 01-80-C2-00-00-03.	Per port
ANA::CPUQ_8021_CFG.CPUQ_BPDU_VAL[3]	Queue to which authentication BPDUs are redirected.	None
ANA::PGID[64-79]	When a port is not yet authenticated, any forwarding of frames to the port can be disabled by clearing the port’s bit in all 16 aggregation masks. After authenticated, these bits must be set.	16

Table 134 • **Configurations for Port-Based Network Access Control *(continued)***

Register/Register Field	Description/Value	Replication
ANA::PGID[80-106]	Source masks. When a port is not yet authenticated, any forwarding of frames received on the port must be disabled. This can be done by setting the ANA::PGID[80+port] to all-zeros. After authenticated, the port's source mask must be set back to its normal value.	Per port

The configuration settings required for port-based network access control enable the following functionality:

- Redirects frames with DMAC 01-80-C2-00-00-03 to CPU, even if the port is not yet authenticated.
- Stops forwarding of frames to ports that are not yet authenticated. This is configured in ANA::PGID[64-79].
- Stops forwarding of frames received on ports that are not yet authenticated. This is configured in ANA::PGID[80-106].

6.4.7.2 MAC-Based Authentication with Secure CPU-Based Learning

The following table lists the configuration settings required for MAC-based network access control with secure CPU-based learning.

Table 135 • **Configurations for MAC-Based Network Access Control with Secure CPU-Based Learning**

Register/Register Field	Description/Value	Replication
ANA:PORT:CPU_FWD_BPDU_CFG.BPDU_REDIR_ENA[3]	Must be set to 1 to redirect frames with destination MAC addresses 01-80-C2-00-00-03 to the CPU Port Module. IEEE 802.1X uses MAC address 01-80-C2-00-00-03.	Per port
ANA::CPUQ_8021_CFG.CPUQ_BPDU_VAL[3]	Queue to which authentication BPDUs are redirected.	None
ANA:PORT:PORT_CFG.LEARN_ENA ANA:PORT:PORT_CFG.LEARNCPU ANA:PORT:PORT_CFG.LEARNDROP ANA:PORT:PORT_CFG.LEARNAUTO	Must be set to support secure CPU-based learning. See Address Learning, page 132. PORT_CFG.LEARN_ENA = 1 PORT_CFG.LEARNCPU = 1 PORT_CFG.LEARNDROP = 1 PORT_CFG.LEARNAUTO = 0	Per port

The MAC-based network access control with secure CPU-based learning enables the following functionality:

- Redirects frames with DMAC 01-80-C2-00-00-03 to CPU.
- Only frames from known, authenticated MAC addresses are forwarded to other ports.
- Frames from unknown MAC addresses are redirected to CPU for authentication. After the address is authenticated, the CPU must insert an entry in the MAC table. The authentication process may be initiated from the CPU when receiving learn frames.

6.4.7.3 MAC-Based Authentication with No Learning

The following table lists the configuration settings required for MAC-based network access control with no learning.

Table 136 • **Configurations for MAC-Based Network Access Control with No Learning**

Register/Register Field	Description/Value	Replication
ANA:PORT:CPU_FWD_BPDU_CFG .BPDU_REDIR_ENA[3]	Must be set to 1 to redirect frames with destination MAC addresses 01-80-C2-00-00-03 to the CPU Port Module. IEEE 802.1X uses MAC address 01-80-C2-00-00-03.	Per port
ANA::CPUQ_8021_CFG.CPUQ_BPDU_VAL[3]	Queue to which authentication BPDUs are redirected.	None
ANA:PORT:PORT_CFG.LEARN_ENA ANA:PORT:PORT_CFG.LEARNCPU ANA:PORT:PORT_CFG.LEARNDROP ANA:PORT:PORT_CFG.LEARNAUTO	Must be set to support no learning. See Address Learning, page 132. PORT_CFG.LEARN_ENA = 1 PORT_CFG.LEARNCPU = 1 PORT_CFG.LEARNDROP = 1 PORT_CFG.LEARNAUTO = 0	None

The MAC-based network access control with no learning enables the following functionality:

- Frames with DMAC 01-80-C2-00-00-03 are redirected to CPU. Unauthenticated and unauthorized devices must initiate an 802.1X session by sending 802.1X BPDUs (MAC address: 01-80-C2-00-00-03). After the address is authenticated, the CPU must insert an entry in the MAC table.
- Only frames from known, authenticated MAC addresses are forwarded to other ports.
- Frames from unknown MAC addresses are discarded and the CPU can therefore not initiate the authentication process.

6.4.8 Link Aggregation

Link aggregation bundles multiple ports (member ports) together into a single logical link. It is primarily used to increase available bandwidth without introducing loops in the network and to improve resilience against faults. A link aggregation group (LAG) can be established with individual links being dynamically added or removed. This enables bandwidth to be incrementally scaled based on changing requirements. A link aggregation group can be quickly reconfigured if faults are identified.

Frames destined for a LAG are sent on only one of the LAG's member ports. The member port on which a frame is forwarded is determined by a 4-bit aggregation code (AC) that is calculated for the frame.

The aggregation code ensures that frames belonging to the same frame flow (for example, a TCP connection) are always forwarded on the same LAG member port. For that reason, reordering of frames within a flow is not possible. The aggregation code is based on the following information:

- SMAC
- DMAC
- Source and destination IPv4 address.
- Source and destination TCP/UDP ports for IPv4 packets
- Source and destination TCP/UDP ports for IPv6 packets
- IPv6 Flow Label

For best traffic distribution among the LAG member ports, enable all six contributions to the aggregation code.

Each LAG can consist of up to 16 member ports. Any quantity of LAGs may be configured for the device (only limited by the quantity of ports on the device.) To configure a proper traffic distribution, the ports within a LAG must use the same link speed.

A port cannot be a member of multiple LAGs.

6.4.8.1 Link Aggregation Configuration

The following table lists the registers associated with link aggregation groups.

Table 137 • **Link Aggregation Group Configuration Registers**

Register/Register Field	Description/Value	Replication
ANA::PGID[0 – 63]	Destination mask	64
ANA::PGID[80 – 106]	Source mask.	Per port
ANA::PGID[64 – 79]	Aggregation mask.	16
ANA::PORT_CFG.PORTID_VAL	Logical port number. Must be set to the same value for all ports that are part of a given LAG; for example, the lowest port number that is a member of the LAG.	Per port
ANA::AGGR_CFG.AC_IP6_FLOW_LBL_ENA	Use IPv6 flow label when calculating AC. Configure identically for all ports. Recommended value is 1.	None
ANA::AGGR_CFG.AC_SIPDIP_ENA	Use IPv4 source and destination IP address when calculating aggregation code. Configure identically for all ports. Recommended value is 1.	None
ANA::AGGR_CFG.AC_TCPUDP_PORT_ENA	Use IPv4 TCP/UDP port when calculating aggregation code. Configure identically for all ports. Recommended value is 1.	None
ANA:: AGGR_CFG.AC_DMAC_ENA	Use destination MAC address when calculating aggregation code. Configure identically for all ports. Recommended value is 1.	None
ANA:: AGGR_CFG.AC_SMAC_ENA	Use source MAC address when calculating aggregation code. Configure identically for all ports. Recommended value is 1.	None
ANA:: AGGR_CFG.AC_RND_ENA	Use random aggregation code. Recommended value is 0.	None

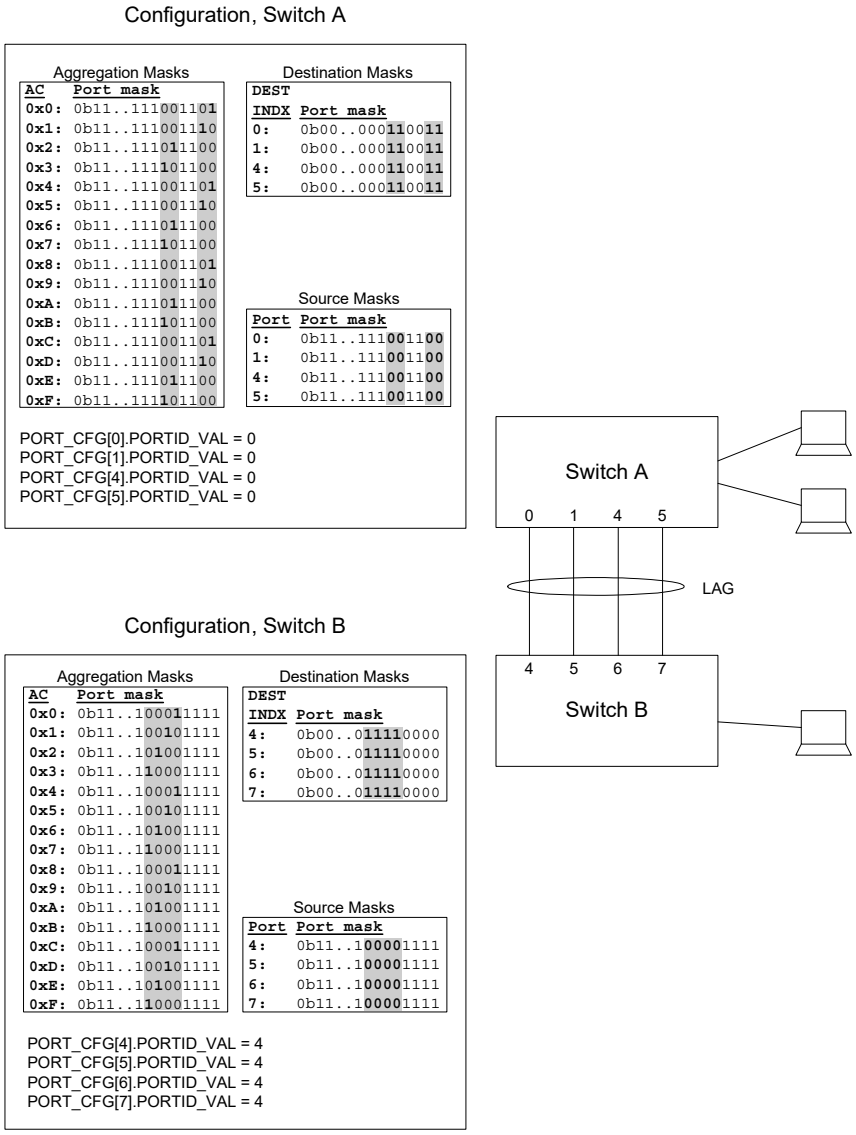
To set up a link aggregation group, the following destination masks, source masks, and aggregation masks must be configured:

- **Destination Masks: ANA::PGID[0-63]** — For each of the member ports, the corresponding destination mask must be configured to include all member ports of the LAG.
- **Source Masks: ANA::PGID[80-106]** — The source masks must be configured to avoid flooding frames that are received at one member port back to another member port of the LAG. As a result, the source masks for each of the member ports must be configured to exclude all of the LAG's member ports.

- **Aggregation Masks: ANA::PGID[64-79]** — The aggregation masks must be configured to ensure that when a frame is destined for the LAG, it gets forwarded to exactly one of the LAG's member ports. Also, the distribution of traffic between member ports is determined by this configuration.

The following illustration shows an example of a LAG configuration.

Figure 51 • **Link Aggregation Example**



In this example, ports 0, 1, 4, and 5 of switch A are configured as a LAG. These ports are connected to 4 ports (4, 5, 6, 7) of switch B, providing an aggregated bandwidth of 4 Gbps between the two switches.

The aggregation masks for switch A are configured such that frames (destined for the LAG) are distributed on the member ports as follows:

- Port 0 if frame's aggregation code (AC) is 0x0, 0x4, 0x8, 0xC
- Port 1 if frame's aggregation code (AC) is 0x1, 0x5, 0x9, 0xD
- Port 4 if frame's aggregation code (AC) is 0x2, 0x6, 0xA, 0xE
- Port 5 if frame's aggregation code (AC) is 0x3, 0x7, 0xB, 0xF

6.4.8.2 Link Aggregation Control Protocol (LACP)

LACP allows switches connected to each other to automatically discover if any ports are member of the same LAG.

To implement LACP, any LACP frames must be redirected to the CPU. Such frames are identified by the DMAC being equal to 01-80-C2-00-00-02 (Slow Protocols Multicast address).

The following table lists the registers associated with configuring the redirection of LACP frames to the CPU.

Table 138 • **Configuration Registers for LACP Frame Redirection to the CPU**

Register/Register Field	Description/Value	Replication
ANA::CPU_FWD_BPDU_CFG.BPDU_REDIR_ENA[2]	Must be set to 1.	Per port

6.4.9 Simple Network Management Protocol (SNMP)

This section provides information about the port module registers and the analyzer registers for SNMP operation.

The following table lists the system registers for SNMP operation.

Table 139 • **System Registers for SNMP Support**

Register	Description	Replication
CNT	The value of the counter. For more information about how to read counters, see Statistics, page 33.	None

The following table lists the analyzer registers for SNMP support.

Table 140 • **Analyzer Registers for SNMP Support**

Register	Description	Replication
MACACCESS	Command register for indirect MAC table access. Supports GET_NEXT command	None
MACHDATA	High part of data word when accessing MAC table.	None
MACLDATA	Low part of data word when accessing MAC table.	None
MACTINDX	Index for direct-mode access to MAC table.	None

For SNMP support according to IETF RFC 1157, use the following features:

- RMON counters
- MAC table GET_NEXT function

For more information about the supported RMON counters, see Port Counters, page 128.

For more information about the MAC table GET_NEXT function, see Table 29, page 50.

6.4.10 Mirroring

To debug network problems, selected traffic can be copied, or mirrored, to a mirror port where a frame analyzer can be attached to analyze the frame flow.

The traffic to be copied to the mirror port can be selected as follows:

- All frames received on a given port (also known as ingress mirroring)
- All frames transmitted on a given port (also known as egress mirroring
- All frames classified to specific VIDs
- All frames sent to the CPU (may be useful for software debugging)
- Frames where the source MAC address is to be learned (also known as learn frame), which may be useful for software debugging

The mirror port may be any port on the device, including the CPU.

6.4.10.1 Mirroring Configuration

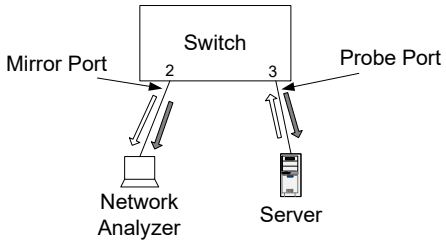
The following table lists configuration registers associated with mirroring.

Table 141 • **Configuration Registers for Mirroring**

Register/Register Field	Description/Value	Replication
ANA::PORT_CFG.SRC_MIRROR_ENA	If set, all frames received on this port are mirrored to the port set configured in MIRRORPORTS, that is, ingress mirroring.	Per port
ANA:: EMIRRORPORTS	Frames forwarded to ports in this mask are mirrored to the port set configured in MIRRORPORTS, that is, egress mirroring.	Per port
ANA::VLANTIDX.VLAN_MIRROR	If set, all frames classified to this VLAN are mirrored to the port set configured in MIRRORPORTS.	One per VID
ANA::AGENCTRL.MIRROR_CPU	Frames destined for the CPU extraction queues are also forwarded to the port set configured in MIRRORPORTS.	None
ANA::MIRRORPORTS	The mirror ports. Usually only one mirror port is configured, that is, only one bit is set in this mask.	None
ANA::CPUQ_CFG.CPUQ_MIRROR	CPU extraction queue used, if CPU is included in MIRRORPORTS.	None
ANA::ADVLEARN.LEARN_MIRROR	Learn frames are also forwarded to ports marked in MIRRORPORTS.	None

The following illustration shows a port mirroring example.

Figure 52 • **Port Mirroring Example**



All traffic to and from the server on port 3 (the probe port) is mirrored to port 2 (the mirror port). Note that the mirror port may become congested, because both the Rx frames and Tx frames on the probe port become Tx frames on the mirror port. The following mirror configuration is required:

ANA::PORT_CFG[3].SRC_MIRROR_ENA = 1
ANA::EMIRRORPORTS[3] = 1
ANA::MIRRORPORTS = 0x0000004

In addition to the mirror configuration settings, the egress configuration of the mirror port (port 2) must be configured identically to the egress configuration of the probe port (port 3). This is to ensure that VLAN

tagging and DSCP remarking at the mirror port is performed consistently with that of the probe port, such that the frame copies at the mirror port are identical to the original frames on the probe port.

Multiple mirror conditions, such as mirror multiple probe ports, VLANs, and so on, can be enabled concurrently to the same mirror port. However, in such configurations, it may not be possible to configure the egress part of the mirror port to perform tagging and DSCP remarking consistent with that of the original frame.

6.5 IGMP and MLD Snooping

This section provides information about the features and configurations related to Internet Group Management Protocol (IGMP) and Multicast Listener Discovery (MLD) snooping.

By default, Layer-3 multicast data traffic is flooded in a Layer-2 network in the broadcast domain spanned by the VLAN. This causes unnecessary traffic in the network and extra processing of unsolicited frames in hosts not listening to the multicast traffic. IGMP and MLD snooping enables a Layer-2 switch to listen to IGMP and MLD conversations between host and routers. The switch can then prune multicast traffic from ports that do not have a multicast listener, and as a result, do not need a copy of the multicast frame. This is done by managing the multicast group addresses and the associated port masks.

IGMP is used to manage IPv4 multicast memberships, and MLD is used to manage IPv6 multicast memberships.

The devices support IGMPv2 and MLDv1. IGPMv2 and MLDv1 use any-source multicasting (ASM), where the multicast listener joins a group and can receive the multicast traffic from any source.

The support in the devices is two-fold:

- Control plane: IGMP and MLD frames are redirected to the CPU. This enables the CPU to listen to the queries and reports.
- Data plane: By monitoring the multicast group registrations and de-registrations signaled through the IGMP and MLD frames, the CPU can setup multicast group addresses and associated ports.

6.5.1 IGMP and MLD Snooping Configuration

To implement IGMP and MLD snooping, any IGMP or MLD frames must be redirected to the CPU. For information about by the conditions by which such frames are identified, see CPU Forwarding Determination, page 46. IGMP and MLD frames can be independently snooped and assigned individual CPU extraction queues.

The following table lists the registers associated with configuring the redirection of IGMP and MLD frames to the CPU.

Table 142 • **Configuration Registers for IGMP and MLD Frame Redirection to CPU**

Register/Register Field	Description/Value	Replication
ANA::CPU_FWD_CFG.IGMP_REDIR_ENA	Must be set to 1 to redirect IGMP frames to the CPU	Per port
ANA::CPU_FWD_CFG.MLD_REDIR_ENA	Must be set to 1 to redirect MLD frames to the CPU	Per port
ANA::CPUQ_CFG.CPUQ_IGMP	CPU extraction queue for IGMP frames	None
ANA::CPUQ_CFG.CPUQ_MLD	CPU extraction queue for MLD frames	None

6.5.2 IP Multicast Forwarding Configuration

The following table lists the registers associated with configuring the multicast group addresses and the associated ports.

Table 143 • **IP Multicast Configuration Registers**

Register/Register Field	Description/Value	Replication
MACHDATA	MAC address and VID when accessing the MAC table.	None
MACLDATA	MAC address when accessing the MAC table.	None
MACTINDX	Direct address into the MAC table for direct read and write.	None
MACACCESS	Flags and command when accessing the MAC table.	None
MACTOPTIONS	Flags when accessing the MAC table	None
FLOODING_IPMC	Index into the PGID table used for flooding of IPv4/6 multicast control and data frames.	None
PGID[63:0]	Destination and flooding masks table	64

IPv4 and IPv6 multicast group addresses are programmed in the MAC table as IPv4 and IPv6 multicast entries. For more information, see MAC Table, page 48. The entry in the MAC table also holds the set of egress ports associated with the group address.

By default, programming an IPv4 or IPv6 multicast entry in the MAC table makes it an any-source multicast, because the actual source IP address is insignificant with respect to forwarding.

The switch provides full control of flooding of unknown IP multicast frames. For more information, see Table 39, page 57. Generally, an IGMP and MLD snooping switch disables flooding of unknown multicast frames, except to ports connecting to multicast routers. Note that unknown IPv4 multicast control frames should be flooded to all ports, because IPv4 is not as strict as IPv6 in terms of registration for IP multicast groups.

6.6 Quality of Service (QoS)

This section discusses features and configurations related to QoS.

The devices include a number of features related to providing low-latency guaranteed services to critical network traffic such as voice and video in contrast to best-effort traffic such as web traffic and file transfers.

All incoming frames are classified to a QoS class, which is used in the queue system when assigning resources, in the arbitration from ingress to egress queues and in the egress scheduler when selecting the next frame for transmission.

The QoS classification enables predefined schemes for handling Priority Code Points (PCP), Drop Eligible Indicator (DEI), and Differentiated Service Code Points (DSCP):

- QoS classification based on PCP and DEI for tagged frames. The mapping table from PCP and DEI to QoS class is programmable per port.
- QoS classification based on DSCP values. Can optionally use only trusted DSCP values. The mapping table from DSCP value to QoS class is common between all ports.
- The devices have the option to work as a DS boundary node connecting two DS domains together by translating incoming/outgoing DSCP values for selected ports.
- The DSCP values can optionally be remarked based on the frame's classified QoS class.
- For untagged or non-IP frames, a default per-port QoS class is programmable.

6.6.1 Basic QoS Configuration

The following table lists the registers associated with configuring basic QoS.

Table 144 • **Basic QoS Configuration Registers**

Register	Description	Replication
ANA:PORT:QOS_CFG	QoS and DSCP configuration	Per port
ANA:PORT:QOS_PCP_DEI_MAP_CFG:	Mapping of DEI and PCP to QoS class and drop precedence level	Per port
ANA::DSCP_CFG	DSCP configuration	Per DSCP

Situation:

Assume a configuration with the following requirements:

- All frames with DSCP=7 must get QoS class 7.
- All frames with DSCP=8 must get QoS class 5.
- DSCP=9 is untrusted and all frames with DSCP=9 should be treated as a non-IP frame.
- VLAN-tagged frames with PCP=7 must get QoS class 7
- All other IP frames must get QoS class 1.
- All other non-IP frames must get QoS class 0.

Solution:

```
# Program overall QoS configuration
QOS_CFG.QOS_DSCP_ENA = 1
QOS_CFG.QOS_PCP_ENA = 1


# Program DSCP trust configuration (“*” = 0 through 63)
DSCP_CFG[*].DSCP_TRUST_ENA = 1
DSCP_CFG[9].DSCP_TRUST_ENA = 0

# Program DSCP QoS configuration (“*” = 0 through 63)
DSCP_CFG[*].QOS_DSCP_VAL = 1
DSCP_CFG[7].QOS_DSCP_VAL = 7
DSCP_CFG[8].QOS_DSCP_VAL = 5

# Program PCP QoS configuration (“*” = 0 through 15)
# Note: both 7 and 15 are programmed in order to don’t care DEI
QOS_PCP_DEI_MAP_CFG[*] = 0
QOS_PCP_DEI_MAP_CFG[7] = 7
QOS_PCP_DEI_MAP_CFG[15] = 7

# Program default QoS class for non-IP, non-tagged frames.
QOS_CFG.QOS_DEFAULT_VAL = 0
```

6.6.2 IPv4 and IPv6 DSCP Remarking

IPv4 and IPv6 packets include a 6-bit Differentiated Services Code Point (DSCP), which switches and routers can use to determine the QoS class of a frame. With a proper value in the DSCP field, packets can be prioritized consistently throughout the network. Compared to QoS classification based on user priority, classification based on DSCP provides two main advantages

- DSCP field is already present in all packets (assuming all traffic is IPv4/IPv6).
- DSCP value is preserved during routing and is therefore better suited for end-to-end QoS signaling.

Some hosts may be able to send packets with an appropriate value in the DSCP field, whereas other hosts may not provide an appropriate value in the DSCP field.

For packets without an appropriate value in the DSCP field, the devices can be configured to write a new DSCP value into the frame, based on the QoS class of the frame. For example, the devices may have determined the QoS class based on the VLAN tag priority information (PCP and DEI). After the packet is transmitted by the egress port, the DSCP field can be rewritten with a value based on the QoS class of the frame. Any subsequent routers or switches can then be easily prioritize the frame, based on the rewritten DSCP value.

The DSCP rewriting functionality available in the devices provide flexible, per-ingress port and per-DSCP-value configuration of whether frames should be subject to DSCP rewrite. If it is determined at the ingress port that the DSCP value should be rewritten and to which value, this is then signaled to the egress ports, where the actual change of the DSCP field is done.

6.6.2.1 DSCP Remarking Configuration

The following table lists the configuration registers associated with DSCP remarking.

Table 145 • **Configuration Registers for DSCP Remarking**

Register/Register Field	Description/Value	Replication
ANA:PORT:DSCP_REWR_CFG	Two-bit DSCP rewrite mode per ingress port: 0x0: No DSCP rewrite. 0x1: Rewrite only if the frame's current DSCP value is zero. 0x2: Rewrite only if the frame's current DSCP value is enabled for remarking in ANA::DSCP_CFG.DSCP_REWR_ENA. 0x3: Rewrite DSCP of all frames, regardless of current DSCP value.	Per ingress port
ANA::DSCP_CFG.DSCP_REWR_ENA	Enables specific DSCP values for rewrite for ports with DSCP rewrite mode set to 0x2.	Per DSCP
ANA::DSCP_REWR_CFG.DSCP_QOS_REWR_VAL	Maps the frame's QoS class to a DSCP value.	Per QoS class
REW::DSCP_CFG.DSCP_REWR_CFG	Enables DSCP rewrite for egress port.	Per egress port
REW::DSCP_REMAP_CFG	Remap table of DSCP values.	None

The configuration related to the ingress port controls whether a frame is to be remarked. For each ingress port, a DSCP rewrite mode is configured in ANA:PORT:DSCP_REWR_CFG. This register defines the four different modes as follows:

- 0x0: No DSCP rewrite, that is, never change the received DSCP value.
- 0x1: Rewrite if DSCP is zero. This may be useful if a DSCP value of zero indicates that the host has not written any value to the DSCP field.
- 0x2: Rewrite selected DSCP values. In ANA::DSCP_CFG.DSCP_REWR_ENA specific DSCP values can be selected for rewrite, for example, if only certain DSCP values are allowed in the network.
- 0x3: Rewrite all DSCP values.

After a frame is selected for DSCP rewrite, based on the configuration for the ingress port, the new DSCP value is determined by mapping the QoS class to a new DSCP value (ANA::DSCP_REWR_CFG.DSCP_QOS_REWR_VAL).

The resulting DSCP value is forwarded to the Rewriter at the egress port, which determines whether to actually write the new DSCP value into the frame (REW::DSCP_CFG.DSCP_REWR_CFG). Optionally, the DSCP value may be translated before written into the frame (REW::DSCP_REMAP_CFG) for applications where the switch acts as an DS boundary node.

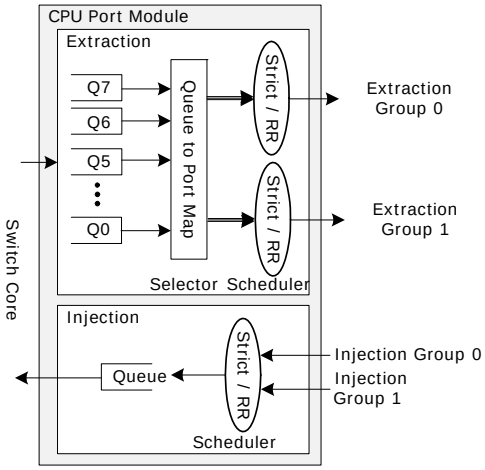
When an IPv4 DSCP is rewritten, the IP header checksum is updated accordingly.

6.7 CPU Extraction and Injection

This section provides information about how the CPU extracts and injects frames to and from the switch core.

The following illustration shows the CPU Port Module used for injection and extraction.

Figure 53 • **CPU Extraction and Injection**



The switch core forwards CPU extracted frames to eight CPU extraction queues. Each of these queue is then mapped to one of two CPU Extraction Groups. For each extraction group there is a scheduler (strict or round robin) which selects between the CPU extraction queues mapped to the same group.

When injecting frames, there are two CPU Injection Groups available where for instance one can be used for the Frame DMA and one can be used for manually injected frames. A scheduler (Strict or round robin) selects between the two injection groups meaning the switch core only sees one stream of frames being injected.

6.7.1 Forwarding to CPU

Several mechanisms can be used to trigger redirection or copying of frames to the CPU. They are listed in the following table.

Table 146 • **Configurations for Redirecting or Copying Frames to the CPU**

Frame Type	Configuration (Including Selection of Extraction Queue)	Redirect or Copy
IEEE 802.1D Reserved Range DMAC = 01-80-C2-00-00-0x	ANA:PORT:CPU_FWD_BPDU_CFG ANA::CPUQ_8021_CFG.CPUQ_BPDU_VAL	Redirect
IEEE 802.1D Allbridge DMAC = 01-80-C2-00-00-10	ANA:PORT: CPU_FWD_CFG.CPU_ALLBRIDGE_REDIR_ENA ANA::CPUQ_CFG.CPUQ_ALLBRIDGE	Redirect
IEEE 802.1D GARP Range DMAC = 01-80-C2-00-00-2x	ANA:PORT:CPU_FWD_GARP_CFG ANA::CPUQ_8021_CFG.CPUQ_GARP_VAL	Redirect
IEEE 802.1D CCM/Link Trace Range DMAC = 01-80-C2-00-00-3x	ANA:PORT:CPU_FWD_CCM_CFG ANA::CPUQ_8021_CFG.CPUQ_CCM_VAL	Redirect
IGMP (IPv4)	ANA:PORT:CPU_IGMP_REDIR_ENA ANA::CPUQ_CFG.CPUQ_IGMP	Redirect
IP Multicast Control (IPv4)	ANA:PORT:CPU_IPMC_CTRL_COPY_ENA ANA::CPUQ_CFG.CPUQ_IPMC_CTRL	Copy

Table 146 • **Configurations for Redirecting or Copying Frames to the CPU *(continued)***

Frame Type	Configuration (Including Selection of Extraction Queue)	Redirect or Copy
MLD (IPv6)	ANA:PORT:CPU_MLD_REDIR_ENA ANA::CPUQ_CFG.CPUQ_MLD	Redirect
CPU-based learning	ANA:PORT:PORT_CFG.LEARNCPU ANA::CPUQ_CFG.CPUQ_LRN	Copy
CPU-based learning of locked MAC table entries seen on a new port	ANA:PORT: PORT_CFG.LOCKED_PORTMOVE_CPU ANA::CPUQ_CFG.CPUQ_LOCKED_PORTMOVE	
CPU-based learning of frames exceeding learn limit in MAC table	ANA:PORT:PORT_CFG.LIMIT_CPU ANA::CPUQ_CFG.CPUQ_LRN	
MAC table match using MAC table	ANA::MACACCESS.MAC_CPU_COPY ANA::CPUQ_CFG.CPUQ_MAC_COPY	Copy
MAC table match using PGID table	ANA::MACACCESS.DEST_IDX ANA::PGID.PGID (bit 26) ANA::PGID.CPUQ_DST_PGID	Redirect or copy
Flooded frames	ANA::MACACCESS.DEST_IDX ANA::PGID.PGID (bit 26) ANA::PGID.CPUQ_DST_PGID	Redirect or copy
Any frame received on selected ports	ANA:PORT:CPU_SRC_COPY_ENA ANA:CPUQ_CFG.CPUQ_SRC_COPY	Copy
Mirroring	ANA::MIRRORPORTS (bit 26) ANA::CPUQ_CFG:CPUQ_MIRROR For more information about mirroring, see Mirroring, page 156.	Copy
SFlow	ANA::CPUQ_CFG.CPUQ_SFLOW For more information about SFlow, see sFlow Sampling, page 62.	Copy

6.7.2 Frame Extraction

The CPU receives frames through the eight CPU extraction queues in the CPU port module. The eight queues are using resources (memory and frame descriptor pointers) from the shared queue system and are subject to the thresholds and congestion rules programmed for the CPU port (port 26) and the shared queue system in general.

Through register access, the CPU can extract frames from the CPU extraction queues. For more information, see Frame Extraction, page 81.

The switch core may place the eight-byte long CPU extraction header before the DMAC or after the SMAC (REW::PORT_CFG.IFH_INSERT_MODE). The CPU extraction header contains relevant side band information about the frame such as the frame's classification result (VLAN tag information, DSCP, or QoS class) and the reason for sending the frame to the CPU. For more information about the contents of the CPU extraction header, see CPU Extraction Header, page 82.

6.7.3 Frame Injection

The CPU can inject frames through the two CPU injection groups. The two groups merge into one injection queue through the injection scheduler (DEVCPU_QS::INJ_GRP_CFG). The injection queue uses resources (memory and frame descriptor pointers) from the shared queue system and is subject to the thresholds and congestion rules programmed for the CPU port (port 26) and the shared queue system in general.

Through register access, the CPU can inject frames to the CPU injection groups. For more information, see Frame Injection, page 83.

The first eight bytes of a frame written into a CPU group is an injection header containing relevant side band information about how the frame must be processed by the switch core. For more information, see Table 66, page 83.

6.7.4 Frame Extraction and Injection Using An External CPU

The following table lists the configuration registers associated with using an external CPU.

Table 147 • **Configuration Registers When Using An External CPU**

Register/Register Field	Description/Value	Replication
SYS::EXT_CPU_CFG.EXT_CPU_PORT	Port number where external CPU is connected.	None
SYS::EXT_CPU_CFG.EXT_CPUQ_MSK	Configures which CPU Extraction Queues are sent to the external CPU.	None
REW::PORT_CFG.IFH_INSERT_ENA	Enables the insertion of the CPU extraction header in egress frames.	Per port
REW::PORT_CFG.IFH_INSERT_MODE	Controls the position of the CPU extraction header.	Per port
SYS::PORT_MODE.INCL_INJ_HDR	Enables ingress port to look for CPU injection header in incoming frames.	Per port

An external CPU can connect up to any front port module and use the Ethernet interface for extracting and injecting frames into the switch core.

Note If an external CPU is connected by means of the serial interface, the frame extraction and injection is performed. For more information, see Frame Extraction, page 163 and Frame Injection, page 163.

When extracting frames, the CPU extraction header can be placed before the DMAC (in the preamble) or after the SMAC (REW::PORT_CFG.IFH_INSERT_MODE). For more information about the contents of the eight-byte long extraction header, see Frame Extraction, page 163.

When injecting frames, the CPU injection header controls whether a frame is processed by the analyzer or forwarded directly to the destination set specified in the injection header. The injection header must be placed before destination MAC address in the frame. For more information about the contents of the eight-byte long injection header, see Frame Injection, page 163.

An internal and external CPU may coexist in a dual CPU system where the two CPUs handles different run-time protocols. When extracting CPU frames, it is selectable which CPU extraction queues are connected to the external CPU and which remain connected to the internal CPU (SYS::EXT_CPU_CFG.EXT_CPUQ_MSK). If a frame is forwarded to the CPU for more than one reason (for example, a BPDU which is also a learn frame), the frame can be forwarded to both the internal CPU extraction queues and to the external CPU.

6.8 Energy Efficient Ethernet

Defined by IEEE 802.3az, Energy Efficient Ethernet (EEE) provides a mechanism for reducing the energy consumption on Ethernet links during times of low utilization. Basically, when the transmission queues on a link are empty, the connecting macros and PHYs can be put into a sleep mode using Low-Power Idles (LPI), where the energy consumption is reduced by turning off unused circuits. When data is ready again for transmission, the macros and PHYs are waked up and data can flow again. The reaction time for bringing the link alive again is in the range of microseconds, so no data is lost due to low-power idles, however, data will experience increased latency.

Both internal PHYs and internal SerDes macros support EEE in both the Rx and Tx direction.

The following table lists configuration registers related to using Energy Efficient Ethernet.

Table 148 • **Configuration Registers When Using Energy Efficient Ethernet**

Register/Register Field	Description/Value	Replication
SYS:PORT:EEE_CFG	Queue system configuration of EEE.	Per port
SYS::EEE_THRESH	EEE thresholds used by queue system.	None
PORT::PCS1G_LPI_CFG	Low power idle configuration for the PCS.	Per SerDes port
PORT::PCS1G_LPI_WAKE_ERROR_CNT	Wake error counter.	Per SerDes port
PORT::PCS1G_LPI_STATUS	Low power idle status.	Per SerDes port
HSIO::SERDES6G_MISC_CFG	Enable LPI in 6G SerDes.	Per SerDes port
IEEE Clause 45 PHY registers	EEE configuration for the internal PHYs.	Per Copper PHY port

Ports with internal copper PHYs support LPI for 100BASE-TX and 1000BASE-T and can also reduce the transmit signal amplitude in a 10BASE-Te mode.

For ports with SerDes, the PCS supports LPI for all modes. When the PCS is in LPI, the connecting SerDes macro is also in LPI.

To enable Energy Efficient Ethernet, configure the following functions:

- Enable the ports for EEE and configure the timers and thresholds in the queue system to determine when the system will attempt to enter the LPI state and how fast it can wake up again.

Enable LPI for the relevant ports in PCS, SerDes macros, and internal PHYs. For more information, see PCS, page 15, SERDES6G, page 18, and Cat5 Twisted Pair Media Interface, page 25.

7 Registers

This section provides information about the programming interface, register maps, register descriptions, and register tables of the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

In writing to registers with reserved bits, use a read-modify-write technique, where the entire register is read, but only the user bits to be changed are modified. Do not change the values of registers and bits marked as reserved. Their read state should not be considered static or unchanging. Unspecified registers and bits must be written to 0 and can be ignored when read.

7.1 Targets and Base Addresses

The following table lists all register targets and associated base addresses for the VSC7420-02, VSC7421-02, and VSC7422-02 devices. The next level lists registers groups and offsets within targets, and the deepest level lists registers within the register groups.

Both register groups and registers may be replicated (repeated) a number of times. The repeat-count and the distance between two repetitions is listed in the “Instances and Address Spacing” column of the tables. If there is only one instance, the spacing is omitted. The “Offset within Target”/”Offset within Register Group” columns hold the offset of the first instance of the register group/register.

To calculate the absolute address of a given register, multiply the register group’s replication number by the register group's address spacing and add it to the register group’s offset within the target. Then multiply the register’s replication number with the register’s address spacing and add it to the register’s offset within the register group. Finally, add these two numbers to the absolute address of the target in question.

Table 149 • **List of Targets and Base Addresses**

Target Name	Base Address	Description	Details
DEVCPU_ORG	0x60000000	CPU Device Origin	Page 167
SYS	0x60010000	Switching Engine Configuration	Page 170
ANA	0x60020000	Analyzer Configuration	Page 194
REW	0x60030000	Rewriter Configuration	Page 221
DEVCPU_GCB	0x60070000	CPU Device General Configuration	Page 225
DEVCPU_QS	0x60080000	CPU Device Queue System	Page 257
HSIO	0x600A0000	High Speed I/O SerDes Configuration	Page 264
DEV[0]	0x601E0000	Port Configuration (GMII)	Page 274
DEV[1]	0x601F0000	Port Configuration (GMII)	Page 274
DEV[2]	0x60200000	Port Configuration (GMII)	Page 274
DEV[3]	0x60210000	Port Configuration (GMII)	Page 274
DEV[4]	0x60220000	Port Configuration (GMII)	Page 274
DEV[5]	0x60230000	Port Configuration (GMII)	Page 274
DEV[6]	0x60240000	Port Configuration (GMII)	Page 274
DEV[7]	0x60250000	Port Configuration (GMII)	Page 274
DEV[8]	0x60260000	Port Configuration (GMII)	Page 274
DEV[9]	0x60270000	Port Configuration (GMII)	Page 274
DEV[10]	0x60280000	Port Configuration (GMII/SERDES)	Page 283
DEV[11]	0x60290000	Port Configuration (GMII/SERDES)	Page 283

Table 149 • **List of Targets and Base Addresses *(continued)***

Target Name	Base Address	Description	Details
DEV[12]	0x602A0000	Port Configuration (SERDES)	Page 283
DEV[13]	0x602B0000	Port Configuration (SERDES)	Page 283
DEV[14]	0x602C0000	Port Configuration (SERDES)	Page 283
DEV[15]	0x602D0000	Port Configuration (SERDES)	Page 283
DEV[16]	0x602E0000	Port Configuration (SERDES)	Page 283
DEV[17]	0x602F0000	Port Configuration (SERDES)	Page 283
DEV[18]	0x60300000	Port Configuration (SERDES)	Page 283
DEV[19]	0x60310000	Port Configuration (SERDES)	Page 283
DEV[20]	0x60320000	Port Configuration (SERDES)	Page 283
DEV[21]	0x60330000	Port Configuration (SERDES)	Page 283
DEV[22]	0x60340000	Port Configuration (SERDES)	Page 283
DEV[23]	0x60350000	Port Configuration (SERDES)	Page 283
DEV[24]	0x60360000	Port Configuration (SERDES)	Page 283
DEV[25]	0x60370000	Port Configuration (SERDES)	Page 283
ICPU_CFG	0x70000000	VCore Configuration	Page 305
UART	0x70100000	VCore UART Configuration	Page 343
TWI	0x70100400	VCore Two-Wire Interface Configuration	Page 355
PHY	MIIM	PHY Configuration	Page 378

7.2 DEVCPU_ORG

Table 150 • **Register Groups in DEVCPU_ORG**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
ORG	0x00000000	1	Origin registers	Page 167

7.2.1 DEVCPU_ORG:ORG

Parent: DEVCPU_ORG

Instances: 1

Table 151 • **Registers in ORG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ERR_ACCESS_DROP	0x00000000	1	Target Module ID is Unknown	Page 168
ERR_TGT	0x00000008	1	Target Module is Busy	Page 168
ERR_CNTS	0x0000000C	1	Error Counters	Page 169

Table 151 • **Registers in ORG *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CFG_STATUS	0x0000001C	1	Configuration and Status Register	Page 169

7.2.1.1 DEVCPU_ORG:ORG:ERR_ACCESS_DROP

Parent: DEVCPU_ORG:ORG

Instances: 1

Table 152 • **Fields in ERR_ACCESS_DROP**

Field Name	Bit	Access	Description	Default
NO_ACTION_STICKY	24	Sticky	Sticky bit that - when set - indicates that at least one request was received by a target, but the target did not do anything with it (Eg. access to a non existing register) '0': No errors occurred. '1': At least one request was received with no action.	0x0
TGT_MODULE_NO_ACTION_STICKY	23:16	R/O	Target Module ID. When the sticky_no_action bit is set, this field holds the ID of the last target that received a request that didn't resolve in an action. 0x01 : Module id 1 0xFF : module id 255	0x00
UTM_STICKY	8	Sticky	Sticky bit that - when set - indicates that at least one request for an unknown target module has been done. '0': No errors occurred. '1': At least one request to an unknown target has been done.	0x0
TGT_MODULE_UTM_STICKY	7:0	R/O	Target Module ID. When the sticky_utm bit is set, this field holds the ID of the last target that was unknown. 0x01 : Module id 1 0xFF : module id 255	0x00

7.2.1.2 DEVCPU_ORG:ORG:ERR_TGT

Parent: DEVCPU_ORG:ORG

Instances: 1

Write all ones to this register to clear it.

Table 153 • **Fields in ERR_TGT**

Field Name	Bit	Access	Description	Default
BSY_STICKY	8	Sticky	Sticky bit that - when set - indicates that at least one request was not processed because the target was busy. '0': No error has occurred '1': A least one request was dropped due to that the target was busy.	0x0
TGT_MODULE_BSY	7:0	R/O	Target Module ID. When the sticky_bsy bit is set, this field holds the ID of the last target that was unable to process a request. 0x01 : Module id 1 0xFF : Module id 255	0x00

7.2.1.3 DEVCPU_ORG:ORG:ERR_CNTS

Parent: DEVCPU_ORG:ORG

Instances: 1

Table 154 • **Fields in ERR_CNTS**

Field Name	Bit	Access	Description	Default
NO_ACTION_CNT	31:24	R/W	No action Counter. Counts the number of requests that were not processed by the Target Module, because the target did not know what to do (e.g. access to a non-existing register). This counter saturates at max.	0x00
UTM_CNT	23:16	R/W	Unknown Target Counter. Counts the number of requests that were not processed by the Target Module, because the target was no found. This counter saturates at max.	0x00
BUSY_CNT	15:8	R/W	Busy Counter. Counts the number of requests that were not processed by the Target Module, because it was busy. This may be because the Target Module was waiting for access to/from its host. This counter saturates at max.	0x00

7.2.1.4 DEVCPU_ORG:ORG:CFG_STATUS

Parent: DEVCPU_ORG:ORG

Instances: 1

Table 155 • **Fields in CFG_STATUS**

Field Name	Bit	Access	Description	Default
RD_ERR_STICKY	1	Sticky	If a new read access is initialized before the previous read access has completed this sticky bit is set. Both the 1st and 2nd read access will be handled, but the 2nd access will overwrite data from the 1st access. '0': A read access that has been initialized before the previous read access had completed has never occurred. '1': At least one time a read access has been initialized before the previous read access had completed.	0x0
ACCESS_IN_PROGRESS	0	R/O	When set a access is in progress. '0': No access is in progress. '1': A access is in progress.	0x0

7.3 SYS

Table 156 • **Register Groups in SYS**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
SYSTEM	0x000081B0	1	Switch Configuration	Page 171
SCH	0x0000845C	1	Scheduler registers	Page 178
SCH_LB	0x00003800	1	Scheduler leaky bucket registers	Page 182
RES_CTRL	0x00004000	1024 0x00000008	Watermarks and status for egress queue system	Page 183
PAUSE_CFG	0x000085A4	1	Watermarks for egress queue system	Page 185
MMGT	0x000037A0	1	Memory manager status	Page 187
MISC	0x000037AC	1	Miscellaneous	Page 188
STAT	0x00000000	3558 0x00000004	Frame statistics	Page 189
POL	0x00006000	256 0x00000020	General policer configuration	Page 190
POL_MISC	0x00008704	1	Flow control configuration	Page 192
ISHP	0x00008000	27 0x00000010	Ingress shaper configuration	Page 193

7.3.1 SYS:SYSTEM

Parent: SYS

Instances: 1

Table 157 • **Registers in SYSTEM**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RESET_CFG	0x00000000	1	Core reset control	Page 171
VLAN_ETYPE_CFG	0x00000008	1	S-tag Ethernet Type	Page 172
PORT_MODE	0x0000000C	28 0x00000004	Per device port configuration	Page 172
FRONT_PORT_MODE	0x0000007C	26 0x00000004	Various Ethernet port configurations	Page 173
SWITCH_PORT_MODE	0x000000E4	27 0x00000004	Various switch port mode settings	Page 173
FRM_AGING	0x00000150	1	Configure Frame Aging	Page 173
STAT_CFG	0x00000154	1	Statistics configuration	Page 174
EEE_CFG	0x00000158	26 0x00000004	Control Energy Efficient Ethernet operation per front port.	Page 174
EEE_THRES	0x000001C0	1	Thresholds for delayed EEE queues	Page 175
IGR_NO_SHARING	0x000001C4	1	Control shared memory users	Page 176
EGR_NO_SHARING	0x000001C8	1	Control shared memory users	Page 176
SW_STATUS	0x000001CC	27 0x00000004	Various status info per switch port	Page 176
EQ_TRUNCATE	0x00000238	27 0x00000004	Truncate frames in queue	Page 177
EQ_PREFER_SRC	0x000002A4	1	Precedence for source ports	Page 177
EXT_CPU_CFG	0x000002A8	1	External CPU port configuration	Page 177

7.3.1.1 SYS:SYSTEM:RESET_CFG

Parent: SYS:SYSTEM

Instances: 1

Controls reset and initialization of the switching core. Proper startup sequence is:

- Enable memories

- Initialize memories

- Enable core

Table 158 • **Fields in RESET_CFG**

Field Name	Bit	Access	Description	Default
CORE_ENA	2	R/W	Switch core is enabled when this field is set.	0x0
MEM_ENA	1	R/W	Core memory controllers are enabled when this field is set.	0x0
MEM_INIT	0	One-shot	Initialize core memories. Field is automatically cleared when operation is complete (approx. 40 us).	0x0

7.3.1.2 SYS:SYSTEM:VLAN_ETYPE_CFG

Parent: SYS:SYSTEM

Instances: 1

Table 159 • **Fields in VLAN_ETYPE_CFG**

Field Name	Bit	Access	Description	Default
VLAN_S_TAG_ETYPE_VAL	15:0	R/W	Custom Ethernet Type for S-tags. Tags with TPID = 0x88A8 are always recognized as S-tags.	0x88A8

7.3.1.3 SYS:SYSTEM:PORT_MODE

Parent: SYS:SYSTEM

Instances: 28

These configurations exists per frontport and for each of the two CPU ports (26+27).

Table 160 • **Fields in PORT_MODE**

Field Name	Bit	Access	Description	Default
RESERVED	4:3	R/W	Must be set to its default.	0x2
L3_PARSE_CFG	2	R/W	Enable frame analysis on Layer-3 and Layer-4 protocol information. If cleared, all frames are seen as non-IP and are handled accordingly. This affects all blocks using IP information such as classification, IP flooding, IP forwarding, and DSCP rewriting.	0x1
DEQUEUE_DIS	1	R/W	Disable dequeuing from the egress queues. Frames are not discarded, but may become aged when dequeuing is re-enabled.	0x0
INCL_INJ_HDR	0	R/W	Enable parsing of 64-bit injection header, which must be prepended all frames received on this port.	0x0

7.3.1.4 SYS:SYSTEM:FRONT_PORT_MODE

Parent: SYS:SYSTEM

Instances: 26

Table 161 • **Fields in FRONT_PORT_MODE**

Field Name	Bit	Access	Description	Default
HDX_MODE	0	R/W	Enables the queue system to support the half duplex mode. Must be set for a port when enabled for half-duplex mode (MAC_MODE_ENA.FDX_ENA cleared).	0x0

7.3.1.5 SYS:SYSTEM:SWITCH_PORT_MODE

Parent: SYS:SYSTEM

Instances: 27

Table 162 • **Fields in SWITCH_PORT_MODE**

Field Name	Bit	Access	Description	Default
PORT_ENA	3	R/W	Enable port for any frame transfer. Frames to or from a port with PORT_ENA cleared are discarded.	0x0
RESERVED	2	R/W	Must be set to its default.	0x1
RESERVED	1	R/W	Must be set to its default.	0x1

7.3.1.6 SYS:SYSTEM:FRM_AGING

Parent: SYS:SYSTEM

Instances: 1

Table 163 • **Fields in FRM_AGING**

Field Name	Bit	Access	Description	Default
MAX_AGE	31:0	R/W	Frames are aged and removed from the queue system when the frame's age timer becomes two. The frame age timer is increased for all frames whenever the configured time, MAX_AGE, has passed. The unit is 4 ns. Effectively, this means that a frame is aged when the frame has waited in the queue system between one or two times the period specified by MAX_AGE. A value of zero disables the aging. A value less than 6000 (24 us) is illegal.	0x00000000

7.3.1.7 SYS:SYSTEM:STAT_CFG

Parent: SYS:SYSTEM

Instances: 1

Table 164 • **Fields in STAT_CFG**

Field Name	Bit	Access	Description	Default
RESERVED	10	R/W	Must be set to its default.	0x1
RESERVED	9	R/W	Must be set to its default.	0x1
RESERVED	8	R/W	Must be set to its default.	0x1
RESERVED	7	R/W	Must be set to its default.	0x1
STAT_CLEAR_PORT	5:1	R/W	Select which port to clear counters for.	0x00
STAT_CLEAR_SHOT	0	One-shot	Set STAT_CLEAR_SHOT to clear all counters for the port selected by STAT_CLEAR_PORT port. Auto-cleared when complete (1us).	0x0

7.3.1.8 SYS:SYSTEM:EEE_CFG

Parent: SYS:SYSTEM

Instances: 26

Table 165 • **Fields in EEE_CFG**

Field Name	Bit	Access	Description	Default
EEE_ENA	29	R/W	Enable EEE operation on the port. A port enters the low power mode when no egress queues have data ready. The port is activated when one of the following conditions is true: - A queue has been non-empty for EEE_TIMER_AGE. - A queue has more than EEE_HIGH_FRAMES frames pending. - A queue has more than EEE_HIGH_BYTES bytes pending. - A queue is marked as a fast queue, and has data pending.	0x0
EEE_FAST_QUEUES	28:21	R/W	Queues set in this mask activate the egress port immediately when any of the queues have data available.	0x00
EEE_TIMER_AGE	20:14	R/W	Maximum time frames in any queue must wait before the port is activated. The default value corresponds to 48 us. Time = 4**(EEE_TIMER_AGE/16) * (EEE_TIMER_AGE mod 16) microseconds	0x23
EEE_TIMER_WAKEUP	13:7	R/W	Time from the egress port is activated until frame transmission is restarted. Default value corresponds to 16 us. Time = 4**(EEE_TIMER_WAKEUP/16) * (EEE_TIMER_WAKEUP mod 16) microseconds	0x14
EEE_TIMER_HOLDOFF	6:0	R/W	When all queues are empty, the port is kept active until this time has passed. Default value corresponds to 5 us. Time = 4**(EEE_TIMER_HOLDOFF/16) * (EEE_TIMER_HOLDOFF mod 16) microseconds	0x05

7.3.1.9 SYS:SYSTEM:EEE_THRES

Parent: SYS:SYSTEM

Instances: 1

Table 166 • **Fields in EEE_THRES**

Field Name	Bit	Access	Description	Default
EEE_HIGH_BYTES	15:8	R/W	Maximum number of bytes in a queue before egress port is activated. Unit is 48 bytes.	0x00
EEE_HIGH_FRAMES	7:0	R/W	Maximum number of frames in a queue before the egress port is activated. Unit is 1 frame.	0x00

7.3.1.10 SYS:SYSTEM:IGR_NO_SHARING

Parent: SYS:SYSTEM

Instances: 1

Table 167 • **Fields in IGR_NO_SHARING**

Field Name	Bit	Access	Description	Default
IGR_NO_SHARING	26:0	R/W	Control whether frames received on the port may use shared resources. If ingress port or queue has reserved memory left to use, frame enqueuing is always allowed. 0: Use shared memory as well 1: Do not use shared memory	0x0000000

7.3.1.11 SYS:SYSTEM:EGR_NO_SHARING

Parent: SYS:SYSTEM

Instances: 1

Table 168 • **Fields in EGR_NO_SHARING**

Field Name	Bit	Access	Description	Default
EGR_NO_SHARING	26:0	R/W	Control whether frames forwarded to the port may use shared resources. If egress port or queue has reserved memory left to use, frame enqueuing is always allowed. 0: Use shared memory as well 1: Do not use shared memory	0x0000000

7.3.1.12 SYS:SYSTEM:SW_STATUS

Parent: SYS:SYSTEM

Instances: 27

Table 169 • **Fields in SW_STATUS**

Field Name	Bit	Access	Description	Default
EQ_AVAIL	9:2	R/O	Status bit per egress queue indicating whether data is ready for transmission.	0x00
PORT_LPI	1	R/O	Status bit indicating whether port is in low-power-idle due to the LPI algorithm (EEE_CFG). If set, transmissions are held back.	0x0
PORT_RX_PAUSED	0	R/O	Status bit indicating whether the switch core is instructing the MAC to pause the ingress port.	0x0

7.3.1.13 SYS:SYSTEM:EQ_TRUNCATE

Parent: SYS:SYSTEM

Instances: 27

Table 170 • **Fields in EQ_TRUNCATE**

Field Name	Bit	Access	Description	Default
EQ_TRUNCATE	7:0	R/W	If a bit is set, frames transmitted from corresponding egress queue are truncated to 92 bytes.	0x00

7.3.1.14 SYS:SYSTEM:EQ_PREFER_SRC

Parent: SYS:SYSTEM

Instances: 1

Table 171 • **Fields in EQ_PREFER_SRC**

Field Name	Bit	Access	Description	Default
EQ_PREFER_SRC	26:0	R/W	When multiple sources have data in the same priority, ingress ports set in this mask are preferred over ingress ports not set when arbitrating frames from ingress to egress. When multiple ports are set, the arbitration between these ports are round-robin.	0x4000000

7.3.1.15 SYS:SYSTEM:EXT_CPU_CFG

Parent: SYS:SYSTEM

Instances: 1

Table 172 • **Fields in EXT_CPU_CFG**

Field Name	Bit	Access	Description	Default
EXT_CPU_PORT	12:8	R/W	Select the port to use as the external CPU port.	0x1B
EXT_CPUQ_MSK	7:0	R/W	Frames destined for a CPU extraction queue set in this mask are sent to the external CPU defined by EXT_CPU_PORT instead of the internal CPU.	0x00

7.3.2 SYS:SCH

Parent: SYS

Instances: 1

Table 173 • **Registers in SCH**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
LB_DWRR_FRM_ADJ	0x00000000	1	Leaky bucket frame adjustment	Page 178
LB_DWRR_CFG	0x00000004	26 0x00000004	Leaky bucked frame adjustment	Page 179
SCH_DWRR_CFG	0x0000006C	26 0x00000004	Deficit weighted round robin control register	Page 179
SCH_SHAPING_CTRL	0x000000D8	26 0x00000004	Scheduler shaping control register	Page 180
SCH_LB_CTRL	0x00000140	1	Leaky bucket control	Page 181
SCH_CPU	0x00000144	1	Map CPU queues to CPU ports	Page 181

7.3.2.1 SYS:SCH:LB_DWRR_FRM_ADJ

Parent: SYS:SCH

Instances: 1

Table 174 • **Fields in LB_DWRR_FRM_ADJ**

Field Name	Bit	Access	Description	Default
FRM_ADJ	4:0	R/W	Value added to leaky buckets and DWRR each time a frame is scheduled. If set to 20, this corresponds to inclusion of minimum Ethernet IFG and preamble. 0-31: Number of bytes added at start of frame	0x00

7.3.2.2 SYS:SCH:LB_DWRR_CFG

Parent: SYS:SCH

Instances: 26

Table 175 • **Fields in LB_DWRR_CFG**

Field Name	Bit	Access	Description	Default
FRM_ADJ_ENA	0	R/W	If enabled, the value configured in SCH_LB_DWRR_FRM_ADJ.FRM_ADJ is added to the frame length for each frame. The modified frame length is used by both the leaky bucket and DWRR algorithm. 0:Disable frame length adjustment. 1:Enable frame length adjustment.	0x0

7.3.2.3 SYS:SCH:SCH_DWRR_CFG

Parent: SYS:SCH

Instances: 26

Table 176 • **Fields in SCH_DWRR_CFG**

Field Name	Bit	Access	Description	Default
DWRR_MODE	30	R/W	Configure DWRR scheduling for port. Weighted- and strict prioritization can be configured. 0: All priorities are scheduled strict 1: The two highest priorities (6, 7) are strict. The rest is DWRR	0x0

Table 176 • **Fields in SCH_DWRR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
COST_CFG	29:0	R/W	Queue cost configuration. Bit vector used to configure the cost of each priority. Bits 4:0: Cost for queue 0. Bits 9:5: Cost for queue 1. Bits 14:10: Cost for queue 2. Bits 19:15: Cost for queue 3. Bits 24:20: Cost for queue 4. Bits 29:25: Cost for queue 5. Within each cost field, the following encoding is used: 0: Cost 1 1: Cost 2 ... 31: Cost 32	0x00000000

7.3.2.4 SYS:SCH:SCH_SHAPING_CTRL

Parent: SYS:SCH

Instances: 26

Table 177 • **Fields in SCH_SHAPING_CTRL**

Field Name	Bit	Access	Description	Default
PRIO_SHAPING_ENA	7:0	R/W	Enable priority shaping. If enabled the BW of a priority is limited to SCH_LB::LB_RATE. xxxxxxx1: Enable shaping for Prio 0 xxxxxx1x: Enable shaping for Prio 1 ... 1xxxxxxx: Enable shaping for Prio N	0x00
PORT_SHAPING_ENA	8	R/W	Enable port shaping. If enabled the total BW of a port is limited to SCH_LB::LB_RATE. 0: Disable port shaping 1: Enable port shaping	0x0

Table 177 • **Fields in SCH_SHAPING_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
PRIO_LB_EXS_ENA	23:16	R/W	Allow this queue to use excess bandwidth. If none of the priorities are allowed (by their priority LB) to transmit. The resulting BW of a queue is a function of the port- and queue LBs, the DWRR and the excess enable bit: 1) Port LB closed. Hold back frames. 2) Port LB open -> Use strict- or DWRR scheduling to distribute traffic between open Queue LBs 3) All Queue LBs closed -> Hold back frames except for Queues which have PRIO_LB_EXS_ENA set. The excess BW is distributed using strict- or DWRR scheduling. xxxxxxx1: Enable excess BW for Prio 0 xxxxxx1x: Enable excess BW for Prio 1 ... 1xxxxxxx: Enable excess BW for Prio N	0x00

7.3.2.5 SYS:SCH:SCH_LB_CTRL

Parent: SYS:SCH

Instances: 1

Table 178 • **Fields in SCH_LB_CTRL**

Field Name	Bit	Access	Description	Default
LB_INIT	0	One-shot	Set to 1 to force a complete initialization of state and configuration of leaky buckets. Must be done before the scheduler is used. Field is automatically cleared whether initialization is complete. 0: No Action 1: Force initialization.	0x0

7.3.2.6 SYS:SCH:SCH_CPU

Parent: SYS:SCH

Instances: 1

Table 179 • **Fields in SCH_CPU**

Field Name	Bit	Access	Description	Default
SCH_CPU_MAP	9:2	R/W	Maps the 8 CPU queues to CPU port 26 or 27. Bit <n> set directs CPU queue <n> to CPU port 26/27.	0x00
SCH_CPU_RR	1:0	R/W	Set the scheduler for CPU port <n> to run round robin between queues instead of strict.	0x0

7.3.3 SYS:SCH_LB

Parent: SYS

Instances: 1

Ethernet leaky bucket configuration per port and per priority.

The address of the configuration is based on the following layout: (Assume the priority count is 8)

0: Leaky bucket for priority 0 of port 0

1: Leaky bucket for priority 1 of port 0

2: Leaky bucket for priority 2 of port 0

3: Leaky bucket for priority 3 of port 0

4: Leaky bucket for priority 4 of port 0

5: Leaky bucket for priority 5 of port 0

6: Leaky bucket for priority 6 of port 0

7: Leaky bucket for priority 7 of port 0

8: Leaky bucket port 0

9: Leaky bucket for priority 0 of port 1

10: Leaky bucket for priority 1 of port 1

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The configuration for each leaky bucket includes rate and threshold configuration.

Table 180 • **Registers in SCH_LB**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
LB_THRES	0x00000000	234 0x00000004	Leaky bucket threshold	Page 183
LB_RATE	0x00000400	234 0x00000004	Leaky bucket rate	Page 183

7.3.3.1 SYS:SCH_LB:LB_THRES

Parent: SYS:SCH_LB

Instances: 234

Table 181 • **Fields in LB_THRES**

Field Name	Bit	Access	Description	Default
LB_THRES	5:0	R/W	Burst capacity of leaky buckets The unit is 4KB (1KB = 1024Bytes). The largest supported threshold is 252KB when the register value is set to all "1"s. Queue shaper Q on port P uses shaper 9*P+Q. Port shaper on port P uses shaper 9*P+8. 0: Always closed 1: Burst capacity = 4096 bytes ... n: Burst capacity = n x 4096 bytes	0x00

7.3.3.2 SYS:SCH_LB:LB_RATE

Parent: SYS:SCH_LB

Instances: 234

Table 182 • **Fields in LB_RATE**

Field Name	Bit	Access	Description	Default
LB_RATE	14:0	R/W	Leaky bucket rate in unit of 100160 bps. Queue shaper Q on port P uses shaper 9*P+Q. Port shaper on port P uses shaper 9*P+8. 0: Open until burst capacity is used, then closed. 1: Rate = 100160 bps n: Rate = n x 100160 bps	0x0000

7.3.4 SYS:RES_CTRL

Parent: SYS

Instances: 1024

Table 183 • **Registers in RES_CTRL**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RES_CFG	0x00000000	1	Watermark configuration	Page 184
RES_STAT	0x00000004	1	Resource status	Page 185

7.3.4.1 SYS:RES_CTRL:RES_CFG

Parent: SYS:RES_CTRL

Instances: 1

The queue system tracks four resource consumptions:

Resource 0: Memory tracked per source

Resource 1: Frame references tracked per source

Resource 2: Memory tracked per destination

Resource 3: Frame references tracked per destination

Before a frame is added to the queue system, some conditions must be met:

- Reserved memory for the specific (SRC, PRIO) or for the specific SRC is available

OR

- Reserved memory for the specific (DST,PRIO) or for the specific DST is available

OR

- Shared memory is available

The frame reference resources are checked for availability like the memory resources. Enqueuing of a frame is allowed if both the memory resource check and the frame reference resource check succeed.

The extra resources consumed when enqueuing a frame are first taken from the reserved (SRC,PRIO), next from the reserved SRC, and last from the shared memory area. The same is done for DST. Both memory consumptions and frame reference consumptions are updated.

The register is layed out the following way:

Index 0-215: Reserved amount for (x,PRIO) at index 8*x+PRIO, x=SRC or DST

Index 224-250: Reserved amount for (x)

Resource 0 is accessed at index 0-255, 1 at index 256-511 etc.

The amount of shared memory is located at index 255. An extra watermark at 254 is used for limiting amount of shared memory used before yellow traffic is discarded.

The amount of shared references is located at index 511. An extra watermark at 510 is used for limiting amount of shared references for yellow traffic.

At index 216-223 there is a watermarks per priority used for limiting how much of the shared buffer must be used per priority.

Likewise at offset 472 there are priority watermarks for references.

The allocation size for memory tracking is 48 bytes, and all frames is added a 4 byte header internally.

Table 184 • **Fields in RES_CFG**

Field Name	Bit	Access	Description	Default
WM_HIGH	10:0	R/W	Watermark for resource. Note, the default value depends on the index. Refer to the congestion scheme documentation for details. Bit 10: Unit; 0:1, 1:16 Bits 9-0: Value to be multiplied with unit	0x000

7.3.4.2 SYS:RES_CTRL:RES_STAT

Parent: SYS:RES_CTRL

Instances: 1

Table 185 • **Fields in RES_STAT**

Field Name	Bit	Access	Description	Default
INUSE	27:14	R/W	Current consumption for corresponding watermark in RES_CFG.	0x0000
MAXUSE	13:0	R/W	Maximum consumption for corresponding watermark in RES_CFG.	0x0000

7.3.5 SYS:PAUSE_CFG

Parent: SYS

Instances: 1

Table 186 • **Registers in PAUSE_CFG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PAUSE_CFG	0x00000000	27 0x00000004	Watermarks for flow control condition per switch port.	Page 186
PAUSE_TOT_CFG	0x0000006C	1	Configure total memory pause condition	Page 186
ATOP	0x00000070	27 0x00000004	Tail dropping level	Page 187

Table 186 • **Registers in PAUSE_CFG *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ATOP_TOT_CFG	0x000000DC	1	Total raw memory use before tail dropping is activated	Page 187
EGR_DROP_FORCE	0x000000E0	1	Configures egress ports for flowcontrol	Page 187

7.3.5.1 SYS:PAUSE_CFG:PAUSE_CFG

Parent: SYS:PAUSE_CFG

Instances: 27

Table 187 • **Fields in PAUSE_CFG**

Field Name	Bit	Access	Description	Default
PAUSE_START	22:12	R/W	Start pausing ingress stream when the amount of memory consumed by the port exceeds this watermark. The TOTPAUSE condition must also be met. See RES_CFG	0x7FF
PAUSE_STOP	11:1	R/W	Stop pausing ingress stream when the amount of memory consumed by the port is below this watermark. See RES_CFG.	0x7FF
PAUSE_ENA	0	R/W	Enable pause feedback to the MAC, allowing transmission of pause frames or HDX collisions to limit ingress data rate.	0x0

7.3.5.2 SYS:PAUSE_CFG:PAUSE_TOT_CFG

Parent: SYS:PAUSE_CFG

Instances: 1

Table 188 • **Fields in PAUSE_TOT_CFG**

Field Name	Bit	Access	Description	Default
PAUSE_TOT_START	21:11	R/W	Assert TOTPAUSE condition when total memory allocation is above this watermark. See RES_CFG	0x000
PAUSE_TOT_STOP	10:0	R/W	Deassert TOTPAUSE condition when total memory allocation is below this watermark. See RES_CFG	0x000

7.3.5.3 SYS:PAUSE_CFG:ATOP

Parent: SYS:PAUSE_CFG

Instances: 27

Table 189 • **Fields in ATOP**

Field Name	Bit	Access	Description	Default
ATOP	10:0	R/W	When a source port consumes more than this level in the packet memory, frames are tail dropped, unconditionally of destination. See RES_CFG	0x7FF

7.3.5.4 SYS:PAUSE_CFG:ATOP_TOT_CFG

Parent: SYS:PAUSE_CFG

Instances: 1

Table 190 • **Fields in ATOP_TOT_CFG**

Field Name	Bit	Access	Description	Default
ATOP_TOT	10:0	R/W	Tail dropping is activate on a port when the port use has exceeded the ATOP watermark for the port, and the total memory use has exceeded this watermark. See RES_CFG	0x7FF

7.3.5.5 SYS:PAUSE_CFG:EGR_DROP_FORCE

Parent: SYS:PAUSE_CFG

Instances: 1

Table 191 • **Fields in EGR_DROP_FORCE**

Field Name	Bit	Access	Description	Default
EGRESS_DROP_FORCE	26:0	R/W	When enabled for a port, frames to the port are discarded, even when the ingress port is enabled for flow control. Applicable to egress ports that should not create head-of-line blocking in ingress ports operating in flow control mode. An example is the CPU port.	0x0000000

7.3.6 SYS:MMGT

Parent: SYS

Instances: 1

Table 192 • **Registers in MMGT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MMGT	0x00000000	1	Packet Memory Status	Page 188
EQ_CTRL	0x00000008	1	Egress queue status	Page 188

7.3.6.1 SYS:MMGT:MMGT

Parent: SYS:MMGT

Instances: 1

Table 193 • **Fields in MMGT**

Field Name	Bit	Access	Description	Default
FREECNT	19:8	R/O	Number of 192-byte free memory words.	0x000

7.3.6.2 SYS:MMGT:EQ_CTRL

Parent: SYS:MMGT

Instances: 1

Table 194 • **Fields in EQ_CTRL**

Field Name	Bit	Access	Description	Default
FP_FREE_CNT	12:0	R/O	Number of free frame references.	0x0000

7.3.7 SYS:MISC

Parent: SYS

Instances: 1

Table 195 • **Registers in MISC**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
REPEATER	0x00000018	1	Frame repeating setup	Page 188

7.3.7.1 SYS:MISC:REPEATER

Parent: SYS:MISC

Instances: 1

Table 196 • **Fields in REPEATER**

Field Name	Bit	Access	Description	Default
REPEATER	26:0	R/W	A bit set in this mask makes the corresponding port skip dequeing from the queue selected by the scheduler. This can be used for simple frame generation and scheduler experiments.	0x0000000

7.3.8 SYS:STAT

Parent: SYS

Instances: 3558

These registers are used for accessing all frame statistics.

Table 197 • **Registers in STAT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CNT	0x00000000	1	Counter values	Page 189

7.3.8.1 SYS:STAT:CNT

Parent: SYS:STAT

Instances: 1

Table 198 • **Fields in CNT**

Field Name	Bit	Access	Description	Default
CNT	31:0	R/W	Counter values. The counters are layed in three main blocks where each port has a share within the block: Rx counters: 0x000 - 0x488 - port0: 0x000 - 0x02A - port1: 0x02B - 0x055 - - port26 (CPU): 0x45E - 0x488 Tx counters: 0x800 - 0xB44 - port0: 0x800 - 0x81E - port1: 0x81F - 0x83D - - port26 (CPU): 0xB26 - 0xB44 Drop counters: 0xC00 - 0xDE5 - port0: 0xC00 - 0xC11 - port1: 0xC12 - 0xC23 - - port26 (CPU): 0xDD4 - 0xDE5	0x00000000

7.3.9 SYS:POL

Parent: SYS

Instances: 256

Port and QoS policers

Table 199 • **Registers in POL**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
POL_PIR_CFG	0x00000000	1	Peak Information Rate configuration for this policer	Page 190
POL_MODE_CFG	0x00000008	1	Common configuration for this policer	Page 191
POL_PIR_STATE	0x0000000C	1	State of this policer	Page 191

7.3.9.1 SYS:POL:POL_PIR_CFG

Parent: SYS:POL

Instances: 1

Table 200 • **Fields in POL_PIR_CFG**

Field Name	Bit	Access	Description	Default
PIR_RATE	20:6	R/W	Accepted rate for this policer. Unit is 100 kbps.	0x0000

Table 200 • **Fields in POL_PIR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
PIR_BURST	5:0	R/W	Burst capacity of this policer. Unit is 4 kilobytes.	0x00

7.3.9.2 SYS:POL:POL_MODE_CFG

Parent: SYS:POL

Instances: 1

Table 201 • **Fields in POL_MODE_CFG**

Field Name	Bit	Access	Description	Default
IPG_SIZE	9:5	R/W	Size of IPG to add to each frame if line rate policing is chosen in FRM_MODE.	0x14
FRM_MODE	4:3	R/W	Accounting mode of this policer. 0: Line rate. Police bytes including IPG_SIZE. 1: Data rate. Police bytes excluding IPG. 2. Frame rate. Police frames with rate unit = 100 fps and burst unit = 32.8 frames. 3: Frame rate. Police frame with rate unit = 1 fps and burst unit = 0.3 frames.	0x0
OVERSHOOT_ENA	0	R/W	If set, overshoot is allowed. This implies that a frame of any length is accepted if the policer is open even if the frame causes the bucket to use more than the remaining capacity. If cleared, overshoot is not allowed. This implies that it is checked that the frame will not use more than the remaining capacity in the bucket before accepting the frame.	0x1

7.3.9.3 SYS:POL:POL_PIR_STATE

Parent: SYS:POL

Instances: 1

Table 202 • **Fields in POL_PIR_STATE**

Field Name	Bit	Access	Description	Default
PIR_LVL	21:0	R/W	Current fill level of this policer. Unit is 0.5 bits.	0x000000

7.3.10 SYS:POL_MISC

Parent: SYS

Instances: 1

Table 203 • **Registers in POL_MISC**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
POL_FLOWC	0x00000000	27 0x00000004	Flow control configuration per policer	Page 192
POL_HYST	0x0000006C	1	Set delay between flow control clearings	Page 192

7.3.10.1 SYS:POL_MISC:POL_FLOWC

Parent: SYS:POL_MISC

Instances: 27

Table 204 • **Fields in POL_FLOWC**

Field Name	Bit	Access	Description	Default
POL_FLOWC	0	R/W	Use MAC flow control for lowering ingress rate 0: Standard policing. Frames are discarded when the rate is exceeded. 1: Flow control policing. Policer instructs the MAC to issue pause frames when the rate is exceeded.	0x0

7.3.10.2 SYS:POL_MISC:POL_HYST

Parent: SYS:POL_MISC

Instances: 1

Table 205 • **Fields in POL_HYST**

Field Name	Bit	Access	Description	Default
POL_FC_HYST	9:4	R/W	Set hysteresis for when to re-open a bucket after the burst capacity has been used. Unit is 1 kilobytes. This applies to policer in flow control mode (POL_FLOWC=1).	0x02
POL_DROP_HYST	3:0	R/W	Set hysteresis for when to re-open a bucket after the burst capacity has been used. Unit is 2 kilobytes. This applies to policer in drop mode (POL_FLOWC=0).	0x0

7.3.11 SYS:ISHP

Parent: SYS

Instances: 27

Table 206 • **Registers in ISHP**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ISHP_CFG	0x00000000	1	Rate and burst configuration	Page 193
ISHP_MODE_CFG	0x00000004	1	Mode of operation	Page 193
ISHP_STATE	0x00000008	1	State of this shaper	Page 194

7.3.11.1 SYS:ISHP:ISHP_CFG

Parent: SYS:ISHP

Instances: 1

Table 207 • **Fields in ISHP_CFG**

Field Name	Bit	Access	Description	Default
ISHP_RATE	21:7	R/W	Accepted rate for this shaper. Unit is 100 kbps.	0x0000
ISHP_BURST	6:1	R/W	Burst capacity of this shaper. Unit is 4kB	0x00
ISHP_ENA	0	R/W	Enable ingress shaping for this port.	0x0

7.3.11.2 SYS:ISHP:ISHP_MODE_CFG

Parent: SYS:ISHP

Instances: 1

Table 208 • **Fields in ISHP_MODE_CFG**

Field Name	Bit	Access	Description	Default
ISHP_IPG_SIZE	6:2	R/W	Size of IPG to add each frame if line rate shaping is chosen in ISHP_MODE.	0x14

Table 208 • **Fields in ISHP_MODE_CFG *(continued)***

Field Name	Bit	Access	Description	Default
ISHP_MODE	1:0	R/W	Accounting mode of this shaper. 0: Line rate. Shape bytes including IPG_size 1: Data rate. Shape bytes excluding IPG 2. Frame rate. Shape frames with rate unit = 100 fps and burst unit = 32.8 frames. 3: Frame rate. Shape frame with rate unit = 1 fps and burst unit = 0.3 frames.	0x0

7.3.11.3 SYS:ISHP:ISHP_STATE

Parent: SYS:ISHP

Instances: 1

Table 209 • **Fields in ISHP_STATE**

Field Name	Bit	Access	Description	Default
ISHP_LVL	21:0	R/W	Current fill level of this shaper. Unit is 0.5 bits.	0x000000

7.4 ANA

Table 210 • **Register Groups in ANA**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
ANA	0x00000D80	1	General analyzer configuration	Page 194
ANA_TABLES	0x00001000	1	MAC, VLAN, and PGID table configuration	Page 204
PORT	0x00000000	27 0x00000080	Per port configurations for Classifier	Page 211
COMMON	0x00000E38	1	Common configurations for Classifier	Page 218

7.4.1 ANA:ANA

Parent: ANA

Instances: 1

Table 211 • **Registers in ANA**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ADVLEARN	0x00000000	1	Advanced Learning Setup	Page 195
VLANMASK	0x00000004	1	VLAN Source Port Mask	Page 196
ANAGEFIL	0x00000008	1	Aging Filter	Page 196
ANEVENTS	0x0000000C	1	Event Sticky Bits	Page 196
STORMLIMIT_BURST	0x00000010	1	Storm policer burst	Page 198
STORMLIMIT_CFG	0x00000014	4 0x00000004	Storm Policer configuration	Page 198
ISOLATED_PORTS	0x00000024	1	Private VLAN Mask for isolated ports	Page 199
COMMUNITY_PORTS	0x00000028	1	Private VLAN Mask for community ports	Page 200
AUTOAGE	0x0000002C	1	Auto Age Timer	Page 200
MACTOPTIONS	0x00000030	1	MAC Table Options	Page 200
LEARNDISC	0x00000034	1	Learn Discard Counter	Page 201
AGENCTRL	0x00000038	1	Analyzer Configuration	Page 201
MIRRORPORTS	0x0000003C	1	Mirror Target Ports	Page 202
EMIRRORPORTS	0x00000040	1	Egress Mirror Mask	Page 203
FLOODING	0x00000044	1	Standard flooding configuration	Page 203
FLOODING_IPMC	0x00000048	1	Flooding configuration for IP multicasts	Page 203
SFLOW_CFG	0x0000004C	27 0x00000004	SFlow sampling configuration per port	Page 204

7.4.1.1 ANA:ANA:ADVLEARN

Parent: ANA:ANA

Instances: 1

Table 212 • **Fields in ADVLEARN**

Field Name	Bit	Access	Description	Default
VLAN_CHK	26	R/W	If this bit is set, a frame discarded because of VLAN ingress filtering is not subject to learning. VLAN ingress filtering is controlled by the VLAN_SRC_CHK flag in the VLAN table (see VLANACCESS register) or the VLANMASK register.	0x0
LEARN_MIRROR	25:0	R/W	Learn frames are also forwarded to ports marked in this mask.	0x0000000

7.4.1.2 ANA:ANA:VLANMASK

Parent: ANA:ANA

Instances: 1

Table 213 • **Fields in VLANMASK**

Field Name	Bit	Access	Description	Default
VLANMASK	26:0	R/W	Mask for requiring VLAN ingress filtering. If the bit for the frame's physical ingress port is set in this mask, then the port must be member of ingress frame's VLAN (VLANACCESS.VLAN_PORT_MASK), otherwise the frame is discarded.	0x0000000

7.4.1.3 ANA:ANA:ANAGEFIL

Parent: ANA:ANA

Instances: 1

This register sets up which entries are touched by an aging operation (manual as well as automatic aging).

In this way, it is possible to have different aging periods in each VLAN and to have quick removal of entries on specific ports.

The register also affects the GET_NEXT MAC table command. When using the register to control the behavior of GET_NEXT, it is recommended to disable automatic aging while executing the GET_NEXT command.

Table 214 • **Fields in ANAGEFIL**

Field Name	Bit	Access	Description	Default
AGE_LOCKED	19	R/W	Select entries to age. If cleared, unlocked entries will be aged and potentially removed. If set, locked entries will be aged but not removed.	0x0
PID_EN	18	R/W	If set, only MAC table entries with a destination index matching PID_VAL are aged.	0x0
PID_VAL	17:13	R/W	Destination index used in selective aging.	0x00
VID_EN	12	R/W	If set, only MAC table entries with a VID matching VID_VAL are aged.	0x0
VID_VAL	11:0	R/W	VID used in selective aging.	0x000

7.4.1.4 ANA:ANA:ANEVENTS

Parent: ANA:ANA

Instances: 1

Table 215 • **Fields in ANEVENTS**

Field Name	Bit	Access	Description	Default
AUTOAGE	24	Sticky	An AUTOAGE run was performed.	0x0
STORM_DROP	22	Sticky	A frame was discarded, because it exceeded the flooding storm limitations configured in STORMLIMIT.	0x0
LEARN_DROP	21	Sticky	A frame was discarded, because it was subject to learning, and the DropMode flag was set in ADVLEARN.	0x0
AGED_ENTRY	20	Sticky	An entry was removed at CPU Learn, or CPU requested an aging process.	0x0
CPU_LEARN_FAILED	19	Sticky	A learn operation failed due to hash table depletion. CPU-based learning only.	0x0
AUTO_LEARN_FAILED	18	Sticky	A learn operation of incoming source MAC address failed due to hash table depletion. Hardware-based learning only.	0x0
LEARN_REMOVE	17	Sticky	An entry was removed when learning a new source MAC address.	0x0
AUTO_LEARNED	16	Sticky	An entry was learned from an incoming frame. Hardware-based learning only.	0x0
AUTO_MOVED	15	Sticky	A station was moved to another port.	0x0
CLASSIFIED_DROP	13	Sticky	A frame was not forwarded due to classification (such as BPDUs).	0x0
CLASSIFIED_COPY	12	Sticky	A frame was copied to the CPU due to classification.	0x0
VLAN_DISCARD	11	Sticky	A frame was discarded due to lack of VLAN membership on source port.	0x0
FWD_DISCARD	10	Sticky	A frame was discarded due to missing forwarding state on source port.	0x0
MULTICAST_FLOOD	9	Sticky	A frame was flooded with multicast flooding mask.	0x0
UNICAST_FLOOD	8	Sticky	A frame was flooded with unicast flooding mask.	0x0
DEST_KNOWN	7	Sticky	A frame was forwarded with known destination MAC address.	0x0

Table 215 • **Fields in ANEVENTS *(continued)***

Field Name	Bit	Access	Description	Default
BUCKET3_MATCH	6	Sticky	A destination was found in hash table bucket 3.	0x0
BUCKET2_MATCH	5	Sticky	A destination was found in hash table bucket 2.	0x0
BUCKET1_MATCH	4	Sticky	A destination was found in hash table bucket 1.	0x0
BUCKET0_MATCH	3	Sticky	A destination was found in hash table bucket 0.	0x0
CPU_OPERATION	2	Sticky	A CPU-initiated operation on the MAC or VLAN table was processed. Default is 1 due to auto-initialization of the MAC and VLAN table.	0x1
DMAC_LOOKUP	1	Sticky	A destination address was looked up in the MAC table.	0x0
SMAC_LOOKUP	0	Sticky	A source address was looked up in the MAC table.	0x0

7.4.1.5 ANA:ANA:STORMLIMIT_BURST

Parent: ANA:ANA

Instances: 1

Table 216 • **Fields in STORMLIMIT_BURST**

Field Name	Bit	Access	Description	Default
STORM_BURST	3:0	R/W	Allowed number of frames in a burst is 2**STORM_BURST. The maximum allowed burst is 4096 frames, which corresponds to STORM_BURST = 12. The STORM_BURST is common for all storm policers.	0x0

7.4.1.6 ANA:ANA:STORMLIMIT_CFG

Parent: ANA:ANA

Instances: 4

0: UC storm policer

1: BC storm policer

2: MC policer

3: Learn policer

Table 217 • **Fields in STORMLIMIT_CFG**

Field Name	Bit	Access	Description	Default
STORM_RATE	6:3	R/W	Allowed rate of storm policer is 2**STORM_UNIT frames per second or kiloframes per second. See STORM_UNIT. The maximum allowed rate is 1024 kiloframes per second, which corresponds to STORM_RATE = 10 with STORM_UNIT set to 0.	0x0
STORM_UNIT	2	R/W	If set, the base unit for the storm policer is one frame per second. If cleared, the base unit is one kiloframe per second.	0x0
STORM_MODE	1:0	R/W	Mode of operation for storm policer. 0: Disabled. 1: Police CPU destination only. 2: Police front port destinations only. 3: Police both CPU and front port destinations.	0x0

7.4.1.7 ANA:ANA:ISOLATED_PORTS

Parent: ANA:ANA

Instances: 1

Table 218 • **Fields in ISOLATED_PORTS**

Field Name	Bit	Access	Description	Default
ISOL_PORTS	26:0	R/W	This mask is used in private VLANs applications. Promiscuous and community ports must be set and isolated ports must be cleared. For frames classified to a private VLAN (see the VLAN_PRIV_VLAN field in VLAN table), the resulting VLAN mask is calculated as follows: - Frames received on a promiscuous port use the VLAN mask directly. - Frames received on a community port use the VLAN mask AND'ed with the ISOL_PORTS. - Frames received on a isolated port use the VLAN mask AND'ed with the COMM_PORTS AND'ed with the ISOL_PORTS. For frames classified to a non-private VLAN, this mask is not used.	0x7FFFFFF

7.4.1.8 ANA:ANA:COMMUNITY_PORTS

Parent: ANA:ANA

Instances: 1

Table 219 • **Fields in COMMUNITY_PORTS**

Field Name	Bit	Access	Description	Default
COMM_PORTS	26:0	R/W	This mask is used in private VLANs applications. Promiscuous and isolated ports must be set and community ports must be cleared. See ISOLATED_PORTS.ISOL_PORTS for details.	0x7FFFFFF

7.4.1.9 ANA:ANA:AUTOAGE

Parent: ANA:ANA

Instances: 1

Table 220 • **Fields in AUTOAGE**

Field Name	Bit	Access	Description	Default
AGE_FAST	21	R/W	Sets the unit of PERIOD to 8.2 us. PERIOD must be a minimum of 3 when using the FAST option.	0x0
AGE_PERIOD	20:1	R/W	Time in seconds between automatic aging of a MAC table entry. Setting AGE_PERIOD to zero effectively disables automatic aging. An inactive unlocked MAC table entry is aged after 2*AGE_PERIOD.	0x00000
AUTOAGE_LOCKED	0	R/W	Also set the AGED_FLAG bit on locked entries. They will not be removed.	0x0

7.4.1.10 ANA:ANA:MACTOPTIONS

Parent: ANA:ANA

Instances: 1

Table 221 • **Fields in MACTOPTIONS**

Field Name	Bit	Access	Description	Default
REDUCED_TABLE	1	R/W	When set, the MAC table will be reduced 256 entries (64 hash-chains of 4)	0x0

Table 221 • **Fields in MACTOPTIONS *(continued)***

Field Name	Bit	Access	Description	Default
SHADOW	0	R/W	Enable MAC table shadow registers. The SHADOW bit affects the behavior of the READ command in MACACCESS.MAC_TABLE_CMD : With the shadow bit set, reading bucket 0 causes the remaining 3 buckets in the row to be stored in "shadow registers". Following read accesses to bucket 1-3 return the content of the shadow registers. This is useful when reading a MAC table, which can change while being read.	0x0

7.4.1.11 ANA:ANA:LEARNDISC

Parent: ANA:ANA

Instances: 1

The total number of MAC table entries that have been or would have been learned, but have been discarded due to a lack of storage space.

Table 222 • **Fields in LEARNDISC**

Field Name	Bit	Access	Description	Default
LEARNDISC	31:0	R/W	Number of discarded learn requests due to MAC table overflow (collisions or MAC table entry limits).	0x00000000

7.4.1.12 ANA:ANA:AGENCTRL

Parent: ANA:ANA

Instances: 1

Table 223 • **Fields in AGENCTRL**

Field Name	Bit	Access	Description	Default
FID_MASK	23:12	R/W	Mask used to enable shared learning among multiple VLANs. The FID value used in learning and MAC table lookup is calculated as: FID = VID and (not FID_MASK) By default, FID_MASK is set to all-zeros, corresponding to independent VLAN learning. In this case FID becomes identical to VID.	0x000

Table 223 • **Fields in AGENCTRL *(continued)***

Field Name	Bit	Access	Description	Default
IGNORE_DMAC_FLAGS	11	R/W	Do not react to flags found in the DMAC entry or the corresponding flags for flooded frames (FLOOD_IGNORE_VLAN).	0x0
IGNORE_SMAC_FLAGS	10	R/W	Do not react to flags found in the SMAC entry. Note, the IGNORE_VLAN flag is not checked for SMAC entries.	0x0
FLOOD_SPECIAL	9	R/W	Flood frames using the lowest 27 bits of DMAC as destination port mask. This is only added for testing purposes.	0x0
FLOOD_IGNORE_VLAN	8	R/W	VLAN mask is not applied to flooded frames.	0x0
MIRROR_CPU	7	R/W	Frames destined for the CPU extraction queues are also forwarded to the port set configured in MIRRORPORTS.	0x0
LEARN_CPU_COPY	6	R/W	If set, auto-learned stations get the CPU_COPY flag set in the MAC table entry.	0x0
LEARN_SRC_KILL	5	R/W	If set, auto-learned stations get the SRC_KILL flag set in the MAC table entry.	0x0
LEARN_IGNORE_VLAN	4	R/W	If set, auto-learned stations get the IGNORE_VLAN flag set in the MAC table entry.	0x0
CPU_CPU_KILL_ENA	3	R/W	If set, CPU injected frames are never sent back to the CPU.	0x1
RESERVED	2	R/W	Must be set to its default.	0x1
RESERVED	1	R/W	Must be set to its default.	0x1
RESERVED	0	R/W	Must be set to its default.	0x1

7.4.1.13 ANA:ANA:MIRRORPORTS

Parent: ANA:ANA

Instances: 1

Table 224 • **Fields in MIRRORPORTS**

Field Name	Bit	Access	Description	Default
MIRRORPORTS	26:0	R/W	Ports set in this mask receive a mirror copy. If CPU is included in mask (bit 26 set), then the frame is copied to CPU extraction queue CPUQ_CFG.CPUQ_MIRROR.	0x0000000

7.4.1.14 ANA:ANA:EMIRRORPORTS

Parent: ANA:ANA

Instances: 1

Table 225 • **Fields in EMIRRORPORTS**

Field Name	Bit	Access	Description	Default
EMIRRORPORTS	26:0	R/W	Frames forwarded to ports in this mask are mirrored to the port set configured in MIRRORPORTS (i.e. egress port mirroring).	0x0000000

7.4.1.15 ANA:ANA:FLOODING

Parent: ANA:ANA

Instances: 1

Table 226 • **Fields in FLOODING**

Field Name	Bit	Access	Description	Default
FLD_UNICAST	17:12	R/W	Set the PGID mask to use when flooding unknown unicast frames.	0x3F
FLD_BROADCAST	11:6	R/W	Set the PGID mask to use when flooding unknown broadcast frames.	0x3F
FLD_MULTICAST	5:0	R/W	Set the PGID mask to use when flooding unknown multicast frames (except IP multicasts).	0x3F

7.4.1.16 ANA:ANA:FLOODING_IPMC

Parent: ANA:ANA

Instances: 1

Table 227 • **Fields in FLOODING_IPMC**

Field Name	Bit	Access	Description	Default
FLD_MC4_CTRL	23:18	R/W	Set the PGID mask to use when flooding unknown IPv4 Multicast Control frames.	0x3F
FLD_MC4_DATA	17:12	R/W	Set the PGID mask to use when flooding unknown IPv4 Multicast Data frames.	0x3F
FLD_MC6_CTRL	11:6	R/W	Set the PGID mask to use when flooding unknown IPv6 Multicast Control frames.	0x3F
FLD_MC6_DATA	5:0	R/W	Set the PGID mask to use when flooding unknown IPv6 Multicast Data frames.	0x3F

7.4.1.17 ANA:ANA:SFLOW_CFG

Parent: ANA:ANA

Instances: 27

Table 228 • **Fields in SFLOW_CFG**

Field Name	Bit	Access	Description	Default
SF_RATE	13:2	R/W	Probability of a frame being SFLOW sampled. Unit is 1/4096. A value of 0 makes 1/4096 of the candidates being forwarded to the SFLOW CPU extraction queue. A values of 4095 makes all candidates being forwarded.	0x000
SF_SAMPLE_RX	1	R/W	Enable SFLOW sampling of frames received on this port.	0x0
SF_SAMPLE_TX	0	R/W	Enable SFLOW sampling of frames transmitted on this port.	0x0

7.4.2 ANA:ANA_TABLES

Parent: ANA

Instances: 1

Table 229 • **Registers in ANA_TABLES**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ANMOVED	0x000001AC	1	Station Move Logger	Page 204
MACHDATA	0x000001B0	1	MAC Address High	Page 205
MACLDATA	0x000001B4	1	MAC Address Low	Page 205
MACACCESS	0x000001B8	1	MAC Table Command	Page 205
MACTINDX	0x000001BC	1	MAC Table Index	Page 207
VLANACCESS	0x000001C0	1	VLAN Table Command	Page 208
VLANTIDX	0x000001C4	1	VLAN Table Index	Page 209
PGID	0x00000000	107 0x00000004	Port Group Identifiers	Page 209
ENTRYLIM	0x00000200	27 0x00000004	MAC Table Entry Limits	Page 210

7.4.2.1 ANA:ANA_TABLES:ANMOVED

Parent: ANA:ANA_TABLES

Instances: 1

Table 230 • **Fields in ANMOVED**

Field Name	Bit	Access	Description	Default
ANMOVED	26:0	R/W	Sticky bit set when a station has been learned on a port while already learned on another port (i.e. port move). The register is cleared by writing 1 to the bits to be cleared. This mask can be used to detect topology problems in the network, where stations are learned on multiple ports repeatedly. If some bits in this register get asserted repeatedly, the ports can be shut down, or management warnings can be issued.	0x0000000

7.4.2.2 ANA:ANA_TABLES:MACHDATA

Parent: ANA:ANA_TABLES

Instances: 1

Table 231 • **Fields in MACHDATA**

Field Name	Bit	Access	Description	Default
VID	27:16	R/W	VID used in MAC table operations through MACACCESS. For read operations, the VID value is returned in this field.	0x000
MACHDATA	15:0	R/W	Most significant 16 MAC address bits used in MAC table operations through MACACCESS.	0x0000

7.4.2.3 ANA:ANA_TABLES:MACLDATA

Parent: ANA:ANA_TABLES

Instances: 1

Table 232 • **Fields in MACLDATA**

Field Name	Bit	Access	Description	Default
MACLDATA	31:0	R/W	Lower 32 MAC address bits used in MAC table operations through MACACCESS.	0x00000000

7.4.2.4 ANA:ANA_TABLES:MACACCESS

Parent: ANA:ANA_TABLES

Instances: 1

This register is used for updating or reading the MAC table from the CPU.

The command (MAC_TABLE_CMD) selects between different operations and uses the following encoding:

000 - IDLE:

The previous operation has completed.

001 - LEARN:

Insert/learn new entry in MAC table. Position given by (MAC, VID) in MACHDATA and MACLDATA.

010 - FORGET:

Delete/unlearn entry given by (MAC, VID) in MACHDATA and MACLDATA.

Both locked and unlocked entries are deleted.

011 - AGE:

Start an age scan on the MAC table.

100 - GET_NEXT:

Get the smallest entry in the MAC table numerically larger than the (MAC, VID) specified in MACHDATA and MACLDATA. The VID and MAC are evaluated as a 60-bit number with the VID being most significant.

101 - INIT:

Table is initialized (completely cleared).

110 - READ:

The READ command is divided into two modes: Direct mode and indirect mode.

Direct mode (read):

With MACACCESS.VALID cleared, the entry pointed to by MACTINDX.INDEX (row) and MACTINDX.BUCKET (column) is read.

Indirect mode (lookup):

With MACACCESS.VALID set, the entry pointed to by (MAC, VID) in the MACHDATA and MACLDATA is read.

111 - WRITE

Write entry. Address of the entry is specified in MACTINDX.INDEX (row) and MACTINDX.BUCKET (column).

An existing entry (locked or unlocked) is overwritten.

The MAC_TABLE_CMD must be IDLE before a new command can be issued.

The AGE and CLEAR commands run for approximately 50 us. The other commands execute immediately.

The flags IGNORE_VLAN and MAC_CPU_COPY are ignored for DMAC lookup if AGENCTRL.IGNORE_DMAC_FLAGS is set.

The flags SRC_KILL and MAC_CPU_COPY are ignored for SMAC lookup if AGENCTRL.IGNORE_SMAC_FLAGS is set.

Table 233 • **Fields in MACACCESS**

Field Name	Bit	Access	Description	Default
IP6_MASK	18:16	R/W	Bits 24:22 in the destination port mask for IPv6 entries.	0x0
MAC_CPU_COPY	15	R/W	Frames matching this entry are copied to the CPU extraction queue CPUQ_CFG.CPUQ_MAC. Applies to both SMAC and DMAC lookup.	0x0
SRC_KILL	14	R/W	Frames matching this entry are discarded. Applies only to the SMAC lookup. For discarding frames based on the DMAC lookup a NULL PGID mask can be used.	0x0
IGNORE_VLAN	13	R/W	The VLAN mask is ignored for this destination. Applies only to DMAC lookup.	0x0
AGED_FLAG	12	R/W	This flag is set on every aging run. Entry is removed if flag is already set. The flag is cleared when the entry is target for a SMAC lookup. Locked entries will not be removed. Bit is for IPv6 Multicast used for port 25.	0x0
VALID	11	R/W	Entry is valid.	0x0
ENTRY_TYPE	10:9	R/W	Type of entry: 0: Normal entry eligible for aging 1: Locked entry. Entry will not be removed by aging 2: IPv4 Multicast entry. Full portset in mac record 3: IPv6 Multicast entry. Full portset in mac record	0x0
DEST_IDX	8:3	R/W	Index for the destination masks table (PGID). For unicasts, this is a number from 0-EXB_PORT_CNT_MINUS_ONE.	0x00
MAC_TABLE_CMD	2:0	R/W	MAC Table Command. See below.	0x0

7.4.2.5 ANA:ANA_TABLES:MACTINDX

Parent: ANA:ANA_TABLES

Instances: 1

Table 234 • **Fields in MACTINDX**

Field Name	Bit	Access	Description	Default
BUCKET	12:11	R/W	Selects one of the four MAC table entries in a row. The row is addressed with the INDEX field.	0x0
M_INDEX	10:0	R/W	The index selects one of the 2048 MAC table rows. Within a row the entry is addressed by the BUCKET field	0x000

7.4.2.6 ANA:ANA_TABLES:VLANACCESS

Parent: ANA:ANA_TABLES

Instances: 1

The VLAN_TBL_CMD field of this register is used for updating and reading the VLAN table. The command (VLAN_TBL_CMD) selects between different operations and uses the following encoding:

00 - IDLE:

The previous operation has completed.

01 - READ:

The VLAN table entry set in VLANTIDX.INDEX is returned in VLANACCESS.VLAN_PORT_MASK and the VLAN flags in VLANTIDX.

10 - WRITE:

The VLAN table entry pointed to by VLANTIDX.INDEX is updated with VLANACCESS.VLAN_PORT_MASK and the VLAN flags in VLANTIDX.

11 - INIT:

The VLAN table is initialized to default values (all ports are members of all VLANs).

The VLAN_TBL_CMD must be IDLE before a new command can be issued. The INIT command run for approximately 50 us whereas the other commands execute immediately. When an operation has completed, VLAN_TBL_CMD changes to IDLE.

Table 235 • **Fields in VLANACCESS**

Field Name	Bit	Access	Description	Default
VLAN_PORT_MASK	28:2	R/W	Frames classified to this VLAN can only be sent to ports in this mask. Note that the CPU port module is always member of all VLANs and its VLAN membership can therefore not be configured through this mask.	0x3FFFFFF

Table 235 • **Fields in VLANACCESS *(continued)***

Field Name	Bit	Access	Description	Default
VLAN_TBL_CMD	1:0	R/W	VLAN Table Command.	0x0

7.4.2.7 ANA:ANA_TABLES:VLANTIDX

Parent: ANA:ANA_TABLES

Instances: 1

Table 236 • **Fields in VLANTIDX**

Field Name	Bit	Access	Description	Default
VLAN_PRIV_VLAN	15	R/W	If set, a VLAN is a private VLAN. See PRIV_VLAN_MASK for details.	0x0
VLAN_LEARN_DISABLED	14	R/W	Disable learning for this VLAN.	0x0
VLAN_MIRROR	13	R/W	If set, all frames classified to this VLAN are mirrored to the port set configured in MIRRORPORTS.	0x0
VLAN_SRC_CHK	12	R/W	If set, VLAN ingress filtering is enabled for this VLAN. If set, a frame's ingress port must be member of the frame's VLAN, otherwise the frame is discarded.	0x0
V_INDEX	11:0	R/W	Index used to select VLAN table entry for read/write operations (see VLANACCESS). This value equals the VID.	0x000

7.4.2.8 ANA:ANA_TABLES:PGID

Parent: ANA:ANA_TABLES

Instances: 107

Three port masks are applied to all frames, allowing transmission to a port if the corresponding bit is set in all masks.

0-63: A mask is applied based on destination analysis

64-79: A mask is applied based on aggregation analysis

80-106: A mask is applied based on source port analysis

Destination analysis:

There are 64 destination masks in total. By default, the first 26 port masks only have the bit corresponding to their port number set. These masks should not be changed, except for aggregation.

The remaining destination masks are set to 0 by default and are available for use for Layer-2 multicasts and flooding (See FLOODING and FLOODING_IPMC).

Aggregation analysis:

The aggregation port masks are used to select only one port within each aggregation group. These 16 masks must be setup to select only one port in each aggregated port group.

For ports, which are not part of any aggregation group, the corresponding bits in all 16 masks must be set.

I.e. if no aggregation is configured, all masks must be set to all-ones.

The aggregation mask used for the forwarding of a given frame is selected by the frame's aggregation code (see AGGRCTRL).

Source port analysis:

The source port masks are used to prevent frames from being looped back to the ports on which they were received, and must be updated according to the

aggregation configuration. A frame that is received on port n, uses mask 80+n as a mask to filter out destination ports to avoid loopback, or to facilitate port grouping (port-based VLANs). The default values are that all bits are set except for the index number.

Table 237 • **Fields in PGID**

Field Name	Bit	Access	Description	Default
PGID	26:0	R/W	When a mask is chosen, bit N must be set for the frame to be transmitted on port N.	0x7FFFFFF
CPUQ_DST_PGID	29:27	R/W	CPU extraction queue used when CPU port is enabled in PGID. Only applicable for the destination analysis.	0x0

7.4.2.9 ANA:ANA_TABLES:ENTRYLIM

Parent: ANA:ANA_TABLES

Instances: 27

Table 238 • **Fields in ENTRYLIM**

Field Name	Bit	Access	Description	Default
ENTRYLIM	17:14	R/W	Maximum number of unlocked entries in the MAC table learned on this port. Locked entries and IPMC entries do not obey this limit. Both auto-learned and unlocked CPU-learned entries obey this limit. 0: 1 entry 1: 2 entries n: 2**n entries >12: 8192 entries	0xD

Table 238 • **Fields in ENTRYLIM *(continued)***

Field Name	Bit	Access	Description	Default
ENTRYSTAT	13:0	R/W	Current number of unlocked MAC table entries learned on this port.	0x0000

7.4.3 ANA:PORT

Parent: ANA

Instances: 27

Table 239 • **Registers in PORT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VLAN_CFG	0x00000000	1	Port VLAN configuration	Page 211
DROP_CFG	0x00000004	1	VLAN acceptance filtering	Page 212
QOS_CFG	0x00000008	1	QoS and DSCP configuration	Page 213
QOS_PCP_DEI_MAP_CFG	0x00000010	16 0x00000004	Mapping of DEI and PCP to QoS class	Page 213
CPU_FWD_CFG	0x00000050	1	CPU forwarding of special protocols	Page 214
CPU_FWD_BPDU_CFG	0x00000054	1	CPU forwarding of BPDU frames	Page 214
CPU_FWD_GARP_CFG	0x00000058	1	CPU forwarding of GARP frames	Page 215
CPU_FWD_CCM_CFG	0x0000005C	1	CPU forwarding of CCM/Link trace frames	Page 215
PORT_CFG	0x00000060	1	Special port configuration	Page 215
POL_CFG	0x00000064	1	Policer selection	Page 217

7.4.3.1 ANA:PORT:VLAN_CFG

Parent: ANA:PORT

Instances: 1

Table 240 • **Fields in VLAN_CFG**

Field Name	Bit	Access	Description	Default
VLAN_AWARE_ENA	20	R/W	Enable VLAN awareness. If set, Q-tag headers are processed during the basic VLAN classification. If cleared, Q-tag headers are ignored during the basic VLAN classification.	0x0

Table 240 • **Fields in VLAN_CFG *(continued)***

Field Name	Bit	Access	Description	Default
VLAN_POP_CNT	19:18	R/W	Number of tag headers to remove from ingress frame. 0: Keep all tags. 1: Pop up to 1 tag (outer tag if available). 2: Pop up to 2 tags (outer and inner tag if available). 3: Reserved.	0x0
VLAN_INNER_TAG_ENA	17	R/W	Set if the inner Q-tag must be used instead of the outer Q-tag. If the received frame is single tagged, the outer tag is used. This bit influences the VLAN acceptance filter (DROP_CFG), the basic VLAN classification (VLAN_CFG), and the basic QoS classification (QOS_CFG).	0x0
VLAN_TAG_TYPE	16	R/W	Tag Protocol Identifier type for port-based VLAN. 0: C-tag (EtherType = 0x8100) 1: S-tag (EtherType = 0x88A8 or configurable value (VLAN_ETYPE_CFG))	0x0
VLAN_DEI	15	R/W	DEI value for port-based VLAN.	0x0
VLAN_PCP	14:12	R/W	PCP value for port-based VLAN.	0x0
VLAN_VID	11:0	R/W	VID value for port-based VLAN.	0x000

7.4.3.2 ANA:PORT:DROP_CFG

Parent: ANA:PORT

Instances: 1

Table 241 • **Fields in DROP_CFG**

Field Name	Bit	Access	Description	Default
DROP_UNTAGGED_ENA	6	R/W	Drop untagged frames.	0x0
DROP_S_TAGGED_ENA	5	R/W	Drop S-tagged frames (VID different from 0 and EtherType = 0x88A8 or configurable value (VLAN_ETYPE_CFG)).	0x0
DROP_C_TAGGED_ENA	4	R/W	Drop C-tagged frames (VID different from 0 and EtherType = 0x8100).	0x0
DROP_PRIO_S_TAGGED_ENA	3	R/W	Drop S-tagged frames (VID=0 and EtherType = 0x88A8 or configurable value (VLAN_ETYPE_CFG)).	0x0

Table 241 • **Fields in DROP_CFG *(continued)***

Field Name	Bit	Access	Description	Default
DROP_PRIO_C_TAGGED_ENA	2	R/W	Drop priority C-tagged frames (VID=0 and EtherType = 0x8100).	0x0
DROP_NULL_MAC_ENA	1	R/W	Drop frames with source or destination MAC address equal to 0x000000000000.	0x0
DROP_MC_SMAC_ENA	0	R/W	Drop frames with multicast source MAC address.	0x0

7.4.3.3 ANA:PORT:QOS_CFG

Parent: ANA:PORT

Instances: 1

Table 242 • **Fields in QOS_CFG**

Field Name	Bit	Access	Description	Default
QOS_DEFAULT_VAL	7:5	R/W	Default QoS class.	0x0
QOS_DSCP_ENA	4	R/W	If set, the QoS class can be based on DSCP values.	0x0
QOS_PCP_ENA	3	R/W	If set, the QoS class can be based on PCP and DEI values for tagged frames.	0x0
DSCP_TRANSLATE_ENA	2	R/W	Set if the DSCP value must be translated before using the DSCP value. If set, the translated DSCP value is given from DSCP_CFG[DSCP].DSCP_TRANSLATE_VAL.	0x0
DSCP_REWR_CFG	1:0	R/W	Configure which DSCP values to rewrite based on QoS class. If the DSCP value is to be rewritten, then the new DSCP = DSCP_REWR_CFG[QoS class].DSCP_QOS_REWR_VAL. 0: Rewrite none. 1: Rewrite if DSCP=0 2: Rewrite for selected values configured in DSCP_CFG[DSCP].DSCP_REWR_ENA. 3: Rewrite all.	0x0

7.4.3.4 ANA:PORT:QOS_PCP_DEI_MAP_CFG

Parent: ANA:PORT

Instances: 16

Table 243 • **Fields in QOS_PCP_DEI_MAP_CFG**

Field Name	Bit	Access	Description	Default
QOS_PCP_DEI_VAL	2:0	R/W	Map the frame's PCP and DEI values to a QoS class. QoS class = QOS_PCP_DEI_MAP_CFG[index] .QOS_PCP_DEI_VAL, where index = 8*DEI + PCP. Only applicable to tagged frames. The use of Inner or outer tag can be selected using VLAN_CFG.VLAN_INNER_TAG_ ENA.	0x0

7.4.3.5 ANA:PORT:CPU_FWD_CFG

Parent: ANA:PORT

Instances: 1

Table 244 • **Fields in CPU_FWD_CFG**

Field Name	Bit	Access	Description	Default
CPU_MLD_REDIR_ENA	4	R/W	If set, MLD frames are redirected to the CPU.	0x0
CPU_IGMP_REDIR_ENA	3	R/W	If set, IGMP frames are redirected to the CPU.	0x0
CPU_IPMC_CTRL_COPY _ENA	2	R/W	If set, IPv4 multicast control frames (destination IP address in the range 224.0.0.x) are copied to the CPU.	0x0
CPU_SRC_COPY_ENA	1	R/W	If set, all frames received on this port are copied to the CPU extraction queue given by CPUQ_CFG.CPUQ_SRC_COPY.	0x0
CPU_ALLBRIDGE_REDIR _ENA	0	R/W	If set, All LANs bridge management group frames (DMAC = 01-80-C2-00-00-10) are redirected to the CPU.	0x0

7.4.3.6 ANA:PORT:CPU_FWD_BPDU_CFG

Parent: ANA:PORT

Instances: 1

Table 245 • **Fields in CPU_FWD_BPDU_CFG**

Field Name	Bit	Access	Description	Default
BPDU_REDIR_ENA	15:0	R/W	If bit x is set, BPDU frame (DMAC = 01-80-C2-00-00-0x) is redirected to the CPU.	0x0000

7.4.3.7 ANA:PORT:CPU_FWD_GARP_CFG

Parent: ANA:PORT

Instances: 1

Table 246 • **Fields in CPU_FWD_GARP_CFG**

Field Name	Bit	Access	Description	Default
GARP_REDIR_ENA	15:0	R/W	If bit x is set, GARP frame (DMAC = 01-80-C2-00-00-2x) is redirected to the CPU.	0x0000

7.4.3.8 ANA:PORT:CPU_FWD_CCM_CFG

Parent: ANA:PORT

Instances: 1

Table 247 • **Fields in CPU_FWD_CCM_CFG**

Field Name	Bit	Access	Description	Default
CCM_REDIR_ENA	15:0	R/W	If bit x is set, CCM/Link trace frame (DMAC = 01-80-C2-00-00-3x) is redirected to the CPU.	0x0000

7.4.3.9 ANA:PORT:PORT_CFG

Parent: ANA:PORT

Instances: 1

Table 248 • **Fields in PORT_CFG**

Field Name	Bit	Access	Description	Default
SRC_MIRROR_ENA	14	R/W	If set, all frames received on this port are mirrored to the port set configured in MIRRORPORTS (ie. ingress mirroring). For egress mirroring, see EMIRRORPORTS.	0x0

Table 248 • **Fields in PORT_CFG** *(continued)*

Field Name	Bit	Access	Description	Default
LIMIT_DROP	13	R/W	If set, learn frames on an ingress port, which has exceeded the maximum number of MAC table entries are discarded. Forwarding to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LIMIT_DROP is ignored.	0x0
LIMIT_CPU	12	R/W	If set, learn frames on an ingress port, which has exceeded the maximum number of MAC table entries are copied to the CPU extraction queue specified in CPUQ_CFG.CPUQ_LRN. Note that if LEARN_ENA is cleared, then the LIMIT_CPU is ignored.	0x0
LOCKED_PORTMOVE_DROP	11	R/W	If set, incoming frames triggering a port move for a locked entry in the MAC table received on this port are discarded. Forwarding to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LOCKED_PORTMOVE_DROP is ignored.	0x0
LOCKED_PORTMOVE_CPU	10	R/W	If set, incoming frames triggering a port move for a locked MAC table entry received on this port are copied to the CPU extraction queue specified in CPUQ_CFG.CPUQ_LOCKED_PORTMOVE. Note that if LEARN_ENA is cleared, then the LOCKED_PORTMOVE_CPU is ignored.	0x0
LEARNDROP	9	R/W	If set, incoming learn frames received on this port are discarded. Forwarding to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LEARNDROP is ignored.	0x0
LEARNCPU	8	R/W	If set, incoming learn frames received on this port are copied to the CPU extraction queue specified in AGENCTRL.CPUQ_LRN. Note that if LEARN_ENA is cleared, then the LEARNCPU is ignored.	0x0
LEARNAUTO	7	R/W	If set, incoming learn frames received on this port are auto learned. Note that if LEARN_ENA is cleared, then the LEARNAUTO is ignored.	0x1

Table 248 • **Fields in PORT_CFG *(continued)***

Field Name	Bit	Access	Description	Default
LEARN_ENA	6	R/W	Enable learning for frames received on this port. If cleared, learning is skipped and any configuration settings in LEARNAUTO, LEARNCPU, LEARNDROP is ignored.	0x1
RECV_ENA	5	R/W	Enable reception of frames. If cleared, all incoming frames on this port are discarded by the analyzer.	0x1
PORTID_VAL	4:0	R/W	Logical port number for front port. If port is not a member of a LLAG, then PORTID must be set to the physical port number. If port is a member of a LLAG, then PORTID must be set to the common PORTID_VAL used for all member ports of the LLAG.	0x00

7.4.3.10 ANA:PORT:POL_CFG

Parent: ANA:PORT

Instances: 1

Table 249 • **Fields in POL_CFG**

Field Name	Bit	Access	Description	Default
POL_CPU_REDIR_8021	19	R/W	If set, frames with a DMAC = IEEE reserved addresses (BPDU, GARP, CCM, ALLBRIGDE), which are redirected to the CPU are not policed by any policers. The frames are still counted in the policer buckets.	0x0
POL_CPU_REDIR_IP	18	R/W	If set, IGMP and MLD frames, which are redirected to the CPU are not policed by any policers. The frames are still counted in the policers buckets.	0x0
PORT_POL_ENA	17	R/W	Enable port policing. Port policing on port P uses policer P.	0x0
QUEUE_POL_ENA	16:9	R/W	Bitmask, where bit<n> enables policing of frames classified to QoS class n on this port. Queue policing of QoS class Q on port P uses policer 32+P*8+Q.	0x00

Table 249 • **Fields in POL_CFG *(continued)***

Field Name	Bit	Access	Description	Default
POL_ORDER	8:0	R/W	Each frame is checked against two policers: PORT(0) and QOS(1). In this register, a bit set will make updating of a policer be dependant on the result from another policer. Bit<n+3*m> set means: Policer state <n> is checked before policer <m> is updated. Bit0: Port policer must be open in order to update port policer with frame Bit1: QoS policer must be open in order to update port policer with frame Bit2: Reserved Bit3: Port policer must be open in order to update QoS policer with frame Bit4: QoS policer must be open in order to update QoS policer with frame Bit5-8: Reserved	0x1FF

7.4.4 ANA:COMMON

Parent: ANA

Instances: 1

Table 250 • **Registers in COMMON**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
AGGR_CFG	0x00000000	1	Aggregation code generation	Page 218
CPUQ_CFG	0x00000004	1	CPU extraction queue configuration	Page 219
CPUQ_8021_CFG	0x00000008	16 0x00000004	CPU extraction queue per address of BPDU, GARP, and CCM frames.	Page 220
DSCP_CFG	0x00000048	64 0x00000004	DSCP configuration per DSCP value.	Page 220
DSCP_REWR_CFG	0x00000148	8 0x00000004	DSCP rewrite values per QoS class	Page 221

7.4.4.1 ANA:COMMON:AGGR_CFG

Parent: ANA:COMMON

Instances: 1

Table 251 • **Fields in AGGR_CFG**

Field Name	Bit	Access	Description	Default
AC_RND_ENA	6	R/W	Use pseudo random number for aggregation code. Overrule other contributions.	0x0
AC_DMAC_ENA	5	R/W	Use the lower 12 bits of the destination MAC address for aggregation code.	0x0
AC_SMAC_ENA	4	R/W	Use the lower 12 bits of the source MAC address for aggregation code.	0x0
AC_IP6_FLOW_LBL_ENA	3	R/W	Use the 20-bit IPv6 flow label for aggregation code.	0x0
AC_IP6_TCPUDP_ENA	2	R/W	Use least significant 8 bits of both source port and destination port of IPv6 frames for aggregation code.	0x0
AC_IP4_SIPDIP_ENA	1	R/W	Use least significant 8 bits of both source IP address and destination IP address of IPv4 frames for aggregation code.	0x0
AC_IP4_TCPUDP_ENA	0	R/W	Use least significant 8 bits of both source port and destination port of IPv4 frames for aggregation code.	0x0

7.4.4.2 ANA:COMMON:CPUQ_CFG

Parent: ANA:COMMON

Instances: 1

Table 252 • **Fields in CPUQ_CFG**

Field Name	Bit	Access	Description	Default
CPUQ_MLD	29:27	R/W	CPU extraction queue used for MLD frames.	0x0
CPUQ_IGMP	26:24	R/W	CPU extraction queue used for IGMP frames.	0x0
CPUQ_IPMC_CTRL	23:21	R/W	CPU extraction queue used for IPv4 multicast control frames.	0x0
CPUQ_ALLBRIDGE	20:18	R/W	CPU extraction queue used for allbridge frames (DMAC = 01-80-C2-00-00-10).	0x0
CPUQ_LOCKED_PORTMOVE	17:15	R/W	CPU extraction queue for frames triggering a port move for a locked MAC table entry.	0x0
CPUQ_SRC_COPY	14:12	R/W	CPU extraction queue for frames copied due to CPU_SRC_COPY_ENA	0x0

Table 252 • **Fields in CPUQ_CFG *(continued)***

Field Name	Bit	Access	Description	Default
CPUQ_MAC_COPY	11:9	R/W	CPU extraction queue for frames copied due to CPU_COPY return by MAC table lookup	0x0
CPUQ_LRN	8:6	R/W	CPU extraction queue for frames copied due to learned or moved stations.	0x0
CPUQ_MIRROR	5:3	R/W	CPU extraction queue for frames copied due to mirroring to the CPU.	0x0
CPUQ_SFLOW	2:0	R/W	CPU extraction queue for frames copied due to SFLOW sampling.	0x0

7.4.4.3 ANA:COMMON:CPUQ_8021_CFG

Parent: ANA:COMMON

Instances: 16

Table 253 • **Fields in CPUQ_8021_CFG**

Field Name	Bit	Access	Description	Default
CPUQ_BPDU_VAL	8:6	R/W	CPU extraction queue used for BPDU frames.	0x0
CPUQ_GARP_VAL	5:3	R/W	CPU extraction queue used for GARP frames.	0x0
CPUQ_CCM_VAL	2:0	R/W	CPU extraction queue used for CCM/Link trace frames.	0x0

7.4.4.4 ANA:COMMON:DSCP_CFG

Parent: ANA:COMMON

Instances: 64

Table 254 • **Fields in DSCP_CFG**

Field Name	Bit	Access	Description	Default
QOS_DSCP_VAL	10:8	R/W	Maps the frame's DSCP value to a QoS class. This is enabled in QOS_CFG.QOS_DSCP_ENA.	0x0
DSCP_TRANSLATE_VAL	7:2	R/W	Translated DSCP value triggered if DSCP translation is set for port (QOS_CFG[port].DSCP_TRANSLATE_ENA)	0x00
DSCP_TRUST_ENA	1	R/W	Must be set for a DSCP value if the DSCP value is to be used for QoS classification.	0x0

Table 254 • **Fields in DSCP_CFG *(continued)***

Field Name	Bit	Access	Description	Default
DSCP_REWR_ENA	0	R/W	Set if the DSCP value is selected to be rewritten. This is controlled in QOS_CFG.DSCP_REWR_CFG.	0x0

7.4.4.5 ANA:COMMON:DSCP_REWR_CFG

Parent: ANA:COMMON

Instances: 8

Table 255 • **Fields in DSCP_REWR_CFG**

Field Name	Bit	Access	Description	Default
DSCP_QOS_REWR_VAL	5:0	R/W	Map the frame's QoS class to a DSCP value. DSCP = DSCP_REWR_CFG[QoS class].DSCP_QOS_REWR_VAL. This is controlled in QOS_CFG.DSCP_REWR_CFG and DSCP_CFG.DSCP_REWR_ENA.	0x00

7.5 REW

Table 256 • **Register Groups in REW**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PORT	0x00000000	28 0x00000080	Per port configurations for Rewriter	Page 221
COMMON	0x00000E00	1	Common configurations for Rewriter	Page 224

7.5.1 REW:PORT

Parent: REW

Instances: 28

Table 257 • **Registers in PORT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PORT_VLAN_CFG	0x00000000	1	Port VLAN configuration	Page 222
TAG_CFG	0x00000004	1	Tagging configuration	Page 222
PORT_CFG	0x00000008	1	Special port configuration	Page 223

Table 257 • **Registers in PORT *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
DSCP_CFG	0x0000000C	1	DSCP updates	Page 223
PCP_DEI_QOS_MAP_CFG	0x00000010	8 0x00000004	Mapping of QoS class to PCP and DEI values.	Page 224

7.5.1.1 REW:PORT:PORT_VLAN_CFG

Parent: REW:PORT

Instances: 1

Table 258 • **Fields in PORT_VLAN_CFG**

Field Name	Bit	Access	Description	Default
PORT_TPID	31:16	R/W	Tag Protocol Identifier for port.	0x0000
PORT_DEI	15	R/W	DEI value for port.	0x0
PORT_PCP	14:12	R/W	PCP value for port.	0x0
PORT_VID	11:0	R/W	VID value for port.	0x001

7.5.1.2 REW:PORT:TAG_CFG

Parent: REW:PORT

Instances: 1

Table 259 • **Fields in TAG_CFG**

Field Name	Bit	Access	Description	Default
TAG_CFG	6:5	R/W	Enable VLAN port tagging. 0: Port tagging disabled. 1: Tag all frames, except when VID=PORT_VLAN_CFG.PORT_VID or VID=0. 2: Tag all frames, except when VID=0. 3: Tag all frames.	0x0
TAG_TPID_CFG	4:3	R/W	Select TPID EtherType in port tag. 0: Use 0x8100. 1: Use 0x88A8. 2: Use custom value from PORT_VLAN_CFG.PORT_TPID. 3: Use PORT_VLAN_CFG.PORT_TPID, unless ingress tag was a C-tag (EtherType = 0x8100)	0x0

Table 259 • **Fields in TAG_CFG *(continued)***

Field Name	Bit	Access	Description	Default
TAG_QOS_CFG	1:0	R/W	Select PCP/DEI fields in port tag. 0: Use classified PCP/DEI values. 1: Reserved. 2: Use PCP/DEI values from port VLAN tag in PORT_VLAN_CFG. 3: Use QoS class mapped to PCP/DEI values (PCP_DEI_QOS_MAP_CFG).	0x0

7.5.1.3 REW:PORT:PORT_CFG

Parent: REW:PORT

Instances: 1

Table 260 • **Fields in PORT_CFG**

Field Name	Bit	Access	Description	Default
IFH_INSERT_ENA	7	R/W	Insert IFH into frame (mainly for CPU ports)	0x0
IFH_INSERT_MODE	6	R/W	Select the position of IFH in the generated frames when IFH_INSERT_ENA is set 0: IFH written before DMAC. 1: IFH written after SMAC.	0x0
FCS_UPDATE_NONCPU_CFG	5:4	R/W	FCS update mode for frames not received on the CPU port. 0: Update FCS if frame data has changed 1: Never update FCS 2: Always update FCS	0x0
FCS_UPDATE_CPU_ENA	3	R/W	If set, update FCS for all frames injected by the CPU. If cleared, never update the FCS.	0x1
FLUSH_ENA	2	R/W	If set, all frames destined for the egress port are discarded. **Note** Flushing must be disabled on ports operating in half-duplex mode.	0x0
AGE_DIS	1	R/W	Disable frame ageing for this egress port. **Note** Frame ageing must be disabled on ports operating in half-duplex mode.	0x0

7.5.1.4 REW:PORT:DSCP_CFG

Parent: REW:PORT

Instances: 1

Table 261 • **Fields in DSCP_CFG**

Field Name	Bit	Access	Description	Default
DSCP_REWR_CFG	1:0	R/W	Egress DSCP rewrite. 0: No update of DSCP value in frame. 1: Update with DSCP value from analyzer. 2: Update with DSCP value from analyzer remapped through DSCP_REMAP_CFG.	0x0

7.5.1.5 REW:PORT:PCP_DEI_QOS_MAP_CFG

Parent: REW:PORT

Instances: 8

Table 262 • **Fields in PCP_DEI_QOS_MAP_CFG**

Field Name	Bit	Access	Description	Default
DEI_QOS_VAL	3	R/W	Map the frame's QoS class to a DEI value. DEI = PCP_DEI_QOS_MAP_CFG[QoS class].DEI_QOS_VAL. This must be enabled in VLAN_CFG.QOS_CFG.	0x0
PCP_QOS_VAL	2:0	R/W	Map the frame's QoS class to a PCP value. PCP = PCP_DEI_QOS_MAP_CFG[QoS class].PCP_QOS_VAL. This must be enabled in VLAN_CFG.QOS_CFG.	0x0

7.5.2 REW:COMMON

Parent: REW

Instances: 1

Table 263 • **Registers in COMMON**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
DSCP_REMAP_CFG	0x00000100	64 0x00000004	Remap table of DSCP values.	Page 224

7.5.2.1 REW:COMMON:DSCP_REMAP_CFG

Parent: REW:COMMON

Instances: 64

Table 264 • **Fields in DSCP_REMAP_CFG**

Field Name	Bit	Access	Description	Default
DSCP_REMAP_VAL	5:0	R/W	One to one DSCP remapping table common for all ports. This table is used when DSCP_CFG.DSCP_REWR_ENA=2.	0x00

7.6 DEVCPU_GCB

Table 265 • **Register Groups in DEVCPU_GCB**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
CHIP_REGS	0x00000000	1		Page 225
SW_REGS	0x00000014	1	Registers for software/software interaction	Page 227
VCORE_ACCESS	0x00000054	1		Page 231
GPIO	0x00000068	1		Page 234
DEVCPU_RST_REGS	0x00000090	1		Page 237
MIIM	0x000000A0	2 0x00000024		Page 239
MIIM_READ_SCAN	0x000000E8	1		Page 243
RAM_STAT	0x00000114	1		Page 244
MISC	0x00000118	1	Miscellaneous Registers	Page 244
SIO_CTRL	0x00000130	1	Serial IO control configuration	Page 247
FAN_CFG	0x000001F0	1	Configuration register for the fan controller	Page 252
FAN_STAT	0x000001F4	1	Fan controller statistics	Page 253
MEMITGR	0x00000234	1	Memory integrity monitor	Page 253

7.6.1 DEVCPU_GCB:CHIP_REGS

Parent: DEVCPU_GCB

Instances: 1

Table 266 • **Registers in CHIP_REGS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GENERAL_PURPOSE	0x00000000	1	general purpose register	Page 226

Table 266 • **Registers in CHIP_REGS *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SI	0x00000004	1	SI registers	Page 226
CHIP_ID	0x00000008	1	Chip Id	Page 227

7.6.1.1 DEVCPU_GCB:CHIP_REGS:GENERAL_PURPOSE

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

Table 267 • **Fields in GENERAL_PURPOSE**

Field Name	Bit	Access	Description	Default
GENERAL_PURPOSE_REG	31:0	R/W	This is a general-purpose register that can be used for testing. The value in this register has no functionality other than general purpose storage.	0x00000000

7.6.1.2 DEVCPU_GCB:CHIP_REGS:SI

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

Configuration of serial interface data format. This register modifies how the SI receives and transmits data, when configuring this register first write 0 (to get to a known state), then configure the desired values.

Table 268 • **Fields in SI**

Field Name	Bit	Access	Description	Default
SI_LSB	5	R/W	Setup SI to use MSB or LSB first. See datasheet for more information. 0: SI expect/transmit MSB first 1: SI expect/transmit LSB first	0x0
SI_ENDIAN	4	R/W	Setup SI to use either big or little endian data format. See datasheet for more information. 0: SI uses little endian notation 1: SI uses big endian notation	0x1
SI_WAIT_STATES	3:0	R/W	Configure the number of padding bytes that the SI must insert before transmitting read-data during reading from the device. 0 : don't insert any padding 1 : Insert 1 byte of padding ... 15: Insert 15 bytes of padding	0x0

7.6.1.3 DEVCPU_GCB:CHIP_REGS:CHIP_ID

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

Table 269 • **Fields in CHIP_ID**

Field Name	Bit	Access	Description	Default
REV_ID	31:28	R/O	Revision ID.	0x3
PART_ID	27:12	R/O	Part ID. VSC7420-02 VSC7421-02 VSC7422-02	 0x7420 0x7421 0x7422
MFG_ID	11:1	R/O	Manufacturer's ID.	0x074
ONE	0	R/O	Returns '1'	0x1

7.6.2 DEVCPU_GCB:SW_REGS

Parent: DEVCPU_GCB

Instances: 1

Table 270 • **Registers in SW_REGS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SEMA_INTR_ENA	0x00000000	1	Semaphore SW interrupt enable	Page 227
SEMA_INTR_ENA_CLR	0x00000004	1	Clear of semaphore SW interrupt enables	Page 228
SEMA_INTR_ENA_SET	0x00000008	1	Masking of semaphore	Page 228
SEMA	0x0000000C	8 0x00000004	Semaphore register	Page 229
SEMA_FREE	0x0000002C	1	Semaphore status	Page 229
SW_INTR	0x00000030	1	Manually assert software interrupt	Page 229
MAILBOX	0x00000034	1	Mailbox register	Page 230
MAILBOX_CLR	0x00000038	1	Mailbox register atomic clear	Page 230
MAILBOX_SET	0x0000003C	1	Mailbox register atomic set	Page 230

7.6.2.1 DEVCPU_GCB:SW_REGS:SEMA_INTR_ENA

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 271 • **Fields in SEMA_INTR_ENA**

Field Name	Bit	Access	Description	Default
SEMA_INTR_IDENT	15:8	R/O	This is a bitwise AND of SEMA_FREE and SEMA_INTR_ENA providing an fast access to the cause of an interrupt, given the current mask.	0x00
SEMA_INTR_ENA	7:0	R/W	Set bits in this register to enable interrupt when the corresponding semaphore is free. In a multi-threaded environment, or with more than one active processor the CPU_SEMA_ENA_SET and CPU_SEMA_ENA_CLR registers can be used for atomic modifications of this register. If interrupt is enabled for a particular semaphore, then software interrupt will be asserted for as long as the semaphore is free (and interrupt is enabled for that semaphore). The lower half of the available semaphores are connected to software Interrupt 0 (SW0), the upper half is connected to software interrupt 1 (SW1).	0x00

7.6.2.2 DEVCPU_GCB:SW_REGS:SEMA_INTR_ENA_CLR

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 272 • **Fields in SEMA_INTR_ENA_CLR**

Field Name	Bit	Access	Description	Default
SEMA_INTR_ENA_CLR	7:0	One-shot	Set to clear corresponding interrupt enable in SEMA_INTR_ENA.	0x00

7.6.2.3 DEVCPU_GCB:SW_REGS:SEMA_INTR_ENA_SET

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 273 • **Fields in SEMA_INTR_ENA_SET**

Field Name	Bit	Access	Description	Default
SEMA_INTR_ENA_SET	7:0	One-shot	Set to set corresponding interrupt enable in SEMA_INTR_ENA.	0x00

7.6.2.4 DEVCPU_GCB:SW_REGS:SEMA

Parent: DEVCPU_GCB:SW_REGS

Instances: 8

Table 274 • **Fields in SEMA**

Field Name	Bit	Access	Description	Default
SEMA	0	R/W	General Semaphore.The process to read this field will read a '1' and thus be granted the semaphore. The semaphore is released by the interface by writing a '1' to this field. Read : '0': Semaphore was not granted. '1': Semaphore was granted. Write : '0': No action. '1': Release semaphore.	0x1

7.6.2.5 DEVCPU_GCB:SW_REGS:SEMA_FREE

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 275 • **Fields in SEMA_FREE**

Field Name	Bit	Access	Description	Default
SEMA_FREE	7:0	R/O	Show which semaphores that are currently free. '0' : Corresponding semaphore is taken. '1' : Corresponding semaphore is free.	0xFF

7.6.2.6 DEVCPU_GCB:SW_REGS:SW_INTR

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

This register provides a simple interface for interrupting on either software interrupt 0 or 1, without implementing semaphore support. Note: setting this field causes a short pulse on the corresponding interrupt connection, this kind of interrupt cannot be used in combination with the SW1_INTR_CONFIG.SW1_INTR_BYPASS feature.

Table 276 • **Fields in SW_INTR**

Field Name	Bit	Access	Description	Default
SW1_INTR	1	One-shot	Set this field to inject software interrupt 1. This field is automatically cleared after interrupt has been generated.	0x0
SW0_INTR	0	One-shot	Set this field to assert software interrupt 0. This field is automatically cleared after interrupt has been generated.	0x0

7.6.2.7 DEVCPU_GCB:SW_REGS:MAILBOX

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 277 • **Fields in MAILBOX**

Field Name	Bit	Access	Description	Default
MAILBOX	31:0	R/W	Read/write register. Atomic modifications can be performed by using the MAILBOX_CLR and MAILBOX_SET registers.	0x00000000

7.6.2.8 DEVCPU_GCB:SW_REGS:MAILBOX_CLR

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 278 • **Fields in MAILBOX_CLR**

Field Name	Bit	Access	Description	Default
MAILBOX_CLR	31:0	One-shot	Set bits in this register to atomically clear corresponding bits in the MAILBOX register. This register returns 0 on read.	0x00000000

7.6.2.9 DEVCPU_GCB:SW_REGS:MAILBOX_SET

Parent: DEVCPU_GCB:SW_REGS

Instances: 1

Table 279 • **Fields in MAILBOX_SET**

Field Name	Bit	Access	Description	Default
MAILBOX_SET	31:0	One-shot	Set bits in this register to atomically set corresponding bits in the MAILBOX register. This register returns 0 on read.	0x00000000

7.6.3 DEVCPU_GCB:VCORE_ACCESS

Parent: DEVCPU_GCB

Instances: 1

Table 280 • **Registers in VCORE_ACCESS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VA_CTRL	0x00000000	1	Control register for VCore accesses	Page 231
VA_ADDR	0x00000004	1	Address register for VCore accesses	Page 232
VA_DATA	0x00000008	1	Data register for VCore accesses	Page 233
VA_DATA_INCR	0x0000000C	1	Data register for VCore accesses (w. auto increment of address)	Page 234
VA_DATA_INERT	0x00000010	1	Data register for VCore accesses (will not initiate access)	Page 234

7.6.3.1 DEVCPU_GCB:VCORE_ACCESS:VA_CTRL

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

Table 281 • **Fields in VA_CTRL**

Field Name	Bit	Access	Description	Default
VA_ERR_RD	3	R/O	This field is set to the value of VA_CTRL:VA_ERR whenever one of the data registers ACC_DATA, ACC_DATA_INCR, or ACC_DATA_RO is read. By reading this field it is possible to determine if the last read-value from one of these registers was erred.	0x0

Table 281 • **Fields in VA_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
VA_ERR	2	R/O	This field is set if the access inside the VCore domain was terminated by an error. This situation can occur when accessing an unmapped part of the VCore memory-map or when accessing a target that reports error (e.g. accessing uninitialized DDR2 memory). If an error occurs during reading, the read-data will be 0x80000000. So as an optimization, software only has to check for error if 0x80000000 is returned (and in that case VA_ERR_RD should be checked). When writing you should always check if successful.	0x0
VA_BUSY_RD	1	R/O	This field is set to the value of VA_CTRL:VA_BUSY whenever one of the data registers ACC_DATA, ACC_DATA_INCR, or ACC_DATA_RO is read. By reading this field it is possible to determine if the last read-value from one of these registers was valid.	0x0
VA_BUSY	0	R/O	This field is set by hardware when an access into VCore domain is started, and cleared when the access is done.	0x0

7.6.3.2 DEVCPU_GCB:VCORE_ACCESS:VA_ADDR

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

Table 282 • **Fields in VA_ADDR**

Field Name	Bit	Access	Description	Default
VA_ADDR	31:0	R/W	The address to access in the VCore domain, all addresses must be 32-bit aligned (i.e. the two least significant bit must always be 0). When accesses are initiated using the ACC_DATA_INCR register, then this field is automatically incremented by 4 at the end of the transfer. The memory region of the VCore that maps to switch-core registers may not be accessed by using these registers.	0x00000000

7.6.3.3 DEVCPU_GCB:VCORE_ACCESS:VA_DATA

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

The VA_DATA, VA_DATA_INCR, and VA_DATA_INERT registers are used for indirect access into the VCore domain. The functionality of the VA_DATA_INCR and VA_DATA_INERT registers are similar to this register - but with minor exceptions. These exceptions are fleshed out in the description of the respective registers.

Table 283 • **Fields in VA_DATA**

Field Name	Bit	Access	Description	Default
VA_DATA	31:0	R/W	Reading or writing from/to this field initiates accesses into the VCore domain. While an access is ongoing (VA_CTRL:VA_BUSY is set) this field may not be written. It is possible to read this field while an access is ongoing, but the data returned will be 0x80000000. When writing to this field; a write into the VCore domain is initiated to the address specified in the VA_ADDR register, with the data that was written to this field. Only 32-bit writes are supported. This field may not be written to until the VA_CTRL:VA_BUSY indicates that no accesses is ongoing. When reading from this field; a read from the VCore domain is initiated from the address specified in the VA_ADDR register. Important: The data that is returned from reading this field (and stating an access) is not the result of the newly initiated read, instead the data from the last access is returned. The result of the newly initiated read access will be ready once the VA_CTRL:VA_BUSY field shows that the access is done. Note: When the result of a read-access is read from this field (the second read), a new access will automatically be initiated. This is desirable when reading a series of addresses from VCore domain. If a new access is not desirable, then the result should be read from the VA_DATA_INERT register instead of this field!	0x00000000

7.6.3.4 DEVCPU_GCB:VCORE_ACCESS:VA_DATA_INCR

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

Table 284 • **Fields in VA_DATA_INCR**

Field Name	Bit	Access	Description	Default
VA_DATA_INCR	31:0	R/W	This field behaves in the same way as ACC_DATA:ACC_DATA. Except when an access is initiated by using this field (either read or write); the address register (ACC_ADDR) is automatically incremented by 4 at the end of the access, i.e. when VA_CTRL:VA_BUSY is deasserted.	0x00000000

7.6.3.5 DEVCPU_GCB:VCORE_ACCESS:VA_DATA_INERT

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

Table 285 • **Fields in VA_DATA_INERT**

Field Name	Bit	Access	Description	Default
VA_DATA_INERT	31:0	R/W	This field behaves in the same way as ACC_DATA:ACC_DATA. Except accesses (read or write) does not initiate VCore accesses. Writing to this register just overwrites the value currently held by all of the data registers (ACC_DATA, ACC_DATA_INCR, and ACC_DATA_INERT).	0x00000000

7.6.4 DEVCPU_GCB:GPIO

Parent: DEVCPU_GCB

Instances: 1

General Purpose I/O Control configuration and status registers.

Each register in this group contains one field with one bit per GPIO pin. Bit 0 in each field corresponds to GPIO0, bit 1 to GPIO1, and so on.

Table 286 • **Registers in GPIO**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPIO_OUT_SET	0x00000000	1	GPIO output set	Page 235

Table 286 • **Registers in GPIO *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPIO_OUT_CLR	0x00000004	1	GPIO output clear	Page 235
GPIO_OUT	0x00000008	1	GPIO output	Page 235
GPIO_IN	0x0000000C	1	GPIO input	Page 236
GPIO_OE	0x00000010	1	GPIO pin direction	Page 236
GPIO_INTR	0x00000014	1	GPIO interrupt	Page 236
GPIO_INTR_ENA	0x00000018	1	GPIO interrupt enable	Page 237
GPIO_INTR_IDENT	0x0000001C	1	GPIO interrupt identity	Page 237
GPIO_ALT	0x00000020	1	GPIO alternate functions	Page 237

7.6.4.1 DEVCPU_GCB:GPIO:GPIO_OUT_SET

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 287 • **Fields in GPIO_OUT_SET**

Field Name	Bit	Access	Description	Default
G_OUT_SET	31:0	One-shot	Setting a bit in this field will immediately set the corresponding bit in GPIO_O::G_OUT. Reading this register always return 0. '0': No change '1': Corresponding bit in GPIO_O::OUT is set.	0x00000000

7.6.4.2 DEVCPU_GCB:GPIO:GPIO_OUT_CLR

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 288 • **Fields in GPIO_OUT_CLR**

Field Name	Bit	Access	Description	Default
G_OUT_CLR	31:0	One-shot	Setting a bit in this field will immediately clear the corresponding bit in GPIO_O::G_OUT. Reading this register always return 0. '0': No change '1': Corresponding bit in GPIO_O::OUT is cleared.	0x00000000

7.6.4.3 DEVCPU_GCB:GPIO:GPIO_OUT

Parent: DEVCPU_GCB:GPIO

Instances: 1

In a multi-threaded software environment using the registers GPIO_OUT_SET and GPIO_OUT_CLR for modifying GPIO values removes the need for software-locked access.

Table 289 • **Fields in GPIO_OUT**

Field Name	Bit	Access	Description	Default
G_OUT	31:0	R/W	Controls the value on the GPIO pins enabled for output (via the GPIO_OE register). This field can be modified directly or by using the GPIO_O_SET and GPIO_O_CLR registers.	0x00000000

7.6.4.4 DEVCPU_GCB:GPIO:GPIO_IN

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 290 • **Fields in GPIO_IN**

Field Name	Bit	Access	Description	Default
G_IN	31:0	R/O	GPIO input register. Reflects the current state of the corresponding GPIO pins.	0x00000000

7.6.4.5 DEVCPU_GCB:GPIO:GPIO_OE

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 291 • **Fields in GPIO_OE**

Field Name	Bit	Access	Description	Default
G_OE	31:0	R/W	Configures the direction of the GPIO pins. '0': Input '1': Output	0x00000000

7.6.4.6 DEVCPU_GCB:GPIO:GPIO_INTR

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 292 • **Fields in GPIO_INTR**

Field Name	Bit	Access	Description	Default
G_INTR	31:0	Sticky	Indicates whether a GPIO input has changed since last clear. '0': No change '1': GPIO has changed	0x00000000

7.6.4.7 DEVCPU_GCB:GPIO:GPIO_INTR_ENA

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 293 • **Fields in GPIO_INTR_ENA**

Field Name	Bit	Access	Description	Default
G_INTR_ENA	31:0	R/W	Enables individual GPIO pins for interrupt.	0x00000000

7.6.4.8 DEVCPU_GCB:GPIO:GPIO_INTR_IDENT

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 294 • **Fields in GPIO_INTR_IDENT**

Field Name	Bit	Access	Description	Default
G_INTR_IDENT	31:0	R/O	Shows which GPIO sources that are currently interrupting. This field is the result of an AND-operation between the GPIO_INTR and the GPIO_INTR_ENA registers.	0x00000000

7.6.4.9 DEVCPU_GCB:GPIO:GPIO_ALT

Parent: DEVCPU_GCB:GPIO

Instances: 1

Table 295 • **Fields in GPIO_ALT**

Field Name	Bit	Access	Description	Default
G_ALT	31:0	R/W	Configures alternate functions for individual GPIO bits. 0: GPIO mode 1: Alternate mode	0x00000000

7.6.5 DEVCPU_GCB:DEVCPU_RST_REGS

Parent: DEVCPU_GCB

Instances: 1

Resets the chip

Table 296 • **Registers in DEVCPU_RST_REGS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SOFT_CHIP_RST	0x00000000	1	Reset part or the whole chip	Page 238
SOFT_DEVCPU_RST	0x00000004	1	Soft reset of devcpu.	Page 238

7.6.5.1 DEVCPU_GCB:DEVCPU_RST_REGS:SOFT_CHIP_RST

Parent: DEVCPU_GCB:DEVCPU_RST_REGS

Instances: 1

Table 297 • **Fields in SOFT_CHIP_RST**

Field Name	Bit	Access	Description	Default
SOFT_PHY_RST	1	R/W	Clear this field to release reset in the Cu-PHY. This field is automatically set during hard-reset and soft-reset of the chip. After reset is released the PHY will indicate when it is ready to be accessed via DEVCPU_GCB::MISC_STAT.PHY_READY.	0x1
SOFT_CHIP_RST	0	R/W	Set this field to reset the whole chip. This field is automatically cleared by the reset. Note: It is possible for the VCore to protect itself from soft-reset of the chip, for more info see RESET.CORE_RST_PROTECT inside the VCore register space.	0x0

7.6.5.2 DEVCPU_GCB:DEVCPU_RST_REGS:SOFT_DEVCPU_RST

Parent: DEVCPU_GCB:DEVCPU_RST_REGS

Instances: 1

Table 298 • **Fields in SOFT_DEVCPU_RST**

Field Name	Bit	Access	Description	Default
SOFT_XTR_RST	1	R/W	Set this field to reset the extraction logic. The reset remains asserted until this field is cleared. Note: Extraction logic is also reset while SOFT_CHIP_RST.SOFT_NON_CFG_RST is set.	0x0

Table 298 • **Fields in SOFT_DEVCPU_RST *(continued)***

Field Name	Bit	Access	Description	Default
SOFT_INJ_RST	0	R/W	Set this field to reset the injection logic. The reset remains asserted until this field is cleared. Note: Injection logic is also reset while SOFT_CHIP_RST.SOFT_NON_CFG_RST is set.	0x0

7.6.6 DEVCPU_GCB:MIIM

Parent: DEVCPU_GCB

Instances: 2

Table 299 • **Registers in MIIM**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MII_STATUS	0x00000000	1	MIIM Status	Page 239
MII_CMD	0x00000008	1	MIIM Command	Page 240
MII_DATA	0x0000000C	1	MIIM Reply Data	Page 241
MII_CFG	0x00000010	1	MIIM Configuration	Page 241
MII_SCAN_0	0x00000014	1	MIIM Scan 0	Page 242
MII_SCAN_1	0x00000018	1	MIIM Scan 1	Page 242
MII_SCAN_LAST_RSLTS	0x0000001C	1	MIIM Results	Page 242
MII_SCAN_LAST_RSLTS_VLD	0x00000020	1	MIIM Results	Page 243

7.6.6.1 DEVCPU_GCB:MIIM:MII_STATUS

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 300 • **Fields in MII_STATUS**

Field Name	Bit	Access	Description	Default
MIIM_STAT_BUSY	3	R/O	Indicates the current state of the MIIM controller. When read operations are done (no longer busy), then read data is available via the DEVCPU_GCB::MII_DATA register. 0: MIIM controller is in idle state 1: MIIM controller is busy performing MIIM cmd (Either read or read cmd).	0x0

Table 300 • **Fields in MII_STATUS *(continued)***

Field Name	Bit	Access	Description	Default
MIIM_STAT_OPR_PEND	2	R/O	The MIIM controller has a CMD fifo of depth one. When this field is 0, then it is safe to write another MIIM command to the MIIM controller. 0 : Read or write not pending 1 : Read or write pending.	0x0
MIIM_STAT_PENDING_RD	1	R/O	Indicates whether a read operation via the MIIM interface is in progress or not. 0 : Read not in progress 1 : Read in progress.	0x0
MIIM_STAT_PENDING_WR	0	R/O	Indicates whether a write operation via the MIIM interface is in progress or not. 0 : Write not in progress 1 : Write in progress.	0x0
MIIM_SCAN_COMPLETE	4	R/O	Signals if all PHYs have been scanned (with auto scan) at least once. 0 : Auto scan has not scanned all PHYs. 1 : Auto scan has scanned all PHY at least once.	0x0

7.6.6.2 DEVCPU_GCB:MIIM:MII_CMD

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 301 • **Fields in MII_CMD**

Field Name	Bit	Access	Description	Default
MIIM_CMD_VLD	31	One-shot	Must be set for starting a new PHY access. This bit is automatically cleared. 0 : Write to this register is ignored. 1 : Write to this register is processed.	0x0
MIIM_CMD_PHYAD	29:25	R/W	Indicates the addressed PHY number.	0x00
MIIM_CMD_REGAD	24:20	R/W	Indicates the addressed of the register within the PHY that shall be accessed.	0x00
MIIM_CMD_WRDATA	19:4	R/W	Data to be written in the PHY register.	0x0000

Table 301 • **Fields in MII_CMD *(continued)***

Field Name	Bit	Access	Description	Default
MIIM_CMD_SINGLE_SCAN	3	R/W	Select if scanning of the PHY shall be done once, or scanning should be done continuously. 0 : Do continuously PHY scanning 1 : Stop once all PHY have been scanned.	0x0
MIIM_CMD_OPR_FIELD	2:1	R/W	Indicates type of operation. Clause 22: 01 : Write 10 : Read Clause 45: 00 : Address 01 : Write 10 : Read inc. 11 : Read.	0x0
MIIM_CMD_SCAN	0	R/W	Indicates whether automatic scanning of PHY registers is enabled. When enabled, the PHY-number for each automatic read is continuously round-robined from PHY_ADDR_LOW through PHY_ADDR_HIGH. This function is started upon a read operation (ACCESS_TYPE). Scan MUST be disabled when doing any configuration of the MIIM controller. 0 : Disabled 1 : Enabled.	0x0

7.6.6.3 DEVCPU_GCB:MIIM:MII_DATA

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 302 • **Fields in MII_DATA**

Field Name	Bit	Access	Description	Default
MIIM_DATA_SUCCESS	17:16	R/O	Indicates whether a read operation failed or succeeded. 00 : OK 11 : Error	0x0
MIIM_DATA_RDDATA	15:0	R/O	Data read from PHY register.	0x0000

7.6.6.4 DEVCPU_GCB:MIIM:MII_CFG

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 303 • **Fields in MII_CFG**

Field Name	Bit	Access	Description	Default
MIIM_CFG_PRESCALE	7:0	R/W	Configures the MIIM clock frequency. This is computed as system_clk/(2*(1+X)), where X is the value written to this register. Note : Setting X to 0 is invalid and will result in the same frequency as setting X to 1.	0x32
MIIM_ST_CFG_FIELD	10:9	R/W	The ST (start-of-frame) field of the MIIM frame format adopts the value of this field. This must be configured for either clause 22 or 45 MIIM operation. "01": Clause 22 "00": Clause 45 Other values are reserved.	0x1

7.6.6.5 DEVCPU_GCB:MIIM:MII_SCAN_0

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 304 • **Fields in MII_SCAN_0**

Field Name	Bit	Access	Description	Default
MIIM_SCAN_PHYADHI	9:5	R/W	Indicates the high PHY number to scan during automatic scanning.	0x00
MIIM_SCAN_PHYADLO	4:0	R/W	Indicates the low PHY number to scan during automatic scanning.	0x00

7.6.6.6 DEVCPU_GCB:MIIM:MII_SCAN_1

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 305 • **Fields in MII_SCAN_1**

Field Name	Bit	Access	Description	Default
MIIM_SCAN_MASK	31:16	R/W	Indicates the mask for comparing the PHY registers during automatic scan.	0x0000
MIIM_SCAN_EXPECT	15:0	R/W	Indicates the expected value for comparing the PHY registers during automatic scan.	0x0000

7.6.6.7 DEVCPU_GCB:MIIM:MII_SCAN_LAST_RSLTS

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 306 • **Fields in MII_SCAN_LAST_RSLTS**

Field Name	Bit	Access	Description	Default
MIIM_LAST_RSLT	31:0	R/O	Indicates for each PHY if a PHY register has matched the expected value (with mask). This register reflects the value of the last reading of the phy register. 0 : Mismatch. 1 : Match.	0x00000000

7.6.6.8 DEVCPU_GCB:MIIM:MII_SCAN_LAST_RSLTS_VLD

Parent: DEVCPU_GCB:MIIM

Instances: 1

Table 307 • **Fields in MII_SCAN_LAST_RSLTS_VLD**

Field Name	Bit	Access	Description	Default
MIIM_LAST_RSLT_VLD	31:0	R/O	Indicates for each PHY if a PHY register matched are valid or not. 0 : Scan result not valid. 1 : Scan result valid.	0x00000000

7.6.7 DEVCPU_GCB:MIIM_READ_SCAN

Parent: DEVCPU_GCB

Instances: 1

Table 308 • **Registers in MIIM_READ_SCAN**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MII_SCAN_RSLTS_STICKY	0x00000000	2 0x00000004	MIIM Results	Page 243

7.6.7.1 DEVCPU_GCB:MIIM_READ_SCAN:MII_SCAN_RSLTS_STICKY

Parent: DEVCPU_GCB:MIIM_READ_SCAN

Instances: 2

Table 309 • **Fields in MII_SCAN_RSLTS_STICKY**

Field Name	Bit	Access	Description	Default
MIIM_SCAN_RSLTS_STICKY	31:0	R/O	Indicates for each PHY if a PHY register has had a mismatch of the expected value (with mask) since last reading of MIIM_SCAN_RSLTS_STICKY. Result is sticky, and result will indicate if there has been a mismatch since the last reading of this register. Upon reading this register, all bits are reset to '1'. 0 : Mismatch 1 : Match.	0x00000000

7.6.8 DEVCPU_GCB:RAM_STAT

Parent: DEVCPU_GCB

Instances: 1

Table 310 • **Registers in RAM_STAT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RAM_INTEGRITY_ERR_STICKY	0x00000000	1	QS RAM status	Page 244

7.6.8.1 DEVCPU_GCB:RAM_STAT:RAM_INTEGRITY_ERR_STICKY

Parent: DEVCPU_GCB:RAM_STAT

Instances: 1

Table 311 • **Fields in RAM_INTEGRITY_ERR_STICKY**

Field Name	Bit	Access	Description	Default
QS_XTR_RAM_INTGR_ERR_STICKY	0	Sticky	Integrity error for QS_XTR RAM '0': No RAM integrity check error occurred '1': A RAM integrity check error occurred Bit is cleared by writing a '1' to this position.	0x0

7.6.9 DEVCPU_GCB:MISC

Parent: DEVCPU_GCB

Instances: 1

Table 312 • **Registers in MISC**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MISC_CFG	0x00000000	1	Miscellaneous Configuration Register	Page 245
MISC_STAT	0x00000004	1		Page 245
PHY_SPEED_1000_STAT	0x00000008	1		Page 246
PHY_SPEED_100_STAT	0x0000000C	1		Page 246
PHY_SPEED_10_STAT	0x00000010	1		Page 246
DUPLEXC_PORT_STAT	0x00000014	1		Page 246

7.6.9.1 DEVCPU_GCB:MISC:MISC_CFG

Parent: DEVCPU_GCB:MISC

Instances: 1

Register to control various muxing in the IO-ring.

Table 313 • **Fields in MISC_CFG**

Field Name	Bit	Access	Description	Default
SW_MODE	7:6	R/W	Set the sw_mode for HSIO. 0: Use for VSC7421-02 (12x CuPHY + 1x QSGMII + 1x 2.5G SGMII) and VSC7422-02. 1: Use for VSC7420-02 and VSC7421-02 (12x CuPHY + 2x 1G SGMII + 2x 2.5G SGMII). 2: Reserved. 3: Reserved.	0x0
QSGMII_FLIP_LANE1	5	R/W	Flip or swap lanes in QSGMII#1.	0x0
QSGMII_FLIP_LANE2	4	R/W	Flip or swap lanes in QSGMII#2.	0x0
QSGMII_FLIP_LANE3	3	R/W	Flip or swap lanes in QSGMII#3.	0x0
QSGMII_SHYST_DIS	2	R/W	Disable hysteresis of synchronization state machine.	0x0
QSGMII_E_DET_ENA	1	R/W	Enable 8b10b error propagation (8b10b error code-groups are replaced by K70.7 error symbols.	0x0
QSGMII_USE_I1_ENA	0	R/W	Use I1 during idle sequencing only.	0x0

7.6.9.2 DEVCPU_GCB:MISC:MISC_STAT

Parent: DEVCPU_GCB:MISC

Instances: 1

Table 314 • **Fields in MISC_STAT**

Field Name	Bit	Access	Description	Default
PHY_READY	3	R/O	This field is set high when the PHY is ready for access after release of PHY reset via DEVCPU_GCB::SOFT_CHIP_RST.SOFT_PHY_RST.	0x0

7.6.9.3 DEVCPU_GCB:MISC:PHY_SPEED_1000_STAT

Parent: DEVCPU_GCB:MISC

Instances: 1

Table 315 • **Fields in PHY_SPEED_1000_STAT**

Field Name	Bit	Access	Description	Default
SPEED_1000	11:0	R/O	p2m_speed1000c status from PHY	0x000

7.6.9.4 DEVCPU_GCB:MISC:PHY_SPEED_100_STAT

Parent: DEVCPU_GCB:MISC

Instances: 1

Table 316 • **Fields in PHY_SPEED_100_STAT**

Field Name	Bit	Access	Description	Default
SPEED_100	11:0	R/O	p2m_speed100 status from PHY	0x000

7.6.9.5 DEVCPU_GCB:MISC:PHY_SPEED_10_STAT

Parent: DEVCPU_GCB:MISC

Instances: 1

Table 317 • **Fields in PHY_SPEED_10_STAT**

Field Name	Bit	Access	Description	Default
SPEED_10	11:0	R/O	p2m_speed10 status from PHY	0x000

7.6.9.6 DEVCPU_GCB:MISC:DUPLEXC_PORT_STAT

Parent: DEVCPU_GCB:MISC

Instances: 1

Table 318 • **Fields in DUPLEXC_PORT_STAT**

Field Name	Bit	Access	Description	Default
DUPLEXC	11:0	R/O	p2m_duplexc_port status from PHY	0x000

7.6.10 DEVCPU_GCB:SIO_CTRL

Parent: DEVCPU_GCB

Instances: 1

Table 319 • **Registers in SIO_CTRL**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SIO_INPUT_DATA	0x00000000	4 0x00000004	Input data registers	Page 247
SIO_INT_POL	0x00000010	4 0x00000004	Interrupt polarity for each GPIO	Page 248
SIO_PORT_INT_ENA	0x00000020	1	Interrupt enable register for each port.	Page 248
SIO_PORT_CONFIG	0x00000024	32 0x00000004	Configuration of output data values	Page 248
SIO_PORT_ENABLE	0x000000A4	1	Port enable register	Page 249
SIO_CONFIG	0x000000A8	1	General configuration register	Page 249
SIO_CLOCK	0x000000AC	1	Configuration of the serial IO clock frequency	Page 251
SIO_INT_REG	0x000000B0	4 0x00000004	Interrupt register	Page 251

7.6.10.1 DEVCPU_GCB:SIO_CTRL:SIO_INPUT_DATA

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

Table 320 • **Fields in SIO_INPUT_DATA**

Field Name	Bit	Access	Description	Default
S_IN	31:0	R/O	Serial input data. The first replication holds bit 0 from all ports, the 2nd replication holds bit 1 from all ports, etc. Values of disabled gpios are undefined. bit order: (port-31 bit-n down to port-0 bit-n)	0x00000000

7.6.10.2 DEVCPU_GCB:SIO_CTRL:SIO_INT_POL

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

Table 321 • **Fields in SIO_INT_POL**

Field Name	Bit	Access	Description	Default
INT_POL	31:0	R/W	Interrupt polarity. Bit n from all ports. This register defines at which logic value an interrupt is generated. For bit 0, this register is also used to define the polarity of the "loss of signal" output. 0 : interrupt at logic value '1' 1 : interrupt at logic value '0' For "loss of signal": 0 : "loss of signal" is active high 1: "loss of signal" is active low	0x00000000

7.6.10.3 DEVCPU_GCB:SIO_CTRL:SIO_PORT_INT_ENA

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

Table 322 • **Fields in SIO_PORT_INT_ENA**

Field Name	Bit	Access	Description	Default
INT_ENA	31:0	R/W	Interrupt enable vector with one enable bit for each port. 0 : Interrupt is disabled for the port. 1 : Interrupt is enabled for the port. port order: (portN down to port0)	0x00000000

7.6.10.4 DEVCPU_GCB:SIO_CTRL:SIO_PORT_CONFIG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 32

Table 323 • **Fields in SIO_PORT_CONFIG**

Field Name	Bit	Access	Description	Default
BIT_SOURCE	11:0	R/W	Output source select for the four outputs from each port. The source select is encoded using three bits for each output bit. The placement of the source select bits for each output bit in the register: Output bit 0: (2 down to 0) Output bit 1: (5 down to 3) Output bit 2: (8 down to 6) Output bit 3: (11 down to 9) Source select encoding for each output bit: 0 : Forced '0' 1 : Forced '1' 2 : Blink mode 0 3 : Blink mode 1 4 : Link activity blink mode 0 5 : Link activity blink mode 1 6 : Link activity blink mode 0 inversed polarity 7 : Link activity blink mode 1 inversed polarity	0x000

7.6.10.5 DEVCPU_GCB:SIO_CTRL:SIO_PORT_ENABLE

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

Table 324 • **Fields in SIO_PORT_ENABLE**

Field Name	Bit	Access	Description	Default
P_ENA	31:0	R/W	Port enable vector with one enable bit for each port. 0 : Port is disabled. 1 : Port is enabled. Port order: (portN down to port0)	0x00000000

7.6.10.6 DEVCPU_GCB:SIO_CTRL:SIO_CONFIG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

Table 325 • **Fields in SIO_CONFIG**

Field Name	Bit	Access	Description	Default
SIO_BMODE_1	21:20	R/W	Configuration for blink mode 1. Supports three different blink modes and a "burst toggle" mode in which blink mode 1 will alternate for each burst. 0 : Blink freq approximately 20Hz 1 : Blink freq approximately 10Hz. 2 : Blink freq approximately 5Hz. 3 : Burst toggle.	0x0
SIO_BMODE_0	19:18	R/W	Configuration of blink mode 0. Supports four different blink modes. 0 : Blink freq approximately 20Hz. 1 : Blink freq approximately 10Hz. 2 : Blink freq approximately 5Hz. 3 : Blink freq approximately 2.5Hz.	0x0
SIO_BLINK_RESET	17	R/W	Reset the blink counters. Used to synchronize the blink modes between different chips. 0 : Blink counter is running. 1 : Blink counter is reset until sio_blink_reset is unset again.	0x0
SIO_INT_ENA	16:13	R/W	Bit interrupt enable. Enables interrupts for the four gpios in a port. Is applied to all ports. 0: Interrupt is disabled for bit n for all ports. 1: Interrupt is enabled for bit n for all ports.	0x0
SIO_BURST_GAP_DIS	12	R/W	Set to disable burst gap.	0x0
SIO_BURST_GAP	11:7	R/W	Configures the length of burst gap in steps of approx. 1 ms. Burst gap can be disabled by setting SIO_CONFIG.SIO_BURST_GAP_DIS. 0: 1.05 ms burst gap. 1: 2.10 ms burst gap. 31: 33.55 ms burst gap.	0x00
SIO_SINGLE_SHOT	6	One-shot	Use this to output a single burst. Will be cleared by hardware when the burst has finished.	0x0
SIO_AUTO_REPEAT	5	R/W	Use this to output repeated bursts interleaved with burst gaps. Must be manually reset again to stop output of bursts.	0x0
SIO_LD_POLARITY	4	R/W	Polarity of the "Ld" signal 0: load signal is active low 1: load signal is active high	0x0
SIO_PORT_WIDTH	3:2	R/W	Number of gpios pr. port. 0: 1 gpio pr. port. 1: 2 gpios pr. port. 2: 3 gpios pr. port. 3: 4 gpios pr. port.	0x0

Table 325 • **Fields in SIO_CONFIG *(continued)***

Field Name	Bit	Access	Description	Default
SIO_REVERSE_OUTPUT	1	R/W	Reverse the output bitstream. The default order of the output bit stream is (displayed in transmitted order): (portN bit3, portN bit2, ..., port0 bit1, port0 bit0) The reverse order of the output bit stream is (displayed in transmitted order): (port0 bit0, port0 bit1, ..., portN bit2, portN bit3) 0 : Do not reverse. 1 : Reverse.	0x0
SIO_REVERSE_INPUT	0	R/W	Reverse the input bitstream. The default order of the input bit stream is (displayed in received order): (port0 bit0, port0 bit1, ..., portN bit2, portN bit3) The reverse order of the input bit stream is (displayed in received order): (portN bit3, portN bit2, ..., port0 bit1, port0 bit0) 0: Do not reverse. 1: Reverse.	0x0

7.6.10.7 DEVCPU_GCB:SIO_CTRL:SIO_CLOCK

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

Table 326 • **Fields in SIO_CLOCK**

Field Name	Bit	Access	Description	Default
SIO_CLK_FREQ	11:0	R/W	SIO controller clock frequency. Divides the 250MHz system clk with value of this field. E.g. the system clk is 250 MHz and this field is set to 10, the output frequency will be 25 MHz. 0 : Disable clock. 1 : Reserved, do not use. Others : Clock divider value.	0x000

7.6.10.8 DEVCPU_GCB:SIO_CTRL:SIO_INT_REG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

Table 327 • **Fields in SIO_INT_REG**

Field Name	Bit	Access	Description	Default
INT_REG	31:0	Sticky	Interrupt register. Bit n from all ports. Disabled gpios are always '0'. 0: No interrupt for given gpio. 1: Interrupt for given gpio. bit order (portM bit-n down to portM bit-0).	0x00000000

7.6.11 DEVCPU_GCB:FAN_CFG

Parent: DEVCPU_GCB

Instances: 1

Table 328 • **Registers in FAN_CFG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
FAN_CFG	0x00000000	1	Configuration register for the fan controller	Page 252

7.6.11.1 DEVCPU_GCB:FAN_CFG:FAN_CFG

Parent: DEVCPU_GCB:FAN_CFG

Instances: 1

Table 329 • **Fields in FAN_CFG**

Field Name	Bit	Access	Description	Default
PWM_FREQ	5:3	R/W	Set the frequency of the PWM output 0: 25 kHz 1: 120 Hz 2: 100 Hz 3: 80 Hz 4: 60 Hz 5: 40 Hz 6: 20 Hz 7: 10 Hz	0x0
INV_POL	2	R/W	Define the polarity of the PWM output. 0: PWM is logic 1 when "on" 1: PWM is logic 0 when "on"	0x0

Table 329 • **Fields in FAN_CFG *(continued)***

Field Name	Bit	Access	Description	Default
GATE_ENA	1	R/W	Enable gating of the TACH input by the PWM output so that only TACH pulses received when PWM is "on" are counted. 0: Disabled 1: Enabled	0x0
PWM_OPEN_COL_ENA	0	R/W	Configure the PWM output to be open collector	0x0
DUTY_CYCLE	23:16	R/W	Define the duty cycle 0x00: Always "off" 0xFF: Always "on"	0x00

7.6.12 DEVCPU_GCB:FAN_STAT

Parent: DEVCPU_GCB

Instances: 1

Table 330 • **Registers in FAN_STAT**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
FAN_CNT	0x00000000	1	TACH counter	Page 253

7.6.12.1 DEVCPU_GCB:FAN_STAT:FAN_CNT

Parent: DEVCPU_GCB:FAN_STAT

Instances: 1

Table 331 • **Fields in FAN_CNT**

Field Name	Bit	Access	Description	Default
FAN_CNT	15:0	R/O	Counts the number of rising edges on the TACH input. The counter is wrapping.	0x0000

7.6.13 DEVCPU_GCB:MEMITGR

Parent: DEVCPU_GCB

Instances: 1

The memory integrity monitor is associated with one or more memories with build-in parity-protection and/or error-correction logic. Through the integrity monitor, address locations of failures and/or corrections can be read out.

There may be more than one integrity controller in the design, also - not all memories has an associated controller.

Table 332 • **Registers in MEMITGR**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MEMITGR_CTRL	0x00000000	1	Monitor control	Page 254
MEMITGR_STAT	0x00000004	1	Monitor status	Page 255
MEMITGR_INFO	0x00000008	1	Memory indication	Page 255
MEMITGR_IDX	0x0000000C	1	Memory index	Page 256

7.6.13.1 DEVCPU_GCB:MEMITGR:MEMITGR_CTRL

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

Table 333 • **Fields in MEMITGR_CTRL**

Field Name	Bit	Access	Description	Default
ACTIVATE	0	One-shot	Setting this field transitions the integrity monitor between operating modes. Transitioning between modes takes time, this field remains set until the new mode is reached. During this time the monitor also reports busy (MEMITGR_MODE.MODE_BUSY is set). From IDLE (MEMITGR_MODE.MODE_IDLE is set) the monitor can transition into either DETECT or LISTEN mode, the DETECT mode is entered if a memory reports an indication - the LISTEN mode is entered if no indications are reported. The first time after reset the monitor will not detect indications, that is; it will transition directly from IDLE to LISTEN mode. From DETECT (MEMITGR_MODE.MODE_DETECT is set) the monitor can transition into either DETECT or LISTEN mode, the DETECT mode is entered if more indications are reported - the LISTEN mode is entered if no more indications are reported. From LISTEN (MEMITGR_MODE.MODE_LISTEN is set) the monitor can transition into IDLE mode.	0x0

7.6.13.2 DEVCPU_GCB:MEMITGR:MEMITGR_STAT

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

Table 334 • **Fields in MEMITGR_STAT**

Field Name	Bit	Access	Description	Default
INDICATION	4	R/O	If this field is set then there is an indication from one of the memories that needs to be analyzed. An indication is either a parity detection or an error correction. This field is only set when the monitor is in LISTEN mode (MEMITGR_MODE.MODE_LISTEN is set), in all other states (including BUSY) this field returns 0.	0x0
MODE_LISTEN	3	R/O	This field is set when the monitor is in LISTEN mode, during listen mode the monitor continually check for parity/correction indications from the memories.	0x0
MODE_DETECT	2	R/O	This field is set when the monitor is in DETECT mode, during detect mode the MEMITGR_INFO register contains valid information about one indication.	0x0
MODE_IDLE	1	R/O	This field is set when the monitor is in IDLE mode.	0x1
MODE_BUSY	0	R/O	The busy signal is a copy of the MEMITGR_CTRL.ACTIVATE field, see description of that field for more information about the different states/modes of the monitor.	0x0

7.6.13.3 DEVCPU_GCB:MEMITGR:MEMITGR_INFO

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

This field is only valid when the monitor is in the DETECT (MEMITGR_MODE.MODE_DETECT is set) mode.

Table 335 • **Fields in MEMITGR_INFO**

Field Name	Bit	Access	Description	Default
MEM_ERR	31	R/O	This field is set if the monitor has detected a parity indication (or an unrecoverable correction).	0x0

Table 335 • **Fields in MEMITGR_INFO *(continued)***

Field Name	Bit	Access	Description	Default
MEM_COR	30	R/O	This field is set if the monitor has detected a correction.	0x0
MEM_ERR_OVF	29	R/O	This field is set if the monitor has detected a parity indication (or an unrecoverable correction) for which the address has not been recorded. If MEMITGR_INFO.MEM_ERR is set then there has been more than one indication, then only the address of the newest indication has been kept. If MEMITGR_INFO.MEM_ERR is cleared then an indication has occurred for which the address could not be stored, this is a very rare situation that can only happen if an indication is detected just as the memory is talking to the monitor.	0x0
MEM_COR_OVF	28	R/O	This field is set if the monitor has correction indication for which the address has not been recorded. If MEMITGR_INFO.MEM_ERR is set then there has also been a parity indication (or an unrecoverable correction) which takes priority over correction indications. If MEMITGR_INFO.MEM_ERR is cleared and MEMITGR_INFO.MEM_COR is set then there has been more than one correction indication, then only the address of the newest correction indication has been kept. If MEMITGR_INFO.MEM_ERR and MEMITGR_INFO.MEM_COR is both cleared then a correction indication has occurred for which the address could not be stored, this is a very rare situation that can only happen if an indication is detected just as the memory is talking to the monitor.	0x0
MEM_ADDR	27:0	R/O	This field is valid only when MEMITGR.MEM_ERR or MEMITGR.MEM_COR is set.	0x0000000

7.6.13.4 DEVCPU_GCB:MEMITGR:MEMITGR_IDX

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

This field is only valid when the monitor is in the DETECT (MEMITGR_MODE.MODE_DETECT is set) mode.

Table 336 • **Fields in MEMITGR_IDX**

Field Name	Bit	Access	Description	Default
MEM_IDX	15:0	R/O	This field contains a unique index for the memory for which info is currently provided in MEMITGR_MEMINFO. Indexes are counted from 1 (not 0).	0x0000

7.7 DEVCPU_QS

Table 337 • **Register Groups in DEVCPU_QS**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
XTR	0x00000000	1	Frame Extraction Related Registers	Page 257
INJ	0x00000034	1	Frame Injection Related Registers	Page 260

7.7.1 DEVCPU_QS:XTR

Parent: DEVCPU_QS

Instances: 1

CPU queue system registers related to frame extraction.

Table 338 • **Registers in XTR**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
XTR_FRM_PRUNING	0x00000000	2 0x00000004	Frame Pruning	Page 257
XTR_GRP_CFG	0x00000008	2 0x00000004	Group Configuration	Page 258
XTR_MAP	0x00000010	2 0x00000004	Map Queue to Group	Page 258
XTR_RD	0x00000018	2 0x00000004	Read from Group FIFO	Page 259
XTR_QU_FLUSH	0x00000028	1	Queue Flush	Page 259
XTR_DATA_PRESENT	0x0000002C	1	Extraction Status	Page 260

7.7.1.1 DEVCPU_QS:XTR:XTR_FRM_PRUNING

Parent: DEVCPU_QS:XTR

Instances: 2

Table 339 • **Fields in XTR_FRM_PRUNING**

Field Name	Bit	Access	Description	Default
PRUNE_SIZE	7:0	R/W	Extracted frames for the corresponding queue are pruned PRUNE_SIZE 32-bit words. Note : PRUNE_SIZE is the frame data size, including the IFH. 0 : No pruning 1: Frames extracted are pruned to 8 bytes. 2: Frames extracted are pruned to 12 bytes. . '0xFF': Frames extracted are pruned to 1024 bytes	0x00

7.7.1.2 DEVCPU_QS:XTR:XTR_GRP_CFG

Parent: DEVCPU_QS:XTR

Instances: 2

Table 340 • **Fields in XTR_GRP_CFG**

Field Name	Bit	Access	Description	Default
BYTE_SWAP	0	R/W	Controls - per extraction group - the byte order of the data word read in XTR_RD. When using little-Endian mode, then the first byte of the destination MAC address is placed at XTR_RD[7:0]. When using network-order, then the first byte of the destination MAC address is placed at XTR_RD[31:25]. 0: Network-order (big-endian). 1: Little-endian.	0x1
STATUS_WORD_POS	1	R/W	Select order of last data and status words. 0: Status just before last data. 1: Status just after last data.	0x1

7.7.1.3 DEVCPU_QS:XTR:XTR_MAP

Parent: DEVCPU_QS:XTR

Instances: 2

Table 341 • **Fields in XTR_MAP**

Field Name	Bit	Access	Description	Default
GRP	4	R/W	Maps a queue to a certain extractor group	0x0
MAP_ENA	0	R/W	Enables extraction of a queue. Disabling of extraction for a queue happens upon next frame boundary. That is, a frame being extracted at the time of queue disabling is not affected. '0' : Queue is not mapped to a queue group (queue is disabled) '1' : Queue is mapped to the queue group defined by XTR::XTR_MAP (queue is enabled)	0x0

7.7.1.4 DEVCPU_QS:XTR:XTR_RD

Parent: DEVCPU_QS:XTR

Instances: 2

Table 342 • **Fields in XTR_RD**

Field Name	Bit	Access	Description	Default
DATA	31:0	R/O	Frame Data. Read from this register to obtain the next 32 bits of the frame data currently stored in the CPU queue system. Each read must check for the special values "0x8000000n", 0<=n<=7, as seen below; Note that when a status word is presented, it can be put just before or just after the last data (XTR_GRP_CFG). n=0-3: EOF. Unused bytes in last is 'n'. n=4 : EOF, but truncated. n=5 : EOF Aborted. Frame invalid. n=6 : Escape. Next read is packet data. n=7 : Data not ready for reading out.	0x00000000

7.7.1.5 DEVCPU_QS:XTR:XTR_QU_FLUSH

Parent: DEVCPU_QS:XTR

Instances: 1

Table 343 • **Fields in XTR_QU_FLUSH**

Field Name	Bit	Access	Description	Default
FLUSH	1:0	R/W	Enable software flushing of a CPU queue. Note that before flushing the a CPU queue it may be necessary to stop the OQS from sending data into the CPU queues. '0': No action '1': Do CPU queue flushing	0x0

7.7.1.6 DEVCPU_QS:XTR:XTR_DATA_PRESENT

Parent: DEVCPU_QS:XTR

Instances: 1

Table 344 • **Fields in XTR_DATA_PRESENT**

Field Name	Bit	Access	Description	Default
DATA_PRESENT	3:2	R/O	When a frame, which should be forwarded to software has been received by the CPU queue system, the corresponding bit is set. When software has extracted all frames from a CPU queue the bit is cleared, i.e. the bit remains set as long as at least one byte of frame data for the corresponding queue is present in the queue system. Note : If a queue isn't map to a group DATA_PRESENT will be '0' '0': No data available for this CPU queue '1': At least one frame is available for this cpu queue	0x0
DATA_PRESENT_GRP	1:0	R/O	When a queue group has a frame present, the bit corresponding to the queue group number gets set. It remains set until all frame data have been extracted. '0': No frames available for this CPU queue group. '1': At least one frame is available for this CPU queue group.	0x0

7.7.2 DEVCPU_QS:INJ

Parent: DEVCPU_QS

Instances: 1

CPU queue system registers related to frame injection.

Table 345 • **Registers in INJ**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
INJ_GRP_CFG	0x00000000	2 0x00000004	Group Configuration	Page 261
INJ_WR	0x00000008	2 0x00000004	Write to Group FIFO	Page 261
INJ_CTRL	0x00000010	2 0x00000004	Injection Control	Page 261
INJ_STATUS	0x00000018	1	Injection Status	Page 262
INJ_ERR	0x0000001C	2 0x00000004	Injection Errors	Page 263

7.7.2.1 DEVCPU_QS:INJ:INJ_GRP_CFG

Parent: DEVCPU_QS:INJ

Instances: 2

Table 346 • **Fields in INJ_GRP_CFG**

Field Name	Bit	Access	Description	Default
BYTE_SWAP	8	R/W	Controls - per injection group - the byte order of the data word in INJ_WR. 0: Network-order (big-endian). 1: Little-endian.	0x1

7.7.2.2 DEVCPU_QS:INJ:INJ_WR

Parent: DEVCPU_QS:INJ

Instances: 2

Table 347 • **Fields in INJ_WR**

Field Name	Bit	Access	Description	Default
DATA	31:0	R/W	Frame Write.Write to this register inject the next 32 bits of the frame data currently injected into the chip.	0x00000000

7.7.2.3 DEVCPU_QS:INJ:INJ_CTRL

Parent: DEVCPU_QS:INJ

Instances: 2

Table 348 • **Fields in INJ_CTRL**

Field Name	Bit	Access	Description	Default
GAP_SIZE	28:21	R/W	It is allowed to inject a number of "dummy" bytes in front of a frame before the actual frame data. The number of bytes that should be discarded is specified with this field.	0x00
ABORT	20	One-shot	Abort frame currently injected. Write: '0': No action '1': Frame currently injected is aborted (Bit is automatically cleared)	0x0
EOF	19	One-shot	EOF must be set before last data of a frame is injected. '0': No action '1': Next word is the last word of the frame injected	0x0
SOF	18	One-shot	SOF must be set before injecting a frame. Write: '0': No action '1': Start of new frame injection Read: '0': First data word has been moved to the IQS. '1': First data word has not been moved to the IQS.	0x0
VLD_BYTES	17:16	R/W	The number of valid bytes in the last word must be set before last data of a frame is injected. 0: Bits 31-0 in the last word are valid. 1: Bits 31-24 in the last word are valid. 2: Bits 31-16 in the last word are valid. 3: Bits 31-7 in the last word are valid. This encoding applies when big-endian is used for INJ_WR.	0x0

7.7.2.4 DEVCPU_QS:INJ:INJ_STATUS

Parent: DEVCPU_QS:INJ

Instances: 1

Table 349 • **Fields in INJ_STATUS**

Field Name	Bit	Access	Description	Default
WMARK_REACHED	5:4	R/O	Before the CPU injects a frame, software may check if the input queue has reached high watermark. If the watermark in the IQS has been reached this bit will be set. '0': Input queue has not reached high watermark '1': Input queue has reached high watermark, and frames injected may be dropped due to buffer overflow.	0x0
FIFO_RDY	3:2	R/O	When '1' the injector group's FIFO is ready for additional data written through the INJ_WR register. '0': The injector group cannot accept additional data. '1': The injector group is able to accept additional data.	0x0
INJ_IN_PROGRESS	1:0	R/O	When '1' the injector group is in the process of receiving a frame, and at least one write to INJ_WR remains before the frame is forwarded to the front ports. When '0' the injector group is waiting for an initiation of a frame injection. '0': A frame injection is not in progress. '1': A frame injection is in progress.	0x0

7.7.2.5 DEVCPU_QS:INJ:INJ_ERR

Parent: DEVCPU_QS:INJ

Instances: 2

The bits in this register are cleared by writing a '1' to the relevant bit-positions.

Table 350 • **Fields in INJ_ERR**

Field Name	Bit	Access	Description	Default
ABORT_ERR_STICKY	1	Sticky	If the CPU aborts an on-going frame injection by a '1' to INJ_CTRL::ABORT, the on-going frame injection is aborted and the injection controller prepares for a new injection. This situation could indicate a software error. '0': No error. '1': Previous frame was aborted with a write to INJ_CTRL::ABORT or due to an internal error.	0x0
WR_ERR_STICKY	0	Sticky	If the CPU writes to INJ_WR without having initiated a frame injection with INJ_CTRL, this sticky bit gets set. '0': No error. '1': Erroneous write to INJ_WR has been made.	0x0

7.8 HSIO

Register collection for control of SerDes macros and LCPLL.

Table 351 • **Register Groups in HSIO**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PLL5G_STATUS	0x00000018	1	PLL5G Status Registers	Page 264
RCOMP_STATUS	0x00000024	1	RCOMP Status Registers	Page 265
SERDES6G_ANA_CFG	0x00000064	1	SERDES6G Analog Configuration Registers	Page 266
SERDES6G_DIG_CFG	0x00000088	1	SERDES6G Digital Configuration Registers	Page 272
MCB_SERDES6G_CFG	0x000000AC	1	MCB SERDES6G Configuration Register	Page 273

7.8.1 HSIO:PLL5G_STATUS

Parent: HSIO

Instances: 1

Status register set for PLL5G.

Table 352 • **Registers in PLL5G_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PLL5G_STATUS0	0x00000000	1	PLL5G Status 0	Page 265

7.8.1.1 HSIO:PLL5G_STATUS:PLL5G_STATUS0

Parent: HSIO:PLL5G_STATUS

Instances: 1

Status register 0 for the PLL5G

Table 353 • **Fields in PLL5G_STATUS0**

Field Name	Bit	Access	Description	Default
LOCK_STATUS	0	R/O	PLL lock status 0: not locked, 1: locked	0x0
READBACK_DATA	8:1	R/O	RCPLL Interface to read back internal data of the FSM.	0x00
CALIBRATION_DONE	9	R/O	RCPLL Flag that indicates that the calibration procedure has finished.	0x0
CALIBRATION_ERR	10	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure.	0x0
OUT_OF_RANGE_ERR	11	R/O	RCPLL Flag that indicates a out of range condition while NOT in calibration mode.	0x0
RANGE_LIM	12	R/O	RCPLL Flag range limiter signaling	0x0

7.8.2 HSIO:RCOMP_STATUS

Parent: HSIO

Instances: 1

Status register set for RCOMP.

Table 354 • **Registers in RCOMP_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RCOMP_STATUS	0x00000000	1	RCOMP Status	Page 265

7.8.2.1 HSIO:RCOMP_STATUS:RCOMP_STATUS

Parent: HSIO:RCOMP_STATUS

Instances: 1

Status register bits for the RCOMP

Table 355 • **Fields in RCOMP_STATUS**

Field Name	Bit	Access	Description	Default
BUSY	12	R/O	Resistor comparison activity 0: resistor measurement finished or inactive 1: resistor measurement in progress	0x0
DELTA_ALERT	7	R/O	Alarm signal if rcomp isn't best choice anymore 0: inactive 1: active	0x0
RCOMP	3:0	R/O	Measured resistor value 0: maximum resistance value 15: minimum resistance value	0x0

7.8.3 HSIO:SERDES6G_ANA_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES6G (analog parts)

Table 356 • **Registers in SERDES6G_ANA_CFG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_DES_CFG	0x00000000	1	SERDES6G Deserializer Cfg	Page 266
SERDES6G_IB_CFG	0x00000004	1	SERDES6G Input Buffer Cfg	Page 268
SERDES6G_IB_CFG1	0x00000008	1	SERDES6G Input Buffer Cfg1	Page 268
SERDES6G_OB_CFG	0x0000000C	1	SERDES6G Output Buffer Cfg	Page 269
SERDES6G_OB_CFG1	0x00000010	1	SERDES6G Output Buffer Cfg1	Page 270
SERDES6G_SER_CFG	0x00000014	1	SERDES6G Serializer Cfg	Page 270
SERDES6G_COMMON_CFG	0x00000018	1	SERDES6G Common Cfg	Page 270
SERDES6G_PLL_CFG	0x0000001C	1	SERDES6G Pll Cfg	Page 271

7.8.3.1 HSIO:SERDES6G_ANA_CFG:SERDES6G_DES_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G deserializer

Table 357 • **Fields in SERDES6G_DES_CFG**

Field Name	Bit	Access	Description	Default
DES_PHS_CTRL	16:13	R/W	Control of phase regulator logic. Bit 3 must always be set to 0. Optimal setting for bits 2:0 are 4 through 7; recommended setting is 6. 0: Disabled 1: Enabled with 99 ppm limit 2: Enabled with 202 ppm limit 3: Enabled with 485 ppm limit 4: Enabled if corresponding PCS is in sync with 50 ppm limit 5: Enabled if corresponding PCS is in sync with 99 ppm limit 6: Enabled if corresponding PCS is in sync with 202 ppm limit 7: Enabled if corresponding PCS is in sync with 485 ppm limit	0x0
DES_MBTR_CTRL	12:10	R/W	Des phase control for 180 degrees deadlock block mode of operation 000: Depending on density of input pattern 001: Active until PCS has synchronized 010: Depending on density of input pattern until PCS has synchronized 011: Never 100: Always All other settings are reserved.	0x0
RESERVED	9:8	R/W	Must always be set to its default.	0x0
DES_BW_HYST	7:5	R/W	Selection of time constant for integrative path of the CDR loop. 0: Reserved 1: Divide by 4 2: Divide by 8 3: Divide by 16 4: Divide by 32 5: Divide by 64 6: Divide by 128 7: Divide by 256 For more information about mode-dependent limitations, see SERDES6G Deserializer Configuration, page 20.	0x0
RESERVED	4	R/W	Must be set to its default.	0x0

Table 357 • **Fields in SERDES6G_DES_CFG *(continued)***

Field Name	Bit	Access	Description	Default
DES_BW_ANA	3:1	R/W	Bandwidth selection for proportional path of the CDR loop. 0: Reserved 1: Reserved 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32 6: Divide by 64 7: Divide by 128 For more information about mode-dependent limitations, see SERDES6G Deserializer Configuration, page 20.	0x0
RESERVED	0	R/W	Must be set to its default.	0x0

7.8.3.2 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 0 for SERDES6G input buffer

Table 358 • **Fields in SERDES6G_IB_CFG**

Field Name	Bit	Access	Description	Default
RESERVED	27:7	R/W	Must be set to its default.	0x00000
IB_VBCOM	6:4	R/W	Level detection thresholds, in steps of approximately 8mV. 0: 60mV 7: 120mV	0x0
IB_RESISTOR_CTRL	3:0	R/W	Resistor control. Value must be taken from RCOMP_STATUS.RCOMP.	0x0

7.8.3.3 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG1

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 1 for SERDES6G input buffer

Table 359 • **Fields in SERDES6G_IB_CFG1**

Field Name	Bit	Access	Description	Default
RESERVED	13:7	R/W	Must be set to its default.	0x00
IB_CTERM_ENA	5	R/W	Common mode termination 0: Disable 1: Enable	0x0
IB_RESERVED	4	R/W	Must be set to 1.	0x0

Table 359 • **Fields in SERDES6G_IB_CFG1 *(continued)***

Field Name	Bit	Access	Description	Default
IB_ENA_OFFSAC	3	R/W	Auto offset compensation for ac path 0: Disable 1: Enable	0x0
IB_ENA_OFFSDC	2	R/W	Auto offset compensation for dc path 0: Disable 1: Enable	0x0
IB_FX100_ENA	1	R/W	Increases timing constant for level detect circuit, must be used in FX100 mode 0: Normal speed 1: Slow speed (oversampling)	0x0
RESERVED	0	R/W	Must be set to its default.	0x0

7.8.3.4 HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 0 for SERDES6G output buffer

Table 360 • **Fields in SERDES6G_OB_CFG**

Field Name	Bit	Access	Description	Default
OB_IDLE	31	R/W	PCIe support 1: idle - force to 0V differential 0: Normal mode	0x0
OB_ENA1V_MODE	30	R/W	Output buffer supply voltage 1: Set to nominal 1V 0: Set to higher voltage	0x0
OB_POL	29	R/W	Polarity of output signal 0: Normal 1: Inverted	0x0
OB_POST0	28:23	R/W	Coefficients for 1st Post Cursor (MSB is sign)	0x00
OB_POST1	22:18	R/W	Coefficients for 2nd Post Cursor (MSB is sign)	0x00
OB_PREC	17:13	R/W	Coefficients for Pre Cursor (MSB is sign)	0x00
RESERVED	12:9	R/W	Must be set to its default.	0x0
OB_SR_H	8	R/W	Half the predriver speed, use for slew rate control 0: Disable - slew rate < 60 ps 1: Enable - slew rate > 60 ps	0x0
OB_RESISTOR_CTRL	7:4	R/W	Resistor control. Value must be taken from RCOMP_STATUS.RCOMP.	0x0

Table 360 • **Fields in SERDES6G_OB_CFG *(continued)***

Field Name	Bit	Access	Description	Default
OB_SR	3:0	R/W	Driver speed, fine adjustment of slew rate 30-60ps (if OB_SR_H = 0), 60-140ps (if OB_SR_H = 1)	0x0

7.8.3.5 HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG1

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 1 for SERDES6G output buffer

Table 361 • **Fields in SERDES6G_OB_CFG1**

Field Name	Bit	Access	Description	Default
OB_ENA_CAS	8:6	R/W	Output skew, used for skew adjustment in SGMII mode	0x0
OB_LEV	5:0	R/W	Level of output amplitude 0: lowest level 63: highest level	0x00

7.8.3.6 HSIO:SERDES6G_ANA_CFG:SERDES6G_SER_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G serializer

Table 362 • **Fields in SERDES6G_SER_CFG**

Field Name	Bit	Access	Description	Default
RESERVED	8:4	R/W	Must be set to its default.	0x00
SER_ENHYS	3	R/W	Enable hysteresis for phase alignment 0: Disable hysteresis 1: Enable hysteresis	0x0
RESERVED	2	R/W	Must be set to its default.	0x0
SER_EN_WIN	1	R/W	Enable window for phase alignment 0: Disable window 1: Enable window	0x0
SER_ENALI	0	R/W	Enable phase alignment 0: Disable phase alignment 1: Enable phase alignment	0x0

7.8.3.7 HSIO:SERDES6G_ANA_CFG:SERDES6G_COMMON_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for common SERDES6G functions Note: When enabling the facility loop (ena_floop) also the phase alignment in the serializer has to be enabled and configured adequate.

Table 363 • **Fields in SERDES6G_COMMON_CFG**

Field Name	Bit	Access	Description	Default
SYS_RST	31	R/W	System reset (low active) 0: Apply reset (not self-clearing) 1: Reset released	0x0
ENA_LANE	18	R/W	Enable lane 0: Disable lane 1: Enable line	0x0
RESERVED	17:12	R/W	Must be set to its default.	0x00
RESERVED	9:8	R/W	Must be set to its default.	0x0
ENA_ELOOP	11	R/W	Enable equipment loop 0: Disable 1: Enable	0x0
ENA_FLOOP	10	R/W	Enable facility loop 0: Disable 1: Enable	0x0
HRATE	7	R/W	Enable half rate 0: Disable 1: Enable	0x1
QRATE	6	R/W	Enable quarter rate 0: Disable 1: Enable	0x0
IF_MODE	5:4	R/W	Interface mode 0: Reserved 1: 10-bit mode 2: Reserved 3: 20-bit mode	0x1

7.8.3.8 HSIO:SERDES6G_ANA_CFG:SERDES6G_PLL_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G RCPLL

Table 364 • **Fields in SERDES6G_PLL_CFG**

Field Name	Bit	Access	Description	Default
RESERVED	20	R/W	Must be set to its default.	0x0
PLL_ENA_ROT	18	R/W	Enable rotation	0x1
PLL_FSM_CTRL_DATA	15:8	R/W	Control data for FSM	0x00
PLL_FSM_ENA	7	R/W	Enable FSM	0x0
RESERVED	6:5	R/W	Must be set to its default.	0x0
RESERVED	3	R/W	Must be set to its default.	0x0

Table 364 • **Fields in SERDES6G_PLL_CFG *(continued)***

Field Name	Bit	Access	Description	Default
PLL_ROT_DIR	2	R/W	Select rotation direction	0x0
PLL_ROT_FRQ	1	R/W	Select rotation frequency	0x1

7.8.4 HSIO:SERDES6G_DIG_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES6G digital BIST and DFT functions.

Table 365 • **Registers in SERDES6G_DIG_CFG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_DIG_CFG	0x00000000	1	SERDES6G Digital Configuration register	Page 272
SERDES6G_MISC_CFG	0x00000018	1	SERDES6G Misc Configuration	Page 272

7.8.4.1 HSIO:SERDES6G_DIG_CFG:SERDES6G_DIG_CFG

Parent: HSIO:SERDES6G_DIG_CFG

Instances: 1

Configuration register for SERDES6G digital functions

Table 366 • **Fields in SERDES6G_DIG_CFG**

Field Name	Bit	Access	Description	Default
SIGDET_AST	5:3	R/W	Signal detect assertion time 0: 0 us 1: 35 us 2: 70 us 3: 105 us 4: 140 us 5..7: reserved	0x0
SIGDET_DST	2:0	R/W	Signal detect de-assertion time 0: 0 us 1: 250 us 2: 350 us 3: 450 us 4: 550 us 5..7: reserved	0x0

7.8.4.2 HSIO:SERDES6G_DIG_CFG:SERDES6G_MISC_CFG

Parent: HSIO:SERDES6G_DIG_CFG

Instances: 1

Configuration register for miscellaneous functions

Table 367 • **Fields in SERDES6G_MISC_CFG**

Field Name	Bit	Access	Description	Default
DES_100FX_CPMD_ENA	8	R/W	Enable deserializer cp/md handling for 100fx mode 0: Disable 1: Enable	0x0
RX_LPI_MODE_ENA	5	R/W	Enable RX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
TX_LPI_MODE_ENA	4	R/W	Enable TX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
RX_DATA_INV_ENA	3	R/W	Enable data inversion received from Deserializer 0: Disable 1: Enable	0x0
TX_DATA_INV_ENA	2	R/W	Enable data inversion sent to Serializer 0: Disable 1: Enable	0x0
LANE_RST	0	R/W	Lane Reset 0: No reset 1: Reset (not self-clearing)	0x0

7.8.5 HSIO:MCB_SERDES6G_CFG

Parent: HSIO

Instances: 1

All SERDES6G macros are accessed via the serial Macro Configuration Bus (MCB). Each macro is configured by one MCB Slave. All MCB Slaves are connected in a daisy-chain loop.

Table 368 • **Registers in MCB_SERDES6G_CFG**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MCB_SERDES6G_ADDR_CFG	0x00000000	1	MCB SERDES6G Address Cfg	Page 273

7.8.5.1 HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG

Parent: HSIO:MCB_SERDES6G_CFG

Instances: 1

Configuration of SERDES6G MCB Slaves to be accessed

Table 369 • **Fields in MCB_SERDES6G_ADDR_CFG**

Field Name	Bit	Access	Description	Default
SERDES6G_WR_ONE_SHOT	31	One-shot	Initiate a write access to marked SERDES6G Slaves 0: No write operation pending 1: Initiate write to slaves (kept 1 until write operation has finished)	0x0
SERDES6G_RD_ONE_SHOT	30	One-shot	Initiate a read access to marked SERDES6G Slaves 0: No read operation pending (read op finished after bit has been set) 1: Initiate a read access (kept 1 until read operation has finished)	0x0
SERDES6G_ADDR	15:0	R/W	Activation vector for SERDES6G-Slaves, one-hot coded, each bit is related to one macro, e.g. bit 0 enables/disables access to macro No. 0 0: Disable macro access via MCB 1: Enable macro access via MCB	0xFFFF

7.9 DEV_GMII

Table 370 • **Register Groups in DEV_GMII**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PORT_MODE	0x00000000	1		Page 274
MAC_CFG_STATUS	0x0000000C	1		Page 275

7.9.1 DEV_GMII:PORT_MODE

Parent: DEV_GMII

Instances: 1

Table 371 • **Registers in PORT_MODE**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CLOCK_CFG	0x00000000	1		Page 274
PORT_MISC	0x00000004	1		Page 275

7.9.1.1 DEV_GMII:PORT_MODE:CLOCK_CFG

Parent: DEV_GMII:PORT_MODE

Instances: 1

Table 372 • **Fields in CLOCK_CFG**

Field Name	Bit	Access	Description	Default
MAC_TX_RST	3	R/W		0x1
MAC_RX_RST	2	R/W		0x1
PORT_RST	1	R/W		0x1
PHY_RST	0	R/W		0x1

7.9.1.2 DEV_GMII:PORT_MODE:PORT_MISC

Parent: DEV_GMII:PORT_MODE

Instances: 1

Table 373 • **Fields in PORT_MISC**

Field Name	Bit	Access	Description	Default
FWD_PAUSE_ENA	3	R/W	Forward pause frames (EtherType = 0x8808, opcode = 0x0001). The reaction to incoming pause frames is controlled independently of FWD_PAUSE_ENA.	0x0
FWD_CTRL_ENA	2	R/W	Forward MAC control frames excluding pause frames (EtherType = 0x8808, opcode different from 0x0001).	0x0
GMII_LOOP_ENA	1	R/W	Loop GMII transmit data directly into receive path.	0x0
DEV_LOOP_ENA	0	R/W	Loop the device bus through this port. The MAC is potentially bypassed.	0x0

7.9.2 DEV_GMII:MAC_CFG_STATUS

Parent: DEV_GMII

Instances: 1

The 1G MAC module contains configuration and status registers related to the MAC module of the 1G Device.

Table 374 • **Registers in MAC_CFG_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_ENA_CFG	0x00000000	1	Mode Configuration Register	Page 276
MAC_MODE_CFG	0x00000004	1	Mode Configuration Register	Page 276

Table 374 • **Registers in MAC_CFG_STATUS *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_MAXLEN_CFG	0x00000008	1	Max Length Configuration Register	Page 277
MAC_TAGS_CFG	0x0000000C	1	VLAN / Service tag configuration register	Page 277
MAC_ADV_CHK_CFG	0x00000010	1	Advanced Check Feature Configuration Register	Page 278
MAC_IFG_CFG	0x00000014	1	Inter Frame Gap Configuration Register	Page 279
MAC_HDX_CFG	0x00000018	1	Half Duplex Configuration Register	Page 279
MAC_FC_CFG	0x00000020	1	MAC Flow Control Configuration Register	Page 280
MAC_FC_MAC_LOW_CFG	0x00000024	1	MAC Flow Control Configuration Register	Page 281
MAC_FC_MAC_HIGH_CFG	0x00000028	1	MAC Flow Control Configuration Register	Page 281
MAC_STICKY	0x0000002C	1	Sticky Bit Register	Page 282

7.9.2.1 DEV_GMII:MAC_CFG_STATUS:MAC_ENA_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 375 • **Fields in MAC_ENA_CFG**

Field Name	Bit	Access	Description	Default
RX_ENA	4	R/W	Receiver Module Enable. '0': Receiver Module Disabled '1': Receiver Module Enabled	0x0
TX_ENA	0	R/W	Transmitter Module Enable. '0': Transmitter Module Disabled '1': Transmitter Module Enabled	0x0

7.9.2.2 DEV_GMII:MAC_CFG_STATUS:MAC_MODE_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 376 • **Fields in MAC_MODE_CFG**

Field Name	Bit	Access	Description	Default
GIGA_MODE_ENA	4	R/W	Enables 1 Gbps mode. '0': 10/100 Mbps mode '1': 1 Gbps mode. Note: FDX_ENA must also be set.	0x1

Table 376 • **Fields in MAC_MODE_CFG *(continued)***

Field Name	Bit	Access	Description	Default
FDX_ENA	0	R/W	Enables Full Duplex: '0': Half Duplex '1': Full duplex. Note: Full duplex MUST be selected if GIGA_MODE is enabled.	0x1

7.9.2.3 DEV_GMII:MAC_CFG_STATUS:MAC_MAXLEN_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 377 • **Fields in MAC_MAXLEN_CFG**

Field Name	Bit	Access	Description	Default
MAX_LEN	15:0	R/W	When set, single tagged frames are allowed to be 4 bytes longer than the MAC_MAXLEN_CFG configuration and double tagged frames are allowed to be 8 bytes longer. Single tagged frames are adjusted if VLAN_AWR_ENA is also set. Double tagged frames are adjusted if both VLAN_AWR_ENA and VLAN_DBL_AWR_ENA are set.	0x05EE

7.9.2.4 DEV_GMII:MAC_CFG_STATUS:MAC_TAGS_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

The MAC can be configured to accept 0, 1 and 2 tags and the TAG value can be user-defined.

Table 378 • **Fields in MAC_TAGS_CFG**

Field Name	Bit	Access	Description	Default
TAG_ID	31:16	R/W	This field defines which EtherTypes are recognized as a VLAN TPID - besides 0x8100. The value is used for all tag positions. I.e. a double tagged frame can have the following tag values: (TAG1,TAG2): (0x8100, 0x8100) (0x8100, TAG_ID) (TAG_ID, 0x8100) or (TAG_ID, TAG_ID) Single tagged frame can have the following TPID values: 0x8100 or TAG_ID.	0x8100
VLAN_DBL_AWR_ENA	1	R/W	If set, double tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). VLAN_AWR_ENA must be set when VLAN_DBL_AWR_ENA is set. '0': The MAC does not look for inner tags. '1': The MAC accepts inner tags with TPID=0x8100 or TAG_ID.	0x0
VLAN_AWR_ENA	0	R/W	If set, single tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). '0': The MAC does not look for any tags. '1': The MAC accepts outer tags with TPID=0x8100 or TAG_ID.	0x0
VLAN_LEN_AWR_ENA	2	R/W	When set, single tagged frames are allowed to be 4 bytes longer than the MAC_MAXLEN_CFG configuration and double tagged frames are allowed to be 8 bytes longer. Single tagged frames are adjusted if VLAN_AWR_ENA is also set. Double tagged frames are adjusted if both VLAN_AWR_ENA and VLAN_DBL_AWR_ENA are set.	0x1

7.9.2.5 DEV_GMII:MAC_CFG_STATUS:MAC_ADV_CHK_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 379 • **Fields in MAC_ADV_CHK_CFG**

Field Name	Bit	Access	Description	Default
LEN_DROP_ENA	0	R/W	Length Drop Enable: Configures the Receive Module to drop frames in reference to in-range and out-of-range errors: '0': Length Drop Disabled '1': Length Drop Enabled.	0x0

7.9.2.6 DEV_GMII:MAC_CFG_STATUS:MAC_IFG_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 380 • **Fields in MAC_IFG_CFG**

Field Name	Bit	Access	Description	Default
TX_IFG	12:8	R/W	Used to adjust the duration of the inter-frame gap in the Tx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX 0x19, 0x13 1000 Mbps: 0x07.	0x07
RX_IFG2	7:4	R/W	Used to adjust the duration of the second part of the inter-frame gap in the Rx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX: 0x8, 0xB 1000 Mbps: 0x1.	0x1
RX_IFG1	3:0	R/W	Used to adjust the duration of the first part of the inter-frame gap in the Rx direction and must be set according to the speed settings. 10/100 Mbps: 0x7 1000 Mbps: 0x5.	0x5

7.9.2.7 DEV_GMII:MAC_CFG_STATUS:MAC_HDX_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 381 • **Fields in MAC_HDX_CFG**

Field Name	Bit	Access	Description	Default
WEXC_DIS	24	R/W	Determines whether the MAC backs off after an excessive collision has occurred. If set, back off is disabled after excessive collisions. '0': Back off after excessive collisions '1': Don't back off after excessive collisions	0x0
SEED	23:16	R/W	Seed value loaded into the PRBS of the MAC. Used to prevent excessive collision events.	0x00
SEED_LOAD	12	R/W	Load SEED value into PRNG register. A SEED value is loaded into the PRNG register of the MAC, when SEED_LOAD is asserted. After a load, the SEED_LOAD must be deasserted. '0': Do not load SEED value '1': Load SEED value.	0x0
RETRY_AFTER_EXC_COL_ENA	8	R/W	This bit is used to setup the MAC to retransmit a frame after an early collision even though 16 (or more) early collisions have occurred. '0': A frame is discarded and counted as an excessive collision if 16 collisions occur for this frame. '1': The MAC retransmits a frame after an early collision, regardless of the number of previous early collisions. The backoff sequence is reset after every 16 collisions.	0x0
LATE_COL_POS	6:0	R/W	Adjustment of early/late collision boundary: This bitgroup is used to adjust the MAC so that a collision on a shared transmission medium before bit 512 is handled as an early collision, whereas a collision after bit 512 is handled as a late collision, i.e. no retransmission is performed.	0x43

7.9.2.8 DEV_GMII:MAC_CFG_STATUS:MAC_FC_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 382 • **Fields in MAC_FC_CFG**

Field Name	Bit	Access	Description	Default
ZERO_PAUSE_ENA	18	R/W	If set, a zero-delay pause frame is transmitted when flow control is deasserted. '0': Don't send zero pause frame. '1': Send zero pause frame.	0x0
TX_FC_ENA	17	R/W	When set the MAC will send pause control frames in the Tx direction. '0': Don't send pause control frames '1': Send pause control frames	0x0
RX_FC_ENA	16	R/W	When set the MAC obeys received pause control frames '0': Don't obey received pause control frames '1': Obey received pause control frames.	0x0
PAUSE_VAL_CFG	15:0	R/W	Pause timer value inserted in generated pause frames. 0: Insert timer value 0 in TX pause frame. ... N: Insert timer value N in TX pause frame.	0x0000
FC_LATENCY_CFG	24:19	R/W	Accepted reaction time for link partner after the port has transmitted a pause frame. Frames starting after this latency are aborted. Unit is 64 byte times. A value of 63 disables the feature. For proper flow control, use FC_LATENCY_CFG = 7.	0x03

7.9.2.9 DEV_GMII:MAC_CFG_STATUS:MAC_FC_MAC_LOW_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 383 • **Fields in MAC_FC_MAC_LOW_CFG**

Field Name	Bit	Access	Description	Default
MAC_LOW	23:0	R/W	Lower three bytes in the SMAC in generated flow control frames. 0xNNN: Lower three DMAC bytes	0x000000

7.9.2.10 DEV_GMII:MAC_CFG_STATUS:MAC_FC_MAC_HIGH_CFG

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Table 384 • **Fields in MAC_FC_MAC_HIGH_CFG**

Field Name	Bit	Access	Description	Default
MAC_HIGH	23:0	R/W	Higher three bytes in the SMAC in generated flow control frames. 0xNNN: Higher three DMAC bytes	0x000000

7.9.2.11 DEV_GMII:MAC_CFG_STATUS:MAC_STICKY

Parent: DEV_GMII:MAC_CFG_STATUS

Instances: 1

Clear the sticky bits by writing a '0' in the relevant bitgroups (writing a '1' sets the bit)!.

Table 385 • **Fields in MAC_STICKY**

Field Name	Bit	Access	Description	Default
RX_IPG_SHRINK_STICKY	9	Sticky	Sticky bit indicating that an inter packet gap shrink was detected (IPG < 12 bytes).	0x0
RX_PREAM_SHRINK_STICKY	8	Sticky	Sticky bit indicating that a preamble shrink was detected (preamble < 8 bytes). '0': no preamble shrink was detected '1': a preamble shrink was detected one or more times Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_STICKY	7	Sticky	Sticky bit indicating that a carrier extend was detected. '0': no carrier extend was detected '1': one or more carrier extends were detected Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_ERR_STICKY	6	Sticky	Sticky bit indicating that a carrier extend error was detected. '0': no carrier extend error was detected '1': one or more carrier extend errors were detected Bit is cleared by writing a '1' to this position.	0x0

Table 385 • **Fields in MAC_STICKY *(continued)***

Field Name	Bit	Access	Description	Default
RX_JUNK_STICKY	5	Sticky	Sticky bit indicating that junk was received (bytes not recognized as a frame). '0': no junk was received '1': junk was received one or more times Bit is cleared by writing a '1' to this position.	0x0
TX_RETRANSMIT_STICKY	4	Sticky	Sticky bit indicating that the transmit MAC asked the host for a frame retransmission. '0': no tx retransmission was initiated '1': one or more tx retransmissions were initiated Bit is cleared by writing a '1' to this position.	0x0
TX_JAM_STICKY	3	Sticky	Sticky bit indicating that the transmit host issued a jamming signal. '0': the transmit host issued no jamming signal '1': the transmit host issued one or more jamming signals Bit is cleared by writing a '1' to this position.	0x0
TX_FIFO_OFLW_STICKY	2	Sticky	Sticky bit indicating that the MAC transmit FIFO has overrun.	0x0
TX_FRM_LEN_OVR_STICKY	1	Sticky	Sticky bit indicating that the transmit frame length has overrun. I.e. a frame longer than 64K occurred. '0': no tx frame length error occurred '1': one or more tx frames length errors occurred Bit is cleared by writing a '1' to this position.	0x0
TX_ABORT_STICKY	0	Sticky	Sticky bit indicating that the transmit host initiated abort was executed.	0x0

7.10 DEV

Table 386 • **Register Groups in DEV**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PORT_MODE	0x00000004	1		Page 284

Table 386 • **Register Groups in DEV *(continued)***

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
MAC_CFG_STATUS	0x00000010	1		Page 285
PCS1G_CFG_STATUS	0x00000040	1	PCS 1G Configuration Status Registers	Page 293
PCS1G_TSTPAT_CFG_STATUS	0x00000084	1	PCS1G Testpattern Configuration and Status Registers	Page 301
PCS_FX100_CONFIGURATION	0x0000008C	1	PCS FX100 Configuration Registers	Page 302
PCS_FX100_STATUS	0x00000090	1	PCS FX100 Status Registers	Page 304

7.10.1 DEV:PORT_MODE

Parent: DEV

Instances: 1

Table 387 • **Registers in PORT_MODE**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CLOCK_CFG	0x00000000	1		Page 284
PORT_MISC	0x00000004	1		Page 285

7.10.1.1 DEV:PORT_MODE:CLOCK_CFG

Parent: DEV:PORT_MODE

Instances: 1

Table 388 • **Fields in CLOCK_CFG**

Field Name	Bit	Access	Description	Default
MAC_TX_RST	7	R/W		0x1
MAC_RX_RST	6	R/W		0x1
PCS_TX_RST	5	R/W		0x1
PCS_RX_RST	4	R/W		0x1
PORT_RST	3	R/W		0x1
PHY_RST	2	R/W	Only applicable to ports 10 and 11.	0x1
LINK_SPEED	1:0	R/W	Selects the link speed. 0: No link 1: 1000/2500 Mbps 2: 100 Mbps 3: 10 Mbps	0x0

7.10.1.2 DEV:PORT_MODE:PORT_MISC

Parent: DEV:PORT_MODE

Instances: 1

Table 389 • **Fields in PORT_MISC**

Field Name	Bit	Access	Description	Default
FWD_PAUSE_ENA	2	R/W	Forward pause frames (EtherType = 0x8808, opcode = 0x0001). The reaction to incoming pause frames is controlled independently of FWD_PAUSE_ENA.	0x0
FWD_CTRL_ENA	1	R/W	Forward MAC control frames excluding pause frames (EtherType = 0x8808, opcode different from 0x0001).	0x0
DEV_LOOP_ENA	0	R/W	Loop the device bus through this port. The MAC is potentially bypassed.	0x0

7.10.2 DEV:MAC_CFG_STATUS

Parent: DEV

Instances: 1

The 1G MAC module contains configuration and status registers related to the MAC module of the 1G Device.

Table 390 • **Registers in MAC_CFG_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_ENA_CFG	0x00000000	1	Mode Configuration Register	Page 286
MAC_MODE_CFG	0x00000004	1	Mode Configuration Register	Page 286
MAC_MAXLEN_CFG	0x00000008	1	Max Length Configuration Register	Page 286
MAC_TAGS_CFG	0x0000000C	1	VLAN / Service tag configuration register	Page 287
MAC_ADV_CHK_CFG	0x00000010	1	Advanced Check Feature Configuration Register	Page 288
MAC_IFG_CFG	0x00000014	1	Inter Frame Gap Configuration Register	Page 288
MAC_HDX_CFG	0x00000018	1	Half Duplex Configuration Register	Page 289
MAC_FC_CFG	0x00000020	1	MAC Flow Control Configuration Register	Page 290

Table 390 • **Registers in MAC_CFG_STATUS *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_FC_MAC_LOW_CFG	0x00000024	1	MAC Flow Control Configuration Register	Page 291
MAC_FC_MAC_HIGH_CFG	0x00000028	1	MAC Flow Control Configuration Register	Page 291
MAC_STICKY	0x0000002C	1	Sticky Bit Register	Page 291

7.10.2.1 DEV:MAC_CFG_STATUS:MAC_ENA_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 391 • **Fields in MAC_ENA_CFG**

Field Name	Bit	Access	Description	Default
RX_ENA	4	R/W	Receiver Module Enable. '0': Receiver Module Disabled '1': Receiver Module Enabled	0x0
TX_ENA	0	R/W	Transmitter Module Enable. '0': Transmitter Module Disabled '1': Transmitter Module Enabled	0x0

7.10.2.2 DEV:MAC_CFG_STATUS:MAC_MODE_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 392 • **Fields in MAC_MODE_CFG**

Field Name	Bit	Access	Description	Default
GIGA_MODE_ENA	4	R/W	Enables 1 Gbps mode. '0': 10/100 Mbps mode '1': 1 Gbps mode. Note: FDX_ENA must also be set.	0x1
FDX_ENA	0	R/W	Enables Full Duplex: '0': Half Duplex '1': Full duplex. Note: Full duplex MUST be selected if GIGA_MODE is enabled.	0x1

7.10.2.3 DEV:MAC_CFG_STATUS:MAC_MAXLEN_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 393 • **Fields in MAC_MAXLEN_CFG**

Field Name	Bit	Access	Description	Default
MAX_LEN	15:0	R/W	When set, single tagged frames are allowed to be 4 bytes longer than the MAC_MAXLEN_CFG configuration and double tagged frames are allowed to be 8 bytes longer. Single tagged frames are adjusted if VLAN_AWR_ENA is also set. Double tagged frames are adjusted if both VLAN_AWR_ENA and VLAN_DBL_AWR_ENA are set.	0x05EE

7.10.2.4 DEV:MAC_CFG_STATUS:MAC_TAGS_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

The MAC can be configured to accept 0, 1 and 2 tags and the TAG value can be user-defined.

Table 394 • **Fields in MAC_TAGS_CFG**

Field Name	Bit	Access	Description	Default
TAG_ID	31:16	R/W	This field defines which EtherTypes are recognized as a VLAN TPID - besides 0x8100. The value is used for all tag positions. I.e. a double tagged frame can have the following tag values: (TAG1,TAG2): (0x8100, 0x8100) (0x8100, TAG_ID) (TAG_ID, 0x8100) or (TAG_ID, TAG_ID) Single tagged frame can have the following TPID values: 0x8100 or TAG_ID.	0x8100
VLAN_DBL_AWR_ENA	1	R/W	If set, double tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). VLAN_AWR_ENA must be set when VLAN_DBL_AWR_ENA is set. '0': The MAC does not look for inner tags. '1': The MAC accepts inner tags with TPID=0x8100 or TAG_ID.	0x0

Table 394 • **Fields in MAC_TAGS_CFG *(continued)***

Field Name	Bit	Access	Description	Default
VLAN_AWR_ENA	0	R/W	If set, single tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). '0': The MAC does not look for any tags. '1': The MAC accepts outer tags with TPID=0x8100 or TAG_ID.	0x0
VLAN_LEN_AWR_ENA	2	R/W	When set, single tagged frames are allowed to be 4 bytes longer than the MAC_MAXLEN_CFG configuration and double tagged frames are allowed to be 8 bytes longer. Single tagged frames are adjusted if VLAN_AWR_ENA is also set. Double tagged frames are adjusted if both VLAN_AWR_ENA and VLAN_DBL_AWR_ENA are set.	0x1

7.10.2.5 DEV:MAC_CFG_STATUS:MAC_ADV_CHK_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 395 • **Fields in MAC_ADV_CHK_CFG**

Field Name	Bit	Access	Description	Default
LEN_DROP_ENA	0	R/W	Length Drop Enable: Configures the Receive Module to drop frames in reference to in-range and out-of-range errors: '0': Length Drop Disabled '1': Length Drop Enabled.	0x0

7.10.2.6 DEV:MAC_CFG_STATUS:MAC_IFG_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 396 • **Fields in MAC_IFG_CFG**

Field Name	Bit	Access	Description	Default
TX_IFG	12:8	R/W	Used to adjust the duration of the inter-frame gap in the Tx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX 0x19, 0x13 1000 Mbps: 0x07.	0x07

Table 396 • **Fields in MAC_IFG_CFG *(continued)***

Field Name	Bit	Access	Description	Default
RX_IFG2	7:4	R/W	Used to adjust the duration of the second part of the inter-frame gap in the Rx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX: 0x8, 0xB 1000 Mbps: 0x1.	0x1
RX_IFG1	3:0	R/W	Used to adjust the duration of the first part of the inter-frame gap in the Rx direction and must be set according to the speed settings. 10/100 Mbps: 0x7 1000 Mbps: 0x5.	0x5

7.10.2.7 DEV:MAC_CFG_STATUS:MAC_HDX_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 397 • **Fields in MAC_HDX_CFG**

Field Name	Bit	Access	Description	Default
WEXC_DIS	24	R/W	Determines whether the MAC backs off after an excessive collision has occurred. If set, back off is disabled after excessive collisions. '0': Back off after excessive collisions '1': Don't back off after excessive collisions	0x0
SEED	23:16	R/W	Seed value loaded into the PRBS of the MAC. Used to prevent excessive collision events.	0x00
SEED_LOAD	12	R/W	Load SEED value into PRNG register. A SEED value is loaded into the PRNG register of the MAC, when SEED_LOAD is asserted. After a load, the SEED_LOAD must be deasserted. '0': Do not load SEED value '1': Load SEED value.	0x0

Table 397 • **Fields in MAC_HDX_CFG *(continued)***

Field Name	Bit	Access	Description	Default
RETRY_AFTER_EXC_COL_ENA	8	R/W	This bit is used to setup the MAC to retransmit a frame after an early collision even though 16 (or more) early collisions have occurred. '0': A frame is discarded and counted as an excessive collision if 16 collisions occur for this frame. '1': The MAC retransmits a frame after an early collision, regardless of the number of previous early collisions. The backoff sequence is reset after every 16 collisions.	0x0
LATE_COL_POS	6:0	R/W	Adjustment of early/late collision boundary: This bitgroup is used to adjust the MAC so that a collision on a shared transmission medium before bit 512 is handled as an early collision, whereas a collision after bit 512 is handled as a late collision, i.e. no retransmission is performed.	0x43

7.10.2.8 DEV:MAC_CFG_STATUS:MAC_FC_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 398 • **Fields in MAC_FC_CFG**

Field Name	Bit	Access	Description	Default
ZERO_PAUSE_ENA	18	R/W	If set, a zero-delay pause frame is transmitted when flow control is deasserted. '0': Don't send zero pause frame. '1': Send zero pause frame.	0x0
TX_FC_ENA	17	R/W	When set the MAC will send pause control frames in the Tx direction. '0': Don't send pause control frames '1': Send pause control frames	0x0
RX_FC_ENA	16	R/W	When set the MAC obeys received pause control frames '0': Don't obey received pause control frames '1': Obey received pause control frames.	0x0

Table 398 • **Fields in MAC_FC_CFG *(continued)***

Field Name	Bit	Access	Description	Default
PAUSE_VAL_CFG	15:0	R/W	Pause timer value inserted in generated pause frames. 0: Insert timer value 0 in TX pause frame. ... N: Insert timer value N in TX pause frame.	0x0000
FC_LATENCY_CFG	24:19	R/W	Accepted reaction time for link partner after the port has transmitted a pause frame. Frames starting after this latency are aborted. Unit is 64 byte times. A value of 63 disables the feature. For proper flow control, use FC_LATENCY_CFG = 7.	0x03

7.10.2.9 DEV:MAC_CFG_STATUS:MAC_FC_MAC_LOW_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 399 • **Fields in MAC_FC_MAC_LOW_CFG**

Field Name	Bit	Access	Description	Default
MAC_LOW	23:0	R/W	Lower three bytes in the SMAC in generated flow control frames. 0xNNN: Lower three DMAC bytes	0x000000

7.10.2.10 DEV:MAC_CFG_STATUS:MAC_FC_MAC_HIGH_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Table 400 • **Fields in MAC_FC_MAC_HIGH_CFG**

Field Name	Bit	Access	Description	Default
MAC_HIGH	23:0	R/W	Higher three bytes in the SMAC in generated flow control frames. 0xNNN: Higher three DMAC bytes	0x000000

7.10.2.11 DEV:MAC_CFG_STATUS:MAC_STICKY

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Clear the sticky bits by writing a '0' in the relevant bitgroups (writing a '1' sets the bit)!.

Table 401 • **Fields in MAC_STICKY**

Field Name	Bit	Access	Description	Default
RX_IPG_SHRINK_STICKY	9	Sticky	Sticky bit indicating that an inter packet gap shrink was detected (IPG < 12 bytes).	0x0
RX_PREAM_SHRINK_STICKY	8	Sticky	Sticky bit indicating that a preamble shrink was detected (preamble < 8 bytes). '0': no preamble shrink was detected '1': a preamble shrink was detected one or more times Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_STICKY	7	Sticky	Sticky bit indicating that a carrier extend was detected. '0': no carrier extend was detected '1': one or more carrier extends were detected Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_ERR_STICKY	6	Sticky	Sticky bit indicating that a carrier extend error was detected. '0': no carrier extend error was detected '1': one or more carrier extend errors were detected Bit is cleared by writing a '1' to this position.	0x0
RX_JUNK_STICKY	5	Sticky	Sticky bit indicating that junk was received (bytes not recognized as a frame). '0': no junk was received '1': junk was received one or more times Bit is cleared by writing a '1' to this position.	0x0
TX_RETRANSMIT_STICKY	4	Sticky	Sticky bit indicating that the transmit MAC asked the host for a frame retransmission. '0': no tx retransmission was initiated '1': one or more tx retransmissions were initiated Bit is cleared by writing a '1' to this position.	0x0

Table 401 • **Fields in MAC_STICKY *(continued)***

Field Name	Bit	Access	Description	Default
TX_JAM_STICKY	3	Sticky	Sticky bit indicating that the transmit host issued a jamming signal. '0': the transmit host issued no jamming signal '1': the transmit host issued one or more jamming signals Bit is cleared by writing a '1' to this position.	0x0
TX_FIFO_OFLW_STICKY	2	Sticky	Sticky bit indicating that the MAC transmit FIFO has overrun.	0x0
TX_FRM_LEN_OVR_STICKY	1	Sticky	Sticky bit indicating that the transmit frame length has overrun. I.e. a frame longer than 64K occurred. '0': no tx frame length error occurred '1': one or more tx frames length errors occurred Bit is cleared by writing a '1' to this position.	0x0
TX_ABORT_STICKY	0	Sticky	Sticky bit indicating that the transmit host initiated abort was executed.	0x0

7.10.3 DEV:PCS1G_CFG_STATUS

Parent: DEV

Instances: 1

Configuration and status register set for PCS1G

Table 402 • **Registers in PCS1G_CFG_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS1G_CFG	0x00000000	1	PCS1G Configuration	Page 294
PCS1G_MODE_CFG	0x00000004	1	PCS1G Mode Configuration	Page 294
PCS1G_SD_CFG	0x00000008	1	PCS1G Signal Detect Configuration	Page 295
PCS1G_ANEG_CFG	0x0000000C	1	PCS1G Aneg Configuration	Page 295
PCS1G_ANEG_NP_CFG	0x00000010	1	PCS1G Aneg Next Page Configuration	Page 296
PCS1G_LB_CFG	0x00000014	1	PCS1G Loopback Configuration	Page 296
PCS1G_ANEG_STATUS	0x00000020	1	PCS1G ANEG Status Register	Page 297

Table 402 • **Registers in PCS1G_CFG_STATUS *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS1G_ANEG_NP_STATUS	0x00000024	1	PCS1G Aneg Next Page Status Register	Page 297
PCS1G_LINK_STATUS	0x00000028	1	PCS1G link status	Page 298
PCS1G_LINK_DOWN_CNT	0x0000002C	1	PCS1G link down counter	Page 298
PCS1G_STICKY	0x00000030	1	PCS1G sticky register	Page 299
PCS1G_LPI_CFG	0x00000038	1	PCS1G Low Power Idle Configuration	Page 299
PCS1G_LPI_WAKE_ERROR_CNT	0x0000003C	1	PCS1G wake error counter	Page 300
PCS1G_LPI_STATUS	0x00000040	1	PCS1G Low Power Idle Status	Page 300

7.10.3.1 DEV:PCS1G_CFG_STATUS:PCS1G_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G main configuration register

Table 403 • **Fields in PCS1G_CFG**

Field Name	Bit	Access	Description	Default
LINK_STATUS_TYPE	4	R/W	Set type of link_status indication at CPU-System 0: Sync_status (from PCS synchronization state machine) 1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (Link up/down)	0x0
PCS_ENA	0	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

7.10.3.2 DEV:PCS1G_CFG_STATUS:PCS1G_MODE_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G mode configuration

Table 404 • **Fields in PCS1G_MODE_CFG**

Field Name	Bit	Access	Description	Default
UNIDIR_MODE_ENA	4	R/W	Unidirectional mode enable. Implementation of 802.3, Clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0
SGMII_MODE_ENA	0	R/W	Selection of PCS operation 0: PCS is used in SERDES mode 1: PCS is used in SGMII mode. Configuration bit PCS1G_ANEG_CFG.SW_RESOLVE_ENA must be set additionally	0x1

7.10.3.3 DEV:PCS1G_CFG_STATUS:PCS1G_SD_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G signal_detect configuration

Table 405 • **Fields in PCS1G_SD_CFG**

Field Name	Bit	Access	Description	Default
SD_SEL	8	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
SD_POL	4	R/W	Signal detect polarity: The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set) 0: Signal Detect input pin must be '0' to indicate a signal detection 1: Signal Detect input pin must be '1' to indicate a signal detection	0x1
SD_ENA	0	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1

7.10.3.4 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation configuration register

Table 406 • **Fields in PCS1G_ANEG_CFG**

Field Name	Bit	Access	Description	Default
ADV_ABILITY	31:16	R/W	Advertised Ability Register: Holds the capabilities of the device as described IEEE 802.3, Clause 37. If SGMII mode is selected (PCS1G_MODE_CFG.SGMII_MODE_ENA = 1), SW_RESOLVE_ENA must be set.	0x0000
SW_RESOLVE_ENA	8	R/W	Software Resolve Abilities 0: If Auto Negotiation fails (no matching HD or FD capabilities) the link is disabled 1: The result of an Auto Negotiation is ignored - the link can be setup via software. This bit must be set in SGMII mode.	0x0
ANEG_RESTART_ONE_SHOT	1	One-shot	Auto Negotiation Restart 0: No action 1: Restart Auto Negotiation	0x0
ANEG_ENA	0	R/W	Auto Negotiation Enable 0: Auto Negotiation Disabled 1: Auto Negotiation Enabled	0x0

7.10.3.5 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_NP_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation configuration register for next-page function

Table 407 • **Fields in PCS1G_ANEG_NP_CFG**

Field Name	Bit	Access	Description	Default
NP_TX	31:16	R/W	Next page register: Holds the next-page information as described in IEEE 802.3, Clause 37	0x0000
NP_LOADED_ONE_SHOT	0	One-shot	Next page loaded 0: next page is free and can be loaded 1: next page register has been filled (to be set after np_tx has been filled)	0x0

7.10.3.6 DEV:PCS1G_CFG_STATUS:PCS1G_LB_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Loop-Back configuration register

Table 408 • **Fields in PCS1G_LB_CFG**

Field Name	Bit	Access	Description	Default
TBI_HOST_LB_ENA	0	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock 0: TBI Loopback Disabled 1:TBI Loopback Enabled	0x0

7.10.3.7 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation status register

Table 409 • **Fields in PCS1G_ANEG_STATUS**

Field Name	Bit	Access	Description	Default
LP_ADV_ABILITY	31:16	R/O	Advertised abilities from link partner as described in IEEE 802.3, Clause 37	0x0000
PR	4	R/O	Resolve priority 0: ANEG is in progress 1: ANEG nearly finished - priority can be resolved (via software)	0x0
PAGE_RX_STICKY	3	Sticky	Status indicating whether a new page has been received. 0: No new page received 1: New page received Bit is cleared by writing a 1 to this position.	0x0
ANEG_COMPLETE	0	R/O	Auto Negotiation Complete 0: No Auto Negotiation has been completed 1: Indicates that an Auto Negotiation has completed successfully	0x0

7.10.3.8 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_NP_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation next page status register

Table 410 • **Fields in PCS1G_ANEG_NP_STATUS**

Field Name	Bit	Access	Description	Default
LP_NP_RX	31:16	R/O	Next page ability register from link partner as described in IEEE 802.3, Clause 37	0x0000

7.10.3.9 DEV:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G link status register

Table 411 • **Fields in PCS1G_LINK_STATUS**

Field Name	Bit	Access	Description	Default
SIGNAL_DETECT	8	R/O	Indicates whether or not the selected Signal Detect input line is asserted 0: No signal detected 1: Signal detected	0x0
LINK_STATUS	4	R/O	Indicates whether the link is up or down. A link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK 0: Link down 1: Link up	0x0
SYNC_STATUS	0	R/O	Indicates if PCS has successfully synchronized 0: PCS is out of sync 1: PCS has synchronized	0x0

7.10.3.10 DEV:PCS1G_CFG_STATUS:PCS1G_LINK_DOWN_CNT

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G link down counter register

Table 412 • **Fields in PCS1G_LINK_DOWN_CNT**

Field Name	Bit	Access	Description	Default
LINK_DOWN_CNT	7:0	R/W	Link Down Counter. A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register	0x00

7.10.3.11 DEV:PCS1G_CFG_STATUS:PCS1G_STICKY

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G status register for sticky bits

Table 413 • **Fields in PCS1G_STICKY**

Field Name	Bit	Access	Description	Default
LINK_DOWN_STICKY	4	Sticky	The sticky bit is set when the link has been down - i.e. if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles. This occurs if e.g. ANEG is restarted or for example if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode). By setting the UDLT bit, the required down time can be reduced to 9,77 us (1.56 us) 0: Link is up 1: Link has been down Bit is cleared by writing a 1 to this position.	0x0
OUT_OF_SYNC_STICKY	0	Sticky	Sticky bit indicating if PCS synchronization has been lost 0: Synchronization has not been lost at any time 1: Synchronization has been lost for one or more clock cycles Bit is cleared by writing a 1 to this position.	0x0

7.10.3.12 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

Configuration register for Low Power Idle (Energy Efficient Ethernet)

Table 414 • **Fields in PCS1G_LPI_CFG**

Field Name	Bit	Access	Description	Default
QSGMII_MS_SEL	20	R/W	QSGMII master/slave selection (only one master allowed per QSGMII). The master drives LPI timing on serdes 0: Slave 1: Master	0x1

Table 414 • **Fields in PCS1G_LPI_CFG *(continued)***

Field Name	Bit	Access	Description	Default
TX_ASSERT_LPIDLE	0	R/W	Assert Low-Power Idle (LPI) in transmit mode 0: Disable LPI transmission 1: Enable LPI transmission	0x0

7.10.3.13 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_WAKE_ERROR_CNT

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Low Power Idle wake error counter (Energy Efficient Ethernet)

Table 415 • **Fields in PCS1G_LPI_WAKE_ERROR_CNT**

Field Name	Bit	Access	Description	Default
WAKE_ERROR_CNT	15:0	R/W	Wake Error Counter. A counter that is incremented when the link partner does not send wake-up burst in due time. The counter saturates at 65535 and is cleared when writing 0 to the register	0x0000

7.10.3.14 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

Status register for Low Power Idle (Energy Efficient Ethernet)

Table 416 • **Fields in PCS1G_LPI_STATUS**

Field Name	Bit	Access	Description	Default
RX_LPI_EVENT_STICKY	12	Sticky	Receiver Low-Power idle occurrence 0: No LPI symbols received 1: Receiver has received LPI symbols Bit is cleared by writing a 1 to this position.	0x0
RX_QUIET	9	R/O	Receiver Low-Power Quiet mode 0: Receiver not in quiet mode 1: Receiver is in quiet mode	0x0
RX_LPI_MODE	8	R/O	Receiver Low-Power Idle mode 0: Receiver not in low power idle mode 1: Receiver is in low power idle mode	0x0

Table 416 • **Fields in PCS1G_LPI_STATUS *(continued)***

Field Name	Bit	Access	Description	Default
TX_LPI_EVENT_STICKY	4	Sticky	Transmitter Low-Power idle occurrence 0: No LPI symbols transmitted 1: Transmitter has transmitted LPI symbols Bit is cleared by writing a 1 to this position.	0x0
TX_QUIET	1	R/O	Transmitter Low-Power Quiet mode 0: Transmitter not in quiet mode 1: Transmitter is in quiet mode	0x0
TX_LPI_MODE	0	R/O	Transmitter Low-Power Idle mode 0: Transmitter not in low power idle mode 1: Transmitter is in low power idle mode	0x0

7.10.4 DEV:PCS1G_TSTPAT_CFG_STATUS

Parent: DEV

Instances: 1

PCS1G testpattern configuration and status register set

Table 417 • **Registers in PCS1G_TSTPAT_CFG_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS1G_TSTPAT_MODE_CFG	0x00000000	1	PCS1G TSTPAT MODE CFG	Page 301
PCS1G_TSTPAT_STATUS	0x00000004	1	PCS1G TSTPAT STATUS	Page 302

7.10.4.1 DEV:PCS1G_TSTPAT_CFG_STATUS:PCS1G_TSTPAT_MODE_CFG

Parent: DEV:PCS1G_TSTPAT_CFG_STATUS

Instances: 1

PCS1G testpattern mode configuration register (Frame based pattern 4 and 5 might be not available depending on chip type)

Table 418 • **Fields in PCS1G_TSTPAT_MODE_CFG**

Field Name	Bit	Access	Description	Default
JTP_SEL	2:0	R/W	Jitter Test Pattern Select: Enables and selects the jitter test pattern to be transmitted. The jitter test patterns are according to the IEEE 802.3, Annex 36A 0: Disable transmission of test patterns 1: High frequency test pattern - repeated transmission of D21.5 code group 2: Low frequency test pattern - repeated transmission of K28.7 code group 3: Mixed frequency test pattern - repeated transmission of K28.5 code group 4: Long continuous random test pattern (packet length is 1524 bytes) 5: Short continuous random test pattern (packet length is 360 bytes)	0x0

7.10.4.2 DEV:PCS1G_TSTPAT_CFG_STATUS:PCS1G_TSTPAT_STATUS

Parent: DEV:PCS1G_TSTPAT_CFG_STATUS

Instances: 1

PCS1G testpattern status register

Table 419 • **Fields in PCS1G_TSTPAT_STATUS**

Field Name	Bit	Access	Description	Default
JTP_ERR_CNT	15:8	R/W	Jitter Test Pattern Error Counter. The counter saturates at 255 and is cleared by writing 0 to the register.	0x00
JTP_ERR	4	R/O	Jitter Test Pattern Error 0: Jitter pattern checker has found no error 1: Jitter pattern checker has found an error	0x0
JTP_LOCK	0	R/O	Jitter Test Pattern Lock 0: Jitter pattern checker has not locked 1: Jitter pattern checker has locked	0x0

7.10.5 DEV:PCS_FX100_CONFIGURATION

Parent: DEV

Instances: 1

Configuration register set for PCS 100Base-FX logic

Table 420 • **Registers in PCS_FX100_CONFIGURATION**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS_FX100_CFG	0x00000000	1	PCS 100Base FX Configuration	Page 303

7.10.5.1 DEV:PCS_FX100_CONFIGURATION:PCS_FX100_CFG

Parent: DEV:PCS_FX100_CONFIGURATION

Instances: 1

Configuration bit groups for 100Base-FX PCS

Table 421 • **Fields in PCS_FX100_CFG**

Field Name	Bit	Access	Description	Default
SD_SEL	26	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
RESERVED	25	R/W	Must be set to its default.	0x1
SD_ENA	24	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1
RESERVED	15:12	R/W	Must be set to its default.	0x4
LINKHYSTTIMER	7:4	R/W	Link hysteresis timer configuration. The hysteresis time lasts [linkhysttimer] * 65536 ns + 2320 ns. If linkhysttime is set to 5, the hysteresis lasts the minimum time of 330 us as specified in IEEE802.3 - 24.3.3.4.	0x5
UNIDIR_MODE_ENA	3	R/W	Unidirectional mode enable. Implementation 0f 802.3 clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0

Table 421 • **Fields in PCS_FX100_CFG *(continued)***

Field Name	Bit	Access	Description	Default
FEFCHK_ENA	2	R/W	Far-End Fault (FEF) detection enable 0: Disable FEF detection 1 Enable FEF detection	0x1
FEFGEN_ENA	1	R/W	Far-End Fault (FEF) generation enable 0: Disable FEF generation 1 Enable FEF generation	0x1
PCS_ENA	0	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

7.10.6 DEV:PCS_FX100_STATUS

Parent: DEV

Instances: 1

Status register set for PCS 100Base-FX logic

Table 422 • **Registers in PCS_FX100_STATUS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS_FX100_STATUS	0x00000000	1	PCS 100Base FX Status	Page 304

7.10.6.1 DEV:PCS_FX100_STATUS:PCS_FX100_STATUS

Parent: DEV:PCS_FX100_STATUS

Instances: 1

Status bit groups for 100Base-FX PCS. Note: If sigdet_cfg != "00" is selected status signal "signal_detect" shows the internal signal_detect value is gated with the status of rx toggle-rate control circuitry.

Table 423 • **Fields in PCS_FX100_STATUS**

Field Name	Bit	Access	Description	Default
PCS_ERROR_STICKY	7	Sticky	PCS error has occurred 1: RX_ER was high while RX_DV active 0: No RX_ER indication found while RX_DV active Bit is cleared by writing a 1 to this position.	0x0

Table 423 • **Fields in PCS_FX100_STATUS *(continued)***

Field Name	Bit	Access	Description	Default
FEF_FOUND_STICKY	6	Sticky	Far-end Fault state has occurred 1: A Far-End Fault has been detected 0: No Far-End Fault occurred Bit is cleared by writing a 1 to this position.	0x0
SSD_ERROR_STICKY	5	Sticky	Stream Start Delimiter error occurred 1: A Start-of-Stream Delimiter error has been detected 0: No SSD error occurred Bit is cleared by writing a 1 to this position.	0x0
SYNC_LOST_STICKY	4	Sticky	Synchronization lost 1: Synchronization lost 0: No sync lost occurred Bit is cleared by writing a 1 to this position.	0x0
FEF_STATUS	2	R/O	Current status of Far-end Fault detection state 1: Link currently in fault state 0: Link is in normal state	0x0
SIGNAL_DETECT	1	R/O	Current status of selected signal_detect input line 1: Proper signal detected 0: No proper signal found	0x0
SYNC_STATUS	0	R/O	Status of synchronization 1: Link established 0: No link found	0x0

7.11 ICPU_CFG

Table 424 • **Register Groups in ICPU_CFG**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
CPU_SYSTEM_CTRL	0x00000000	1	Configurations for the CPU system.	Page 306
SPI_MST	0x00000050	1	SPI Master Configuration	Page 308
MPU8051	0x00000068	1	Configuration/status for the 8051	Page 309
INTR	0x00000084	1	Interrupt Registers	Page 313
TIMERS	0x00000208	1	Timer Registers	Page 339
TWI_DELAY	0x000002A4	1	Configuration registers	Page 342

7.11.1 ICPU_CFG:CPU_SYSTEM_CTRL

Parent: ICPU_CFG

Instances: 1

Table 425 • **Registers in CPU_SYSTEM_CTRL**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPR	0x00000000	8 0x00000004	General Purpose Register	Page 306
RESET	0x00000020	1	Reset Settings	Page 306
GENERAL_STAT	0x00000028	1	General status	Page 307

7.11.1.1 ICPU_CFG:CPU_SYSTEM_CTRL:GPR

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 8

Table 426 • **Fields in GPR**

Field Name	Bit	Access	Description	Default
GPR	31:0	R/W	General purpose 8 times 32-bit registers for software development and debug.	0x00000000

7.11.1.2 ICPU_CFG:CPU_SYSTEM_CTRL:RESET

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 1

Table 427 • **Fields in RESET**

Field Name	Bit	Access	Description	Default
CPU_RELEASE	4	R/W	Set this field to enable the VCore CPU. This field is only valid when automatic booting of the VCore CPU has been disabled via VCore_Cfg inputs. This field has no effect when the VCore CPU is configured for automatically boot. Note: By using this field it is possible for an external CPU to manually load a code image to memory, change into normal mode, and then release the VCore CPU after which it will boot from memory rather than FLASH. 0: VCore CPU is forced in reset 1: VCore CPU is allowed to boot	0x0

Table 427 • **Fields in RESET *(continued)***

Field Name	Bit	Access	Description	Default
CORE_RST_CPU_ONLY	3	R/W	Set this field to enable VCore System reset protection. It is possible to protect the VCore System from soft-reset (issued via RESET:CORE_RST_FORCE) and watchdog-timeout. When this field is set the aforementioned resets only reset the VCore CPU, not the VCore System. 0: WDT event reset entire VCore 1: WDT event only reset the VCore CPU	0x0
CORE_RST_PROTECT	2	R/W	Set this field to enable VCore reset protection. It is possible to protect the entire VCore from chip-level soft-reset (issued via DEVCPU_GCB::SOFT_CHIP_RST.SOFT_CHIP_RST). Setting this field does not protect against hard-reset of the chip (by asserting the reset pin). 0: No reset protection 1: VCore is protected from chip-level-soft-reset	0x0
CORE_RST_FORCE	1	One-shot	Set this field to generate a soft reset for the VCore. This field will be cleared when the reset has taken effect. It is possible to protect the VCore system (everything else than the VCore CPU) from reset via RESET.CORE_RST_CPU_ONLY. 0: VCore is not reset 1: Initiate soft reset of the VCore	0x0
RESERVED	0	R/W	Must be set to its default.	0x1

7.11.1.3 ICPU_CFG:CPU_SYSTEM_CTRL:GENERAL_STAT

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 1

Table 428 • **Fields in GENERAL_STAT**

Field Name	Bit	Access	Description	Default
CPU_SLEEP	3	R/O	This field is set if the VCore CPU has entered sleep mode.	0x0
BOOT_MODE	1	R/O	This field shows which boot strategy that has been configured for the VCore CPU. 0: Automatic booting 1: Manual booting	0x0

7.11.2 ICPU_CFG:SPI_MST

Parent: ICPU_CFG

Instances: 1

Table 429 • **Registers in SPI_MST**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SPI_MST_CFG	0x00000000	1	SPI Master Configuration	Page 308
SW_MODE	0x00000014	1	Manual control of the SPI interface	Page 308

7.11.2.1 ICPU_CFG:SPI_MST:SPI_MST_CFG

Parent: ICPU_CFG:SPI_MST

Instances: 1

Table 430 • **Fields in SPI_MST_CFG**

Field Name	Bit	Access	Description	Default
FAST_READ_ENA	10	R/W	The type of read-instruction that the SPI Controller generates for reads. 0: READ (slow read - Instruction code - 0x03) 1: FAST READ (fast read - Instruction code - 0x0B)	0x0
CS_DESELECT_TIME	9:5	R/W	The minimum number of SPI clock cycles for which the SPI chip select (SI_nEn) must be deasserted in between transfers. Typical value of this is 100 ns. Setting this field to 0 is illegal.	0x1F
CLK_DIV	4:0	R/W	Controls the clock frequency for the SPI interface (SI_Clk). The clock frequency is VCore system clock divided by the value of this field. Setting this field to 0 or 1 value is illegal.	0x1F

7.11.2.2 ICPU_CFG:SPI_MST:SW_MODE

Parent: ICPU_CFG:SPI_MST

Instances: 1

Table 431 • **Fields in SW_MODE**

Field Name	Bit	Access	Description	Default
SW_PIN_CTRL_MODE	13	R/W	Set to enable software pin control mode (Bit banging), when set software has direct control of the SPI interface. This mode is used for writing into flash.	0x0
SW_SPI_SCK	12	R/W	Value to drive on SI_Clk output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_SCK_OE	11	R/W	Set to enable drive of SI_Clk output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_SDO	10	R/W	Value to drive on SI_DO output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_SDO_OE	9	R/W	Set to enable drive of SI_DO output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_CS	5	R/W	Value to drive on SI_nEn output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_CS_OE	1	R/W	Set to enable drive of SI_nEn output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_SDI	0	R/O	Current value of the SI_DI input.	0x0

7.11.3 ICPU_CFG:MPU8051

Parent: ICPU_CFG

Instances: 1

Table 432 • **Registers in MPU8051**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MPU8051_STAT	0x00000004	1	Status from the 8051	Page 310
MPU8051_MMAP	0x00000008	1	Configuration of the 8051 memory mapping mechanism	Page 310

Table 432 • **Registers in MPU8051 *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MEMACC_CTRL	0x0000000C	1	Configuration of and status for the load/examine of the onchip 8051 memory.	Page 311
MEMACC	0x00000010	1	Configure where in the onchip 8051 memory to load/examine.	Page 312
MEMACC_SBA	0x00000014	1		Page 312

7.11.3.1 ICPU_CFG:MPU8051:MPU8051_STAT

Parent: ICPU_CFG:MPU8051

Instances: 1

These read only fields can be used for debugging 8051 programs.

Table 433 • **Fields in MPU8051_STAT**

Field Name	Bit	Access	Description	Default
MPU8051_STOP	8	R/O	Set when the 8051 has stopped itself by setting bit 2 in the PCON SFR register.	0x0
MPU8051_GPR	7:0	R/O	A read-only copy of the 8051 GPR register at SFR address 0xF0.	0x00

7.11.3.2 ICPU_CFG:MPU8051:MPU8051_MMAP

Parent: ICPU_CFG:MPU8051

Instances: 1

The MAP_* and MSADDR_* fields in this register is similar to the corresponding 8051 SFR register for control mapping the on-chip memory into the 8051 memory space. These fields must be used to configure 8051 memory mapping if the 8051 on-chip memory is loaded manually via an external processor. If the 8051 program itself does loading of on-chip memory then it must instead use the SFR equivalents.

Table 434 • **Fields in MPU8051_MMAP**

Field Name	Bit	Access	Description	Default
MSADDR_CODE_HIGH	7	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0

Table 434 • **Fields in MPU8051_MMAP *(continued)***

Field Name	Bit	Access	Description	Default
MSADDR_CODE_LOW	6	R/W	Configure which half of the on-chip memory an 8051 code-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MSADDR_DATA_HIGH	5	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the high 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MSADDR_DATA_LOW	4	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MAP_CODE_HIGH	3	R/W	Set to map 8051 code-accesses in the high 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_CODE_LOW	2	R/W	Set to map 8051 code-accesses in the low 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_DATA_HIGH	1	R/W	Set to map 8051 data-accesses in the high 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_DATA_LOW	0	R/W	Set to map 8051 data-accesses in the low 32KByte memory range to on-chip memory instead of FLASH.	0x0

7.11.3.3 ICPU_CFG:MPU8051:MEMACC_CTRL

Parent: ICPU_CFG:MPU8051

Instances: 1

Table 435 • **Fields in MEMACC_CTRL**

Field Name	Bit	Access	Description	Default
MEMACC_EXAMINE	1	R/W	This field controls if the onchip 8051 memory is either loaded (written) or examined (read). 0: Load data from SBA to onchip memory. 1: Examine data from onchip memory to SBA.	0x0
MEMACC_DO	0	One-shot	Set this field to start an access with the parameters specified by MEMACC_CTRL.MEMACC_EXAMINE, MEMACC.MEMACC_START, MEMACC.MEMACC_STOP, and MEMACC_SBA.MEMACC_SBA_START. This field is cleared when the requested number of 32-bit words has been transfered.	0x0

7.11.3.4 ICPU_CFG:MPU8051:MEMACC

Parent: ICPU_CFG:MPU8051

Instances: 1

When loading (or examining) onchip 8051 memory, then it is only possible to move 32-bit words. This is why bits [17:16] and [1:0] of this register is not implemented. Setting START and STOP addresses determines how many words that are loaded (or examined). For example, when loading programs of less than 64KBytes, decreasing the stop address will speed up the load time.

When manually loading or examining the onchip 8051 memory via an external CPU the data has to be put somewhere in SBA memory space on its way into or out-of the onchip 8051 memory, for this the 8 x 32-bit general purpose registers starting at 0x70000000 is a good choice. By using all (or some) of these registers it is possible to move up to 8 32-bit words to/from the onchip memory per access.

Table 436 • **Fields in MEMACC**

Field Name	Bit	Access	Description	Default
MEMACC_STOP	31:18	R/W	Ending 32-bit word address when loading or examining the onchip 8051 memory, the value of this field must be equal to or higher than the MEMACC.MEMACC_START field.	0x3FFF
MEMACC_START	15:2	R/W	Starting 32-bit word address when loading or examining the onchip 8051 memory.	0x0000

7.11.3.5 ICPU_CFG:MPU8051:MEMACC_SBA

Parent: ICPU_CFG:MPU8051

Instances: 1

There is no stop address in the SBA address space. The number of 32-bit words which is moved per access is determined by the MEMACC.MEMACC_START and MEMACC.MEMACC_STOP.

Table 437 • **Fields in MEMACC_SBA**

Field Name	Bit	Access	Description	Default
MEMACC_SBA_START	31:2	R/W	This field determines where in the SBA memory space (32-bit alligned) the automatic load/examine mechanims reads/writes data to/from the onchip 8051 memory.	0x10000000

7.11.4 ICPU_CFG:INTR

Parent: ICPU_CFG

Instances: 1

Table 438 • **Registers in INTR**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
INTR	0x00000000	1	Interrupt sticky bits	Page 314
INTR_ENA	0x00000004	1	Interrupt enable	Page 317
INTR_ENA_CLR	0x00000008	1	Clear interrupt enable	Page 318
INTR_ENA_SET	0x0000000C	1	Set interrupt enable	Page 319
INTR_RAW	0x00000010	1	Raw of interrupt source	Page 320
ICPU_IRQ0_ENA	0x00000014	1	Enable of ICPU_IRQ0 interrupt	Page 321
ICPU_IRQ0_IDENT	0x00000018	1	Sources of ICPU_IRQ0 interrupt	Page 322
ICPU_IRQ1_ENA	0x0000001C	1	Enable of ICPU_IRQ1 interrupt	Page 323
ICPU_IRQ1_IDENT	0x00000020	1	Sources of ICPU_IRQ1 interrupt	Page 323
EXT_IRQ0_ENA	0x00000024	1	Enable of EXT_IRQ0 interrupt	Page 325
EXT_IRQ0_IDENT	0x00000028	1	Sources of EXT_IRQ0 interrupt	Page 325
DEV_IDENT	0x00000034	1	Device interrupts	Page 326
EXT_IRQ0_INTR_CFG	0x00000038	1	EXT_IRQ0 interrupt configuration	Page 326
SW0_INTR_CFG	0x00000040	1	SW0 interrupt configuration	Page 328
SW1_INTR_CFG	0x00000044	1	SW1 interrupt configuration	Page 328
MIIM1_INTR_CFG	0x00000048	1	MIIM1 interrupt configuration	Page 329

Table 438 • **Registers in INTR *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MIIM0_INTR_CFG	0x0000004C	1	MIIM0 interrupt configuration	Page 329
UART_INTR_CFG	0x00000058	1	UART interrupt configuration	Page 330
TIMER0_INTR_CFG	0x0000005C	1	TIMER0 interrupt configuration	Page 331
TIMER1_INTR_CFG	0x00000060	1	TIMER1 interrupt configuration	Page 331
TIMER2_INTR_CFG	0x00000064	1	TIMER2 interrupt configuration	Page 331
TWI_INTR_CFG	0x0000006C	1	TWI interrupt configuration	Page 332
GPIO_INTR_CFG	0x00000070	1	GPIO interrupt configuration	Page 332
SGPIO_INTR_CFG	0x00000074	1	SGPIO interrupt configuration	Page 333
DEV_ALL_INTR_CFG	0x00000078	1	DEV_ALL interrupt configuration	Page 334
BLK_ANA_INTR_CFG	0x0000007C	1	BLK_ANA interrupt configuration	Page 334
XTR_RDY0_INTR_CFG	0x00000080	1	XTR_RDY0 interrupt configuration	Page 335
XTR_RDY1_INTR_CFG	0x00000084	1	XTR_RDY1 interrupt configuration	Page 336
INJ_RDY0_INTR_CFG	0x00000090	1	INJ_RDY0 interrupt configuration	Page 336
INJ_RDY1_INTR_CFG	0x00000094	1	INJ_RDY1 interrupt configuration	Page 337
INTEGRITY_INTR_CFG	0x000000A4	1	INTEGRITY interrupt configuration	Page 338
DEV_ENA	0x000000AC	1	Device Interrupt enable	Page 338

7.11.4.1 ICPU_CFG:INTR:INTR

Parent: ICPU_CFG:INTR

Instances: 1

Asserted for the active interrupt sources.

Table 439 • **Fields in INTR**

Field Name	Bit	Access	Description	Default
MIIM1_INTR	28	Sticky	This field is set when MIIM master1 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the MIIM master1 interrupt event is no longer active.	0x0
MIIM0_INTR	27	Sticky	This field is set when MIIM master0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the MIIM master0 interrupt event is no longer active.	0x0
INTEGRITY_INTR	25	Sticky	This field is set when integrity interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if there are no longer any pending integrity interrupt event.	0x0
INJ_RDY1_INTR	21	Sticky	This field is set when inj-group-1 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the inj-group-1 interrupt event is no longer active.	0x0
INJ_RDY0_INTR	20	Sticky	This field is set when inj-group-0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the inj-group-0 interrupt event is no longer active.	0x0
XTR_RDY1_INTR	17	Sticky	This field is set when xtr-group-1 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the xtr-group-1 interrupt event is no longer active.	0x0
XTR_RDY0_INTR	16	Sticky	This field is set when xtr-group-0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the xtr-group-0 interrupt event is no longer active.	0x0
BLK_ANA_INTR	15	Sticky	This field is set when analyzer interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the analyzer interrupt event is no longer active.	0x0

Table 439 • **Fields in INTR *(continued)***

Field Name	Bit	Access	Description	Default
DEV_ALL_INTR	14	Sticky	This field is set when interrupt from any device (port) is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if there is still a pending interrupt from any device. This is a cascaded interrupt, read DEV_IDENT to see which device(s) that is/are currently interrupting.	0x0
SGPIO_INTR	13	Sticky	This field is set when Serial-GPIO interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the Serial-GPIO interrupt event is no longer active.	0x0
GPIO_INTR	12	Sticky	This field is set when Parallel-GPIO interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the Parallel-GPIO interrupt event is no longer active.	0x0
TWI_INTR	11	Sticky	This field is set when TWI interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the TWI interrupt event is no longer active.	0x0
TIMER2_INTR	9	Sticky	This field is set when Timer-2 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the Timer-2 interrupt event is no longer active.	0x0
TIMER1_INTR	8	Sticky	This field is set when Timer-1 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the Timer-1 interrupt event is no longer active.	0x0
TIMER0_INTR	7	Sticky	This field is set when Timer-0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the Timer-0 interrupt event is no longer active.	0x0
UART_INTR	6	Sticky	This field is set when UART interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the UART interrupt event is no longer active.	0x0

Table 439 • **Fields in INTR *(continued)***

Field Name	Bit	Access	Description	Default
SW1_INTR	3	Sticky	This field is set when SW1 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the SW1 interrupt event is no longer active.	0x0
SW0_INTR	2	Sticky	This field is set when SW0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the SW0 interrupt event is no longer active.	0x0
EXT_IRQ0_INTR	0	Sticky	This field is set when EXT_IRQ0 interrupt is detected. Clearing of this field is done by writing 1 to this field. This field can only be cleared if the EXT_IRQ0 interrupt event is no longer active.	0x0

7.11.4.2 ICPU_CFG:INTR:INTR_ENA

Parent: ICPU_CFG:INTR

Instances: 1

Controls if active interrupt indications (from INTR) can propagate to their destinations. In a multi-threaded environment, or with more than one active processor the INTR_ENA_SET and INTR_ENA_CLR registers can be used for atomic modifications of this register. Writing 1 to any bit(s) in the INTR_ENA_SET register will set the corresponding bit(s) in this register, Writing 1 to any bit in the INTR_ENA_CLR register will clear the corresponding bit(s) in this register.

Table 440 • **Fields in INTR_ENA**

Field Name	Bit	Access	Description	Default
MIIM1_INTR_ENA	28	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
MIIM0_INTR_ENA	27	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
INTEGRITY_INTR_ENA	25	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
INJ_RDY1_INTR_ENA	21	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
INJ_RDY0_INTR_ENA	20	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
XTR_RDY1_INTR_ENA	17	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
XTR_RDY0_INTR_ENA	16	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0

Table 440 • **Fields in INTR_ENA *(continued)***

Field Name	Bit	Access	Description	Default
BLK_ANA_INTR_ENA	15	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
DEV_ALL_INTR_ENA	14	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
SGPIO_INTR_ENA	13	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
GPIO_INTR_ENA	12	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
TWI_INTR_ENA	11	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
TIMER2_INTR_ENA	9	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
TIMER1_INTR_ENA	8	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
TIMER0_INTR_ENA	7	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
UART_INTR_ENA	6	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
SW1_INTR_ENA	3	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
SW0_INTR_ENA	2	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0
EXT_IRQ0_INTR_ENA	0	R/W	Set this field to enable the interrupt to propagate to its destination.	0x0

7.11.4.3 ICPU_CFG:INTR:INTR_ENA_CLR

Parent: ICPU_CFG:INTR

Instances: 1

Table 441 • **Fields in INTR_ENA_CLR**

Field Name	Bit	Access	Description	Default
MIIM1_INTR_ENA_CLR	28	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
MIIM0_INTR_ENA_CLR	27	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
INTEGRITY_INTR_ENA_CLR	25	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
INJ_RDY1_INTR_ENA_CLR	21	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
INJ_RDY0_INTR_ENA_CLR	20	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
XTR_RDY1_INTR_ENA_CLR	17	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0

Table 441 • **Fields in INTR_ENA_CLR *(continued)***

Field Name	Bit	Access	Description	Default
XTR_RDY0_INTR_ENA_CLR	16	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
BLK_ANA_INTR_ENA_CLR	15	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
DEV_ALL_INTR_ENA_CLR	14	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
SGPIO_INTR_ENA_CLR	13	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
GPIO_INTR_ENA_CLR	12	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
TWI_INTR_ENA_CLR	11	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
TIMER2_INTR_ENA_CLR	9	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
TIMER1_INTR_ENA_CLR	8	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
TIMER0_INTR_ENA_CLR	7	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
UART_INTR_ENA_CLR	6	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
SW1_INTR_ENA_CLR	3	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
SW0_INTR_ENA_CLR	2	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0
EXT_IRQ0_INTR_ENA_CLR	0	One-shot	Set to clear corresponding interrupt enable in INTR_ENA.	0x0

7.11.4.4 ICPU_CFG:INTR:INTR_ENA_SET

Parent: ICPU_CFG:INTR

Instances: 1

Table 442 • **Fields in INTR_ENA_SET**

Field Name	Bit	Access	Description	Default
MIIM1_INTR_ENA_SET	28	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
MIIM0_INTR_ENA_SET	27	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
INTEGRITY_INTR_ENA_SET	25	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
INJ_RDY1_INTR_ENA_SET	21	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
INJ_RDY0_INTR_ENA_SET	20	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0

Table 442 • **Fields in INTR_ENA_SET *(continued)***

Field Name	Bit	Access	Description	Default
XTR_RDY1_INTR_ENA_SET	17	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
XTR_RDY0_INTR_ENA_SET	16	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
BLK_ANA_INTR_ENA_SET	15	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
DEV_ALL_INTR_ENA_SET	14	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
SGPIO_INTR_ENA_SET	13	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
GPIO_INTR_ENA_SET	12	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
TWI_INTR_ENA_SET	11	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
TIMER2_INTR_ENA_SET	9	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
TIMER1_INTR_ENA_SET	8	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
TIMER0_INTR_ENA_SET	7	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
UART_INTR_ENA_SET	6	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
SW1_INTR_ENA_SET	3	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
SW0_INTR_ENA_SET	2	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0
EXT_IRQ0_INTR_ENA_SET	0	One-shot	Set this field to set corresponding interrupt enable in INTR_ENA.	0x0

7.11.4.5 ICPU_CFG:INTR:INTR_RAW

Parent: ICPU_CFG:INTR

Instances: 1

Shows the current value of the interrupt source to the interrupt controller (interrupts are active high). External interrupt inputs are corrected for polarity before being presented in this register.

Table 443 • **Fields in INTR_RAW**

Field Name	Bit	Access	Description	Default
MIIM1_RAW	28	R/O	Current value of interrupt source input to the interrupt controller.	0x0
MIIM0_RAW	27	R/O	Current value of interrupt source input to the interrupt controller.	0x0
INTEGRITY_RAW	25	R/O	Current value of interrupt source input to the interrupt controller.	0x0

Table 443 • **Fields in INTR_RAW *(continued)***

Field Name	Bit	Access	Description	Default
INJ_RDY1_RAW	21	R/O	Current value of interrupt source input to the interrupt controller.	0x0
INJ_RDY0_RAW	20	R/O	Current value of interrupt source input to the interrupt controller.	0x0
XTR_RDY1_RAW	17	R/O	Current value of interrupt source input to the interrupt controller.	0x0
XTR_RDY0_RAW	16	R/O	Current value of interrupt source input to the interrupt controller.	0x0
BLK_ANA_RAW	15	R/O	Current value of interrupt source input to the interrupt controller.	0x0
DEV_ALL_RAW	14	R/O	Current value of interrupt source input to the interrupt controller.	0x0
SGPIO_RAW	13	R/O	Current value of interrupt source input to the interrupt controller.	0x0
GPIO_RAW	12	R/O	Current value of interrupt source input to the interrupt controller.	0x0
TWI_RAW	11	R/O	Current value of interrupt source input to the interrupt controller.	0x0
TIMER2_RAW	9	R/O	Current value of interrupt source input to the interrupt controller.	0x0
TIMER1_RAW	8	R/O	Current value of interrupt source input to the interrupt controller.	0x0
TIMER0_RAW	7	R/O	Current value of interrupt source input to the interrupt controller.	0x0
UART_RAW	6	R/O	Current value of interrupt source input to the interrupt controller.	0x0
SW1_RAW	3	R/O	Current value of interrupt source input to the interrupt controller.	0x0
SW0_RAW	2	R/O	Current value of interrupt source input to the interrupt controller.	0x0
EXT_IRQ0_RAW	0	R/O	Current value of interrupt source input to the interrupt controller, is already corrected for polarity as configured via EXT_IRQ0_INTR_CFG.EXT_IRQ0_INTR_POL.	0x0

7.11.4.6 ICPU_CFG:INTR:ICPU_IRQ0_ENA

Parent: ICPU_CFG:INTR

Instances: 1

Table 444 • **Fields in ICPU_IRQ0_ENA**

Field Name	Bit	Access	Description	Default
ICPU_IRQ0_ENA	0	R/W	Enables ICPU_IRQ0 interrupt 0: Interrupt is disabled 1: Interrupt is enabled	0x0

7.11.4.7 ICPU_CFG:INTR:ICPU_IRQ0_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

Identifies the source(s) of an active interrupt on output interrupt: ICPU_IRQ0. All asserted interrupts are shown as active high.

Table 445 • **Fields in ICPU_IRQ0_IDENT**

Field Name	Bit	Access	Description	Default
ICPU_IRQ0_MIIM1_IDENT	28	R/O	Set when MIIM1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_MIIM0_IDENT	27	R/O	Set when MIIM0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_INTEGRITY_IDENT	25	R/O	Set when INTEGRITY interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_INJ_RDY1_IDENT	21	R/O	Set when INJ_RDY1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_INJ_RDY0_IDENT	20	R/O	Set when INJ_RDY0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_XTR_RDY1_IDENT	17	R/O	Set when XTR_RDY1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_XTR_RDY0_IDENT	16	R/O	Set when XTR_RDY0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_BLK_ANA_IDENT	15	R/O	Set when BLK_ANA interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_DEV_ALL_IDENT	14	R/O	Set when DEV_ALL interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_SGPIO_IDENT	13	R/O	Set when SGPIO interrupt is a source of the ICPU_IRQ0 interrupt.	0x0

Table 445 • **Fields in ICPU_IRQ0_IDENT *(continued)***

Field Name	Bit	Access	Description	Default
ICPU_IRQ0_GPIO_IDENT	12	R/O	Set when GPIO interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_TWI_IDENT	11	R/O	Set when TWI interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_TIMER2_IDENT	9	R/O	Set when TIMER2 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_TIMER1_IDENT	8	R/O	Set when TIMER1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_TIMER0_IDENT	7	R/O	Set when TIMER0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_UART_IDENT	6	R/O	Set when UART interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_SW1_IDENT	3	R/O	Set when SW1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_SW0_IDENT	2	R/O	Set when SW0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ0_EXT_IRQ0_IDENT	0	R/O	Set when EXT_IRQ0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0

7.11.4.8 ICPU_CFG:INTR:ICPU_IRQ1_ENA

Parent: ICPU_CFG:INTR

Instances: 1

Table 446 • **Fields in ICPU_IRQ1_ENA**

Field Name	Bit	Access	Description	Default
ICPU_IRQ1_ENA	0	R/W	Enables ICPU_IRQ1 interrupt 0: Interrupt is disabled 1: Interrupt is enabled	0x0

7.11.4.9 ICPU_CFG:INTR:ICPU_IRQ1_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

Identifies the source(s) of an active interrupt on output interrupt: ICPU_IRQ1. All asserted interrupts are shown as active high.

Table 447 • **Fields in ICPU_IRQ1_IDENT**

Field Name	Bit	Access	Description	Default
ICPU_IRQ1_MIIM1_IDENT	28	R/O	Set when MIIM1 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ1_MIIM0_IDENT	27	R/O	Set when MIIM0 interrupt is a source of the ICPU_IRQ0 interrupt.	0x0
ICPU_IRQ1_INTEGRITY_IDENT	25	R/O	Set when INTEGRITY interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_INJ_RDY1_IDENT	21	R/O	Set when INJ_RDY1 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_INJ_RDY0_IDENT	20	R/O	Set when INJ_RDY0 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_XTR_RDY1_IDENT	17	R/O	Set when XTR_RDY1 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_XTR_RDY0_IDENT	16	R/O	Set when XTR_RDY0 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_BLK_ANA_IDENT	15	R/O	Set when BLK_ANA interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_DEV_ALL_IDENT	14	R/O	Set when DEV_ALL interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_SGPIO_IDENT	13	R/O	Set when SGPIO interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_GPIO_IDENT	12	R/O	Set when GPIO interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_TWI_IDENT	11	R/O	Set when TWI interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_TIMER2_IDENT	9	R/O	Set when TIMER2 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_TIMER1_IDENT	8	R/O	Set when TIMER1 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_TIMER0_IDENT	7	R/O	Set when TIMER0 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0

Table 447 • **Fields in ICPU_IRQ1_IDENT *(continued)***

Field Name	Bit	Access	Description	Default
ICPU_IRQ1_UART_IDENT	6	R/O	Set when UART interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_SW1_IDENT	3	R/O	Set when SW1 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_SW0_IDENT	2	R/O	Set when SW0 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0
ICPU_IRQ1_EXT_IRQ0_IDENT	0	R/O	Set when EXT_IRQ0 interrupt is a source of the ICPU_IRQ1 interrupt.	0x0

7.11.4.10 ICPU_CFG:INTR:EXT_IRQ0_ENA

Parent: ICPU_CFG:INTR

Instances: 1

Table 448 • **Fields in EXT_IRQ0_ENA**

Field Name	Bit	Access	Description	Default
EXT_IRQ0_ENA	0	R/W	Enables EXT_IRQ0 interrupt 0: Interrupt is disabled 1: Interrupt is enabled	0x0

7.11.4.11 ICPU_CFG:INTR:EXT_IRQ0_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

Identifies the source(s) of an active interrupt on output interrupt: EXT_IRQ0. All asserted interrupts are shown as active high.

Table 449 • **Fields in EXT_IRQ0_IDENT**

Field Name	Bit	Access	Description	Default
EXT_IRQ0_MIIM1_IDENT	28	R/O	Set when MIIM1 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_MIIM0_IDENT	27	R/O	Set when MIIM0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_INTEGRITY_IDENT	25	R/O	Set when INTEGRITY interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_INJ_RDY1_IDENT	21	R/O	Set when INJ_RDY1 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_INJ_RDY0_IDENT	20	R/O	Set when INJ_RDY0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_XTR_RDY1_IDENT	17	R/O	Set when XTR_RDY1 interrupt is a source of the EXT_IRQ0 interrupt.	0x0

Table 449 • **Fields in EXT_IRQ0_IDENT *(continued)***

Field Name	Bit	Access	Description	Default
EXT_IRQ0_XTR_RDY0_IDENT	16	R/O	Set when XTR_RDY0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_BLK_ANA_IDENT	15	R/O	Set when BLK_ANA interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_DEV_ALL_IDENT	14	R/O	Set when DEV_ALL interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_SGPIO_IDENT	13	R/O	Set when SGPIO interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_GPIO_IDENT	12	R/O	Set when GPIO interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_TWI_IDENT	11	R/O	Set when TWI interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_TIMER2_IDENT	9	R/O	Set when TIMER2 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_TIMER1_IDENT	8	R/O	Set when TIMER1 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_TIMER0_IDENT	7	R/O	Set when TIMER0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_UART_IDENT	6	R/O	Set when UART interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_SW1_IDENT	3	R/O	Set when SW1 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_SW0_IDENT	2	R/O	Set when SW0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0
EXT_IRQ0_EXT_IRQ0_IDENT	0	R/O	Set when EXT_IRQ0 interrupt is a source of the EXT_IRQ0 interrupt.	0x0

7.11.4.12 ICPU_CFG:INTR:DEV_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

Shows the sources of the DEV_ALL interrupt.

Table 450 • **Fields in DEV_IDENT**

Field Name	Bit	Access	Description	Default
DEV_IDENT	31:0	R/O	Bits in this field is set when the corresponding device is interrupting, bit 0 corresponds to device 0, bit 1 to device 1 and so on. When any bit in this field is set the DEV_ALL interrupt is also asserted.	0x00000000

7.11.4.13 ICPU_CFG:INTR:EXT_IRQ0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 451 • **Fields in EXT_IRQ0_INTR_CFG**

Field Name	Bit	Access	Description	Default
EXT_IRQ0_INTR_DRV	6	R/W	Configures when to drive the external interrupt EXT_IRQ0 output, this setting applies only when EXT_IRQ0 is configured for output mode. 0: Only drive when interrupt is active 1: Always driven	0x0
EXT_IRQ0_INTR_DIR	5	R/W	Controls the direction of external interrupt: EXT_IRQ0. In input mode the interrupt can used as source in the interrupt controller, in this mode any configurations related to the output mode of the interrupt has no effect. In output mode sources can be assigned to the interrupt, in this mode the EXT_IRQ0 must not be enabled as interrupt source (INTR_ENA.EXT_IRQ0_INTR_ENA must remain 0). 0: Input 1: Output	0x0
EXT_IRQ0_INTR_POL	4	R/W	Controls the interrupt polarity of external interrupt: EXT_IRQ0. This setting is applies to both to input and output mode. The polarity is corrected at the edge of the chip, internally interrupts are always active-high. 0: Active low 1: Active high	0x0
EXT_IRQ0_INTR_FORCE	3	One-shot	Set to force assertion of EXT_IRQ0 interrupt. This field is cleared immediately after generating interrupt.	0x0
EXT_IRQ0_INTR_TRIGGER	2	R/W	Controls whether interrupts from the EXT_IRQ0 interrupt are edge (low-to-high-transition) or level (interrupt while high value is seen) sensitive. 0: LEVEL sensitive 1: EDGE sensitive	0x0
EXT_IRQ0_INTR_SEL	1:0	R/W	Selects the destination of the EXT_IRQ0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.14 ICPU_CFG:INTR:SW0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 452 • **Fields in SW0_INTR_CFG**

Field Name	Bit	Access	Description	Default
SW0_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
SW0_INTR_FORCE	3	One-shot	Set to force assertion of SW0 interrupt. This field is cleared immediately after generating interrupt.	0x0
SW0_INTR_SEL	1:0	R/W	Selects the destination of the SW0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.15 ICPU_CFG:INTR:SW1_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 453 • **Fields in SW1_INTR_CFG**

Field Name	Bit	Access	Description	Default
SW1_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
SW1_INTR_FORCE	3	One-shot	Set to force assertion of SW1 interrupt.	0x0

Table 453 • **Fields in SW1_INTR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
SW1_INTR_SEL	1:0	R/W	Selects the destination of the SW1 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.16 ICPU_CFG:INTR:MIIM1_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 454 • **Fields in MIIM1_INTR_CFG**

Field Name	Bit	Access	Description	Default
MIIM1_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
MIIM1_INTR_FORCE	3	One-shot	Set to force assertion of MIIM1 interrupt. This field is cleared immediately after generating interrupt.	0x0
MIIM1_INTR_SEL	1:0	R/W	Selects the destination of the MIIM1 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.17 ICPU_CFG:INTR:MIIM0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 455 • **Fields in MIIM0_INTR_CFG**

Field Name	Bit	Access	Description	Default
MIIM0_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
MIIM0_INTR_FORCE	3	One-shot	Set to force assertion of MIIM0 interrupt. This field is cleared immediately after generating interrupt.	0x0
MIIM0_INTR_SEL	1:0	R/W	Selects the destination of the MIIM0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.18 ICPU_CFG:INTR:UART_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 456 • **Fields in UART_INTR_CFG**

Field Name	Bit	Access	Description	Default
UART_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
UART_INTR_FORCE	3	One-shot	Set to force assertion of UART interrupt. This field is cleared immediately after generating interrupt.	0x0

Table 456 • **Fields in UART_INTR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
UART_INTR_SEL	1:0	R/W	Selects the destination of the UART interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.19 ICPU_CFG:INTR:TIMER0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 457 • **Fields in TIMER0_INTR_CFG**

Field Name	Bit	Access	Description	Default
TIMER0_INTR_FORCE	3	One-shot	Set to force assertion of TIMER0 interrupt. This field is cleared immediately after generating interrupt.	0x0
TIMER0_INTR_SEL	1:0	R/W	Selects the destination of the TIMER0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.20 ICPU_CFG:INTR:TIMER1_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 458 • **Fields in TIMER1_INTR_CFG**

Field Name	Bit	Access	Description	Default
TIMER1_INTR_FORCE	3	One-shot	Set to force assertion of TIMER1 interrupt. This field is cleared immediately after generating interrupt.	0x0
TIMER1_INTR_SEL	1:0	R/W	Selects the destination of the TIMER1 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.21 ICPU_CFG:INTR:TIMER2_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 459 • **Fields in TIMER2_INTR_CFG**

Field Name	Bit	Access	Description	Default
TIMER2_INTR_FORCE	3	One-shot	Set to force assertion of TIMER2 interrupt. This field is cleared immediately after generating interrupt.	0x0
TIMER2_INTR_SEL	1:0	R/W	Selects the destination of the TIMER2 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.22 ICPU_CFG:INTR:TWI_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 460 • **Fields in TWI_INTR_CFG**

Field Name	Bit	Access	Description	Default
TWI_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
TWI_INTR_FORCE	3	One-shot	Set to force assertion of TWI interrupt. This field is cleared immediately after generating interrupt.	0x0
TWI_INTR_SEL	1:0	R/W	Selects the destination of the TWI interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.23 ICPU_CFG:INTR:GPIO_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 461 • **Fields in GPIO_INTR_CFG**

Field Name	Bit	Access	Description	Default
GPIO_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
GPIO_INTR_FORCE	3	One-shot	Set to force assertion of GPIO interrupt. This field is cleared immediately after generating interrupt.	0x0
GPIO_INTR_SEL	1:0	R/W	Selects the destination of the GPIO interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.24 ICPU_CFG:INTR:SGPIO_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 462 • **Fields in SGPIO_INTR_CFG**

Field Name	Bit	Access	Description	Default
SGPIO_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
SGPIO_INTR_FORCE	3	One-shot	Set to force assertion of SGPIO interrupt. This field is cleared immediately after generating interrupt.	0x0

Table 462 • **Fields in SGPIO_INTR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
SGPIO_INTR_SEL	1:0	R/W	Selects the destination of the SGPIO interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.25 ICPU_CFG:INTR:DEV_ALL_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 463 • **Fields in DEV_ALL_INTR_CFG**

Field Name	Bit	Access	Description	Default
DEV_ALL_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
DEV_ALL_INTR_FORCE	3	One-shot	Set to force assertion of DEV_ALL interrupt. This field is cleared immediately after generating interrupt.	0x0
DEV_ALL_INTR_SEL	1:0	R/W	Selects the destination of the DEV_ALL interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.26 ICPU_CFG:INTR:BLK_ANA_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 464 • **Fields in BLK_ANA_INTR_CFG**

Field Name	Bit	Access	Description	Default
BLK_ANA_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set, the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer have any effect.	0x0
BLK_ANA_INTR_FORCE	3	One-shot	Set to force assertion of BLK_ANA interrupt. This field is cleared immediately after generating interrupt.	0x0
BLK_ANA_INTR_SEL	1:0	R/W	Selects the destination of the BLK_ANA interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0 3: EXT_IRQ1	0x0

7.11.4.27 ICPU_CFG:INTR:XTR_RDY0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 465 • **Fields in XTR_RDY0_INTR_CFG**

Field Name	Bit	Access	Description	Default
XTR_RDY0_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
XTR_RDY0_INTR_FORCE	3	One-shot	Set to force assertion of XTR_RDY0 interrupt. This field is cleared immediately after generating interrupt.	0x0

Table 465 • **Fields in XTR_RDY0_INTR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
XTR_RDY0_INTR_SEL	1:0	R/W	Selects the destination of the XTR_RDY0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.28 ICPU_CFG:INTR:XTR_RDY1_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 466 • **Fields in XTR_RDY1_INTR_CFG**

Field Name	Bit	Access	Description	Default
XTR_RDY1_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
XTR_RDY1_INTR_FORCE	3	One-shot	Set to force assertion of XTR_RDY1 interrupt. This field is cleared immediately after generating interrupt.	0x0
XTR_RDY1_INTR_SEL	1:0	R/W	Selects the destination of the XTR_RDY1 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.29 ICPU_CFG:INTR:INJ_RDY0_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 467 • **Fields in INJ_RDY0_INTR_CFG**

Field Name	Bit	Access	Description	Default
INJ_RDY0_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
INJ_RDY0_INTR_FORCE	3	One-shot	Set to force assertion of INJ_RDY0 interrupt. This field is cleared immediately after generating interrupt.	0x0
INJ_RDY0_INTR_SEL	1:0	R/W	Selects the destination of the INJ_RDY0 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.30 ICPU_CFG:INTR:INJ_RDY1_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 468 • **Fields in INJ_RDY1_INTR_CFG**

Field Name	Bit	Access	Description	Default
INJ_RDY1_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
INJ_RDY1_INTR_FORCE	3	One-shot	Set to force assertion of INJ_RDY1 interrupt. This field is cleared immediately after generating interrupt.	0x0

Table 468 • **Fields in INJ_RDY1_INTR_CFG *(continued)***

Field Name	Bit	Access	Description	Default
INJ_RDY1_INTR_SEL	1:0	R/W	Selects the destination of the INJ_RDY1 interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.31 ICPU_CFG:INTR:INTEGRITY_INTR_CFG

Parent: ICPU_CFG:INTR

Instances: 1

Table 469 • **Fields in INTEGRITY_INTR_CFG**

Field Name	Bit	Access	Description	Default
INTEGRITY_INTR_BYPASS	4	R/W	Set to bypass sticky interrupt functionality. When set the value from the interrupting source is passed directly to the destination interrupt. This feature can be useful when mapping a small number of interrupts via external interrupt output to an external CPU. When this field is set, the TRIGGER and FORCE fields no longer has any effect.	0x0
INTEGRITY_INTR_FORCE	3	One-shot	Set to force assertion of INTEGRITY interrupt. This field is cleared immediately after generating interrupt.	0x0
INTEGRITY_INTR_SEL	1:0	R/W	Selects the destination of the INTEGRITY interrupt. 0: ICPU_IRQ0 1: ICPU_IRQ1 2: EXT_IRQ0	0x0

7.11.4.32 ICPU_CFG:INTR:DEV_ENA

Parent: ICPU_CFG:INTR

Instances: 1

Table 470 • **Fields in DEV_ENA**

Field Name	Bit	Access	Description	Default
DEV_ENA	31:0	R/W	Clear individual bits in this register to disable interrupts from specific devices.	0x00000000

7.11.5 ICPU_CFG:TIMERS

Parent: ICPU_CFG

Instances: 1

Table 471 • **Registers in TIMERS**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
WDT	0x00000000	1	Watchdog Timer	Page 339
TIMER_TICK_DIV	0x00000004	1	Timer Tick Divider	Page 340
TIMER_VALUE	0x00000008	3 0x00000004	Timer value	Page 340
TIMER_RELOAD_VALUE	0x00000014	3 0x00000004	Timer Reload Value	Page 341
TIMER_CTRL	0x00000020	3 0x00000004	Timer Control	Page 341

7.11.5.1 ICPU_CFG:TIMERS:WDT

Parent: ICPU_CFG:TIMERS

Instances: 1

Table 472 • **Fields in WDT**

Field Name	Bit	Access	Description	Default
WDT_STATUS	9	R/O	Shows whether the last reset was caused by a watchdog timer reset. This field is updated during reset, therefore it is always valid. 0: Reset was not caused by WDT 1: Reset was caused by WDT timeout	0x0
WDT_ENABLE	8	R/W	Use this field to enable or disable the watchdog timer. When the WDT is enabled, it causes a reset after 2 seconds if it is not periodically reset. This field is only read by the WDT after a successful lock sequence (WDT_LOCK). 0: WDT is disabled 1: WDT is enabled	0x0

Table 472 • **Fields in WDT *(continued)***

Field Name	Bit	Access	Description	Default
WDT_LOCK	7:0	R/W	Use this field to configure and reset the WDT. When writing 0xBE to this field immediately followed by writing 0xEF, the WDT resets and configurations are read from this register (as set when the 0xEF is written). When the WDT is enabled, writing any value other than 0xBE or 0xEF after 0xBE is written, causes a WDT reset as if the timer had run out.	0x00

7.11.5.2 ICPU_CFG:TIMERS:TIMER_TICK_DIV

Parent: ICPU_CFG:TIMERS

Instances: 1

Table 473 • **Fields in TIMER_TICK_DIV**

Field Name	Bit	Access	Description	Default
TIMER_TICK_DIV	17:0	R/W	The timer tick generator runs from a 250MHz base clock. By default, the divider value generates a timer tick every 100 us (10 KHz). The timer tick is used for all of the timers (except the WDT). This field must not be set to generate a timer tick of less than 0.1 us (higher than 10 MHz). If this field is changed, it may take up to 2 ms before the timers are running stable at the new frequency. The timer tick frequency is: 250MHz/(TIMER_TICK_DIV+1).	0x061A7

7.11.5.3 ICPU_CFG:TIMERS:TIMER_VALUE

Parent: ICPU_CFG:TIMERS

Instances: 3

Table 474 • **Fields in TIMER_VALUE**

Field Name	Bit	Access	Description	Default
TIMER_VAL	31:0	R/W	The current value of the timer. When enabled via TIMER_CTRL.TIMER_ENA the timer decrements at every timer tick (see TIMER_TICK_DIV for more info on timer tick frequency). When the timer has reached 0, and a timer-tick is received, then an interrupt is generated. For example; If a periodic interrupt is needed every 1ms, and the timer tick is generated every 100us then the TIMER_VALUE (and TIMER_RELOAD_VALUE) must be configured to 9. By default the timer will reload from the TIMER_RELOAD_VALUE when interrupt is generated, and then continue decrementing from the reloaded value. It is possible to make the timer stop after generating interrupt by setting TIMER_CTRL.ONE_SHOT.	0x00000000

7.11.5.4 ICPU_CFG:TIMERS:TIMER_RELOAD_VALUE

Parent: ICPU_CFG:TIMERS

Instances: 3

Table 475 • **Fields in TIMER_RELOAD_VALUE**

Field Name	Bit	Access	Description	Default
RELOAD_VAL	31:0	R/W	The contents of this field are loaded into the corresponding timer (TIMER_VALUE) when it wraps (decrements a zero).	0x00000000

7.11.5.5 ICPU_CFG:TIMERS:TIMER_CTRL

Parent: ICPU_CFG:TIMERS

Instances: 3

Table 476 • **Fields in TIMER_CTRL**

Field Name	Bit	Access	Description	Default
ONE_SHOT_ENA	2	R/W	When set the timer will automatically disable itself after it has generated interrupt.	0x0

Table 476 • **Fields in TIMER_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
TIMER_ENA	1	R/W	When enabled, the corresponding timer decrements at each timer-tick. If TIMER_CTRL.ONE_SHOT_ENA is set this field is cleared when the timer reach 0 and interrupt is generated. 0: Timer is disabled 1: Timer is enabled	0x0
FORCE_RELOAD	0	One-shot	Set this field to force the reload of the timer, this will set the TIMER_VALUE to TIMER_RELOAD_VALUE for the corresponding timer. This field can be set at the same time as enabling the counter, in that case the counter will be reloaded and then enabled for counting.	0x0

7.11.6 ICPU_CFG:TWI_DELAY

Parent: ICPU_CFG

Instances: 1

Table 477 • **Registers in TWI_DELAY**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TWI_CONFIG	0x00000000	1	Configuration registers	Page 342

7.11.6.1 ICPU_CFG:TWI_DELAY:TWI_CONFIG

Parent: ICPU_CFG:TWI_DELAY

Instances: 1

Table 478 • **Fields in TWI_CONFIG**

Field Name	Bit	Access	Description	Default
TWI_CNT_RELOAD	8:1	R/W	Configure the hold time delay to apply to SDA after SCK when transmitting from the device. The delay depends on the VCore system clock period. If for example the VCore system clock is 125MHz then the period is 8ns, in turn the hold time will then be (TWI_CNT_RELOAD+2) * 8ns. Replace the clock period for other VCore system frequencies. The resulting value should be as close to 300ns as possible without going below 300ns.	0x00
TWI_DELAY_ENABLE	0	R/W	Set this field to enable hold time on the TWI SDA output. When enabled the TWI_CONFIG.TWI_CNT_RELOAD field determines the amount of hold time to apply to SDA.	0x0

7.12 UART

Table 479 • **Register Groups in UART**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
UART	0x00000000	1	UART registers	Page 343

7.12.1 UART:UART

Parent: UART

Instances: 1

Table 480 • **Registers in UART**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RBR_THR	0x00000000	1	Receive Buffer / Transmit Holding Register / Divisor (Low)	Page 344
IER	0x00000004	1	Interrupt Enable Register / Divisor (High)	Page 345

Table 480 • **Registers in UART *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
IIR_FCR	0x00000008	1	Interrupt Identification Register / FIFO Control Register	Page 346
LCR	0x0000000C	1	Line Control Register	Page 348
MCR	0x00000010	1	Modem Control Register	Page 349
LSR	0x00000014	1	Line Status Register	Page 350
MSR	0x00000018	1	Modem Status Register	Page 353
SCR	0x0000001C	1	Scratchpad Register	Page 354
USR	0x0000007C	1	UART Status Register	Page 354

7.12.1.1 UART:UART:RBR_THR

Parent: UART:UART

Instances: 1

When the LCR.DLAB is set, this register is the lower 8 bits of the 16-bit Divisor register that contains the baud rate divisor for the UART.

The output baud rate is equal to the VCore system clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (VCore clock freq) / (16 * divisor). Note that with the Divisor set to zero, the baud clock is disabled and no serial communications occur. In addition, once this register is set, wait at least 0.1us before transmitting or receiving data.

Table 481 • **Fields in RBR_THR**

Field Name	Bit	Access	Description	Default
RBR_THR	7:0	R/W	Use this register to access the Rx and Tx FIFOs. When reading: The data in this register is valid only if LSR.DR is set. If FIFOs are disabled (IIR_FCR.FIFOE), the data in this register must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. When FIFOs are enabled (IIR_FCR.FIFOE), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data is lost and an overrun error occurs. When writing: Data should only be written to this register when the LSR.THRE indicates that there is room in the FIFO. If FIFOs are disabled (IIR_FCR.FIFOE), writes to this register while LSR.THRE is zero, causes the register to be overwritten. When FIFOs are enabled (IIR_FCR.FIFOE) and LSR.THRE is set, 16 characters may be written to this register before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.	0x00

7.12.1.2 UART:UART:IER

Parent: UART:UART

Instances: 1

When the LCR.DLAB is set, this register is the upper 8 bits of the 16-bit Divisor register that contains the baud rate divisor for the UART. For more information and a description of how to calculate the baud rate, see RBR_THR.

Table 482 • **Fields in IER**

Field Name	Bit	Access	Description	Default
PTIME	7	R/W	Programmable THRE interrupt mode enable. This is used to enable or disable the generation of THRE interrupt. 0: Disabled 1: Enabled	0x0

Table 482 • **Fields in IER *(continued)***

Field Name	Bit	Access	Description	Default
EDSSI	3	R/W	Enable modem status interrupt. This is used to enable or disable the generation of Modem Status interrupt. This is the fourth highest priority interrupt. 0: Disabled 1: Enabled	0x0
ELSI	2	R/W	Enable receiver line status interrupt. This is used to enable or disable the generation of Receiver Line Status interrupt. This is the highest priority interrupt. 0: Disabled 1: Enabled	0x0
ETBEI	1	R/W	Enable transmit holding register empty interrupt. This is used to enable or disable the generation of Transmitter Holding Register Empty interrupt. This is the third highest priority interrupt. 0: Disabled 1: Enabled	0x0
ERBFI	0	R/W	Enable received data available interrupt. This is used to enable or disable the generation of Received Data Available interrupt and the Character Timeout interrupt (if FIFOs are enabled). These are the second highest priority interrupts. 0: Disabled 1: Enabled	0x0

7.12.1.3 UART:UART:IIR_FCR

Parent: UART:UART

Instances: 1

This register has special meaning when reading, here the lowest 4 bits indicate interrupting sources. The encoding is as follows:

0110; type: Receiver line status, priority: Highest. Overrun/parity/ framing errors or break interrupt. Cleared by reading LSR.

0100; type: Received data available, priority: Second. RCVR FIFO trigger level reached. Cleared when FIFO drops below the trigger level.

1100; type: Character timeout indication, priority: Second. No characters in or out of the RCVR FIFO during the last four character times and there is at least 1 character in it during this time. Cleared by reading the receiver buffer register.

0010; type: Transmit holding register empty, priority: Third. Transmitter holding register empty (Prog. THRE Mode disabled) or XMIT FIFO at or below threshold (Prog. THRE Mode enabled). Cleared by reading the IIR register (if source of interrupt); or, writing into THR (THRE Mode disabled) or XMIT FIFO above threshold (THRE Mode enabled).

0000; type: Modem status, priority: Fourth. Clear to send. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt. Cleared by reading the Modem status register.

0111; type: Busy detect indication, priority: Fifth. Master has tried to write to the Line Control register while the UART is busy (USR[0] is set to one). Cleared by reading the UART status register.

0001: No interrupting sources.

Table 483 • **Fields in IIR_FCR**

Field Name	Bit	Access	Description	Default
FIFOSE_RT	7:6	R/W	When reading this field, the current status of the FIFO is returned; 00 for disabled or 11 for enabled. Writing this field selects the trigger level in the receive FIFO at which the Received Data Available interrupt is generated (see encoding.) In auto flow control mode, it is used to determine when to generate back-pressure using the RTS signal. 00: 1 character in the Rx FIFO 01: Rx FIFO 1/4 full 10: Rx FIFO 1/2 full 11: Rx FIFO 2 less than full	0x1
TET	5:4	R/W	Tx empty trigger. When the THRE mode is enabled (IER.PTIME), this field selects the empty threshold level at which the THRE Interrupts are generated. 00: Tx FIFO empty 01: 2 characters in the Tx FIFO 10: Tx FIFO 1/4 full 11: Tx FIFO 1/2 full	0x0
XFIFOR	2	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. Tx FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is self-clearing. It is not necessary to clear this bit.	0x0
RFIFOR	1	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. Rx FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is self-clearing. It is not necessary to clear this bit.	0x0

Table 483 • **Fields in IIR_FCR *(continued)***

Field Name	Bit	Access	Description	Default
FIFOE	0	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. FIFO Enable. This enables or disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs are reset.	0x0

7.12.1.4 UART:UART:LCR

Parent: UART:UART

Instances: 1

Writes can be made to this register, with the exception of the BC field, only when UART is not busy, that is, when USR.BUSY is zero. This register can always be read.

Table 484 • **Fields in LCR**

Field Name	Bit	Access	Description	Default
DLAB	7	R/W	Divisor latch access bit. This bit is used to enable reading and writing of the Divisor registers (RBR_THR and IER) to set the baud rate of the UART. To access other registers, this bit must be cleared after initial baud rate setup.	0x0
BC	6	R/W	Break control bit.This bit is used to cause a break condition to be transmitted to the receiving device. If set to one, the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial output is forced low until the Break bit is cleared.	0x0
EPS	4	R/W	Even parity select. This bit is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.	0x0

Table 484 • **Fields in LCR *(continued)***

Field Name	Bit	Access	Description	Default
PEN	3	R/W	Parity enable. This bit is used to enable or disable parity generation and detection in both transmitted and received serial characters. 0: Parity disabled 1: Parity enabled	0x0
STOP	2	R/W	Number of stop bits. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR.DLS), one and a half stop bits are transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when LCR.DLS is zero, otherwise, 2 stop bits	0x0
DLS	1:0	R/W	Data length select. This is used to select the number of data bits per character that the peripheral transmits and receives. The following settings specify the number of bits that may be selected. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	0x0

7.12.1.5 UART:UART:MCR

Parent: UART:UART

Instances: 1

Table 485 • **Fields in MCR**

Field Name	Bit	Access	Description	Default
AFCE	5	R/W	Auto flow control enable. This mode requires that FIFOs are enabled and that MCR.RTS is set. 0: Auto flow control mode disabled 1: Auto flow control mode enabled	0x0

Table 485 • **Fields in MCR *(continued)***

Field Name	Bit	Access	Description	Default
LB	4	R/W	Loopback Bit. This is used to put the UART into a diagnostic mode for test purposes. The transmit line is held high, while serial transmit data is looped back to the receive line internally. In this mode, all the interrupts are fully functional. In addition, in loopback mode, the modem control input CTS is disconnected, and the modem control output RTS is looped back to the input internally.	0x0
RTS	1	R/W	Request to send. This is used to directly control the Request to Send (RTS) output. The RTS output is used to inform the partner that the UART is ready to exchange data. The RTS is still controlled from this field when Auto RTS Flow Control is enabled (MCR.AFCE), but the output can be forced high by the flow control mechanism. If this field is cleared, the UART permanently indicates backpressure to the partner. 0: RTS is set high 1: RTS is set low	0x0

7.12.1.6 UART:UART:LSR

Parent: UART:UART

Instances: 1

Table 486 • **Fields in LSR**

Field Name	Bit	Access	Description	Default
RFE	7	R/W	Receiver FIFO error bit. This bit is only valid when FIFOs are enabled. This is used to indicate whether there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. 0: No error in Rx FIFO 1: Error in Rx FIFO	0x0

Table 486 • **Fields in LSR** ***(continued)***

Field Name	Bit	Access	Description	Default
TEMT	6	R/W	Transmitter empty bit. If FIFOs are enabled, this bit is set whenever the Transmitter Shift Register and the FIFO are both empty.	0x1
THRE	5	R/W	If FIFO (IIR_FCR.FIFOE) and THRE mode are enabled (IER.PTIME), this bit indicates that the Tx FIFO is full. Otherwise, this bit indicates that the Tx FIFO is empty.	0x1
BI	4	R/W	Break interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input is held in a logic 0 state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all-zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.	0x0

Table 486 • **Fields in LSR *(continued)***

Field Name	Bit	Access	Description	Default
FE	3	R/W	Framing error bit. This is used to indicate the a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. A framing error is associated with a received character. Therefore, in FIFO mode, an error is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues to receive the other bit, that is, data and/or parity, and then stops. Note that this field is set if a break interrupt has occurred, as indicated by Break Interrupt (LSR.BI). This field is cleared on read. 0: No framing error 1: Framing error	0x0
PE	2	R/W	Parity error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable bit (LCR.PEN) is set. A parity error is associated with a received character. Therefore, in FIFO mode, an error is revealed when the character with the parity error arrives at the top of the FIFO. Note that this field is set if a break interrupt has occurred, as indicated by Break Interrupt (LSR.BI). This field is cleared on read. 0: No parity error 1: Parity error	0x0

Table 486 • **Fields in LSR *(continued)***

Field Name	Bit	Access	Description	Default
OE	1	R/W	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In non-FIFO mode, the OE bit is set when a new character arrives before the previous character was read. When this happens, the data in the RBR is overwritten. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. This field is cleared on read. 0: No overrun error 1: Overrun error	0x0
DR	0	R/W	Data ready. This is used to indicate that the receiver contains at least one character in the receiver FIFO. This bit is cleared when the RX FIFO is empty. 0: No data ready 1: Data ready	0x0

7.12.1.7 UART:UART:MSR

Parent: UART:UART

Instances: 1

Table 487 • **Fields in MSR**

Field Name	Bit	Access	Description	Default
CTS	4	R/O	Clear to send. This field indicates the current state of the modem control line, CTS. When the Clear to Send input (CTS) is asserted, it is an indication that the partner is ready to exchange data with the UART. 0: CTS input is deasserted (logic 0) 1: CTS input is asserted (logic 1)	0x0

Table 487 • **Fields in MSR *(continued)***

Field Name	Bit	Access	Description	Default
DCTS	0	R/O	Delta clear to send. This is used to indicate that the modem control line, CTS, has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. Note: If the DCTS bit is not set, the CTS signal is asserted, and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed, if the CTS signal remains asserted. A read of the MSR after reset can be performed to prevent unwanted interrupts. 0: No change on CTS since the last read of the MSR 1: Change on CTS since the last read of the MSR	0x0

7.12.1.8 UART:UART:SCR

Parent: UART:UART

Instances: 1

Table 488 • **Fields in SCR**

Field Name	Bit	Access	Description	Default
SCR	7:0	R/W	This register is for programmers to use as a temporary storage space. It has no functional purpose for the UART.	0x00

7.12.1.9 UART:UART:USR

Parent: UART:UART

Instances: 1

Table 489 • **Fields in USR**

Field Name	Bit	Access	Description	Default
BUSY	0	R/O	UART busy. 0: UART is idle or inactive 1: UART is busy (actively transferring data)	0x0

7.13 TWI

Table 490 • **Register Groups in TWI**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
TWI	0x00000000	1	Two-Wire Interface Controller Registers	Page 355

7.13.1 TWI:TWI

Parent: TWI

Instances: 1

Table 491 • **Registers in TWI**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CFG	0x00000000	1	TWI Configuration	Page 356
TAR	0x00000004	1	Target Address	Page 358
SAR	0x00000008	1	Slave Address	Page 358
DATA_CMD	0x00000010	1	Rx/Tx Data Buffer and Command	Page 359
SS_SCL_HCNT	0x00000014	1	Standard Speed TWI Clock SCL High Count	Page 360
SS_SCL_LCNT	0x00000018	1	Standard Speed TWI Clock SCL Low Count	Page 361
FS_SCL_HCNT	0x0000001C	1	Fast Speed TWI Clock SCL High Count	Page 361
FS_SCL_LCNT	0x00000020	1	Fast Speed TWI Clock SCL Low Count	Page 362
INTR_STAT	0x0000002C	1	Interrupt Status	Page 362
INTR_MASK	0x00000030	1	Interrupt Mask	Page 362
RAW_INTR_STAT	0x00000034	1	Raw Interrupt Status	Page 363
RX_TL	0x00000038	1	Receive FIFO Threshold	Page 367
TX_TL	0x0000003C	1	Transmit FIFO Threshold	Page 368
CLR_INTR	0x00000040	1	Clear Combined and Individual Interrupt	Page 368
CLR_RX_UNDER	0x00000044	1	Clear RX_UNDER Interrupt	Page 368
CLR_RX_OVER	0x00000048	1	Clear RX_OVER Interrupt	Page 369
CLR_TX_OVER	0x0000004C	1	Clear TX_OVER Interrupt	Page 369
CLR_RD_REQ	0x00000050	1	Clear RD_REQ Interrupt	Page 369
CLR_TX_ABRT	0x00000054	1	Clear TX_ABRT Interrupt	Page 369

Table 491 • **Registers in TWI *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CLR_RX_DONE	0x00000058	1	Clear RX_DONE Interrupt	Page 370
CLR_ACTIVITY	0x0000005C	1	Clear ACTIVITY Interrupt	Page 370
CLR_STOP_DET	0x00000060	1	Clear STOP_DET Interrupt	Page 370
CLR_START_DET	0x00000064	1	Clear START_DET Interrupt	Page 371
CLR_GEN_CALL	0x00000068	1	Clear GEN_CALL Interrupt	Page 371
CTRL	0x0000006C	1	TWI Control	Page 371
STAT	0x00000070	1	TWI Status	Page 372
TXFLR	0x00000074	1	Transmit FIFO Level	Page 373
RXFLR	0x00000078	1	Receive FIFO Level	Page 374
TX_ABRT_SOURCE	0x00000080	1	Transmit Abort Source	Page 374
SDA_SETUP	0x00000094	1	SDA Setup	Page 376
ACK_GEN_CALL	0x00000098	1	ACK General Call	Page 376
ENABLE_STATUS	0x0000009C	1	Enable Status	Page 377

7.13.1.1 TWI:TWI:CFG

Parent: TWI:TWI

Instances: 1

Table 492 • **Fields in CFG**

Field Name	Bit	Access	Description	Default
SLAVE_DIS	6	R/W	This bit controls whether the TWI controller has its slave disabled. If this bit is set (slave is disabled), the controller functions only as a master and does not perform any action that requires a slave. '0': slave is enabled '1': slave is disabled	0x1

Table 492 • **Fields in CFG *(continued)***

Field Name	Bit	Access	Description	Default
RESTART_ENA	5	R/W	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several operations. When RESTART is disabled, the master is prohibited from performing the following functions: * Change direction within a transfer (split) * Send a START BYTE * Combined format transfers in 7-bit addressing modes * Read operation with a 10-bit address * Send multiple bytes per transfer By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting RAW_INTR_STAT.TX_ABRT. '0': disable '1': enable	0x1
MASTER_10BITADDR	4	R/W	Controls whether transfers starts in 7- or 10-bit addressing mode when acting as a master. '0': 7-bit addressing '1': 10-bit addressing	0x0
SLAVE_10BITADDR	3	R/W	Controls whether the TWI controller responds to 7- or 10-bit addresses in slave mode. In 7-bit mode; transactions that involve 10-bit addressing are ignored and only the lower 7 bits of the SAR register are compared. '0': 7-bit addressing. '1': 10-bit addressing.	0x0
SPEED	2:1	R/W	These bits control at which speed the TWI controller operates; its setting is relevant only in master mode. Hardware protects against illegal values being programmed by software. '1': standard mode (100 kbit/s) '2': fast mode (400 kbit/s)	0x2

Table 492 • **Fields in CFG *(continued)***

Field Name	Bit	Access	Description	Default
MASTER_ENA	0	R/W	This bit controls whether the TWI master is enabled. '0': master disabled '1': master enabled	0x1

7.13.1.2 TWI:TWI:TAR

Parent: TWI:TWI

Instances: 1

Table 493 • **Fields in TAR**

Field Name	Bit	Access	Description	Default
GC_OR_START_ENA	11	R/W	This bit indicates whether software performs a General Call or START BYTE command. '0': ignore bit 10 GC_OR_START and use TAR normally '1': perform special TWI command as specified in GC_OR_START bit	0x0
GC_OR_START	10	R/W	If TAR.SPECIAL is set to 1, then this bit indicates whether a General Call or START byte command is to be performed. '0': General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting RAW_INTR_STAT.TX_ABRT. The TWI controller remains in General Call mode until the TAR.SPECIAL field is cleared. '1': START BYTE	0x0
TAR	9:0	R/W	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the TAR and SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.	0x055

7.13.1.3 TWI:TWI:SAR

Parent: TWI:TWI

Instances: 1

Table 494 • **Fields in SAR**

Field Name	Bit	Access	Description	Default
SAR	9:0	R/W	The SAR holds the slave address when the TWI is operating as a slave. For 7-bit addressing, only SAR[6:0] is used. This register can be written only when the TWI interface is disabled (ENABLE = 0).	0x055

7.13.1.4 TWI:TWI:DATA_CMD

Parent: TWI:TWI

Instances: 1

Table 495 • **Fields in DATA_CMD**

Field Name	Bit	Access	Description	Default
CMD	8	R/W	This bit controls whether a read or a write is performed. This bit does not control the direction when the TWI acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that CPU data is to be transmitted and as DATA. When programming this bit, please remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (RAW_INTR_STAT.R_TX_ABRT), unless TAR.SPECIAL has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master TWI read transfer, a RD_REQ interrupt may have occurred simultaneously due to a remote TWI master addressing this controller. In this type of scenario, the TWI controller ignores the DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt. '1' = Read '0' = Write	0x0
DATA	7:0	R/W	This register contains the data to be transmitted or received on the TWI bus. If you are writing to this register and want to perform a read, this field is ignored by the controller. However, when you read this register, these bits return the value of data received on the TWI interface.	0x00

7.13.1.5 TWI:TWI:SS_SCL_HCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (4us / VCore clock period) - 8.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 707 = (4us / 5.6ns) - 8.

Table 496 • **Fields in SS_SCL_HCNT**

Field Name	Bit	Access	Description	Default
SS_SCL_HCNT	15:0	R/W	This register sets the SCL clock divider for the high-period in standard speed. This value must result in a high period of no less than 4us.	0x033A

7.13.1.6 TWI:TWI:SS_SCL_LCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (4.7us / VCore clock period) - 1.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 839 = (4.7us / 5.6ns) - 1.

Table 497 • **Fields in SS_SCL_LCNT**

Field Name	Bit	Access	Description	Default
SS_SCL_LCNT	15:0	R/W	This register sets the SCL clock divider for the low-period in standard speed. This value must result in a value no less than 4.7us.	0x03D3

7.13.1.7 TWI:TWI:FS_SCL_HCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (0.6us / VCore clock period) - 8.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 100 = (0.6us / 5.6ns) - 8.

Table 498 • **Fields in FS_SCL_HCNT**

Field Name	Bit	Access	Description	Default
FS_SCL_HCNT	15:0	R/W	This register sets the SCL clock divider for the high-period in fast speed. This value must result in a value no less than 0.6us.	0x0075

7.13.1.8 TWI:TWI:FS_SCL_LCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (1.3us / VCore clock period) - 1.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 232 = (1.3us / 5.6ns) - 1.

0

Table 499 • **Fields in FS_SCL_LCNT**

Field Name	Bit	Access	Description	Default
FS_SCL_LCNT	15:0	R/W	This register sets the SCL clock divider for the low-period in fast speed. This value must result in a value no less than 1.3us.	0x010E

7.13.1.9 TWI:TWI:INTR_STAT

Parent: TWI:TWI

Instances: 1

Each field in this register has a corresponding mask field in the INTR_MASK register. These fields are cleared by reading the matching interrupt clear register. The unmasked raw versions of these fields are available in the RAW_INTR_STAT register.

See RAW_INTR_STAT for a description of these fields

Table 500 • **Fields in INTR_STAT**

Field Name	Bit	Access	Description	Default
GEN_CALL	11	R/O		0x0
START_DET	10	R/O		0x0
STOP_DET	9	R/O		0x0
ACTIVITY	8	R/O		0x0
RX_DONE	7	R/O		0x0
TX_ABRT	6	R/O		0x0
RD_REQ	5	R/O		0x0
TX_EMPTY	4	R/O		0x0
TX_OVER	3	R/O		0x0
RX_FULL	2	R/O		0x0
RX_OVER	1	R/O		0x0
RX_UNDER	0	R/O		0x0

7.13.1.10 TWI:TWI:INTR_MASK

Parent: TWI:TWI

Instances: 1

These fields mask the corresponding interrupt status fields (RAW_INTR_STAT). They are active high; a value of 0 prevents the corresponding field in RAW_INTR_STAT from generating an interrupt.

Table 501 • **Fields in INTR_MASK**

Field Name	Bit	Access	Description	Default
M_GEN_CALL	11	R/W		0x1
M_START_DET	10	R/W		0x0
M_STOP_DET	9	R/W		0x0
M_ACTIVITY	8	R/W		0x0
M_RX_DONE	7	R/W		0x1
M_TX_ABRT	6	R/W		0x1
M_RD_REQ	5	R/W		0x1
M_TX_EMPTY	4	R/W		0x1
M_TX_OVER	3	R/W		0x1
M_RX_FULL	2	R/W		0x1
M_RX_OVER	1	R/W		0x1
M_RX_UNDER	0	R/W		0x1

7.13.1.11 TWI:TWI:RAW_INTR_STAT

Parent: TWI:TWI

Instances: 1

Unlike the INTR_STAT register, these fields are not masked so they always show the true status of the TWI controller.

Table 502 • **Fields in RAW_INTR_STAT**

Field Name	Bit	Access	Description	Default
R_GEN_CALL	11	R/O	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling TWI controller or when the CPU reads bit 0 of the CLR_GEN_CALL register. The TWI controller stores the received data in the Rx buffer.	0x0
R_START_DET	10	R/O	Indicates whether a START or RESTART condition has occurred on the TWI regardless of whether the TWI controller is operating in slave or master mode.	0x0
R_STOP_DET	9	R/O	Indicates whether a STOP condition has occurred on the TWI controller regardless of whether the TWI controller is operating in slave or master mode.	0x0

Table 502 • **Fields in RAW_INTR_STAT** ***(continued)***

Field Name	Bit	Access	Description	Default
R_ACTIVITY	8	R/O	This bit captures TWI activity and stays set until it is cleared. There are four ways to clear it: * Disabling the TWI controller * Reading the CLR_ACTIVITY register * Reading the CLR_INTR register * VCore system reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the TWI controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
R_RX_DONE	7	R/O	When the TWI controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0

Table 502 • **Fields in RAW_INTR_STAT** ***(continued)***

Field Name	Bit	Access	Description	Default
R_TX_ABRT	6	R/O	This bit is set to 1 when the TWI controller is acting as a master is unable to complete a command that the processor has sent. The conditions that set this field are: * No slave acknowledges the address byte. * The addressed slave receiver does not acknowledge a byte of data. * Attempting to send a master command when configured only to be a slave. * When CFG.RESTART_ENA is set to 0 (RESTART condition disabled), and the processor attempts to issue a TWI function that is impossible to perform without using RESTART conditions. * High-speed master code is acknowledged (this controller does not support high-speed). * START BYTE is acknowledged. * General Call address is not acknowledged. * When a read request interrupt occurs and the processor has previously placed data in the Tx buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. *The TWI controller loses arbitration of the bus between transfers and is then accessed as a slave-transmitter. * If a read command is issued after a General Call command has been issued. Disabling the TWI reverts it back to normal operation. * If the CPU attempts to issue read command before a RD_REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed.	0x0

Table 502 • **Fields in RAW_INTR_STAT** ***(continued)***

Field Name	Bit	Access	Description	Default
R_RD_REQ	5	R/O	This bit is set to 1 when the TWI controller acts as a slave and another TWI master is attempting to read data from this controller. The TWI controller holds the TWI bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the DATA_CMD register. This bit is set to 0 just after the required data is written to the DATA_CMD register.	0x0
R_TX_EMPTY	4	R/O	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When ENABLE is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ENABLE_STATUS.BUSY=0, this bit is set to 0.	0x0
R_TX_OVER	3	R/O	Set during transmit if the transmit buffer is filled to TX_BUFFER_DEPTH and the processor attempts to issue another TWI command by writing to the DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0

Table 502 • **Fields in RAW_INTR_STAT *(continued)***

Field Name	Bit	Access	Description	Default
R_RX_FULL	2	R/O	Set when the receive buffer reaches or goes above the RX_TL threshold in the RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (ENABLE=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the ENABLE field is programmed with a 0, regardless of the activity that continues.	0x0
R_RX_OVER	1	R/O	Set if the receive buffer is completely filled to RX_BUFFER_DEPTH and an additional byte is received from an external TWI device. The TWI controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (ENABLE=0), this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0
R_RX_UNDER	0	R/O	Set if the processor attempts to read the receive buffer when it is empty by reading from the DATA_CMD register. If the module is disabled (ENABLE=0), this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0

7.13.1.12 TWI:TWI:RX_TL

Parent: TWI:TWI

Instances: 1

Table 503 • **Fields in RX_TL**

Field Name	Bit	Access	Description	Default
RX_TL	2:0	R/W	Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in RAW_INTR_STAT register). The valid range is 0-7. A value of 0 sets the threshold for 1 entry, and a value of 7 sets the threshold for 8 entries.	0x0

7.13.1.13 TWI:TWI:TX_TL

Parent: TWI:TWI

Instances: 1

Table 504 • **Fields in TX_TL**

Field Name	Bit	Access	Description	Default
TX_TL	2:0	R/W	Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in RAW_INTR_STAT register). The valid range is 0-7. A value of 0 sets the threshold for 0 entries, and a value of 7 sets the threshold for 7 entries.	0x0

7.13.1.14 TWI:TWI:CLR_INTR

Parent: TWI:TWI

Instances: 1

Table 505 • **Fields in CLR_INTR**

Field Name	Bit	Access	Description	Default
CLR_INTR	0	R/O	Read this register to clear the combined interrupt, all individual interrupts, and the TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the TX_ABRT_SOURCE register for an exception to clearing TX_ABRT_SOURCE.	0x0

7.13.1.15 TWI:TWI:CLR_RX_UNDER

Parent: TWI:TWI

Instances: 1

Table 506 • **Fields in CLR_RX_UNDER**

Field Name	Bit	Access	Description	Default
CLR_RX_UNDER	0	R/O	Read this register to clear the R_RX_UNDER interrupt (bit 0) of the RAW_INTR_STAT register.	0x0

7.13.1.16 TWI:TWI:CLR_RX_OVER

Parent: TWI:TWI

Instances: 1

Table 507 • **Fields in CLR_RX_OVER**

Field Name	Bit	Access	Description	Default
CLR_RX_OVER	0	R/O	Read this register to clear the R_RX_OVER interrupt (bit 1) of the RAW_INTR_STAT register.	0x0

7.13.1.17 TWI:TWI:CLR_TX_OVER

Parent: TWI:TWI

Instances: 1

Table 508 • **Fields in CLR_TX_OVER**

Field Name	Bit	Access	Description	Default
CLR_TX_OVER	0	R/O	Read this register to clear the R_TX_OVER interrupt (bit 3) of the RAW_INTR_STAT register.	0x0

7.13.1.18 TWI:TWI:CLR_RD_REQ

Parent: TWI:TWI

Instances: 1

Table 509 • **Fields in CLR_RD_REQ**

Field Name	Bit	Access	Description	Default
CLR_RD_REQ	0	R/O	Read this register to clear the R_RD_REQ interrupt (bit 5) of the RAW_INTR_STAT register.	0x0

7.13.1.19 TWI:TWI:CLR_TX_ABRT

Parent: TWI:TWI

Instances: 1

Table 510 • **Fields in CLR_TX_ABRT**

Field Name	Bit	Access	Description	Default
CLR_TX_ABRT	0	R/O	Read this register to clear the R_TX_ABRT interrupt (bit 6) of the RAW_INTR_STAT register, and the TX_ABRT_SOURCE register. Refer to Bit 9 of the TX_ABRT_SOURCE register for an exception to clearing TX_ABRT_SOURCE.	0x0

7.13.1.20 TWI:TWI:CLR_RX_DONE

Parent: TWI:TWI

Instances: 1

Table 511 • **Fields in CLR_RX_DONE**

Field Name	Bit	Access	Description	Default
CLR_RX_DONE	0	R/O	Read this register to clear the R_RX_DONE interrupt (bit 7) of the RAW_INTR_STAT register.	0x0

7.13.1.21 TWI:TWI:CLR_ACTIVITY

Parent: TWI:TWI

Instances: 1

Table 512 • **Fields in CLR_ACTIVITY**

Field Name	Bit	Access	Description	Default
CLR_ACTIVITY	0	R/O	Reading this register clears the ACTIVITY interrupt if the TWI controller is not active anymore. If the TWI controller is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the R_ACTIVITY interrupt (bit 8) of the RAW_INTR_STAT register.	0x0

7.13.1.22 TWI:TWI:CLR_STOP_DET

Parent: TWI:TWI

Instances: 1

Table 513 • **Fields in CLR_STOP_DET**

Field Name	Bit	Access	Description	Default
CLR_STOP_DET	0	R/O	Read this register to clear the R_STOP_DET interrupt (bit 9) of the RAW_INTR_STAT register.	0x0

7.13.1.23 TWI:TWI:CLR_START_DET

Parent: TWI:TWI

Instances: 1

Table 514 • **Fields in CLR_START_DET**

Field Name	Bit	Access	Description	Default
CLR_START_DET	0	R/O	Read this register to clear the R_START_DET interrupt (bit 10) of the RAW_INTR_STAT register.	0x0

7.13.1.24 TWI:TWI:CLR_GEN_CALL

Parent: TWI:TWI

Instances: 1

Table 515 • **Fields in CLR_GEN_CALL**

Field Name	Bit	Access	Description	Default
CLR_GEN_CALL	0	R/O	Read this register to clear the R_GEN_CALL interrupt (bit 11) of RAW_INTR_STAT register.	0x0

7.13.1.25 TWI:TWI:CTRL

Parent: TWI:TWI

Instances: 1

Table 516 • **Fields in CTRL**

Field Name	Bit	Access	Description	Default
ENABLE	0	R/W	Controls whether the TWI controller is enabled. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When TWI controller is disabled, the following occurs: * The TX FIFO and RX FIFO get flushed. * The interrupt bits in the RAW_INTR_STAT register are cleared. * Status bits in the INTR_STAT register are still active until the TWI controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. '0': Disables TWI controller '1': Enables TWI controller	0x0

7.13.1.26 TWI:TWI:STAT

Parent: TWI:TWI

Instances: 1

Table 517 • **Fields in STAT**

Field Name	Bit	Access	Description	Default
SLV_ACTIVITY	6	R/O	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. '0': Slave FSM is in IDLE state so the Slave part of the controller is not Active '1': Slave FSM is not in IDLE state so the Slave part of the controller is Active	0x0

Table 517 • **Fields in STAT *(continued)***

Field Name	Bit	Access	Description	Default
MST_ACTIVITY	5	R/O	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. '0': Master FSM is in IDLE state so the Master part of the controller is not Active '1': Master FSM is not in IDLE state so the Master part of the controller is Active	0x0
RFF	4	R/O	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. '0': Receive FIFO is not full '1': Receive FIFO is full	0x0
RFNE	3	R/O	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. '0': Receive FIFO is empty '1': Receive FIFO is not empty	0x0
TFE	2	R/O	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. '0': Transmit FIFO is not empty '1': Transmit FIFO is empty	0x1
TFNF	1	R/O	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. '0': Transmit FIFO is full '1': Transmit FIFO is not full	0x1
BUS_ACTIVITY	0	R/O	TWI Activity Status.	0x0

7.13.1.27 TWI:TWI:TXFLR

Parent: TWI:TWI

Instances: 1

Table 518 • **Fields in TXFLR**

Field Name	Bit	Access	Description	Default
TXFLR	2:0	R/O	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.	0x0

7.13.1.28 TWI:TWI:RXFLR

Parent: TWI:TWI

Instances: 1

Table 519 • **Fields in RXFLR**

Field Name	Bit	Access	Description	Default
RXFLR	2:0	R/O	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.	0x0

7.13.1.29 TWI:TWI:TX_ABRT_SOURCE

Parent: TWI:TWI

Instances: 1

Table 520 • **Fields in TX_ABRT_SOURCE**

Field Name	Bit	Access	Description	Default
ABRT_SLVRD_INTX	15	R/W	When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 to DATA_CMD.CMD.	0x0
ABRT_SLV_ARBLOST	14	R/W	Slave lost the bus while transmitting data to a remote master. TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then the TWI controller no longer own the bus.	0x0
ABRT_SLVFLUSH_TXFIFO	13	R/W	Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.	0x0

Table 520 • **Fields in TX_ABRT_SOURCE *(continued)***

Field Name	Bit	Access	Description	Default
ARB_LOST	12	R/W	Master has lost arbitration, or if TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: the TWI controller can be both master and slave at the same time.	0x0
ABRT_MASTER_DIS	11	R/W	User tries to initiate a Master operation with the Master mode disabled.	0x0
ABRT_10B_RD_NORSTRT	10	R/W	The restart is disabled (RESTART_ENA bit (CFG[5]) = 0) and the master sends a read command in 10-bit addressing mode.	0x0
ABRT_SBYTE_NORSTRT	9	R/W	To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (CFG[5]=1), the SPECIAL bit must be cleared (TAR[11]), or the GC_OR_START bit must be cleared (TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. '1': The restart is disabled (RESTART_ENA bit (CFG[5]) = 0) and the user is trying to send a START Byte.	0x0
ABRT_SBYTE_ACKDET	7	R/W	Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).	0x0
ABRT_GCALL_READ	5	R/W	TWI controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (DATA_CMD[9] is set to 1).	0x0
ABRT_GCALL_NOACK	4	R/W	TWI controller in master mode sent a General Call and no slave on the bus acknowledged the General Call.	0x0

Table 520 • **Fields in TX_ABRT_SOURCE *(continued)***

Field Name	Bit	Access	Description	Default
ABRT_TXDATA_NOACK	3	R/W	This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).	0x0
ABRT_10ADDR2_NOACK	2	R/W	Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.	0x0
ABRT_10ADDR1_NOACK	1	R/W	Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.	0x0
ABRT_7B_ADDR_NOACK	0	R/W	Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.	0x0

7.13.1.30 TWI:TWI:SDA_SETUP

Parent: TWI:TWI

Instances: 1

This field must be set accordingly to the VCore system frequency; value = 100ns / VCore clock period.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency and fast TWI speed this field must not be set lower than (round up): 18 = 100ns / 5.6ns. For normal TWI speed this field must not be set lower than (round up): 45 = 250ns / 5.6ns.

Table 521 • **Fields in SDA_SETUP**

Field Name	Bit	Access	Description	Default
SDA_SETUP	7:0	R/W	This register controls the amount of time delay (in terms of number of VCore clock periods) introduced in the rising edge of SCL, relative to SDA changing, when the TWI controller services a read request in a slave-receiver operation. The minimum for fast mode is 100ns, for normal mode the minimum is 250ns.	0x15

7.13.1.31 TWI:TWI:ACK_GEN_CALL

Parent: TWI:TWI

Instances: 1

Table 522 • **Fields in ACK_GEN_CALL**

Field Name	Bit	Access	Description	Default
ACK_GEN_CALL	0	R/W	ACK General Call. When set to 1, the TWI controller responds with a ACK when it receives a General Call. Otherwise, the controller responds with a NACK.	0x1

7.13.1.32 TWI:TWI:ENABLE_STATUS

Parent: TWI:TWI

Instances: 1

Table 523 • **Fields in ENABLE_STATUS**

Field Name	Bit	Access	Description	Default
SLV_FIFO_FILLED_AND_FLUSHED	2	R/O	Slave FIFO Filled and Flushed. This bit indicates if a Slave-Receiver operation has been aborted with at least 1 data byte received from a TWI transfer due to the setting of ENABLE from 1 to 0. When read as 1, the TWI controller is deemed to have been actively engaged in an aborted TWI transfer (with matching address) and the data phase of the TWI transfer has been entered, even though the data byte has been responded with a NACK. When read as 0, the TWI controller is deemed to have been disabled when the TWI bus is idle.	0x0
SLV_RX_ABORTED	1	R/O	Slave-Receiver Operation Aborted. This bit indicates if a Slave-Receiver operation has been aborted due to the setting of the ENABLE register from 1 to 0. When read as 1, the TWI controller is deemed to have forced a NACK during any part of a TWI transfer, irrespective of whether the TWI address matches the slave address set in the TWI controller (SAR register). When read as 0, the TWI controller is deemed to have been disabled when the TWI bus is idle.	0x0

Table 523 • **Fields in ENABLE_STATUS *(continued)***

Field Name	Bit	Access	Description	Default
BUSY	0	R/O	When read as 1, the TWI controller is deemed to be actively involved in an TWI transfer, irrespective of whether being in an address or data phase for all master or slave modes. When read as 0, the TWI controller is deemed completely inactive.	0x0

7.14 PHY

Table 524 • **Register Groups in PHY**

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PHY_STD	0x00000000	1	IEEE Standard and Main Registers	Page 378
PHY_EXT1	0x00000000	1	Extended Page 1 Registers	Page 403
PHY_EXT2	0x00000000	1	Extended Page 2 Registers	Page 409
PHY_GP	0x00000000	1	General Purpose Registers	Page 411
PHY_EEE	0x00000000	1	Clause 45 Registers to Support Energy Efficient	Page 413

7.14.1 PHY:PHY_STD

Parent: PHY

Instances: 1

The following section lists the standard register set for the PHY.

Table 525 • **Registers in PHY_STD**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CTRL	0x00000000	1	Control (Address 0)	Page 380
PHY_STAT	0x00000001	1	Status (Address 1)	Page 381
PHY_IDF1	0x00000002	1	PHY Identifier Number 1 (Address 2)	Page 382
PHY_IDF2	0x00000003	1	PHY Identifier Number 2 (Address 3)	Page 382
PHY_AUTONEG_ADVERTISMENT	0x00000004	1	Auto-Negotiation Advertisement (Address 4)	Page 382
PHY_AUTONEG_LP_ABILITY	0x00000005	1	Auto-Negotiation Link Partner Base Page Ability (Address 5)	Page 383

Table 525 • **Registers in PHY_STD *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_AUTONEG_EXP	0x00000006	1	Auto-Negotiation Expansion (Address 6)	Page 384
PHY_AUTONEG_NEXT PAGE_TX	0x00000007	1	Auto-Negotiation Next-Page Transmit (Address 7)	Page 384
PHY_AUTONEG_LP_N EXTPAGE_RX	0x00000008	1	Auto-Negotiation Next-Page Receive (Address 8)	Page 385
PHY_CTRL_1000BT	0x00000009	1	1000BASE-T Control (Address 9)	Page 385
PHY_STAT_1000BT	0x0000000A	1	1000BASE-T Status (Address 10)	Page 386
MMD_ACCESS_CFG	0x0000000D	1	MMD Access Control Register (Address 13)	Page 387
MMD_ADDR_DATA	0x0000000E	1	MMD Address or Data Register (Address 14)	Page 387
PHY_STAT_1000BT_E XT1	0x0000000F	1	1000BASE-T Status Extension Number 1 (Address 15)	Page 388
PHY_STAT_100BTX	0x00000010	1	100BASE-TX Status (Address 16)	Page 388
PHY_STAT_1000BT_E XT2	0x00000011	1	1000BASE-T Status Extension Number 2 (Address 17)	Page 389
PHY_BYPASS_CTRL	0x00000012	1	Bypass Control (Address 18)	Page 390
PHY_ERROR_CNT1	0x00000013	1	Error Counter Number 1 (Address 19)	Page 391
PHY_ERROR_CNT2	0x00000014	1	Error Counter Number 2 (Address 20)	Page 392
PHY_ERROR_CNT3	0x00000015	1	Error Counter Number 3 (Address 21)	Page 392
PHY_CTRL_STAT_EXT	0x00000016	1	Extended Control and Status (Address 22)	Page 392
PHY_CTRL_EXT1	0x00000017	1	Extended Control Number 1 (Address 23)	Page 395
PHY_CTRL_EXT2	0x00000018	1	Extended Control Number 2 (Address 24)	Page 395
PHY_INT_MASK	0x00000019	1	Interrupt Mask (Address 25)	Page 397
PHY_INT_STAT	0x0000001A	1	Interrupt Status (Address 26)	Page 398
PHY_AUX_CTRL_STAT	0x0000001C	1	Auxiliary Control and Status (Address 28)	Page 400

Table 525 • **Registers in PHY_STD *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_MEMORY_PAGE_ACCESS	0x0000001F	1	Memory Page Access (Address 31)	Page 403

7.14.1.1 PHY:PHY_STD:PHY_CTRL

Parent: PHY:PHY_STD

Instances: 1

Table 526 • **Fields in PHY_CTRL**

Field Name	Bit	Access	Description	Default
SOFTWARE_RESET_ENA	15	R/W	Initiate software reset. This field is cleared as part of this operation. After enabling this field, you must wait at least 4 us before PHY registers can be accessed again.	0x0
LOOPBACK_ENA	14	R/W	Enable loopback mode. The loopback mechanism works at the current speed. If the link is down (see PHY_STAT.LINK_STATUS), SPEED_SEL_LSB_CFG and SPEED_SEL_MSB_CFG determine the operating speed of the loopback.	0x0
SPEED_SEL_LSB_CFG	13	R/W	Least significant bit of the speed selection, along with SPEED_SEL_MSB_CFG, this field determines the speed when auto-negotiation is disabled (See AUTONEG_ENA). 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved	0x0
AUTONEG_ENA	12	R/W	Enable auto-negotiation. When cleared, the speed and duplex-mode are determined by SPEED_SEL_LSB_CFG, SPEED_SEL_MSB_CFG, and DUPLEX_MODE_CFG.	0x1
POWER_DOWN_ENA	11	R/W	Enable power-down mode. This disables PHY operation until this bit is cleared or the PHY is reset.	0x0
ISOLATE_ENA	10	R/W	Isolate the PHY from the integrated MAC.	0x0
AUTONEG_RESTART_ENA	9	R/W	Restart an auto-negotiation cycle; the PHY clears this field when auto-negotiation is restarted.	0x0

Table 526 • **Fields in PHY_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
DUPLEX_MODE_CFG	8	R/W	Configure duplex mode when auto-negotiation is disabled (see AUTONEG_ENA). 0: Half-duplex 1: Full-duplex	0x0
COLLISION_TEST_ENA	7	R/W	Enable collision indication test-mode, when enabled the PHY indicate collision when the MAC transmits data to the PHY.	0x0
SPEED_SEL_MSB_CFG	6	R/W	See SPEED_SEL_LSB_CFG.	0x1

7.14.1.2 PHY:PHY_STD:PHY_STAT

Parent: PHY:PHY_STD

Instances: 1

Table 527 • **Fields in PHY_STAT**

Field Name	Bit	Access	Description	Default
MODE_100BT4	15	R/O	The PHY is not 100BASE-T4 capable.	0x0
MODE_100BX_FDX	14	R/O	The PHY is 100BASE-X FDX capable.	0x1
MODE_100BX_HDX	13	R/O	The PHY is 100BASE-X HDX capable.	0x1
MODE_10BT_FDX	12	R/O	The PHY is 10BASE-T FDX capable.	0x1
MODE_10BT_HDX	11	R/O	The PHY is 10BASE-T HDX capable.	0x1
MODE_100BT2_FDX	10	R/O	The PHY is not 100BASE-T2 FDX capable.	0x0
MODE_100BT2_HDX	9	R/O	The PHY is not 100BASE-T2 HDX capable.	0x0
EXT_STATUS	8	R/O	Extended status information are available; see the PHY_STAT_EXT register.	0x1
PREAMBLE_SUPPRESS	6	R/O	The PHY accepts management frames with preamble suppressed.	0x1
AUTONEG_COMPLETE	5	R/O	This field is set when auto-negotiation is completed and cleared during active auto-negotiation cycles.	0x0
REMOTE_FAULT	4	R/O	This field is set when the PHY detects a remote fault condition and cleared on register read.	0x0
AUTONEG_ABILITY	3	R/O	The PHY is capable of auto-negotiation.	0x1

Table 527 • **Fields in PHY_STAT *(continued)***

Field Name	Bit	Access	Description	Default
LINK_STAT	2	R/O	This field is cleared when the link is down. It is set when the link is up and a previous link-down indication was read from the register.	0x0
JABBER_DETECT	1	R/O	This field is set when the PHY detects a jabber condition and cleared on register read.	0x0
EXT_CAPABILITY	0	R/O	The PHY provides an extended set of capabilities.	0x1

7.14.1.3 PHY:PHY_STD:PHY_IDF1

Parent: PHY:PHY_STD

Instances: 1

Table 528 • **Fields in PHY_IDF1**

Field Name	Bit	Access	Description	Default
OUI_MS	15:0	R/O	Microsemi's organizationally unique identifier bits 3 through 18.	0x0007

7.14.1.4 PHY:PHY_STD:PHY_IDF2

Parent: PHY:PHY_STD

Instances: 1

Table 529 • **Fields in PHY_IDF2**

Field Name	Bit	Access	Description	Default
OUI_LS	15:10	R/O	Microsemi's organizationally unique identifier bits 19 through 24.	0x01
MODEL_NUMBER	9:4	R/O	The device model number.	0x2D
REVISION_NUMBER	3:0	R/O	The device revision number.	0x0

7.14.1.5 PHY:PHY_STD:PHY_AUTONEG_ADVERTISMENT

Parent: PHY:PHY_STD

Instances: 1

Table 530 • **Fields in PHY_AUTONEG_ADVERTISMENT**

Field Name	Bit	Access	Description	Default
NEXT_PAGE_ENA	15	R/W	Advertises desire to engage in next-page exchange. When this field is set, next-page control is returned to the user for additional next-pages following the 1000BASE-T next-page exchange.	0x0
REMOTE_FAULT_CFG	13	R/W	Transmit Remote Fault.	0x0
ASYM_PAUSE_CFG	11	R/W	Advertise asymmetric pause capability.	0x0
SYM_PAUSE_CFG	10	R/W	Advertise symmetric pause capability.	0x0
ADV_100BT4_CFG	9	R/W	Advertise 100BASE-T4 capability.	0x0
ADV_100BX_FDX_CFG	8	R/W	Advertise 100BASE-X FDX capability.	0x1
ADV_100BX_HDX_CFG	7	R/W	Advertise 100BASE-X HDX capability.	0x1
ADV_10BT_FDX_CFG	6	R/W	Advertise 10BASE-T FDX capability.	0x1
ADV_10BT_HDX_CFG	5	R/W	Advertise 10BASE-T HDX capability.	0x1
SELECTOR_FIELD_CFG	4:0	R/W	Select types of message send by auto-negotiation.	0x01

7.14.1.6 PHY:PHY_STD:PHY_AUTONEG_LP_ABILITY

Parent: PHY:PHY_STD

Instances: 1

Table 531 • **Fields in PHY_AUTONEG_LP_ABILITY**

Field Name	Bit	Access	Description	Default
LP_NEXT_PAGE	15	R/O	Link partner advertises desire to engage in next-page exchange.	0x0
LP_ACKNOWLEDGE	14	R/O	Link partner advertises that link code word was successfully received.	0x0
LP_REMOTE_FAULT	13	R/O	Link partner advertises remote fault.	0x0
LP_ASYM_PAUSE	11	R/O	Link partner advertises asymmetric pause capability.	0x0
LP_SYM_PAUSE	10	R/O	Link partner advertises symmetric pause capability.	0x0
LP_100BT4	9	R/O	Link partner advertises 100BASE-T4 capability.	0x0

Table 531 • **Fields in PHY_AUTONEG_LP_ABILITY *(continued)***

Field Name	Bit	Access	Description	Default
LP_100BX_FDX	8	R/O	Link partner advertises 100BASE-X FDX capability.	0x0
LP_100BX_HDX	7	R/O	Link partner advertises 100BASE-X HDX capability.	0x0
LP_10BT_FDX	6	R/O	Link partner advertises 10BASE-T FDX capability.	0x0
LP_10BT_HDX	5	R/O	Link partner advertises 10BASE-T HDX capability.	0x0
LP_SELECTOR_FIELD	4:0	R/O	Link partner advertises select type of message send by auto-negotiation.	0x00

7.14.1.7 PHY:PHY_STD:PHY_AUTONEG_EXP

Parent: PHY:PHY_STD

Instances: 1

Table 532 • **Fields in PHY_AUTONEG_EXP**

Field Name	Bit	Access	Description	Default
PARALLEL_DET_FAULT	4	R/O	This field is set when the PHY detects a Receive Link Integrity Test Failure condition and cleared on register read.	0x0
LP_NEXT_PAGE_ABLE	3	R/O	Set if link partner is next-page capable.	0x0
NEXT_PAGE_ABLE	2	R/O	The PHY is next-page capable.	0x1
NEXT_PAGE_RECEIVED	1	R/O	This field is set when the PHY receives a valid next-page and cleared on register read.	0x0
LP_AUTONEG_ABLE	0	R/O	Set if link partner is auto-negotiation capable.	0x0

7.14.1.8 PHY:PHY_STD:PHY_AUTONEG_NEXTPAGE_TX

Parent: PHY:PHY_STD

Instances: 1

Table 533 • **Fields in PHY_AUTONEG_NEXTPAGE_TX**

Field Name	Bit	Access	Description	Default
NEXT_PAGE_CFG	15	R/W	Set to indicate that more pages will follow; clear if current page is the last.	0x0
MESSAGE_PAGE_CFG	13	R/W	Set to indicate that this is a message page; clear if the current page consists of unformatted code.	0x1

Table 533 • **Fields in PHY_AUTONEG_NEXTPAGE_TX *(continued)***

Field Name	Bit	Access	Description	Default
ACKNOWLEDGE2_CFG	12	R/W	Set to indicate ability to comply with the request of the last received page.	0x0
TOGGLE	11	R/O	Alternates between 0 and 1 for each transmitted page.	0x0
MESSAGE_FIELD_CFG	10:0	R/W	Contains page information - either message or unformatted code. MESSAGE_PAGE_CFG must indicate if this page contains either a message or unformatted code.	0x001

7.14.1.9 PHY:PHY_STD:PHY_AUTONEG_LP_NEXTPAGE_RX

Parent: PHY:PHY_STD

Instances: 1

Table 534 • **Fields in PHY_AUTONEG_LP_NEXTPAGE_RX**

Field Name	Bit	Access	Description	Default
LP_NEXT_PAGE_RX	15	R/O	Set by link partner to indicate that more pages follow. When cleared, this is the last of the next-pages.	0x0
LP_ACKNOWLEDGE_RX	14	R/O	Set by link partner to acknowledge the reception of last message.	0x0
LP_MESSAGE_PAGE	13	R/O	Set by Link partner if this page contains a message. When cleared this page contains unformatted code.	0x0
LP_ACKNOWLEDGE2	12	R/O	Set by link partner to indicate that it is able to act on transmitted information.	0x0
LP_TOGGLE	11	R/O	Will alternate between 0 and 1 for each received page. Used to check for errors.	0x0
LP_MESSAGE_FIELD	10:0	R/O	Contains page information, MESSAGE_PAGE indicates if this page contains either a message or unformatted code.	0x000

7.14.1.10 PHY:PHY_STD:PHY_CTRL_1000BT

Parent: PHY:PHY_STD

Instances: 1

Table 535 • **Fields in PHY_CTRL_1000BT**

Field Name	Bit	Access	Description	Default
TX_TEST_MODE_CFG	15:13	R/W	Configure 1000BASE-T test modes; this field is only valid in 1000BASE-T mode. Other encodings are reserved and must not be selected. 0: Normal operation 1: Transmit waveform test. 2: Transmit jitter test in master mode. 3: Transmit jitter test in slave mode. 4: Transmit distortion test.	0x0
MS_MANUAL_CFG_ENA	12	R/W	Enable manual configuration of master/slave value.	0x0
MS_MANUAL_CFG	11	R/W	Configure if the PHY should configure itself as either master or slave during master/slave negotiations. This field is only valid when MS_MANUAL_CFG_ENA is set. 0: Configure as slave. 1: Configure as master.	0x0
PORT_TYPE_CFG	10	R/W	Set to indicate multi-port device, clear to indicate single-port device.	0x1
ADV_1000BT_FDX_CFG	9	R/W	Set to advertise 1000BASE-T FDX capability.	0x1
ADV_1000BT_HDX_CFG	8	R/W	Set to advertise 1000BASE-T HDX capability.	0x1

7.14.1.11 PHY:PHY_STD:PHY_STAT_1000BT

Parent: PHY:PHY_STD

Instances: 1

Table 536 • **Fields in PHY_STAT_1000BT**

Field Name	Bit	Access	Description	Default
MS_CFG_FAULT	15	R/O	This field is set when the PHY detects a master/slave configuration fault condition and cleared on register read.	0x0
MS_CFG_RESOLUTION	14	R/O	This field indicates the result of a master/slave Negotiation. 0: Local PHY is resolved to slave. 1: Local PHY is resolved to master.	0x1

Table 536 • **Fields in PHY_STAT_1000BT *(continued)***

Field Name	Bit	Access	Description	Default
LOCAL_RECEIVER_STAT	13	R/O	The status of the local receiver (loc_rcvr_status as defined in IEEE Std. 802.3). 0: Local receiver status is NOT_OK. 1: Local receiver status is OK.	0x0
REMOTE_RECEIVER_STAT	12	R/O	The status of the remote receiver (rem_rcvr_status as defined in IEEE Std. 802.3). 0: Remote receiver status is NOT_OK. 1: Remote receiver status is OK.	0x0
LP_1000BT_FDX	11	R/O	Set if link partner advertises 1000BASE-T FDX capability.	0x0
LP_1000BT_HDX	10	R/O	Set if link partner advertises 1000BASE-T HDX capability.	0x0
IDLE_ERR_CNT	7:0	R/O	Counts each occurrence of rxerror_status = Error (rx_error_status as defined in IEEE Std. 802.3. This field is cleared on read and saturates at all-ones.	0x00

7.14.1.12 PHY:PHY_STD:MMD_ACCESS_CFG

Parent: PHY:PHY_STD

Instances: 1

The bits in this register of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 537 • **Fields in MMD_ACCESS_CFG**

Field Name	Bit	Access	Description	Default
MMD_FUNCTION	15:14	R/W	Function. 0: Address 1: Data, no post increment 2: Data, post increment for read and write 3: Data, post increment for write only	0x0
MMD_DVAD	4:0	R/W	Device address as defined in IEEE 802.3az, table 45-1.	0x00

7.14.1.13 PHY:PHY_STD:MMD_ADDR_DATA

Parent: PHY:PHY_STD

Instances: 1

The bits in this register of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 538 • **Fields in MMD_ADDR_DATA**

Field Name	Bit	Access	Description	Default
MMD_ADDR_DATA	15:0	R/W	If MMD_ACCESS_CFG.MMD_FUNCTION is 0, MMD_ADDR_DATA specifies the address of register of the device that is specified by MMD_ACCESS_CFG.MMD_DVAD. Otherwise, MMD_ADDR_DATA specifies the data to be written to or read from the register.	0x0000

7.14.1.14 PHY:PHY_STD:PHY_STAT_1000BT_EXT1

Parent: PHY:PHY_STD

Instances: 1

Table 539 • **Fields in PHY_STAT_1000BT_EXT1**

Field Name	Bit	Access	Description	Default
MODE_1000BX_FDX	15	R/O	The PHY is not 1000BASE-X FDX capable.	0x0
MODE_1000BX_HDX	14	R/O	The PHY is not 1000BASE-X HDX capable.	0x0
MODE_1000BT_FDX	13	R/O	The PHY is 1000BASE-T FDX capable.	0x1
MODE_1000BT_HDX	12	R/O	The PHY is 1000BASE-T HDX capable.	0x1

7.14.1.15 PHY:PHY_STD:PHY_STAT_100BTX

Parent: PHY:PHY_STD

Instances: 1

These fields are only valid in 100BASE-T mode.

Table 540 • **Fields in PHY_STAT_100BTX**

Field Name	Bit	Access	Description	Default
DESCRAM_LOCKED	15	R/O	This field is set when the 100BASE-TX descrambler is in lock and cleared when it is out of lock.	0x0
DESCRAM_ERR	14	R/O	This field is set when the PHY detects a descrambler error condition and cleared on register read.	0x0

Table 540 • **Fields in PHY_STAT_100BTX *(continued)***

Field Name	Bit	Access	Description	Default
LINK_DISCONNECT	13	R/O	This field is set when the PHY detects a 100BASE-TX link disconnect condition and cleared on register read.	0x0
LINK_STAT_100	12	R/O	This field is set when the 100BASE-TX link status is active and cleared when inactive.	0x0
RECEIVE_ERR	11	R/O	This field is set when the PHY detects a receive error condition and cleared on register read.	0x0
TRANSMIT_ERR	10	R/O	This field is set when the PHY detects a transmit error condition and cleared on register read.	0x0
SSD_ERR	9	R/O	This field is set when the PHY detects a Start-of-Stream Delimiter Error condition and cleared on register read.	0x0
ESD_ERR	8	R/O	This field is set when the PHY detects an End-of-Stream Delimiter Error condition and cleared on register read.	0x0

7.14.1.16 PHY:PHY_STD:PHY_STAT_1000BT_EXT2

Parent: PHY:PHY_STD

Instances: 1

These fields are only valid in 1000BASE-T mode.

Table 541 • **Fields in PHY_STAT_1000BT_EXT2**

Field Name	Bit	Access	Description	Default
DESCRAM_LOCKED_1000	15	R/O	This field is set when the 1000BASE-T descrambler is in lock and cleared when it is out of lock.	0x0
DESCRAM_ERR_1000	14	R/O	This field is set when the PHY detects a Descrambler Error condition and cleared on register read.	0x0
LINK_DISCONNECT_1000	13	R/O	This field is set when the PHY detects a 1000BASE-T link disconnect condition and cleared on register read.	0x0
LINK_STAT_1000	12	R/O	This field is set when the 1000BASE-T link status is active and cleared when inactive.	0x0

Table 541 • **Fields in PHY_STAT_1000BT_EXT2 *(continued)***

Field Name	Bit	Access	Description	Default
RECEIVE_ERR_1000	11	R/O	This field is set when the PHY detects a Receive Error condition and cleared on register read.	0x0
TRANSMIT_ERR_1000	10	R/O	This field is set when the PHY detects a Transmit Error condition and cleared on register read.	0x0
SSD_ERR_1000	9	R/O	This field is set when the PHY detects a Start-of-Stream Delimiter Error condition and cleared on register read.	0x0
ESD_ERR_1000	8	R/O	This field is set when the PHY detects an End-of-Stream Delimiter Error condition and cleared on register read.	0x0
CARRIER_EXT_ERR_1000	7	R/O	This field is set when the PHY detects a 1000BASE-T Carrier Extension Error condition and cleared on register read.	0x0
BCM5400_ERR_1000	6	R/O	This field is set when the PHY detects a non-compliant BCM5400 condition. This field is only valid when the 1000BASE-T descrambler is in locked state (see DESCRAM_LOCKED_1000).	0x0
MDI_CROSSOVER_ERR	5	R/O	This field is set when the PHY detects an MDI crossover error condition.	0x0

7.14.1.17 PHY:PHY_STD:PHY_BYPASS_CTRL

Parent: PHY:PHY_STD

Instances: 1

Table 542 • **Fields in PHY_BYPASS_CTRL**

Field Name	Bit	Access	Description	Default
TX_DIS	15	R/W	Disable the PHY transmitter. When set, the analog blocks are powered down and zeros are send to the DAC.	0x0
ENC_DEC_4B5B	14	R/W	If set, bypass the 4B5B encoder/decoder.	0x0
SCRAMBLER	13	R/W	If set, bypass the scrambler.	0x0
DESCRAMBLER	12	R/W	If set, bypass the descrambler.	0x0
PCS_RX	11	R/W	If set, bypass the PCS receiver.	0x0
PCS_TX	10	R/W	If set, bypass the PCS transmit.	0x0
LFI_TIMER	9	R/W	If set, bypass the link fail inhibit (LFI) timer.	0x0

Table 542 • **Fields in PHY_BYPASS_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
FORCED_SPEED_AUTO_MDIX_DIS	7	R/W	Bit for disabling HP AutoMDIX in forced 10/100 speeds, even though auto-negotiation is disabled. 0: The HP Auto-MDIX function is enabled. 1: Default value. The HP Auto-MDIX function is disabled. Use the default value when in auto-negotiation mode.	0x1
PAIR_SWAP_DIS	5	R/W	Disable automatic pair swap correction. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
POL_INV_DIS	4	R/W	Disable automatic polarity inversion correction. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
PARALLEL_DET_DIS	3	R/W	When cleared, the PHY ignores its advertised abilities when performing parallel detect. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x1
PULSE_SHAPING_DIS	2	R/W	If set, disable the pulse shaping filter.	0x0
AUTO_NP_EXCHANGE_DIS	1	R/W	Disable automatic exchange of 1000BASE-T next pages. If this feature is disabled, you have the responsibility of sending next pages, determining capabilities, and configuration of the PHY after successful exchange of pages. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

7.14.1.18 PHY:PHY_STD:PHY_ERROR_CNT1

Parent: PHY:PHY_STD

Instances: 1

Table 543 • **Fields in PHY_ERROR_CNT1**

Field Name	Bit	Access	Description	Default
RX_ERR_CNT	7:0	R/O	Counter containing the number of packets received with errors for 100/1000BASE-TX. The counter saturates at 255 and it is cleared when read.	0x00

7.14.1.19 PHY:PHY_STD:PHY_ERROR_CNT2

Parent: PHY:PHY_STD

Instances: 1

Table 544 • **Fields in PHY_ERROR_CNT2**

Field Name	Bit	Access	Description	Default
FALSE_CARRIER_CNT	7:0	R/O	Counter containing the number of false carrier incidents for 100/1000BASE-TX. The counter saturates at 255 and it is cleared when read.	0x00

7.14.1.20 PHY:PHY_STD:PHY_ERROR_CNT3

Parent: PHY:PHY_STD

Instances: 1

Table 545 • **Fields in PHY_ERROR_CNT3**

Field Name	Bit	Access	Description	Default
LINK_DIS_CNT	7:0	R/O	Counter containing the number of copper media link disconnects. The counter saturates at 255 and it is cleared when read.	0x00

7.14.1.21 PHY:PHY_STD:PHY_CTRL_STAT_EXT

Parent: PHY:PHY_STD

Instances: 1

Table 546 • **Fields in PHY_CTRL_STAT_EXT**

Field Name	Bit	Access	Description	Default
LINK_10BT_FORCE_ENA	15	R/W	When this field is set, the PHY link integrity state machine is bypassed, and the PHY is forced into link pass status. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x0
JABBER_DETECT_DIS	14	R/W	Disable jabber detect function. When this is disabled, the PHY allows transmission requests to be arbitrarily long without shutting down the transmitter. When cleared, the PHY shuts down the transmitter after the specified time limit specified by IEEE. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x0
ECHO_10BT_DIS	13	R/W	When this field is set, the state of the TX_EN pin does not echo onto the CRS pin, which effectively disables CRS from being asserted in half-duplex operation. When cleared, the TX_EN pin is echoed onto the CRS pin. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x1
SQE_10BT_DIS	12	R/W	Disable SQE (Signal Quality Error) pulses on the MAC interface. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x1

Table 546 • **Fields in PHY_CTRL_STAT_EXT** ***(continued)***

Field Name	Bit	Access	Description	Default
SQUELCH_10BT_CFG	11:10	R/W	Configure squelch control (this only applies in the 10BASE-T mode). This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA. 0: The PHY uses the squelch threshold levels prescribed by the IEEE 10BASE-T specification. 1: In this mode, the squelch levels are decreased, which may improve the bit error rate performance on long loops 2: In this mode, the squelch levels are increased, which may improve the bit error rate in high-noise environments 3: Reserved.	0x0
STICKY_RESET_ENA	9	R/W	When set, all fields described as sticky retain their value during software reset. When cleared, all fields marked as sticky are reset to their default values during software reset. This does not affect hardware resets. This is a super-sticky field, which means that it always retain its value during software reset.	0x1
EOF_ERR	8	R/O	When set, this field indicates that a defective EOF (End Of Frame) sequence was received since the last time this field was read. This field is cleared on read.	0x0
LINK_10BT_DISCONNECT	7	R/O	When set, this field indicates that the carrier integrity monitor has broken the 10BASE-T connection since the last read of this bit. This field is cleared on read.	0x0
LINK_10BT_STAT	6	R/O	This field is set when a 10BASE-T link is active. Cleared when inactive.	0x0
BROADCAST_WRITE_ENA	0	R/W	Enable any MII write operation (regardless of destination PHY) to be interpreted as a write to this PHY. This only applies to writes; read-operations are still interpreted with correct address. This is particularly useful when similar settings should be propagated to multiple PHYs. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

7.14.1.22 PHY:PHY_STD:PHY_CTRL_EXT1

Parent: PHY:PHY_STD

Instances: 1

Table 547 • **Fields in PHY_CTRL_EXT1**

Field Name	Bit	Access	Description	Default
RESERVED	15:4	R/W	Must be set to its default.	0x000
FAR_END_LOOPBACK_ENA	3	R/W	Enable far end loopback in this PHY. In this mode all incoming traffic on the media interface is retransmitted back to the link partner. In addition, the incoming data also appears on the internal Rx interface to the MAC. Any data send to the PHY from the internal MAC is ignored when this mode is active.	0x0

7.14.1.23 PHY:PHY_STD:PHY_CTRL_EXT2

Parent: PHY:PHY_STD

Instances: 1

Table 548 • **Fields in PHY_CTRL_EXT2**

Field Name	Bit	Access	Description	Default
EDGE_RATE_CFG	15:13	R/W	Control the transmit DAC slew rate in 100BASE-TX mode only. The difference between each setting is approximately 200ps to 300ps, with the +3 setting resulting in the slowest edge rate, and the -4 setting resulting in the fastest edge rate. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 011: +5 Edge rate (slowest). 010: +4 Edge rate. 001: +3 Edge rate. 000: +2 Edge rate. 111: +1 Edge rate. 110: Nominal edge rate. 101: -1 Edge rate. 100: -2 Edge rate (fastest).	0x1

Table 548 • **Fields in PHY_CTRL_EXT2** ***(continued)***

Field Name	Bit	Access	Description	Default
PICMG_REDUCED_POWER_ENA	12	R/W	Enable PICMC reduce power mode: In this mode, portions of the DSP processor are turned off, which reduces the PHY's operating power. The DSP performance characteristics in this mode are configured to support the channel characteristics specified in the PICMC 2.16 and PICMC 3.0 specifications. The application of this mode is in environments that have a high signal to noise ratio on the media. For example, Ethernet over backplane, or where cable length is short (less than 10m). When this field is cleared, the PHY operates in normal DSP mode. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
RESERVED	8:6	R/W	Must be set to its default.	0x1
JUMBO_PKT_ENA	5:4	R/W	Controls the symbol buffering for the receive synchronization FIFO used in 1000BASE-T mode. Other encodings are reserved and must not be selected. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. Note: When set, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the field encoding description results in a higher jumbo packet length. 00: Normal IEEE 1518-byte packet length. 01: 9-kilobyte jumbo packet length (12 kilobytes with 60 ppm or better reference clock). 10: 12-kilobyte jumbo packet length (16 kilobytes with 70 ppm or better reference clock). 11: Reserved.	0x0
RESERVED	3:1	R/W	Must be set to its default.	0x0
CON_LOOPBACK_1000BT_ENA	0	R/W	Set PHY into 1000BASE-T connector loopback mode. When enabled, the PHY only works with a connector loopback.	0x0

7.14.1.24 PHY:PHY_STD:PHY_INT_MASK

Parent: PHY:PHY_STD

Instances: 1

Table 549 • **Fields in PHY_INT_MASK**

Field Name	Bit	Access	Description	Default
PHY_INT_ENA	15	R/W	Enable global PHY interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SPEED_STATE_CHANGE_INT_ENA	14	R/W	Set to unmask speed change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LINK_STATE_CHANGE_INT_ENA	13	R/W	Set to unmask link state/energy detected change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FDX_STATE_CHANGE_INT_ENA	12	R/W	Set to unmask FDX change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
AUTONEG_ERR_INT_ENA	11	R/W	Set to unmask auto-negotiation error interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
AUTONEG_DONE_INT_ENA	10	R/W	Set to unmask auto-negotiation-done/interlock done interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
INLINE_POW_DET_INT_ENA	9	R/W	Set to unmask In-line Powered Device Detected interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SYMBOL_ERR_INT_ENA	8	R/W	Set to unmask Symbol Error interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FAST_LINK_FAIL_INT_ENA	7	R/W	Set to unmask fast link failure interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

Table 549 • **Fields in PHY_INT_MASK *(continued)***

Field Name	Bit	Access	Description	Default
TX_FIFO_INT_ENA	6	R/W	Set to unmask TX FIFO interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
RX_FIFO_INT_ENA	5	R/W	Set to unmask RX FIFO interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FALSE_CARRIER_INT_ENA	3	R/W	Set to unmask False Carrier interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LINK_SPEED_DOWNSHIFT_INT_ENA	2	R/W	Set to unmask link speed downshift interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
MASTER_SLAVE_INT_ENA	1	R/W	Set to unmask master/slave interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
RX_ER_INT_ENA	0	R/W	Set to unmask RX_ER interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

7.14.1.25 PHY:PHY_STD:PHY_INT_STAT

Parent: PHY:PHY_STD

Instances: 1

Table 550 • **Fields in PHY_INT_STAT**

Field Name	Bit	Access	Description	Default
PHY_INT_PEND	15	R/O	Set when an unacknowledged 'global' PHY interrupt is pending, the cause of the interrupt can be determined by examining the other fields of this register. This field is set no matter the state of PHY_INT_MASK.PHY_INT_ENA. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

Table 550 • **Fields in PHY_INT_STAT** ***(continued)***

Field Name	Bit	Access	Description	Default
SPEED_STATE_CHANGE_INT_PEND	14	R/O	Set when a speed interrupt is pending, this is activated when the operating speed of the PHY changes (requires that auto-negotiation is enabled; see PHY_CTRL.AUTONEG_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
LINK_STATE_CHANGE_INT_PEND	13	R/O	Set when a Link State/Energy Detected interrupt is pending. This interrupt occurs when the link status of the PHY changes, or if ActiPHY mode is enabled and energy is detected on the media (see PHY_AUX_CTRL_STAT.ACTIPHY_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FDX_STATE_CHANGE_INT_PEND	12	R/O	Set when an FDX interrupt is pending. FDX interrupt is caused when the FDX/HDX state of the PHY changes (requires that auto-negotiation is enabled; see PHY_CTRL.AUTONEG_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
AUTONEG_ERR_INT_PEND	11	R/O	Set when an auto-negotiation Error interrupt is pending, this is caused when an error is detected by the auto-negotiation state machine. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
AUTONEG_DONE_INT_PEND	10	R/O	Set when an auto-negotiation-Done/Interlock Done interrupt is pending, this is caused when the Auto-negotiation finishes a negotiation process. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
INLINE_POW_DET_INT_PEND	9	R/O	Set when an In-line Powered Device Detected interrupt is pending. This interrupt is caused when a device requiring in-line power is detected (requires that detection is enabled; see PHY_CTRL_EXT4.INLINE_DETECT_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

Table 550 • **Fields in PHY_INT_STAT *(continued)***

Field Name	Bit	Access	Description	Default
SYMBOL_ERR_INT_PEND	8	R/O	Set when a Symbol Error interrupt is pending, this is caused by detection of a symbol error by the descrambler. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FAST_LINK_FAIL_INT_PEND	7	R/O	Set when a fast link failure interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
TX_FIFO_INT_PEND	6	R/O	Set when a TX FIFO interrupt is pending. TX FIFO interrupt is generated by TX FIFO underflow or overflow. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
RX_FIFO_INT_PEND	5	R/O	Set when a RX FIFO interrupt is pending. This interrupt is caused by RX FIFO underflow or overflow. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FALSE_CARRIER_INT_PEND	3	R/O	Set when a False Carrier interrupt is pending. False Carrier interrupt is generated when the PHY detects a false carrier. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
LINK_SPEED_DOWNSHIFT_INT_PEND	2	R/O	Set when a link speed downshift interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
MASTER_SLAVE_ERR_INT_PEND	1	R/O	Set when a master/slave interrupt is pending. This interrupt is set when a master/slave resolution error us detected. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
RX_ER_INT_PEND	0	R/O	Set when a RX_ER interrupt is pending. This interrupt is set when an RX_ER condition occurs. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

7.14.1.26 PHY:PHY_STD:PHY_AUX_CTRL_STAT

Parent: PHY:PHY_STD

Instances: 1

Copied fields have the same default values as their source fields.

Table 551 • **Fields in PHY_AUX_CTRL_STAT**

Field Name	Bit	Access	Description	Default
AUTONEG_COMPLETE_AUX	15	R/O	A read-only copy of PHY_STAT.AUTONEG_COMPLETE. Repeated here for convenience. See note for this register.	0x0
AUTONEG_STAT	14	R/O	When set the auto-negotiation function has been disabled (in PHY_CTRL.AUTONEG_ENA.)	0x0
NO_MDI_X_IND	13	R/O	When this field is set, the auto-negotiation state machine has determined that crossover does not exist in the signal path. This field is only valid after 'descrambler lock' has been achieved (see PHY_STAT_1000BT_EXT.DESCRAM_LOCKED) and 'automatic pair swap correction' is enabled (see PHY_BYPASS_CTRL.PAIR_SWAP_DISABLE).	0x0
CD_PAIR_SWAP	12	R/O	When this field is set, the PHY has determined that the subchannel cable pairs C and D were swapped between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE).	0x0
A_POL_INVERSION	11	R/O	When set, this field indicates that the polarity of pair A was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE). 0: Polarity is swapped on pair A. 1: Polarity is not swapped on pair A.	0x0
B_POL_INVERSION	10	R/O	When set, this field indicates that the polarity of pair B was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE). 0: Polarity is swapped on pair B. 1: Polarity is not swapped on pair B.	0x0

Table 551 • **Fields in PHY_AUX_CTRL_STAT** ***(continued)***

Field Name	Bit	Access	Description	Default
C_POL_INVERSION	9	R/O	When set, this field indicates that the polarity of pair C was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and in 1000BASE-T mode. 0: Polarity is swapped on pair C. 1: Polarity is not swapped on pair C.	0x0
D_POL_INVERSION	8	R/O	When set, this field indicates that the polarity of pair D was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and in 1000BASE-T mode. 0: Polarity is swapped on pair D. 1: Polarity is not swapped on pair D.	0x0
ACTIPHY_LINK_TIMER_MSB_CFG	7	R/W	Most significant bit of the link status time-out timer. Together with ACTIPHY_LINK_TIMER_LSB_CFG, this field determines the duration from losing the link to the ActiPHY enters low power state. 0: 1 seconds. 1: 2 seconds. 2: 3 seconds. 3: 4 seconds.	0x0
ACTIPHY_ENA	6	R/W	Enable ActiPHY power management mode. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FDX_STAT	5	R/O	This field indicates the actual FDX/HDX operating mode of the PHY. 0: Half-duplex. 1: Full-duplex.	0x0
SPEED_STAT	4:3	R/O	This field indicates the actual operating speed of the PHY. 0: Speed is 10BASE-T. 1: Speed is 100BASE-TX. 2: Speed is 1000-BASE-T. 3: Reserved.	0x0

Table 551 • **Fields in PHY_AUX_CTRL_STAT *(continued)***

Field Name	Bit	Access	Description	Default
ACTIPHY_LINK_TIMER_LSB_CFG	2	R/W	See ACTIPHY_LINK_TIMER_MSB_CFG.	0x1

7.14.1.27 PHY:PHY_STD:PHY_MEMORY_PAGE_ACCESS

Parent: PHY:PHY_STD

Instances: 1

Table 552 • **Fields in PHY_MEMORY_PAGE_ACCESS**

Field Name	Bit	Access	Description	Default
PAGE_ACCESS_CFG	4:0	R/W	This bit controls the mapping of PHY registers 0x10 through 0x1E. When changing pages, all registers in the range 0x10 through 0x1E are replaced - even if the new memory-page does not define all addresses in the range 0x10 through 0x1E. 0: Register Page 0 is mapped (standard set). 1: Register Page 1 is mapped (extended set 1). 2: Register Page 2 is mapped (extended set 2). 16: Register Page 16 is mapped (general purpose).	0x00

7.14.2 PHY:PHY_EXT1

Parent: PHY

Instances: 1

Set register 0x1F to 0x0001 to make the extended set of registers visible in the address range 0x10 through 0x1E. Set register 0x1F to 0x0000 to revert back to the standard register set.

Table 553 • **Registers in PHY_EXT1**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CRC_GOOD_CNT	0x00000012	1	CRC Good Counter (Address 18E1)	Page 404
PHY_EXT_MODE_CTRL	0x00000013	1	Extended Mode Control (Address 19E1)	Page 404
PHY_CTRL_EXT3	0x00000014	1	Extended Control Number 3 (Address 20E1)	Page 404

Table 553 • **Registers in PHY_EXT1 *(continued)***

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CTRL_EXT4	0x00000017	1	Extended Control Number 4 (Address 23E1)	Page 406
PHY_1000BT_EPG1	0x0000001D	1	1000BASE-T Ethernet Packet Generator Number 1 (Address 29E1)	Page 407
PHY_1000BT_EPG2	0x0000001E	1	1000BASE-T Ethernet Packet Generator Number 2 (Address 30E1)	Page 409

7.14.2.1 PHY:PHY_EXT1:PHY_CRC_GOOD_CNT

Parent: PHY:PHY_EXT1

Instances: 1

Table 554 • **Fields in PHY_CRC_GOOD_CNT**

Field Name	Bit	Access	Description	Default
PACKET_SINCE_LAST_READ	15	R/O	Packet received since last read. This is a self-clearing bit.	0x0
CRC_GOOD_PKT_CNT	13:0	R/O	Counter containing the number of packets with valid CRCs; this counter does not saturate and rolls over. This is a self-clearing field.	0x0000

7.14.2.2 PHY:PHY_EXT1:PHY_EXT_MODE_CTRL

Parent: PHY:PHY_EXT1

Instances: 1

Table 555 • **Fields in PHY_EXT_MODE_CTRL**

Field Name	Bit	Access	Description	Default
FORCE_MDI_CROSSOVER_ENA	3:2	R/W	Force MDI crossover. 00: Normal HP Auto-MDIX operation. 01: Reserved. 10: Copper media forced to MDI. 11: Copper media forced MDI-X.	0x0

7.14.2.3 PHY:PHY_EXT1:PHY_CTRL_EXT3

Parent: PHY:PHY_EXT1

Instances: 1

Table 556 • **Fields in PHY_CTRL_EXT3**

Field Name	Bit	Access	Description	Default
RESERVED	15	R/W	Must be set to its default.	0x1
ACTIPHY_SLEEP_TIMER	14:13	R/W	This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0x1
ACTIPHY_WAKEUP_TIMER	12:11	R/W	This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: 160 ms. 01: 400 ms. 10: 800 ms. 11: 2 seconds.	0x0
NO_PREAMBLE_10BT_ENA	5	R/W	If set, 10BASE-T asserts RX_DV indication when data is presented to the receiver even without a preamble preceding it.This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SPEED_DOWNSHIFT_ENA	4	R/W	Enables automatic downshift the auto-negotiation advertisement to the next lower available speed after the number of failed 1000BASE-T auto-negotiation attempts specified in SPEED_DOWNSHIFT_CFG. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

Table 556 • **Fields in PHY_CTRL_EXT3 *(continued)***

Field Name	Bit	Access	Description	Default
SPEED_DOWNSHIFT_CFG	3:2	R/W	Configures the number of unsuccessful 1000BASE-T auto-negotiation attempts that are required before the auto-negotiation advertisement is downshifted to the next lower available speed. This field applies only if automatic downshift of speed is enabled (see SPEED_DOWNSHIFT_ENA). This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: Downshift after 2 failed attempts. 01: Downshift after 3 failed attempts. 10: Downshift after 4 failed attempts. 11: Downshift after 5 failed attempts.	0x1
SPEED_DOWNSHIFT_STAT	1	R/O	This status field indicates that a downshift is required in order for link to be established. If automatic downshifting is enabled (see SPEED_DOWNSHIFT_ENA), the current link speed is a result of a downshift.	0x0

7.14.2.4 PHY:PHY_EXT1:PHY_CTRL_EXT4

Parent: PHY:PHY_EXT1

Instances: 1

The reset value of the address fields (PHY_ADDR) corresponds to the PHY in which it resides.

Table 557 • **Fields in PHY_CTRL_EXT4**

Field Name	Bit	Access	Description	Default
PHY_ADDR	15:11	R/O	This field contains the PHY address of the current PHY port.	0x00
INLINE_POW_DET_ENA	10	R/W	Enables detection of inline powered device as part of the auto-negotiation process. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

Table 557 • **Fields in PHY_CTRL_EXT4 *(continued)***

Field Name	Bit	Access	Description	Default
INLINE_POW_DET_STAT	9:8	R/O	This field shows the status if a device is connected to the PHY that requires inline power. This field is only valid if inline powered device detection is enabled (see INLINE_POW_DET_ENA). 00: Searching for devices. 01: Device found that requires inline power. 10: Device found that does not require inline power. 11: Reserved.	0x0
CRC_1000BT_CNT	7:0	R/O	This field indicates how many packets are received that contain a CRC error. This field is cleared on read and saturates at all ones.	0x00

7.14.2.5 PHY:PHY_EXT1:PHY_1000BT_EPG1

Parent: PHY:PHY_EXT1

Instances: 1

Table 558 • **Fields in PHY_1000BT_EPG1**

Field Name	Bit	Access	Description	Default
EPG_ENA	15	R/W	Enables the Ethernet packet generator. When this field is set, the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled.	0x0
EPG_RUN_ENA	14	R/W	Begin transmission of Ethernet packets. Clear to stop the transmission of packets. If a transmission is in progress, the transmission of packets is stopped after the current packet is transmitted. This field is valid only when the EPG is enabled (see EPG_ENA).	0x0

Table 558 • **Fields in PHY_1000BT_EPG1** ***(continued)***

Field Name	Bit	Access	Description	Default
TRANSMIT_DURATION_CFG	13	R/W	Configure the duration of the packet generation. When set, the EPG continuously transmits packets as long as field EPG_RUN_ENA is set. When cleared, the EPG transmits 30,000,000 packets when field EPG_RUN_ENA is set, after which time, field EPG_RUN_ENA is automatically cleared. This field is latched when packet generation begins by setting EPG_RUN_ENA in this register.	0x0
PACKET_LEN_CFG	12:11	R/W	This field selects the length of packets to be generated by the EPG. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register. 00: 125-byte packets. 01: 64-byte packets. 10: 1518-byte packets. 11: 10,000-byte packets.	0x0
INTER_PACKET_GAB_CFG	10	R/W	This field configures the inter packet gab for packets generated by the EPG. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register. 0: 96 ns inter-packet gap. 1: 9,192 ns inter-packet gap.	0x0
DEST_ADDR_CFG	9:6	R/W	This field configures the low nibble of the most significant byte of the destination MAC address. The rest of the destination MAC address is all-ones. For example, setting this field to 0x2 results in packets generated with a destination MAC address of 0xF2FFFFFFFFFF. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x1

Table 558 • **Fields in PHY_1000BT_EPG1 *(continued)***

Field Name	Bit	Access	Description	Default
SRC_ADDR_CFG	5:2	R/W	This field configures the low nibble of the most significant byte of the source MAC address. The rest of the source MAC address is all-ones. For example, setting this field to 0xE results in packets generated with a source MAC address of 0xFEFFFFFFFFFF. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x0
PAYLOAD_TYPE	1	R/W	Payload type. 0: Fixed based on payload pattern. 1: Randomly generated payload pattern.	0x0
BAD_FCS_ENA	0	R/W	When this field is set, the EPG generates packets containing an invalid Frame Check Sequence (FCS). When cleared, the EPG generates packets with a valid FCS. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x0

7.14.2.6 PHY:PHY_EXT1:PHY_1000BT_EPG2

Parent: PHY:PHY_EXT1

Instances: 1

Table 559 • **Fields in PHY_1000BT_EPG2**

Field Name	Bit	Access	Description	Default
PACKET_PAYLOAD_CFG	15:0	R/W	Each packet generated by the EPG contains a repeating sequence of this field as payload. This field is latched when generation of packets begins by setting PHY_1000BT_EPG1.EPG_RUN_ENA.	0x0000

7.14.3 PHY:PHY_EXT2

Parent: PHY

Instances: 1

Set register 0x1F to 0x0002 to make the extended set of registers visible in the address range 0x10 through 0x1E. Set register 0x1F to 0x0000 to revert back to the standard register set.

Table 560 • **Registers in PHY_EXT2**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_PMD_TX_CTRL	0x00000010	1	Cu PMD Transmit Control (Address 16E2)	Page 410
PHY_EEE_CTRL	0x00000011	1	EEE Control (Address 17E2)	Page 410

7.14.3.1 PHY:PHY_EXT2:PHY_PMD_TX_CTRL

Parent: PHY:PHY_EXT2

Instances: 1

This register consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetic from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. Please contact the Microsemi Applications Support team for further help with changing these values.

Table 561 • **Fields in PHY_PMD_TX_CTRL**

Field Name	Bit	Access	Description	Default
SIG_AMPL_1000BT	15:12	R/W	1000BT signal amplitude trim.	0x0
SIG_AMPL_100BTX	11:8	R/W	100BASE-TX signal amplitude trim.	0x2
SIG_AMPL_10BT	7:4	R/W	10BASE-T signal amplitude trim.	0xF
SIG_AMPL_10BTE	3:0	R/W	10BASE-Te signal amplitude trim.	0x0

7.14.3.2 PHY:PHY_EXT2:PHY_EEE_CTRL

Parent: PHY:PHY_EXT2

Instances: 1

Table 562 • **Fields in PHY_EEE_CTRL**

Field Name	Bit	Access	Description	Default
EEE_10BTE_ENA	15	R/W	Enable energy efficient (IEEE 802.3az) 10BASE-Te operating mode.	0x0

Table 562 • **Fields in PHY_EEE_CTRL *(continued)***

Field Name	Bit	Access	Description	Default
FORCE_1000BT_ENA	5	R/W	Enable 1000BT force mode to allow PHY to link up in 1000BT mode without forcing master/slave when PHY_STD::PHY_CTRL.SPEED_SEL_LSB_CFG=0 and PHY_STD::PHY_CTRL.SPEED_SEL_MSB_CFG=1.	0x0
FORCE_LPI_TX_ENA	4	R/W	Force transmit LPI. 0: Transmit idles being received from the MAC. 1: Enable the EPG to transmit LPI on the MDI instead of normal idles when receiving normal idles from the MAC.	0x0
EEE_LPI_TX_100BTX_DIS	3	R/W	Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0x0
EEE_LPI_RX_100BTX_DIS	2	R/W	Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0x0
EEE_LPI_TX_1000BT_DIS	1	R/W	Disable transmission of EEE LPI on transmit path MDI in 1000BT mode when receiving LPI from MAC.	0x0
EEE_LPI_RX_1000BT_DIS	0	R/W	Disable transmission of EEE LPI on receive path MAC interface in 1000BT mode when receiving LPI from the MDI.	0x0

7.14.4 PHY:PHY_GP

Parent: PHY

Instances: 1

Set register 0x1F to 0x0010 to access the general purpose registers. This sets all 32 registers to the general purpose register space. Set register 0x1F to 0x0000 to revert back to the standard register set.

Table 563 • **Registers in PHY_GP**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_COMA_MODE_CTRL	0x0000000E	1	Coma Mode Control (Address 14G)	Page 412
PHY_GLOBAL_INT_STAT	0x0000001D	1	Global Interrupt Status (Address 29G)	Page 412

7.14.4.1 PHY:PHY_GP:PHY_COMA_MODE_CTRL

Parent: PHY:PHY_GP

Instances: 1

Table 564 • **Fields in PHY_COMA_MODE_CTRL**

Field Name	Bit	Access	Description	Default
COMA_MODE_OE	13	R/W	COMA_MODE output enable. Active low. 0: COMA_MODE pin is an output. 1: COMA_MODE pin is an input.	0x1
COMA_MODE_OUTPUT	12	R/W	COMA_MODE output data.	0x0
COMA_MODE_INPUT	11	R/O	COMA_MODE input data.	0x0

7.14.4.2 PHY:PHY_GP:PHY_GLOBAL_INT_STAT

Parent: PHY:PHY_GP

Instances: 1

Table 565 • **Fields in PHY_GLOBAL_INT_STAT**

Field Name	Bit	Access	Description	Default
TMON_INT_SRC	12	R/O	Indicates that the temperature monitor is the source of the interrupt when this bit is cleared. This bit is is set high when this register is read.	0x1
PHY11_INT_SRC	11	R/O	Indicates that PHY11 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY11.	0x1
PHY10_INT_SRC	10	R/O	Indicates that PHY10 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY10.	0x1
PHY9_INT_SRC	9	R/O	Indicates that PHY9 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY9.	0x1
PHY8_INT_SRC	8	R/O	Indicates that PHY8 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY8.	0x1

Table 565 • **Fields in PHY_GLOBAL_INT_STAT *(continued)***

Field Name	Bit	Access	Description	Default
PHY7_INT_SRC	7	R/O	Indicates that PHY7 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY7.	0x1
PHY6_INT_SRC	6	R/O	Indicates that PHY6 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY6.	0x1
PHY5_INT_SRC	5	R/O	Indicates that PHY5 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY5.	0x1
PHY4_INT_SRC	4	R/O	Indicates that PHY4 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY4.	0x1
PHY3_INT_SRC	3	R/O	Indicates that PHY3 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY3.	0x1
PHY2_INT_SRC	2	R/O	Indicates that PHY2 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY2.	0x1
PHY1_INT_SRC	1	R/O	Indicates that PHY1 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY1.	0x1
PHY0_INT_SRC	0	R/O	Indicates that PHY0 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY0.	0x1

7.14.5 PHY:PHY_EEE

Parent: PHY

Instances: 1

Access to these registers is through the IEEE standard registers MMD_ACCESS_CFG and MMD_ADDR_DATA.

Table 566 • **Registers in PHY_EEE**

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_PCS_STATUS1	0x00000000	1	PCS Status 1 (Address 3.1)	Page 414
PHY_EEE_CAPABILITIES	0x00000001	1	EEE Capabilities (Address 3.20)	Page 414
PHY_EEE_WAKE_ERR_CNT	0x00000002	1	EEE Wake Error Counter (Address 3.22)	Page 415
PHY_EEE_ADVERTISEMENT	0x00000003	1	EEE Advertisement (Address 7.60)	Page 415
PHY_EEE_LP_ADVERTISEMENT	0x00000004	1	EEE Link Partner Advertisement (Address 7.61)	Page 416

7.14.5.1 PHY:PHY_EEE:PHY_PCS_STATUS1

Parent: PHY:PHY_EEE

Instances: 1

Status of the EEE operation from the PCS for the link that is currently active.

Table 567 • **Fields in PHY_PCS_STATUS1**

Field Name	Bit	Access	Description	Default
TX_LPI_RECV	11	R/O	0: LPI not received 1: Tx PCS has received LPI	0x0
RX_LPI_RECV	10	R/O	1: Rx PCS has received LPI 0: LPI not received	0x0
TX_LPI_INDICATION	9	R/O	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI	0x0
RX_LPI_INDICATION	8	R/O	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI	0x0
PCS_RECV_LINK_STAT	2	R/O	1: PCS receive link up 0: PCS receive link down	0x0

7.14.5.2 PHY:PHY_EEE:PHY_EEE_CAPABILITIES

Parent: PHY:PHY_EEE

Instances: 1

Indicate the capability of the PCS to support EEE functions for each PHY type.

Table 568 • **Fields in PHY_EEE_CAPABILITIES**

Field Name	Bit	Access	Description	Default
EEE_1000BT	2	R/O	Set if EEE is supported for 1000BASE-T. 1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T	0x1
EEE_100BTX	1	R/O	Set if EEE is supported for 100BASE-TX. 1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX	0x1

7.14.5.3 PHY:PHY_EEE:PHY_EEE_WAKE_ERR_CNT

Parent: PHY:PHY_EEE

Instances: 1

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 569 • **Fields in PHY_EEE_WAKE_ERR_CNT**

Field Name	Bit	Access	Description	Default
EEE_WAKE_ERR_CNT	15:0	R/O	Count of wake time faults for a PHY.	0x0000

7.14.5.4 PHY:PHY_EEE:PHY_EEE_ADVERTISEMENT

Parent: PHY:PHY_EEE

Instances: 1

Defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code.

Table 570 • **Fields in PHY_EEE_ADVERTISEMENT**

Field Name	Bit	Access	Description	Default
EEE_1000BT_ADV	2	R/W	Set if EEE is supported for 1000BASE-T. 1: Advertise that the 1000BASE-T has EEE capability. 0: Do not advertise that the 1000BASE-T has EEE capability.	0x0
EEE_100BTX_ADV	1	R/W	Set if EEE is supported for 100BASE-TX. 1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0x0

7.14.5.5 PHY:PHY_EEE:PHY_EEE_LP_ADVERTISEMENT

Parent: PHY:PHY_EEE

Instances: 1

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register.

Table 571 • **Fields in PHY_EEE_LP_ADVERTISEMENT**

Field Name	Bit	Access	Description	Default
EEE_1000BT_LP_ADV	2	R/O	Set if EEE is supported for 1000BASE-T by link partner. 1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T	0x0
EEE_100BTX_LP_ADV	1	R/O	Set if EEE is supported for 100BASE-TX by link partner. 1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX	0x0

8 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

8.1 DC Characteristics

This section contains the DC specifications for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

8.1.1 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see Pins by Function for VSC7420XJQ-02, page 438, Pins by Function for VSC7421XJQ-02, page 487, or Pins by Function for VSC7422XJQ-02, page 538.

All internal pull-up resistors are connected to their respective I/O supply.

Table 572 • **Internal Pull-Up or Pull-Down Resistors**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Internal pull-up resistor, GPIO and SI pins	R_{PU}	33	53	90	kΩ
Internal pull-up resistor, all other pins	R_{PD}	96	120	144	kΩ
Internal pull-down resistor	R_{PD}	96	120	144	kΩ

8.1.2 Reference Clock

The following table lists the DC specifications for the differential RefClk signal. Differential and single-ended modes are supported. For more information about single-ended mode operation, see Single-Ended RefClk Input, page 589.

Table 573 • **Reference Clock Input DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit
Input voltage range	V_{IP}, V_{IN}	–25	1260	mV
Input differential voltage, peak-to-peak	$\|V_{ID}\|$	150(1)	1000	mV
Input common-mode voltage	V_{CM}	0	1200(2)	mV

1. To meet jitter specifications, the minimum input differential voltage must be 400 mV. When using a single-ended clock input, the RefClk_P low voltage level must be lower than V_{DD_A} – 200 mV, and the high voltage level must be higher than V_{DD_A} + 200 mV.
2. The maximum common-mode voltage is given without any differential signal, because the input is internally AC-coupled. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

8.1.3 SGMII DC Definitions and Test Circuits

This section provides information about the definitions and test circuits that apply to certain parameters for the Enhanced SerDes interface. The following illustrations show the DC definitions for the SGMII inputs and outputs.

Figure 54 • **SGMII DC Input Definitions**

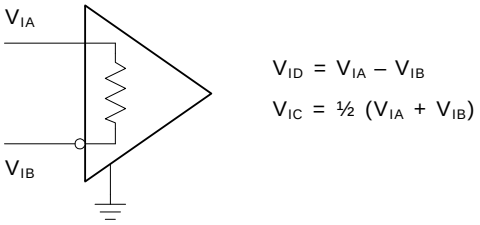


Figure 55 • **SGMII DC Transmit Test Circuit**

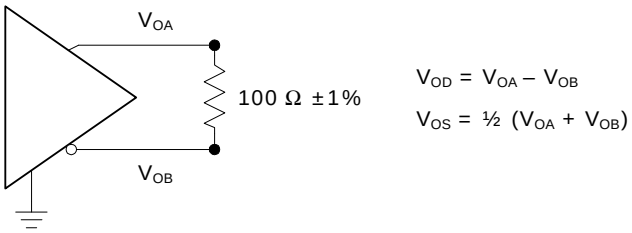
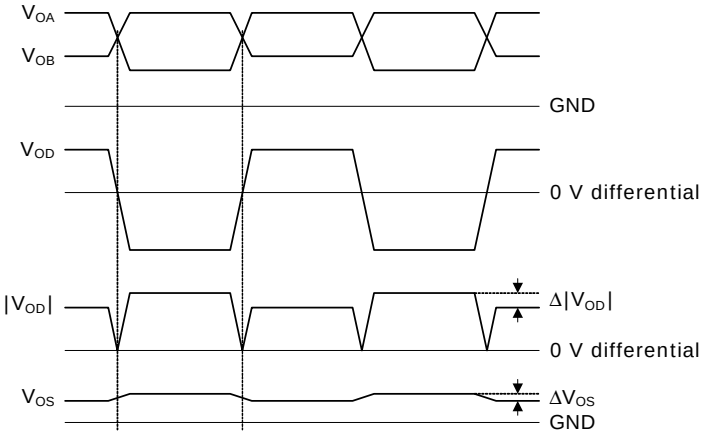


Figure 56 • **SGMII DC Definitions**

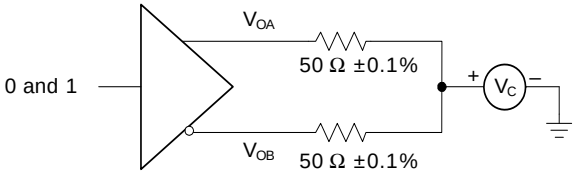


$\Delta|V_{OD}| = | |V_{OAH} - V_{OBL}| - |V_{OBH} - V_{OAL}| |$

$\Delta V_{OS} = | ½(V_{OAH} + V_{OBL}) - ½(V_{OAL} + V_{OBH}) |$

The following illustrations show the SMGII DC driver output impedance test circuit and the DC input definitions.

Figure 57 • **SGMII DC Driver Output Impedance Test Circuit**



8.1.4 Enhanced SerDes Interface

All DC specifications for the Enhanced SerDes interface are compliant with the QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI version 2.0 requirements where applicable.

The Enhanced SerDes interface supports four major modes: SGMII, QSGMII, 2.5G, and SFP. The values in the following table apply to modes specified.

Table 574 • **Enhanced SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output differential peak voltage(1), 1.0 V, SFP, 2.5G, and QSGMII modes	$\|V_{ODp}\|$	250	400	mV	V_{DD_VS} = 1.0 V. R_L = 100 Ω ±1%.
Output differential peak voltage(1), 1.0 V and 1.2 V, SGMII mode	$\|V_{ODp}\|$	150	400	mV	V_{DD_VS} = 1.0 V, V_{DD_VS} = 1.2 V. R_L = 100 Ω ±1%.
Output differential peak voltage(1), 1.2 V, SFP mode	$\|V_{ODp}\|$	300	600	mV	V_{DD_VS} = 1.2 V. R_L = 100 Ω ±1%.
Output differential peak voltage(1), 1.2 V, QSGMII mode	$\|V_{ODp}\|$	200	400	mV	V_{DD_VS} = 1.2 V. R_L = 100 Ω ±1%.
Output differential peak voltage(1), 1.2 V, 2.5G mode	$\|V_{ODp}\|$	360	600	mV	V_{DD_VS} = 1.2 V. R_L = 100 Ω ±1%, maximum drive
DC output impedance, single-ended, SGMII mode	R_O	40	140	Ω	V_C = 1.0 V and 1.2 V. See Figure 57, page 418.
R_O mismatch between A and B(2), SGMII mode	ΔR_O		10	%	V_C = 1.0 V and 1.2 V. See Figure 57, page 418.
Change in $\|V_{OD}\|$ between 0 and 1, SGMII mode	$\Delta\|V_{OD}\|$		25	mV	R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1, SGMII mode	ΔV_{OS}		25	mV	R_L = 100 Ω ±1%.
Output current, driver shorted to GND, SGMII and QSGMII modes	$\|I_{OSA}\|$, $\|I_{OSB}\|$		40	mA	
Output current, drivers shorted together, SGMII and QSGMII modes	$\|I_{OSAB}\|$		12	mA	

1. Voltage is adjustable in 64 steps. For more information about setting the adjustable voltages, see the OB_LEV bit in Table 361, page 270. To meet the return loss specification, the maximum swing is 600 mV peak-to-peak for V_{DD_VS} = 1.0 V and 950 mV peak-to-peak for V_{DD_VS} = 1.2 V.
2. Matching of reflection coefficients. For more information about test methods, see IEEE 1596.3-1996.

The following table lists the DC specifications for the Enhanced SerDes receivers. In most applications, AC-coupling is required. For more information, see Enhanced SerDes Interface, page 591.

Table 575 • **Enhanced SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range, V_{IA} or V_{IB}(1)	V_I	–0.25		1.2	V

Table 575 • **Enhanced SerDes Receiver DC Specifications *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input differential peak voltage[2], SGMII and SFP modes	$\|V_{ID}\|$	50		800	mV
Input differential peak voltage[2], QSGMII mode	$\|V_{ID}\|$	50		600	mV
Input differential peak voltage[2], 2.5G mode	$\|V_{ID}\|$	50		800	mV
Receiver differential input impedance	R_I	80	100	120	Ω

1. QSGMII DC input sensitivity is <400 mV.
2. Ranges specified are for optimal operation.

8.1.5 MIIM, GPIO, SI, JTAG, and Miscellaneous Signals

This section provides the DC specifications for the MII Management (MIIM), GPIO, SI, JTAG, and miscellaneous signals. The following I/O signals comply with the specifications provided in this section.

Table 576 •

MDC	JTAG_nTRST	Reserved
MDIO	JTAG_TMS	RefClk_Sel[2:0]
GPIO[31:0]	JTAG_TDO	VCORE_CFG[2:0]
SI_Clk	JTAG_TCK	
SI_DI	JTAG_TDI	
SI_DO	nReset	
SI_nEn	COMA_MODE	

The outputs and inputs meet or exceed the requirements of the LVTTL and LVCMOS standard, JEDEC JESD8-B (September 1999) standard, unless otherwise stated. The inputs are Schmitt-trigger for noise immunity.

Table 577 • **MIIM, GPIO, SI, JTAG, and Miscellaneous Signals DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, I_{OH} = –12 mA	V_{OH}	1.7		V	
Output high voltage, I_{OH} = –2 mA	V_{OH}	2.1		V	
Output low voltage, I_{OL} = 12 mA	V_{OL}		0.7	V	
Output low voltage, I_{OL} = 2 mA	V_{OL}		0.4	V	
Input high voltage	V_{IH}	1.85	3.6	V	
Input low voltage	V_{IL}	–0.3	0.8	V	
Input high current[1]	I_{IH}		10	µA	$V_I = V_{DD_IO}$
Input low current[1]	I_{IL}	–10		µA	V_I = 0 V
Input capacitance	C_I		10	pF	

1. Input high current and input low current equals the maximum leakage current, excluding the current in the built-in pull resistors.

8.2 AC Characteristics

This section provides the AC specifications for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

8.2.1 Reference Clock

The signal applied to the RefClk differential input must comply with the requirements listed in the following table at the pin of the device.

To meet QSGMII jitter generation requirements, Microsemi requires the use of a differential reference clock source. Use of a 25 MHz single-ended reference clock is not recommended. However, to implement a QSGMII chip interconnect using a 25 MHz single-ended reference clock and achieve error-free data transfer on that interface, use an Ethernet PHY with higher jitter tolerance than specified in the standard, such as Microsemi's VSC8512-02 or VSC8522-02. For more information about QSGMII interoperability when using a 25 MHz single-ended reference clock, contact your Microsemi representative.

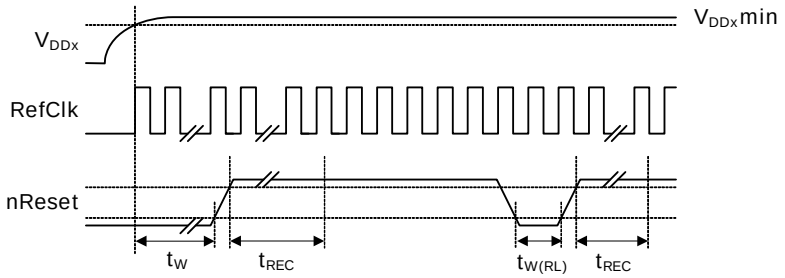
Table 578 • **Reference Clock AC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
RefClk frequency, RefClk_Sel = 000	f	–100 ppm	125	100 ppm	MHz	
RefClk frequency, RefClk_Sel = 001	f	–100 ppm	156.25	100 ppm	MHz	
RefClk frequency, RefClk_Sel = 100	f	–100 ppm	25	100 ppm	MHz	
Clock duty cycle		40		60	%	Measured at 50% threshold.
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80% threshold.
RefClk input RMS jitter, bandwidth between 12 kHz and 500 kHz				20	ps	
RefClk input RMS jitter, bandwidth between 500 kHz and 15 MHz				4	ps	
RefClk input RMS jitter, bandwidth between 15 MHz and 40 MHz				20	ps	
RefClk input RMS jitter, bandwidth between 40 MHz and 80 MHz				100	ps	
Jitter gain from RefClk to SerDes output, bandwidth between 0 MHz and 0.1 MHz				0.3	dB	
Jitter gain from RefClk to SerDes output, bandwidth between 0.1 MHz and 7 MHz				3	dB	
Jitter gain from RefClk to SerDes output, bandwidth above 7 MHz				3 – 20 × log (f/7 MHz)	dB	

8.2.2 Reset Timing

The nReset signal waveform and the required measurement points for the timing specification are shown in the following illustration.

Figure 58 • **nReset Signal Timing Specifications**



The signal applied to the nReset input must comply with the specifications listed in the following table at the reset pin of the device.

Table 579 • **nReset Timing Specifications**

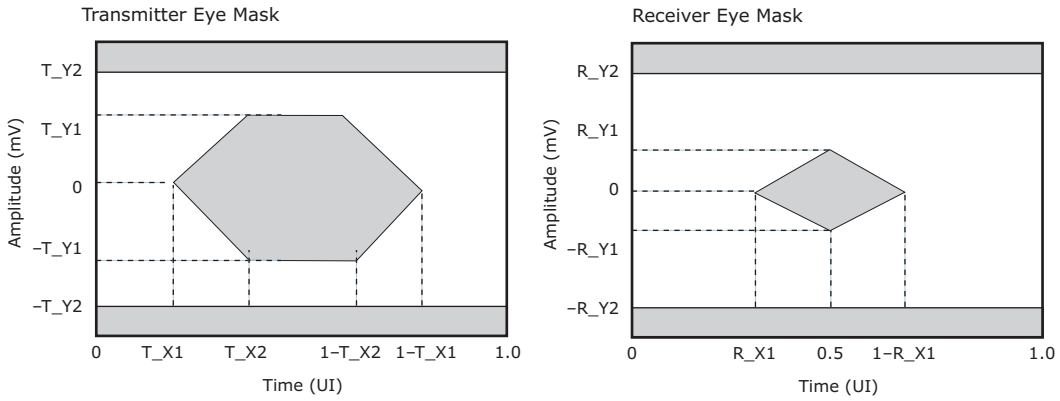
Parameter	Symbol	Minimum	Maximum	Unit
nReset assertion time after power supplies and clock stabilize	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		50	ms
nReset pulse width	$t_{W(RL)}$	100		ns

8.2.3 Enhanced SerDes Interface

All AC specifications for the Enhanced SerDes interface are compliant with the QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI version 2.0 requirements where applicable.

The Enhanced SerDes interface supports four major modes: SGMII, QSGMII, 2.5G, and SFP. The values in the tables in the following sections apply to modes listed in the condition column and are based on the test circuit shown in Figure 55, page 418. The transmit and receive eye specifications in the tables relate to the eye diagrams shown in the following illustration, with the compliance load as defined in the test circuit.

Figure 59 • **QSGMII Transient Parameters**



8.2.3.1 Enhanced SerDes Outputs

The following table provides the AC specifications for the Enhanced SerDes outputs in SGMII mode.

Table 580 • **Enhanced SerDes Output AC Specifications in SGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 1.25G	UI				800 ps.
V_{OD} ringing compared to V_S	V_{RING}		±10	%	R_L = 100 Ω ±1%.
V_{OD} rise time and fall time	t_R, t_F	100	200	ps	20% to 80% of V_S, R_L = 100 Ω ±1%.
Differential output peak-to-peak voltage	V_{OD}		30	mV	Tx disabled.
Differential output return loss, 1000BASE-KX mode, 50 MHz to 625 MHz	RL_{TX_DIFF}	≥10		dB	R_L = 100 Ω ±1%.
Differential output return loss, 1000BASE-KX mode, 625 MHz to 1250 MHz	RL_{TX_DIFF}	10–10 × log (f/625 MHz)		dB	R_L = 100 Ω ±1%
Common mode return loss, 1000BASE-KX mode	RL_{CM}	6		dB	50 MHz to 625 MHz
Intrapair skew, SGMII mode	t_{SKEW}		20	ps	

The following table provides the AC specifications for the Enhanced SerDes outputs in QSGMII mode.

Table 581 • **Enhanced SerDes Output AC Specifications in QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps.
V_{OD} rise time and fall time	t_R, t_F	30	96	ps	20% to 80% of V_S, R_L = 100 Ω ±1%.
Differential output peak-to-peak voltage	V_{OD}		30	mV	Tx disabled.
Differential output return loss 100 MHz to 2.5 GHz	RL_{TX_DIFF}	8		dB	R_L = 100 Ω ±1%.
Differential output return loss, 1000BASE-KX mode, 2.5 GHz to 5 GHz	RL_{TX_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%.
Eye mask (T_X1)			0.15	UI	
Eye mask (T_X2)			0.4	UI	
Eye mask (T_Y1)		200		mV	
Eye mask (T_Y2)			450	mV	

The following table provides the AC specifications for the Enhanced SerDes outputs in 2.5G mode.

Table 582 • **Enhanced SerDes Output AC Specifications in 2.5G Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 2.5G	UI				320 ps.

Table 582 • **Enhanced SerDes Output AC Specifications in 2.5G Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
V_{OD} rise time and fall time	t_R, t_F	60	130	ps	20% to 80% of V_S, R_L = 100 Ω ±1%.
Differential output peak-to-peak voltage, SGMII mode	V_{OD}		30	mV	Tx disabled.
Differential output return loss, 100 MHz to 625 MHz	RL_{TX_DIFF}	10		dB	R_L = 100 Ω ±1%.
Differential output return loss, 625 MHz to 3.125 GHz		10–10 × log (*f*/625 MHz)		dB	R_L = 100 Ω ±1%.
Eye mask (T_X1)			0.175	UI	
Eye mask (T_X2)			0.390	UI	
Eye mask (T_Y1)		200		mV	
Eye mask (T_Y2)			400	mV	

8.2.3.2 Enhanced SerDes Driver Jitter Characteristics

The following table lists the jitter characteristics for the Enhanced SerDes driver in SGMII mode.

Table 583 • **Enhanced SerDes Driver Jitter Characteristics in SGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Total output jitter	$t_{JIT(O)}$	192	ps	Measured according to IEEE 802.3.38.5.
Deterministic output jitter	$t_{JIT(OD)}$	80	ps	Measured according to IEEE 802.3.38.5.

The following table lists the jitter characteristics for the Enhanced SerDes driver in QSGMII mode.

Table 584 • **Enhanced SerDes Driver Jitter Characteristics in QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Total output jitter	$t_{JIT(O)}$	60	ps	Measured according to IEEE 802.3.38.5.
Deterministic output jitter	$t_{JIT(OD)}$	10	ps	Measured according to IEEE 802.3.38.5.

8.2.3.3 Enhanced SerDes Inputs

The following table lists the AC specifications for the Enhanced SerDes inputs in SGMII mode.

Table 585 • **Enhanced SerDes Input AC Specifications in SGMII Mode**

Parameter	Symbol	Minimum	Unit	Condition
Unit interval, 1.25G	UI		ps	800 ps.
Differential input return loss	RL_{RX_DIFF}	10	dB	50 MHz to 625 MHz, R_L = 100 Ω ±1%.
Common-mode input return loss		6	dB	50 MHz to 625 MHz.

The following table lists the AC specifications for the Enhanced SerDes inputs in QSGMII mode.

Table 586 • **Enhanced SerDes Input AC Specifications in QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps.
Differential input return loss, 100 MHz to 2.5 GHz	RL_{RX_DIFF}	8		dB	R_L = 100 Ω ±1%.
Differential input return loss, 2.5 GHz to 5 GHz	RL_{RX_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%.
Common-mode input return loss		6		dB	100 MHz to 2.5 GHz.
Eye mask (R_X1)			0.3	UI	
Eye mask (R_Y1)			50	mV	
Eye mask (R_Y2)			450	mV	

The following table lists the AC specifications for the Enhanced SerDes inputs in 2.5G mode.

Table 587 • **Enhanced SerDes Input AC Specifications in 2.5G Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 2.5G	UI				320 ps.
Differential input return loss	RL_{RX_DIFF}	10		dB	100 MHz to 2.5 GHz, R_L = 100 Ω ±1%.
Common-mode input return loss		6		dB	100 MHz to 2.5 GHz.
Eye mask (R_X1)			0.275	UI	
Eye mask (R_X2)			0.5	UI	
Eye mask (R_Y1)		100		mV	
Eye mask (R_Y2)			800	mV	

8.2.3.4 Enhanced SerDes Receiver Jitter Tolerance

The following table lists jitter tolerances for the Enhanced SerDes receiver in SGMII mode.

Table 588 • **Enhanced SerDes Receiver Jitter Tolerance in SGMII Mode**

Parameter	Symbol	Minimum	Unit	Condition
Total input jitter tolerance, 1000BASE-KX and SFP modes	$t_{JIT(I)}$	600	ps	Above 637 kHz. Measured according to IEEE 802.3 38.6.8.
Deterministic input jitter tolerance, 1000BASE-KX and SFP mode	$t_{JIT(ID)}$	370	ps	Above 637 kHz. Measured according to IEEE 802.3 38.6.8.
Cycle distortion input jitter tolerance, 100BASE-FX mode	D_{CD}	1.4	ns	Measured according to ISO/IEC 9314-3:1990. IB_ENA_CMV_TERM = 1 IB_ENA_DC_COUPLING = 1

Table 588 • **Enhanced SerDes Receiver Jitter Tolerance in SGMII Mode**

Parameter	Symbol	Minimum	Unit	Condition
Data-dependent input jitter tolerance, 100BASE-FX mode	D_{DJ}	2.2	ns	Measured according to ISO/IEC 9314-3:1990. IB_ENA_CMV_TERM = 1 IB_ENA_DC_COUPLING = 1
Random input jitter tolerance, peak-to-peak, 100BASE-FX mode	R_J	2.27	ns	Measured according to. ISO/IEC 9314-3:1990. IB_ENA_CMV_TERM = 1 IB_ENA_DC_COUPLING = 1

The following table lists jitter tolerances for the Enhanced SerDes receiver in QSGMII mode.

Table 589 • **Enhanced SerDes Receiver Jitter Tolerance in QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Bounded high-probability jitter(1)	BHP_J	90	ps	92 ps peak-to-peak random jitter, and 38 ps sinusoidal jitter (SJHF).
Sinusoidal jitter, maximum	SJ_{MAX}	1000	ps	
Sinusoidal jitter, high frequency	SJ_{HF}	10	ps	
Total input jitter tolerance	$t_{JIT(I)}$	120	ps	92 ps peak-to-peak random jitter, and 38 ps sinusoidal jitter (SJHF).

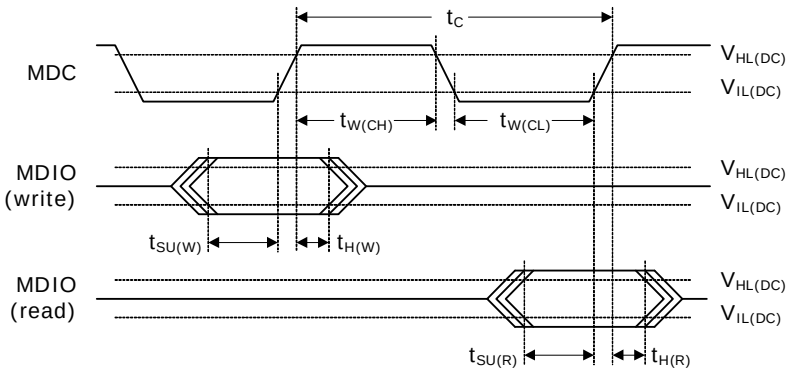
1. This is the sum of uncorrelated bounded high probability jitter (0.15 UI) and correlated bounded high probability jitter (0.30 UI).
Uncorrelated bounded high probability jitter is defined as jitter distribution where the value of the jitter shows no correlation to any signal level being transmitted. Formally defined as deterministic jitter ($T_{_DJ}$).
Correlated bounded high probability jitter is defined as jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted.

8.2.4 MII Management

All AC specifications for the MII Management (MIIM) interface meet or exceed the requirements of IEEE 802.3-2002 (clause 22.2-4).

All MIIM AC timing requirements are specified relative to the input low and input high threshold levels. The following illustration shows the MIIM waveforms and required measurement points for the signals.

Figure 60 • **MIIM Timing Diagram**



The setup time of MDIO relative to the rising edge of MDC is defined as the length of time between when the MDIO exits and remains out of the switching region and when MDC enters the switching region. The

hold time of MDIO relative to the rising edge of MDC is defined as the length of time between when MDC exits the switching region and when MDIO enters the switching region.

All MIIM signals comply with the specifications in the following table. The MDIO signal requirements are requested at the pin of the device.

Table 590 • **MIIM Timing Specifications**

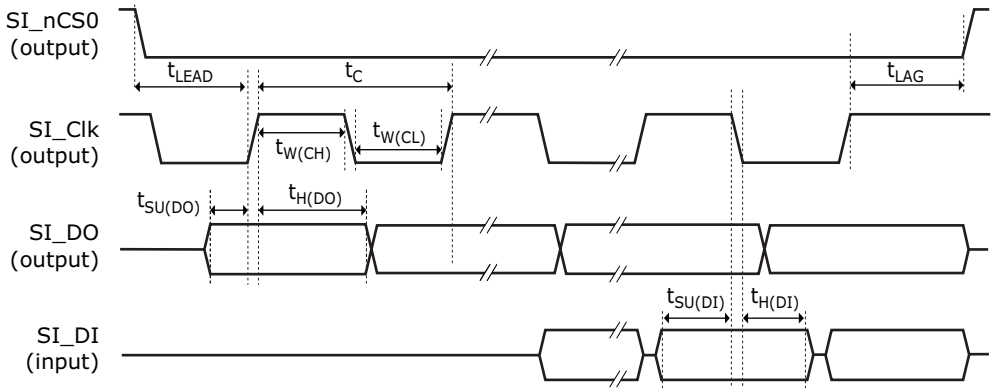
Parameter	Symbol	Minimum	Maximum	Unit	Condition
MDC frequency(1)	f	0.488	20.83	MHz	
MDC cycle time(2)	t_C	48	2048	ns	
MDC time high	$t_{W(CH)}$	20		ns	C_L = 50 pF
MDC time low	$t_{W(CL)}$	20		ns	C_L = 50 pF
MDC input rise and fall time for slave mode	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
MDIO setup time to MDC on write	$t_{SU(W)}$	15		ns	C_L = 50 pF
MDIO hold time from MDC on write	$t_{H(W)}$	15		ns	C_L = 50 pF
MDIO setup time to MDC on read	$t_{SU(R)}$	30		ns	C_L = 50 pF on MDC
MDIO hold time from MDC on read	$t_{H(R)}$	0		ns	C_L = 50 pF

1. For the maximum value, the devices support an MDC clock speed of up to 20 MHz for faster communication with the PHYs. If the standard frequency of 2.5 MHz is used, the MIIM interface is designed to meet or exceed the IEEE 802.3 requirements of the minimum MDC high and low times of 160 ns and an MDC cycle time of minimum 400 ns, which is not possible at faster speeds.
2. Calculated as $t_C = 1/f$.

8.2.5 Serial CPU Interface (SI) Master Mode

All serial CPU interface (SI) timing requirements for master mode are specified relative to the input low and input high threshold levels. The following illustration shows the timing parameters and measurement points.

Figure 61 • **SI Timing Diagram for Master Mode**



All SI signals comply with the specifications shown in the following table. The SI input timing requirements are requested at the pins of the device.

Table 591 • **SI Timing Specifications for Master Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	f		25(1)	MHz	

Table 591 • **SI Timing Specifications for Master Mode *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock cycle time	t_C	40		ns	
Clock time high	$t_{W(CH)}$	16		ns	
Clock time low	$t_{W(CL)}$	16		ns	
Clock rise time and fall time	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$. C_L = 30 pF.
DO setup time to clock	$t_{SU(DO)}$	10		ns	
DO hold time from clock	$t_{H(DO)}$	10		ns	
Enable active before first clock	t_{LEAD}	10		ns	
Enable inactive after clock	t_{LAG}	5		ns	
DI setup time to clock	$t_{SU(DI)}$	22		ns	
DI hold time from clock	$t_{H(DI)}$	–2		ns	

1. Frequency is programmable. The startup frequency is 4 MHz.

8.2.6 Serial CPU Interface (SI) for Slave Mode

All serial CPU interface (SI) slave mode timing requirements are specified relative to the input low and input high threshold levels. The following illustrations show the timing parameters and measurement points for SI input and output data.

Figure 62 • **SI Input Data Timing Diagram for Slave Mode**

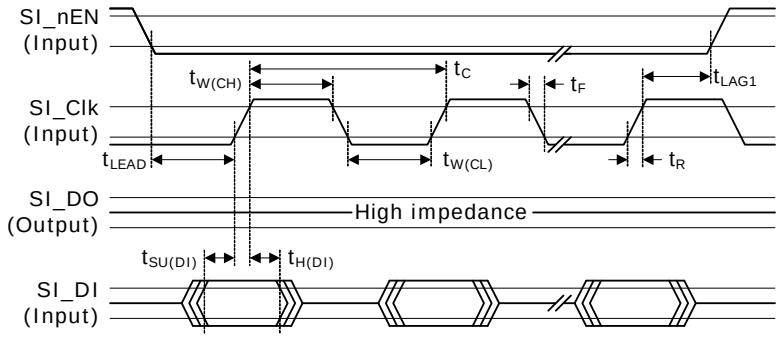
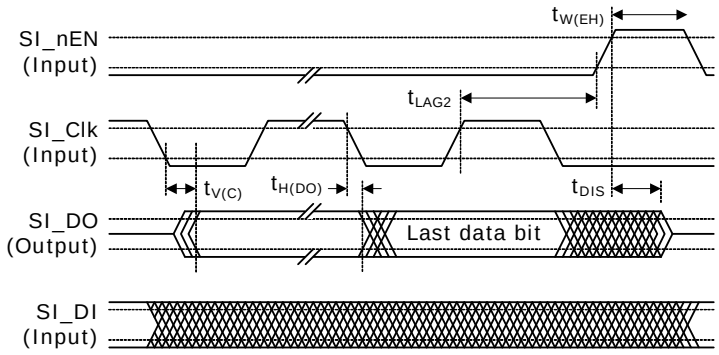


Figure 63 • **SI Output Data Timing Diagram for Slave Mode**



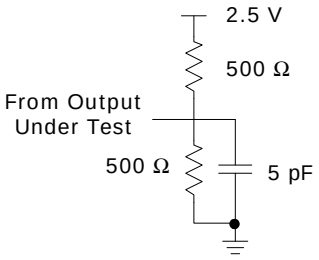
All SI signals comply with the specifications shown in the following table. The SI input timing requirements are requested at the pins of the device.

Table 592 • **SI Timing Specifications for Slave Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	f		25	MHz	
Clock cycle time	t_C	40		ns	
Clock time high	$t_{W(CH)}$	16		ns	
Clock time low	$t_{W(CL)}$	16		ns	
Clock rise time and fall time	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
DI setup time to clock	$t_{SU(DI)}$	4		ns	
DI hold time from clock	$t_{H(DI)}$	4		ns	
Enable active before first clock	t_{LEAD}	10		ns	
Enable inactive after clock (input cycle)(1)	t_{LAG1}	25		ns	
Enable inactive after clock (output cycle)	t_{LAG2}	See note(2)		ns	
Enable inactive width	$t_{W(EH)}$	20		ns	
DO valid after clock	$t_{V(C)}$		20	ns	C_L = 30 pF.
DO hold time from clock	$t_{H(DO)}$	0		ns	C_L = 0 pF.
DO disable time(3)	t_{DIS}		15	ns	See Figure 64, page 429.

1. t_{LAG1} is defined only for write operations to the device, not for read operations.
2. The last rising edge on the clock is necessary for the external master to read in the data. The lag time depends on the necessary hold time on the external master data input.
3. Pin begins to float when a 300 mV change from the loaded V_{OH} or V_{OL} level occurs.

Figure 64 • **SI_DO Disable Test Circuit**

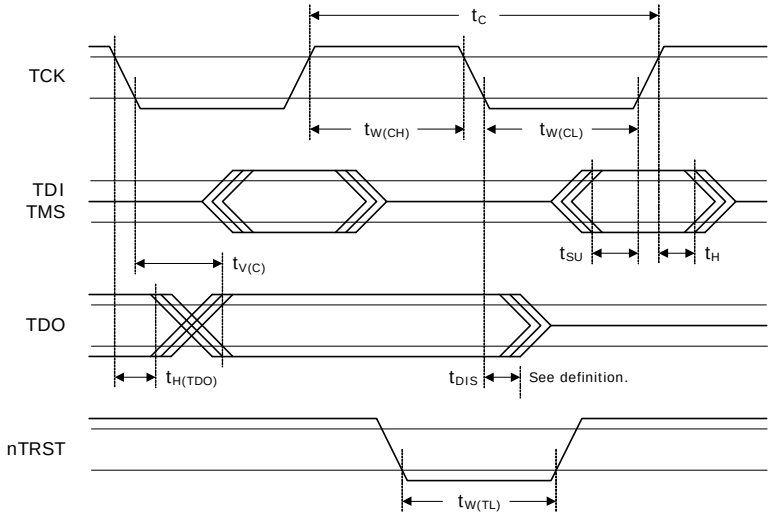


8.2.7 JTAG Interface

All AC specifications for the JTAG interface meet or exceed the requirements of IEEE 1149.1-2001.

The following illustration shows the JTAG transmit and receive waveforms and required measurement points for the different signals.

Figure 65 • **JTAG Interface Timing Diagram**



All JTAG signals comply with the specifications in the following table. The JTAG receive signal requirements are requested at the pin of the device.

The JTAG_nTRST signal is asynchronous to the clock and does not have a setup or hold time requirement.

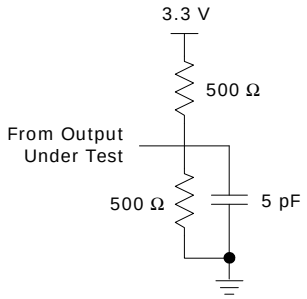
Table 593 • **JTAG Interface AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time(1)	t_{DIS}		30	ns	See Figure 66, page 431.
nTRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

The following illustration shows the test circuit for the TDO disable time.

Figure 66 • **Test Circuit for TDO Disable Time**

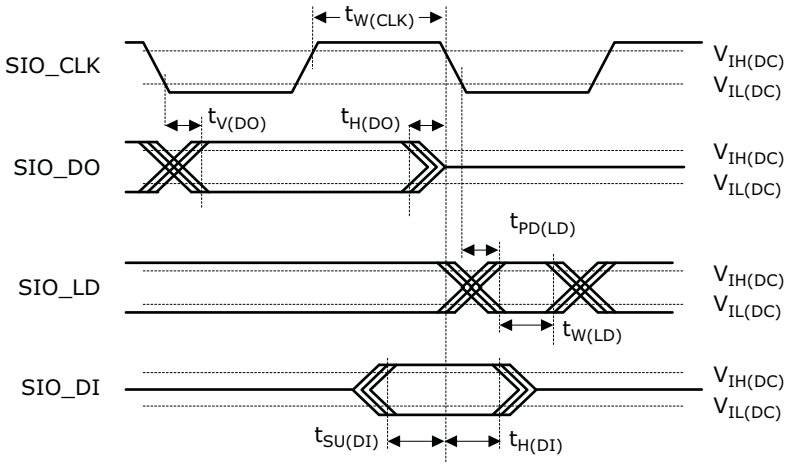


8.2.8 Serial Inputs/Outputs

This section provides the AC characteristics for the serial I/O signals: SIO_CLK, SIO_LD, SIO_DO, and SIO_DI. The SI signals are alternate function signals on the GPIO_[0:3] pins. For more information about the GPIO pin mapping, see the Pins by Function section for the appropriate device.

The serial I/O timing diagram is shown in the following illustration.

Figure 67 • **Serial I/O Timing Diagram**



The following table lists the serial I/O timing specifications.

Table 594 • **Serial I/O Timing Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency(1)	*f*		25	MHz	
SIO_CLK clock pulse width	$t_{W(CLK)}$	16		ns	25 MHz clock
SIO_DO valid after clock falling	$t_{V(DO)}$		6	ns	
SIO_DO hold time from clock falling	$t_{H(DO)}$		6	ns	
SIO_LD propagation delay from clock falling	$t_{PD(LD)}$	40		ns	
SIO_LD width	$t_{W(LD)}$	10		ns	
SIO_DI setup time to clock	$t_{SU(DI)}$	25		ns	
SIO_DI hold time from clock	$t_{H(DI)}$	4		ns	

1. The SIO clock frequency is programmable.

8.2.9 Two-Wire Serial Interface

This section provides the AC specifications for the two-wire serial interface signals TWI_SCL and TWI_SDA. The two-wire serial interface signals are alternate function signals on the GPIO_5 and GPIO_6 pins. For more information about the GPIO pin mapping, see the Pins by Function section for the appropriate device.

The two-wire serial interface signals are compatible with the Philips I^2C-BUS specifications, except for the minimum rise time and fall time requirements for fast mode.

Figure 68 • **Two-Wire Serial Read Timing Diagram**

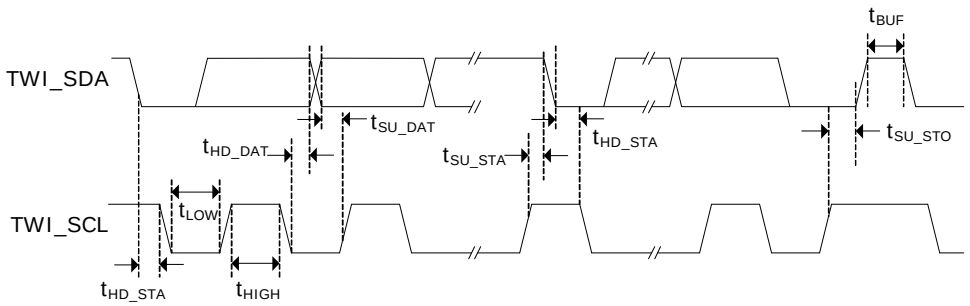
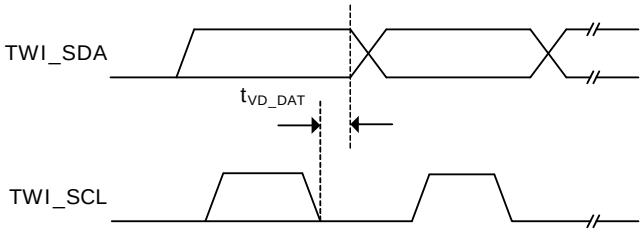


Figure 69 • **Two-Wire Serial Write Timing Diagram**



For the specifications listed in the following table, standard mode is defined as 100 kHz and fast mode is 400 kHz. The data in this table assumes that the software-configurable two-wire interface timing parameters, SS_SCL_HCNT, SS_SCL_LCNT, FS_SCL_HCNT, and FS_SCL_LCNT, are set to valid values for the selected speed. For more information about setting the values for the selected speed, see Table 496, page 361 through Table 499, page 362.

Table 595 • **Two-Wire Serial Interface AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TWI_SCL clock frequency, standard mode	*f*		100	kHz	
TWI_SCL clock frequency, fast mode	*f*		400	kHz	
TWI_SCL low period, standard mode	t_{LOW}	4.7		µs	
TWI_SCL low period, fast mode	t_{LOW}	1.3		µs	
TWI_SCL high period, standard mode	t_{HIGH}	4.0		µs	
TWI_SCL high period, fast mode	t_{HIGH}	0.6		µs	
TWI_SCL and TWI_SDA rise time, standard mode			1000	ns	

Table 595 • **Two-Wire Serial Interface AC Specifications *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TWI_SCL and TWI_SDA rise time, fast mode			300	ns	
TWI_SCL and TWI_SDA fall time, standard mode			300	ns	
TWI_SDA setup time to TWI_SCL fall, standard mode	t_{SU_DAT}	250		ns	
TWI_SDA setup time to TWI_SCL fall, fast mode	t_{SU_DAT}	100	300	ns	
TWI_SDA hold time to TWI_SCL fall, standard mode(1)	t_{HD_DAT}	300	3450	ns	300 ns delay enabled in ICPU_CFG::TWI_CONFIG register.
TWI_SDA hold time to TWI_SCL fall, fast mode(1)	t_{HD_DAT}	300	900	ns	300 ns delay enabled in ICPU_CFG::TWI_CONFIG register.
Setup time for repeated START condition, standard mode	t_{SU_STA}	4.7		µs	
Setup time for repeated START condition, fast mode	t_{SU_SAT}	0.6		µs	
Hold time after repeated START condition, standard mode	t_{HD_STA}	4.0		µs	
Hold time after repeated START condition, fast mode	t_{HD_STA}	0.6		µs	
Bus free time between STOP and START conditions, standard mode	t_{BUF}	4.7		µs	
Bus free time between STOP and START conditions, fast mode	t_{BUF}	1.3		µs	
Clock to valid data out, standard and fast modes(2)	t_{VD_DAT}	300		ns	
Pulse width of spike suppressed by input filter on TWI_SCL or TWI_SDA		0	5	ns	

1. An external device must provide a hold time of at least 300 ns for the TWI_SDA signal to bridge the undefined region of the falling edge of the TWI_SCL signal.
2. Some external devices may require more data in hold time (target device's t_{HD_DAT}) than what is provided by t_{VD_DAT}, for example, 300 ns to 900 ns. The minimum value of t_{VD_DAT} is adjustable; the typical value given represents the recommended minimum value, which is enabled in CPU_CFG::TWI_CONFIG.

8.3 Current and Power Consumption

This section provides the current and power consumption requirements for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

8.3.1 Current Consumption

This section provides the operating current consumption parameters for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

Typical current consumption values are over nominal supply settings at 25 °C case temperature, and maximum traffic load. Maximum current consumption values are over worst-case process, temperature, and supply settings, and maximum traffic load.

The following table lists the typical and maximum operating current consumption values for the VSC7420-02 device.

Table 596 • **Operating Current for VSC7420-02**

Parameter	Symbol	Typical	Maximum	Unit	Condition
V_{DD} operating current	I_{DD}	1.2	2	A	V_{TYP} = 1.0 V
V_{DD_A} operating current	I_{DD_A}	0.16	0.27	A	V_{TYP} = 1.0 V
V_{DD_AL} operating current	I_{DD_AL}	0.16	0.25	A	V_{TYP} = 1.0 V
V_{DD_AH} operating current	I_{DD_AH}	0.9	0.9	A	V_{TYP} = 2.5 V
V_{DD_VS} operating current	I_{DD_VS}	0.13	0.13	A	V_{TYP} = 1.0 V or 1.2 V
V_{DD_IO} operating current	I_{DD_IO}	0.1	0.1	A	V_{TYP} = 2.5 V

The following table lists the typical and maximum operating current consumption values for the VSC7421-02 and VSC7422-02 devices.

Table 597 • **Operating Current for VSC7421-02 and VSC7422-02**

Parameter	Symbol	Typical	Maximum	Unit	Condition
V_{DD} operating current	I_{DD}	1.7	2.6	A	V_{TYP} = 1.0 V
V_{DD_A} operating current	I_{DD_A}	0.22	0.27	A	V_{TYP} = 1.0 V
V_{DD_AL} operating current	I_{DD_AL}	0.2	0.3	A	V_{TYP} = 1.0 V
V_{DD_AH} operating current	I_{DD_AH}	1.4	1.6	A	V_{TYP} = 2.5 V
V_{DD_VS} operating current	I_{DD_VS}	0.15	0.15	A	V_{TYP} = 1.0 V or 1.2 V
V_{DD_IO} operating current	I_{DD_IO}	0.1	0.1	A	V_{TYP} = 2.5 V

8.3.2 Power Consumption

This section provides the power consumption parameters for the VSC7420-02, VSC7421-02, and VSC7422-02 devices, based on current consumption.

Typical power consumption values are over nominal supplies and 25 °C case temperature. Maximum power consumption values are over maximum temperature and all supplies at maximum voltages.

The following table lists the typical and maximum power consumption values for the VSC7420-02 device.

Table 598 • **Power Consumption for VSC7420-02**

Parameter	Typical	Maximum	Unit
Power consumption, SGMII in LVDS mode V_{DD_VS} = 1.0 V	4.2	5.5	W
Power consumption, SGMII in high-drive mode V_{DD_VS} = 1.2 V	4.2	5.6	W

The following table lists the typical and maximum power consumption values for the VSC7421-02 and VSC7422-02 devices.

Table 599 • **Power Consumption for VSC7421-02 and VSC7422-02**

Parameter	Typical	Maximum	Unit
Power consumption, SGMII in LVDS mode V_{DD_VS} = 1.0 V	6.0	8.1	W
Power consumption, SGMII in high-drive mode V_{DD_VS} = 1.2 V	6.1	8.2	W

8.3.3 Power Supply Sequencing

During power on and off, V_{DD_A} and V_{DD_VS} must never be more than 300 mV above V_{DD}.

V_{DD_VS} must be powered, even if the associated interface is not used. These power supplies must not remain at ground or left floating.

There are no sequencing requirements for V_{DD_AL}, V_{DD_AH}, and V_{DD_IO}. These power supplies can remain at ground or left floating if not used.

The nReset and JTAG_nTRST inputs must be held low until all power supply voltages have reached their recommended operating condition values.

8.4 Operating Conditions

The following table lists the recommended operating conditions.

Table 600 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for core supply	V_{DD}	0.95	1.00	1.05	V
Power supply voltage for analog circuits	V_{DD_A}	0.95	1.00	1.05	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AL}	0.95	1.00	1.05	V
Power supply voltage for analog driver in twisted pair interface	V_{DD_AH}	2.38	2.50	2.62	V
Power supply voltage for Enhanced SerDes interface, 1.0 V(1)	V_{DD_VS}	0.95	1.00	1.05	V
Power supply voltage for Enhanced SerDes interface, 1.2 V	V_{DD_VS}	1.14	1.20	1.26	V
Power supply voltage for MIIM and miscellaneous I/O	V_{DD_IO}	2.38	2.50	2.62	V
VSC7420-02, VSC7421-02, and VSC7422-02 operating temperature(2)	T	0		125	°C
VSC7420-04, VSC7421-04, and VSC7422-04 operating temperature(2)	T	–40		125	°C

1. The 1.0 V power supply for the enhanced SerDes interface is enabled in HSIO::SERDES6G_OB_CFG.OB_ENA1V_MODE.
2. Minimum specification is ambient temperature, and the maximum is junction temperature.

8.5 Stress Ratings

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 601 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{DD}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{DD_A}	–0.3	1.10	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AL}	–0.3	1.10	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AH}	–0.3	2.75	V
Power supply voltage for Enhanced SerDes interface	V_{DD_VS}	–0.3	1.32	V
Power supply voltage for MIIM and miscellaneous I/O	V_{DD_IO}	–0.3	2.75	V
Storage temperature	T_S	–55	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–500	500	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	–1750	1750	V

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

9 Pin Descriptions for VSC7420XJQ-02

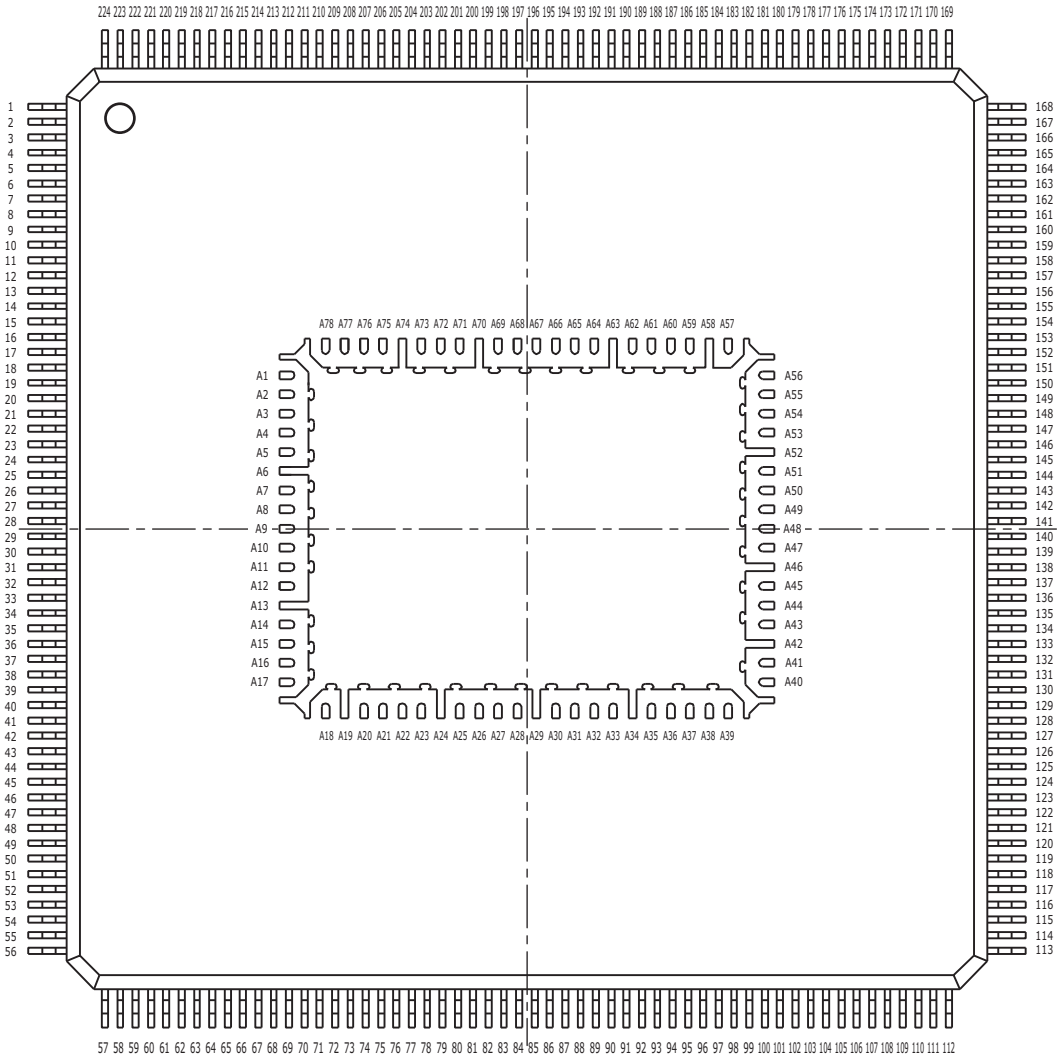
The VSC7420XJQ-02 device has 302 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

9.1 Pin Diagram for VSC7420XJQ-02

The following illustration shows the pin diagram for the VSC7420XJQ-02 device, as seen from the top view looking through the device.

Figure 70 • **Pin Diagram for VSC7420XJQ-02**



9.2 Pins by Function for VSC7420XJQ-02

This section contains the functional pin descriptions for the VSC7420XJQ-02 device. The following table lists the definitions for the pin type symbols.

Table 602 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

9.2.1 Analog Bias Signals

The following table lists the pins associated with the analog bias signals.

Table 603 • **Analog Bias Pins**

Name	Type	Description
SerDes_Rext_[1:0]	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Ref_filt_[2:0]	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Ref_rext_[2:0]	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.

9.2.2 Clock Circuits

The following table lists the pins associated with the system clock interface.

Table 604 • **System Clock Interface Pins**

Name	Type	Description
RefClk_Sel[2:0]	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to V_{DD_IO}. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
RefClk_P RefClk_N	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to V_{DD_A}. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.

9.2.3 General-Purpose Inputs and Outputs

The following table lists the pins associated with general-purpose inputs and outputs. The GPIO pins have an alternate function signal, which is mapped out in the following table. The overlaid functions are selected by software on a pin-by-pin basis. The MIIM slave interface is enabled depending on the VCORE_CFG settings and override the normal GPIO and alternate functions.

Table 605 • **GPIO Pin Mapping**

Name	Overlaid Function 1	Type	MIIM Slave Interface
GPIO_0	SIO_CLK	I/O, PU, ST, 3V	
GPIO_1	SIO_LD	I/O, PU, ST, 3V	
GPIO_2	SIO_DO	I/O, PU, ST, 3V	
GPIO_3	SIO_DI	I/O, PU, ST, 3V	
GPIO_4	TACHO	I/O, PU, ST, 3V	
GPIO_5	TWI_SCL	I/O, PU, ST, 3V	
GPIO_6	TWI_SDA	I/O, PU, ST, 3V	
GPIO_7	None	I/O, PU, ST, 3V	
GPIO_8	EXT_IRQ0	I/O, PU, ST, 3V	
GPIO_15	None	I/O, PU, ST, 3V	SLV_MDC
GPIO_16	None	I/O, PU, ST, 3V	SLV_MDIO
GPIO_29	PWM	I/O, PU, ST, 3V	

Table 605 • **GPIO Pin Mapping *(continued)***

Name	Overlaid Function 1	Type	MIIM Slave Interface
GPIO_30	UART_TX	I/O, PU, ST, 3V	
GPIO_31	UART_RX	I/O, PU, ST, 3V	

9.2.4 JTAG Interface

The following table lists the pins associated with the JTAG interface. The JTAG interface can be connected to the boundary scan TAP controller.

The JTAG signals are not 5 V tolerant.

Table 606 • **JTAG Interface Pins**

Name	Type	Description
JTAG_nTRST	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
JTAG_CLK	I, PU, ST, 3V	JTAG clock.
JTAG_TDI	I, PU, ST, 3V	JTAG test data in.
JTAG_TDO	OZ, 3V	JTAG test data out.
JTAG_TMS	I, PU, ST, 3V	JTAG test mode select.

9.2.5 MII Management Interface

The following table lists the pins associated with the MII Management interface.

Table 607 • **MII Management Interface Pins**

Name	Type	Description
MDIO	I/O, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
MDC	O, 3V	Management data clock. MDC is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.

9.2.6 Miscellaneous Signals

The following table lists the pins associated with a particular interface or facility on the device.

Table 608 • **Miscellaneous Pins**

Name	Type	Description
nReset	I, PD, ST, 3V	Global device reset, active low.

Table 608 • **Miscellaneous Pins *(continued)***

Name	Type	Description
COMA_MODE	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
VCORE_CFG[2:0]	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
EXT_IRQ0(1)	I/O PD, 3V	This pin interrupts inputs or outputs to the internal VCore-Ie CPU system or to an external processor. Signal polarity is programmable. See Figure 6, page 26.
Reserved_[5:8] Reserved_29	I, PD, ST, 3V	Tie to V_{DD_IO}.
Reserved_4	I, PD, ST, 3V	Tie to V_{SS}.
Reserved_[10:15] Reserved_[17:18] Reserved_[22:24] Reserved_[50:81] Reserved_[124:127] Reserved_[136:139]	I, PD, ST, 3V	Leave floating.

1. Available as an alternate function on the GPIO_8 pin.

9.2.7 Power Supplies and Ground

The following table lists the power supply and ground pins.

Table 609 • **Power Supply and Ground Pins**

Name	Type	Description
VDD	Power	1.0 V power supply voltage for core
VDD_A	Power	1.0 V power supply voltage for analog circuits
VDD_AL	Power	1.0 V power supply voltage for analog circuits for twisted pair interface
VDD_AH	Power	2.5 V power supply voltage for analog driver in twisted pair interface
VDD_IO	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os
VDD_VS	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface
VSS	Ground	Ground reference

9.2.8 Serial CPU Interface

The serial CPU interface (SI) can be used as a serial slave, master, or boot interface.

As a slave interface, it allows external CPUs to access internal registers. As a master interface, it allows the device to access external devices using a programmable protocol. The serial CPU interface also allows the internal VCore-Ie CPU system to boot from an attached serial memory device when the VCORE_CFG signals are set appropriately.

The following table lists the pins associated with the serial CPU interface (SI).

Table 610 • **Serial CPU Interface Pins**

Name	Type	Description
SI_Clk	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
SI_DI	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
SI_DO	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
SI_nEn	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.

9.2.9 Enhanced SerDes Interface

The following pins are associated with the Enhanced SerDes interface.

Table 611 • **Enhanced SerDes Interface Pins**

Name	Type	Description
SerDes_E[1:0]_RxP, N SerDes_E[1:0]_RxP, N	I, Diff, TD	Differential Enhanced SerDes data inputs.
SerDes_E[1:0]_TxP, N SerDes_E[1:0]_TxP, N	O, Diff	Differential Enhanced SerDes data outputs.

9.2.10 Twisted Pair Interface

The following pins are associated with the twisted pair interface. The PHYn_LED[1:0] LED control signals associated with the twisted pair interfaces are alternate functions on the GPIOs. For more information about the GPIO pin mapping, see Table 605, page 439.

Table 612 • **Twisted Pair Interface Pins**

Name	Type	Description
P0_D0P P1_D0P P2_D0P P3_D0P P4_D0P P5_D0P P6_D0P P7_D0P	A_{DIFF}	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Table 612 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D0N P1_D0N P2_D0N P3_D0N P4_D0N P5_D0N P6_D0N P7_D0N	A_{DIFF}	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
P0_D1P P1_D1P P2_D1P P3_D1P P4_D1P P5_D1P P6_D1P P7_D1P	A_{DIFF}	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
P0_D1N P1_D1N P2_D1N P3_D1N P4_D1N P5_D1N P6_D1N P7_D1N	A_{DIFF}	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
P0_D2P P1_D2P P2_D2P P3_D2P P4_D2P P5_D2P P6_D2P P7_D2P	A_{DIFF}	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
P0_D2N P1_D2N P2_D2N P3_D2N P4_D2N P5_D2N P6_D2N P7_D2N	A_{DIFF}	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
P0_D3P P1_D3P P2_D3P P3_D3P P4_D3P P5_D3P P6_D3P P7_D3P	A_{DIFF}	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Table 612 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D3N P1_D3N P2_D3N P3_D3N P4_D3N P5_D3N P6_D3N P7_D3N	A_{DIFF}	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

9.3 Pins by Number for VSC7420XJQ-02

This section provides a numeric list of the VSC7420XJQ-02 pins.

1	VDD_AL_1
2	Reserved_50
3	Reserved_51
4	Reserved_52
5	Reserved_53
6	Reserved_54
7	Reserved_55
8	Reserved_56
9	Reserved_57
10	Reserved_58
11	Reserved_59
12	Reserved_60
13	Reserved_61
14	Reserved_62
15	Reserved_63
16	Reserved_64
17	Reserved_65
18	Ref_filt_2
19	Ref_rext_2
20	VDD_AL_2
21	Reserved_66
22	Reserved_67
23	Reserved_68
24	Reserved_69
25	Reserved_70
26	Reserved_71
27	Reserved_72
28	Reserved_73
29	Reserved_74
30	Reserved_75
31	Reserved_76
32	Reserved_77
33	Reserved_78
34	Reserved_79
35	Reserved_80
36	Reserved_81
37	VDD_AL_3
38	GPIO_31
39	VDD_IO_1
40	GPIO_29
41	GPIO_16
42	GPIO_15
43	GPIO_8
44	GPIO_7
45	GPIO_5
46	GPIO_4
47	GPIO_3
48	SI_DO
49	GPIO_1
50	GPIO_0
51	SI_nEn
52	SI_DI
53	SI_Clk
54	MDC
55	MDIO
56	VDD_IO_2
57	VDD_1
58	VDD_2
59	VDD_3
60	VDD_A_1
61	VDD_VS_1
62	VDD_VS_2
63	VDD_A_2
64	VDD_A_3
65	Reserved_23
66	Reserved_22
67	VDD_IO_3
68	VDD_A_4
69	RefClk_N
70	RefClk_P
71	VDD_A_5
72	VDD_A_6
73	VDD_VS_3
74	VDD_A_7
75	VDD_VS_4
76	VDD_4
77	VDD_5
78	VDD_6
79	VDD_VS_5
80	VDD_A_8
81	VDD_VS_6
82	VDD_A_9
83	VDD_IO_4
84	VDD_VS_7
85	VDD_A_10
86	VDD_7
87	VDD_8
88	VDD_9
89	VDD_10
90	VDD_11
91	VDD_A_11
92	VDD_VS_8
93	VDD_A_12
94	VDD_VS_9
95	VDD_A_13
96	VDD_VS_10
97	VDD_VS_11
98	VDD_A_14
99	VDD_12
100	VDD_13
101	VDD_14
102	VDD_15
103	VDD_VS_12
104	VDD_A_15
105	VDD_16
106	SerDes_Rext_0
107	SerDes_Rext_1
108	VDD_IO_5
109	VDD_17
110	VDD_18

Pins by number *(continued)*

111 VDD_19	150 P2_D3N	189 P5_D1N
112 VDD_20	151 P2_D3P	190 P5_D1P
113 VDD_21	152 P2_D2N	191 P5_D0N
114 VDD_22	153 P2_D2P	192 P5_D0P
115 VDD_23	154 P2_D1N	193 Ref_filt_1
116 VDD_24	155 P2_D1P	194 Ref_rext_1
117 VDD_25	156 P2_D0N	195 P6_D3N
118 VDD_26	157 P2_D0P	196 P6_D3P
119 VDD_27	158 P3_D3N	197 P6_D2N
120 VDD_28	159 P3_D3P	198 P6_D2P
121 VDD_29	160 VDD_AL_10	199 P6_D1N
122 VDD_30	161 P3_D2N	200 P6_D1P
123 VDD_31	162 P3_D2P	201 VDD_AL_12
124 VDD_32	163 P3_D1N	202 P6_D0N
125 VDD_33	164 P3_D1P	203 P6_D0P
126 VDD_AL_4	165 P3_D0N	204 P7_D3N
127 VDD_AL_5	166 P3_D0P	205 P7_D3P
128 VDD_AL_6	167 Reserved_5	206 P7_D2N
129 VDD_AL_7	168 Reserved_6	207 P7_D2P
130 VDD_AL_8	169 Reserved_7	208 P7_D1N
131 P0_D3N	170 Reserved_8	209 P7_D1P
132 P0_D3P	171 JTAG_TRST	210 P7_D0N
133 VDD_AL_9	172 JTAG_DO	211 P7_D0P
134 P0_D2N	173 JTAG_TMS	212 Reserved_12
135 P0_D2P	174 JTAG_DI	213 Reserved_13
136 P0_D1N	175 JTAG_CLK	214 COMA_MODE
137 P0_D1P	176 P4_D3N	215 RefClk_Sel2
138 P0_D0N	177 P4_D3P	216 RefClk_Sel0
139 P0_D0P	178 P4_D2N	217 RefClk_Sel1
140 P1_D3N	179 P4_D2P	218 Reserved_4
141 P1_D3P	180 P4_D1N	219 Reserved_29
142 P1_D2N	181 P4_D1P	220 VCORE_CFG2
143 P1_D2P	182 P4_D0N	221 VCORE_CFG1
144 P1_D1N	183 VDD_AL_11	222 VCORE_CFG0
145 P1_D1P	184 P4_D0P	223 VDD_IO_21
146 P1_D0N	185 P5_D3N	224 nRESET
147 P1_D0P	186 P5_D3P	A1 Reserved_15
148 Ref_filt_0	187 P5_D2N	A2 VDD_AH_1
149 Ref_rext_0	188 P5_D2P	A3 VDD_AH_2

Pins by number *(continued)*

A4	VDD_AH_3
A5	VDD_AH_4
A6	VSS_1
A7	VDD_AH_5
A8	VDD_AH_6
A9	VDD_AH_7
A10	VDD_34
A11	Reserved_24
A12	GPIO_30
A13	VSS_2
A14	GPIO_6
A15	GPIO_2
A16	Reserved_18
A17	Reserved_17
A18	VSS_163
A19	VSS_3
A20	Reserved_139
A21	Reserved_138
A22	Reserved_137
A23	Reserved_136
A24	VSS_4
A25	Reserved_127
A26	Reserved_126
A27	Reserved_125
A28	Reserved_124
A29	VSS_5
A30	SerDes_E1_RxP
A31	SerDes_E1_RxN
A32	SerDes_E1_TxP
A33	SerDes_E1_TxN
A34	VSS_6
A35	SerDes_E0_TxN
A36	SerDes_E0_TxP
A37	SerDes_E0_RxN
A38	SerDes_E0_RxP
A39	VSS_7
A40	VSS_8
A41	VSS_9
A42	VSS_10
A43	VDD_35
A44	VDD_36
A45	VDD_37
A46	VSS_11
A47	VDD_AH_8
A48	VDD_AH_9
A49	VDD_AH_10
A50	VDD_AH_11
A51	VDD_AH_12
A52	VSS_12
A53	VDD_AH_13
A54	VDD_AH_14
A55	VDD_AH_15
A56	Reserved_10
A57	Reserved_11
A58	VSS_13
A59	VDD_IO_6
A60	VDD_IO_7
A61	VDD_38
A62	VDD_39
A63	VSS_14
A64	VDD_AH_16
A65	VDD_AH_17
A66	VDD_AH_18
A67	VDD_AH_19
A68	VDD_AH_20
A69	VDD_AH_21
A70	VSS_15
A71	VDD_IO_8
A72	VDD_40
A73	VDD_41
A74	VSS_16
A75	VDD_IO_9
A76	VDD_IO_10
A77	VDD_IO_11
A78	Reserved_14

9.4 Pins by Name for VSC7420XJQ-02

This section provides an alphabetical list of the VSC7420XJQ-02 pins.

COMA_MODE	214
GPIO_0	50
GPIO_1	49
GPIO_2	A15
GPIO_3	47
GPIO_4	46
GPIO_5	45
GPIO_6	A14
GPIO_7	44
GPIO_8	43
GPIO_15	42
GPIO_16	41
GPIO_29	40
GPIO_30	A12
GPIO_31	38
JTAG_CLK	175
JTAG_DI	174
JTAG_DO	172
JTAG_TMS	173
JTAG_TRST	171
MDC	54
MDIO	55
nRESET	224
P0_D0N	138
P0_D0P	139
P0_D1N	136
P0_D1P	137
P0_D2N	134
P0_D2P	135
P0_D3N	131
P0_D3P	132
P1_D0N	146
P1_D0P	147
P1_D1N	144
P1_D1P	145
P1_D2N	142
P1_D2P	143
P1_D3N	140
P1_D3P	141
P2_D0N	156
P2_D0P	157
P2_D1N	154
P2_D1P	155
P2_D2N	152
P2_D2P	153
P2_D3N	150
P2_D3P	151
P3_D0N	165
P3_D0P	166
P3_D1N	163
P3_D1P	164
P3_D2N	161
P3_D2P	162
P3_D3N	158
P3_D3P	159
P4_D0N	182
P4_D0P	184
P4_D1N	180
P4_D1P	181
P4_D2N	178
P4_D2P	179
P4_D3N	176
P4_D3P	177
P5_D0N	191
P5_D0P	192
P5_D1N	189
P5_D1P	190
P5_D2N	187
P5_D2P	188
P5_D3N	185
P5_D3P	186
P6_D0N	202
P6_D0P	203
P6_D1N	199
P6_D1P	200
P6_D2N	197
P6_D2P	198
P6_D3N	195
P6_D3P	196
P7_D0N	210
P7_D0P	211
P7_D1N	208
P7_D1P	209
P7_D2N	206
P7_D2P	207
P7_D3N	204
P7_D3P	205
Ref_filt_0	148
Ref_filt_1	193
Ref_filt_2	18
Ref_rext_0	149
Ref_rext_1	194
Ref_rext_2	19
RefClk_N	69
RefClk_P	70
RefClk_Sel0	216
RefClk_Sel1	217
RefClk_Sel2	215
Reserved_4	218
Reserved_5	167
Reserved_6	168
Reserved_7	169
Reserved_8	170
Reserved_10	A56
Reserved_11	A57
Reserved_12	212
Reserved_13	213
Reserved_14	A78
Reserved_15	A1
Reserved_17	A17

Pins by name *(continued)*

Reserved_18	A16
Reserved_22	66
Reserved_23	65
Reserved_24	A11
Reserved_29	219
Reserved_50	2
Reserved_51	3
Reserved_52	4
Reserved_53	5
Reserved_54	6
Reserved_55	7
Reserved_56	8
Reserved_57	9
Reserved_58	10
Reserved_59	11
Reserved_60	12
Reserved_61	13
Reserved_62	14
Reserved_63	15
Reserved_64	16
Reserved_65	17
Reserved_66	21
Reserved_67	22
Reserved_68	23
Reserved_69	24
Reserved_70	25
Reserved_71	26
Reserved_72	27
Reserved_73	28
Reserved_74	29
Reserved_75	30
Reserved_76	31
Reserved_77	32
Reserved_78	33
Reserved_79	34
Reserved_80	35
Reserved_81	36
Reserved_124	A28
Reserved_125	A27

Reserved_126	A26
Reserved_127	A25
Reserved_136	A23
Reserved_137	A22
Reserved_138	A21
Reserved_139	A20
SerDes_E0_RxN	A37
SerDes_E0_RxP	A38
SerDes_E0_TxN	A35
SerDes_E0_TxP	A36
SerDes_E1_RxN	A31
SerDes_E1_RxP	A30
SerDes_E1_TxN	A33
SerDes_E1_TxP	A32
SerDes_Rext_0	106
SerDes_Rext_1	107
SI_Clk	53
SI_DI	52
SI_DO	48
SI_nEn	51
VCORE_CFG0	222
VCORE_CFG1	221
VCORE_CFG2	220
VDD_1	57
VDD_2	58
VDD_3	59
VDD_4	76
VDD_5	77
VDD_6	78
VDD_7	86
VDD_8	87
VDD_9	88
VDD_10	89
VDD_11	90
VDD_12	99
VDD_13	100
VDD_14	101
VDD_15	102
VDD_16	105

VDD_17	109
VDD_18	110
VDD_19	111
VDD_20	112
VDD_21	113
VDD_22	114
VDD_23	115
VDD_24	116
VDD_25	117
VDD_26	118
VDD_27	119
VDD_28	120
VDD_29	121
VDD_30	122
VDD_31	123
VDD_32	124
VDD_33	125
VDD_34	A10
VDD_35	A43
VDD_36	A44
VDD_37	A45
VDD_38	A61
VDD_39	A62
VDD_40	A72
VDD_41	A73
VDD_A_1	60
VDD_A_2	63
VDD_A_3	64
VDD_A_4	68
VDD_A_5	71
VDD_A_6	72
VDD_A_7	74
VDD_A_8	80
VDD_A_9	82
VDD_A_10	85
VDD_A_11	91
VDD_A_12	93
VDD_A_13	95
VDD_A_14	98

Pins by name *(continued)*

VDD_A_15	104
VDD_AH_1	A2
VDD_AH_2	A3
VDD_AH_3	A4
VDD_AH_4	A5
VDD_AH_5	A7
VDD_AH_6	A8
VDD_AH_7	A9
VDD_AH_8	A47
VDD_AH_9	A48
VDD_AH_10	A49
VDD_AH_11	A50
VDD_AH_12	A51
VDD_AH_13	A53
VDD_AH_14	A54
VDD_AH_15	A55
VDD_AH_16	A64
VDD_AH_17	A65
VDD_AH_18	A66
VDD_AH_19	A67
VDD_AH_20	A68
VDD_AH_21	A69
VDD_AL_1	1
VDD_AL_2	20
VDD_AL_3	37
VDD_AL_4	126
VDD_AL_5	127
VDD_AL_6	128
VDD_AL_7	129
VDD_AL_8	130
VDD_AL_9	133
VDD_AL_10	160
VDD_AL_11	183
VDD_AL_12	201
VDD_IO_1	39
VDD_IO_2	56
VDD_IO_3	67
VDD_IO_4	83
VDD_IO_5	108
VDD_IO_6	A59
VDD_IO_7	A60
VDD_IO_8	A71
VDD_IO_9	A75
VDD_IO_10	A76
VDD_IO_11	A77
VDD_IO_21	223
VDD_VS_1	61
VDD_VS_2	62
VDD_VS_3	73
VDD_VS_4	75
VDD_VS_5	79
VDD_VS_6	81
VDD_VS_7	84
VDD_VS_8	92
VDD_VS_9	94
VDD_VS_10	96
VDD_VS_11	97
VDD_VS_12	103
VSS_1	A6
VSS_2	A13
VSS_3	A19
VSS_4	A24
VSS_5	A29
VSS_6	A34
VSS_7	A39
VSS_8	A40
VSS_9	A41
VSS_10	A42
VSS_11	A46
VSS_12	A52
VSS_13	A58
VSS_14	A63
VSS_15	A70
VSS_16	A74
VSS_163	A18

10 Pin Descriptions for VSC7420XJG-02

The VSC7420XJG-02 device has 672 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

10.1 Pin Identifications

The following table lists the definitions for the pin type symbols.

Table 613 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

10.2 Pin Diagram for VSC7420XJG-02

The following illustration shows the pin diagram for the VSC7420XJG-02 device, as seen from the top view looking through the device. For clarity, the device is shown in two halves, the top left and top right.

Figure 71 • **VSC7420XJG-02 Pin Diagram, Top Left**

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	#N/A	RESERVED_57	RESERVED_55	RESERVED_53	RESERVED_51	P7_D0P	P7_D1P	P7_D2P	P7_D3P	P6_D0P	P6_D1P	P6_D2P	P6_D3P
B	VSS_1	RESERVED_56	RESERVED_54	RESERVED_52	RESERVED_50	P7_D0N	P7_D1N	P7_D2N	P7_D3N	P6_D0N	P6_D1N	P6_D2N	P6_D3N
C	RESERVED_59	RESERVED_58	COMA_MODE	NRESET	VDD_IO_21	VSS_178	VCORE_CFG0	VCORE_CFG1	VCORE_CFG2	RESERVED_29	RESERVED_4	REFCLK_SEL0	REFCLK_SEL1
D	RESERVED_61	RESERVED_60	RESERVED_205	VDD_AH_1	VDD_AH_2	RESERVED_206	RESERVED_207	RESERVED_208	RESERVED_209	RESERVED_248	VDD_AH_4	RESERVED_211	RESERVED_13
E	RESERVED_63	RESERVED_62	RESERVED_216	VDD_AH_7	VDD_AH_8	VDD_IO_1	VDD_IO_2	VDD_AH_9	VDD_AL_1	VDD_AL_2	VDD_AH_10	VDD_AH_11	REF_REXT_1
F	RESERVED_65	RESERVED_64	RESERVED_218	VDD_AH_17	VDD_AH_18	VDD_IO_5	VDD_AH_3	VDD_AH_19	VDD_AL_5	VDD_AL_6	VDD_AH_20	VDD_AH_21	RESERVED_219
G	RESERVED_67	RESERVED_66	VSS_3	RESERVED_15	VSS_4	VDD_1	VDD_2	VDD_3	VDD_AL_9	VDD_AL_10	VDD_4	VDD_5	RESERVED_247
H	RESERVED_69	RESERVED_68	VSS_7	RESERVED_14	VSS_8	VDD_11	VDD_12	VDD_13	VDD_14	VDD_15	VDD_16	VDD_17	RESERVED_246
J	RESERVED_71	RESERVED_70	VDD_AH_27	VDD_AH_28	VDD_AL_13	VDD_AL_14	VDD_AL_15	RESERVED_240	RESERVED_241	RESERVED_242	RESERVED_243	RESERVED_244	RESERVED_245
K	RESERVED_73	RESERVED_72	VSS_11	REF_REXT_2	VDD_AL_19	VDD_AL_20	VDD_AL_21	VSS_12	VSS_13	VSS_14	VSS_15	VSS_16	VSS_17
L	RESERVED_75	RESERVED_74	VSS_25	REF_FILT_2	VSS_26	VDD_25	VDD_26	VSS_27	VSS_28	VSS_29	VSS_30	VSS_31	VSS_32
M	RESERVED_77	RESERVED_76	VDD_AH_31	VDD_AH_32	VDD_AH_33	VDD_29	VDD_30	VSS_41	VSS_42	VSS_43	VSS_44	VSS_45	VSS_46
N	RESERVED_79	RESERVED_78	VSS_53	VSS_54	VSS_55	VDD_33	VDD_34	VSS_56	VSS_57	VSS_58	VSS_59	VSS_60	VSS_61
P	RESERVED_81	RESERVED_80	VSS_71	RESERVED_24	VDD_IO_7	VDD_37	VDD_38	VSS_72	VSS_73	VSS_74	VSS_75	VSS_76	VSS_77
R	GPIO_31	GPIO_30	GPIO_29	RESERVED_190	VDD_IO_8	VDD_41	VDD_42	VSS_86	VSS_87	VSS_88	VSS_89	VSS_90	VSS_91
T	RESERVED_189	RESERVED_188	RESERVED_187	RESERVED_186	VDD_IO_9	VDD_45	VDD_46	VSS_98	VSS_99	VSS_100	VSS_101	VSS_102	VSS_103
U	RESERVED_99	RESERVED_98	RESERVED_41	RESERVED_40	VDD_IO_10	VSS_110	VSS_111	VSS_112	VSS_113	VSS_114	VSS_115	VSS_116	VSS_117
V	RESERVED_39	RESERVED_38	RESERVED_37	GPIO_16	VDD_IO_11	VDD_49	VDD_50	VDD_51	VDD_52	VDD_53	VDD_54	VDD_55	VDD_56
W	GPIO_15	RESERVED_36	RESERVED_35	RESERVED_34	VDD_IO_12	VDD_65	VDD_66	VDD_67	VDD_68	VDD_69	VDD_70	VDD_71	VDD_72
Y	RESERVED_33	RESERVED_32	RESERVED_31	GPIO_8	VDD_IO_13	RESERVED_146	RESERVED_141	REFCLK_P	RESERVED_137	RESERVED_134	RESERVED_129	VSS_126	RESERVED_126
AA	GPIO_7	GPIO_6	GPIO_5	GPIO_4	VDD_IO_14	RESERVED_147	RESERVED_140	REFCLK_N	RESERVED_136	RESERVED_135	RESERVED_128	VSS_145	RESERVED_127
AB	GPIO_3	GPIO_2	GPIO_1	GPIO_0	VDD_IO_15	VSS_129	VSS_130	VSS_131	VSS_132	VSS_133	VSS_134	VSS_135	VSS_136
AC	SI_DO	SI_NEN	VSS_148	VDD_IO_16	VDD_IO_17	VDD_A_1	VDD_A_2	VDD_A_3	VDD_A_4	VDD_A_5	VDD_A_6	VDD_A_7	VDD_A_8
AD	SI_CLK	SI_DI	RESERVED_18	VDD_IO_18	VSS_149	VDD_VS_1	VDD_VS_2	VDD_VS_3	VDD_VS_4	VDD_VS_5	VDD_VS_6	VDD_VS_7	VDD_VS_8
AE	VSS_151	RESERVED_17	VDD_IO_19	VSS_163	VSS_152	RESERVED_144	RESERVED_143	RESERVED_22	RESERVED_139	RESERVED_132	RESERVED_131	VSS_153	RESERVED_124
AF	#N/A	VDD_IO_20	MDIO	MDC	VSS_158	RESERVED_145	RESERVED_142	RESERVED_23	RESERVED_138	RESERVED_133	RESERVED_130	VSS_159	RESERVED_125

Figure 72 • **VSC7420XJG-02 Pin Diagram, Top Right**

14	15	16	17	18	19	20	21	22	23	24	25	26	
P5_D0P	P5_D1P	P5_D2P	P5_D3P	P4_D0P	P4_D1P	P4_D2P	P4_D3P	P3_D0P	P3_D1P	P3_D2P	P3_D3P	#N/A	A
P5_D0N	P5_D1N	P5_D2N	P5_D3N	P4_D0N	P4_D1N	P4_D2N	P4_D3N	P3_D0N	P3_D1N	P3_D2N	P3_D3N	VSS_2	B
REFCLK_SEL2	RESERVED_8	RESERVED_7	RESERVED_6	RESERVED_5	RESERVED_201	RESERVED_202	RESERVED_203	RESERVED_191	RESERVED_192	RESERVED_204	P2_D0N	P2_D0P	C
RESERVED_12	RESERVED_212	VDD_AH_5	JTAG_CLK	JTAG_DI	JTAG_DO	JTAG_TMS	JTAG_TRST	RESERVED_213	RESERVED_214	RESERVED_215	P2_D1N	P2_D1P	D
REF_FILT_1	VDD_AH_12	VDD_AH_13	VDD_AL_3	VDD_AL_4	VDD_AH_14	VDD_IO_3	VDD_IO_4	VDD_AH_15	VDD_AH_16	RESERVED_217	P2_D2N	P2_D2P	E
RESERVED_220	VDD_AH_22	VDD_AH_23	VDD_AL_7	VDD_AL_8	VDD_AH_24	VDD_AH_6	VDD_IO_6	VDD_AH_25	VDD_AH_26	RESERVED_221	P2_D3N	P2_D3P	F
RESERVED_223	VDD_6	VDD_7	VDD_AL_11	VDD_AL_12	VDD_8	VDD_9	VDD_10	VSS_5	RESERVED_10	VSS_6	P1_D0N	P1_D0P	G
RESERVED_225	VDD_18	VDD_19	VDD_20	VDD_21	VDD_22	VDD_23	VDD_24	VSS_9	RESERVED_11	VSS_10	P1_D1N	P1_D1P	H
RESERVED_232	RESERVED_233	RESERVED_234	RESERVED_235	RESERVED_236	RESERVED_237	VDD_AL_16	VDD_AL_17	VDD_AL_18	VDD_AH_29	VDD_AH_30	P1_D2N	P1_D2P	J
VSS_18	VSS_19	VSS_20	VSS_21	VSS_22	VSS_23	VDD_AL_22	VDD_AL_23	VDD_AL_24	REF_REXT_0	VSS_24	P1_D3N	P1_D3P	K
VSS_33	VSS_34	VSS_35	VSS_36	VSS_37	VSS_38	VDD_27	VDD_28	VSS_39	REF_FILT_0	VSS_40	P0_D0N	P0_D0P	L
VSS_47	VSS_48	VSS_49	VSS_50	VSS_51	VSS_52	VDD_31	VDD_32	VDD_AH_34	VDD_AH_35	VDD_AH_36	P0_D1N	P0_D1P	M
VSS_62	VSS_63	VSS_64	VSS_65	VSS_66	VSS_67	VDD_35	VDD_36	VSS_68	VSS_69	VSS_70	P0_D2N	P0_D2P	N
VSS_78	VSS_79	VSS_80	VSS_81	VSS_82	VSS_83	VDD_39	VDD_40	VSS_164	VSS_84	VSS_85	P0_D3N	P0_D3P	P
VSS_92	VSS_93	VSS_94	VSS_95	VSS_96	VSS_97	VDD_43	VDD_44	VSS_165	RESERVED_20	RESERVED_19	RESERVED_148	VSS_179	R
VSS_104	VSS_105	VSS_106	VSS_107	VSS_108	VSS_109	VDD_47	VDD_48	VSS_166	RESERVED_21	RESERVED_166	RESERVED_165	RESERVED_164	T
VSS_118	VSS_119	VSS_120	VSS_121	VSS_122	VSS_123	VSS_124	VSS_125	VSS_167	RESERVED_160	RESERVED_162	RESERVED_159	RESERVED_161	U
VDD_57	VDD_58	VDD_59	VDD_60	VDD_61	VDD_62	VDD_63	VDD_64	VSS_168	RESERVED_156	RESERVED_158	RESERVED_155	RESERVED_157	V
VDD_73	VDD_74	VDD_75	VDD_76	VDD_77	VDD_78	VDD_79	VDD_80	VSS_169	RESERVED_163	RESERVED_154	RESERVED_171	RESERVED_153	W
RESERVED_121	RESERVED_118	VSS_127	SERDES_E1_TXP	RESERVED_110	RESERVED_105	VSS_128	SERDES_E0_TXP	VSS_170	RESERVED_167	RESERVED_168	RESERVED_170	RESERVED_172	Y
RESERVED_120	RESERVED_119	VSS_146	SERDES_E1_TXN	RESERVED_111	RESERVED_104	VSS_147	SERDES_E0_TXN	VSS_171	RESERVED_173	RESERVED_169	RESERVED_150	RESERVED_151	AA
VSS_137	VSS_138	VSS_139	VSS_140	VSS_141	VSS_142	VSS_143	VSS_144	VSS_172	RESERVED_180	RESERVED_152	RESERVED_179	RESERVED_182	AB
VDD_A_9	VDD_A_10	VDD_A_11	VDD_A_12	VDD_A_13	VDD_A_14	VDD_A_15	VDD_A_16	VSS_173	RESERVED_178	RESERVED_181	RESERVED_184	RESERVED_177	AC
VDD_VS_9	VDD_VS_10	VDD_VS_11	VDD_VS_12	VDD_VS_13	VDD_VS_14	VDD_VS_15	VDD_VS_16	VSS_150	VSS_174	RESERVED_183	RESERVED_175	RESERVED_176	AD
RESERVED_123	RESERVED_116	VSS_154	SERDES_E1_RXP	RESERVED_108	RESERVED_107	VSS_155	SERDES_E0_RXP	SERDES_REXT_0	VSS_156	VSS_175	RESERVED_174	VSS_157	AE
RESERVED_122	RESERVED_117	VSS_160	SERDES_E1_RXN	RESERVED_109	RESERVED_106	VSS_161	SERDES_E0_RXN	SERDES_REXT_1	VSS_162	VSS_177	VSS_176	#N/A	AF

10.3 Pins by Function for VSC7420XJG-02

This section contains the functional pin descriptions for the VSC7420XJG-02 device.

Functional Group	Name	Number	Type	Description
Analog Bias	Ref_filt_0	L23	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_1	E14	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_2	L4	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_rext_0	K23	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	Ref_rext_1	E13	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	Ref_rext_2	K4	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	SerDes_Rext_0	AE22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Analog Bias	SerDes_Rext_1	AF22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Enhanced SerDes Interface	SerDes_E0_RxN	AF21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_RxP	AE21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_TxN	AA21	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E0_TxP	Y21	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E1_RxN	AF17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_RxP	AE17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_TxN	AA17	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E1_TxP	Y17	O, Diff	Differential Enhanced SerDes data outputs.
General Purpose I/O	GPIO_0	AB4	I/O, PU, ST, 3V	Overlaid function 1: SIO_CLK.
General Purpose I/O	GPIO_1	AB3	I/O, PU, ST, 3V	Overlaid function 1: SIO_LD.
General Purpose I/O	GPIO_2	AB2	I/O, PU, ST, 3V	Overlaid function 1: SIO_DO.
General Purpose I/O	GPIO_3	AB1	I/O, PU, ST, 3V	Overlaid function 1: SIO_DI.

General Purpose I/O	GPIO_4	AA4	I/O, PU, ST, 3V	Overlaid function 1: TACHO.
General Purpose I/O	GPIO_5	AA3	I/O, PU, ST, 3V	Overlaid function 1: TWI_SCL.
General Purpose I/O	GPIO_6	AA2	I/O, PU, ST, 3V	Overlaid function 1: TWI_SDA.
General Purpose I/O	GPIO_7	AA1	I/O, PU, ST, 3V	General-purpose input/output.
General Purpose I/O	GPIO_8	Y4	I/O, PU, ST, 3V	Overlaid function 1: EXT_IRQ0.
General Purpose I/O	GPIO_15	W1	I/O, PU, ST, 3V	MIIM slave interface: SLV_MDC.
General Purpose I/O	GPIO_16	V4	I/O, PU, ST, 3V	MIIM slave interface: SLV_MDIO.
General Purpose I/O	GPIO_29	R3	I/O, PU, ST, 3V	Overlaid function 1: PWM.
General Purpose I/O	GPIO_30	R2	I/O, PU, ST, 3V	Overlaid function 1: UART_TX.
General Purpose I/O	GPIO_31	R1	I/O, PU, ST, 3V	Overlaid function 1: UART_RX.
JTAG Interface	JTAG_CLK	D17	I, PU, ST, 3V	JTAG clock.
JTAG Interface	JTAG_DI	D18	I, PU, ST, 3V	JTAG test data in.
JTAG Interface	JTAG_DO	D19	OZ, 3V	JTAG test data out.
JTAG Interface	JTAG_TMS	D20	I, PU, ST, 3V	JTAG test mode select.
JTAG Interface	JTAG_TRST	D21	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
MII Management Interface	MDC	AF4	O, 3V	Management data clock. MDC is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.
MII Management Interface	MDIO	AF3	I/O, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
Miscellaneous	COMA_MODE	C3	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
Miscellaneous	nRESET	C4	I, PD, ST, 3V	Global device reset, active low.
Miscellaneous	VCORE_CFG0	C7	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.

Miscellaneous	VCORE_CFG1	C8	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Miscellaneous	VCORE_CFG2	C9	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Power Supply	VDD_1	G6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_2	G7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_3	G8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_4	G11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_5	G12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_6	G15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_7	G16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_8	G19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_9	G20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_10	G21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_11	H6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_12	H7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_13	H8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_14	H9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_15	H10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_16	H11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_17	H12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_18	H15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_19	H16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_20	H17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_21	H18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_22	H19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_23	H20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_24	H21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_25	L6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_26	L7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_27	L20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_28	L21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_29	M6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_30	M7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_31	M20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_32	M21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_33	N6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_34	N7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_35	N20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_36	N21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_37	P6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_38	P7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_39	P20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_40	P21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_41	R6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_42	R7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_43	R20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_44	R21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_45	T6	Power	1.0 V power supply voltage for core.

Power Supply	VDD_46	T7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_47	T20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_48	T21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_49	V6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_50	V7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_51	V8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_52	V9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_53	V10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_54	V11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_55	V12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_56	V13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_57	V14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_58	V15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_59	V16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_60	V17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_61	V18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_62	V19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_63	V20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_64	V21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_65	W6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_66	W7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_67	W8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_68	W9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_69	W10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_70	W11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_71	W12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_72	W13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_73	W14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_74	W15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_75	W16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_76	W17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_77	W18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_78	W19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_79	W20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_80	W21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_A_1	AC6	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_2	AC7	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_3	AC8	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_4	AC9	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_5	AC10	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_6	AC11	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_7	AC12	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_8	AC13	Power	1.0 V power supply voltage for analog circuits.

Power Supply	VDD_A_9	AC14	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_10	AC15	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_11	AC16	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_12	AC17	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_13	AC18	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_14	AC19	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_15	AC20	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_16	AC21	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_AH_1	D4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_2	D5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_3	F7	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_4	D11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_5	D16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_6	F20	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_7	E4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_8	E5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_9	E8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_10	E11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_11	E12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_12	E15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.

Power Supply	VDD_AH_13	E16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_14	E19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_15	E22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_16	E23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_17	F4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_18	F5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_19	F8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_20	F11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_21	F12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_22	F15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_23	F16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_24	F19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_25	F22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_26	F23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_27	J3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_28	J4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_29	J23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_30	J24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.

Power Supply	VDD_AH_31	M3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_32	M4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_33	M5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_34	M22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_35	M23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_36	M24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AL_1	E9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_2	E10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_3	E17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_4	E18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_5	F9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_6	F10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_7	F17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_8	F18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_9	G9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_10	G10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_11	G17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_12	G18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.

Power Supply	VDD_AL_13	J5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_14	J6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_15	J7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_16	J20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_17	J21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_18	J22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_19	K5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_20	K6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_21	K7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_22	K20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_23	K21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_24	K22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_IO_1	E6	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_2	E7	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_3	E20	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_4	E21	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_5	F6	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_6	F21	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.

Power Supply	VDD_IO_7	P5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_8	R5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_9	T5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_10	U5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_11	V5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_12	W5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_13	Y5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_14	AA5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_15	AB5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_16	AC4	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_17	AC5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_18	AD4	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_19	AE3	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_20	AF2	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_IO_21	C5	Power	2.5 V power supply for MII Management interface, and miscellaneous I/Os.
Power Supply	VDD_VS_1	AD6	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_2	AD7	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_3	AD8	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_4	AD9	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.

Power Supply	VDD_VS_5	AD10	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_6	AD11	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_7	AD12	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_8	AD13	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_9	AD14	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_10	AD15	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_11	AD16	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_12	AD17	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_13	AD18	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_14	AD19	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_15	AD20	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VDD_VS_16	AD21	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interface.
Power Supply	VSS_1	B1	Ground	Ground reference.
Power Supply	VSS_2	B26	Ground	Ground reference.
Power Supply	VSS_3	G3	Ground	Ground reference.
Power Supply	VSS_4	G5	Ground	Ground reference.
Power Supply	VSS_5	G22	Ground	Ground reference.
Power Supply	VSS_6	G24	Ground	Ground reference.
Power Supply	VSS_7	H3	Ground	Ground reference.
Power Supply	VSS_8	H5	Ground	Ground reference.
Power Supply	VSS_9	H22	Ground	Ground reference.
Power Supply	VSS_10	H24	Ground	Ground reference.
Power Supply	VSS_11	K3	Ground	Ground reference.
Power Supply	VSS_12	K8	Ground	Ground reference.
Power Supply	VSS_13	K9	Ground	Ground reference.
Power Supply	VSS_14	K10	Ground	Ground reference.
Power Supply	VSS_15	K11	Ground	Ground reference.
Power Supply	VSS_16	K12	Ground	Ground reference.
Power Supply	VSS_17	K13	Ground	Ground reference.
Power Supply	VSS_18	K14	Ground	Ground reference.
Power Supply	VSS_19	K15	Ground	Ground reference.
Power Supply	VSS_20	K16	Ground	Ground reference.
Power Supply	VSS_21	K17	Ground	Ground reference.
Power Supply	VSS_22	K18	Ground	Ground reference.
Power Supply	VSS_23	K19	Ground	Ground reference.
Power Supply	VSS_24	K24	Ground	Ground reference.
Power Supply	VSS_25	L3	Ground	Ground reference.
Power Supply	VSS_26	L5	Ground	Ground reference.
Power Supply	VSS_27	L8	Ground	Ground reference.
Power Supply	VSS_28	L9	Ground	Ground reference.

Power Supply	VSS_29	L10	Ground	Ground reference.
Power Supply	VSS_30	L11	Ground	Ground reference.
Power Supply	VSS_31	L12	Ground	Ground reference.
Power Supply	VSS_32	L13	Ground	Ground reference.
Power Supply	VSS_33	L14	Ground	Ground reference.
Power Supply	VSS_34	L15	Ground	Ground reference.
Power Supply	VSS_35	L16	Ground	Ground reference.
Power Supply	VSS_36	L17	Ground	Ground reference.
Power Supply	VSS_37	L18	Ground	Ground reference.
Power Supply	VSS_38	L19	Ground	Ground reference.
Power Supply	VSS_39	L22	Ground	Ground reference.
Power Supply	VSS_40	L24	Ground	Ground reference.
Power Supply	VSS_41	M8	Ground	Ground reference.
Power Supply	VSS_42	M9	Ground	Ground reference.
Power Supply	VSS_43	M10	Ground	Ground reference.
Power Supply	VSS_44	M11	Ground	Ground reference.
Power Supply	VSS_45	M12	Ground	Ground reference.
Power Supply	VSS_46	M13	Ground	Ground reference.
Power Supply	VSS_47	M14	Ground	Ground reference.
Power Supply	VSS_48	M15	Ground	Ground reference.
Power Supply	VSS_49	M16	Ground	Ground reference.
Power Supply	VSS_50	M17	Ground	Ground reference.
Power Supply	VSS_51	M18	Ground	Ground reference.
Power Supply	VSS_52	M19	Ground	Ground reference.
Power Supply	VSS_53	N3	Ground	Ground reference.
Power Supply	VSS_54	N4	Ground	Ground reference.
Power Supply	VSS_55	N5	Ground	Ground reference.
Power Supply	VSS_56	N8	Ground	Ground reference.
Power Supply	VSS_57	N9	Ground	Ground reference.
Power Supply	VSS_58	N10	Ground	Ground reference.
Power Supply	VSS_59	N11	Ground	Ground reference.
Power Supply	VSS_60	N12	Ground	Ground reference.
Power Supply	VSS_61	N13	Ground	Ground reference.
Power Supply	VSS_62	N14	Ground	Ground reference.
Power Supply	VSS_63	N15	Ground	Ground reference.
Power Supply	VSS_64	N16	Ground	Ground reference.
Power Supply	VSS_65	N17	Ground	Ground reference.
Power Supply	VSS_66	N18	Ground	Ground reference.
Power Supply	VSS_67	N19	Ground	Ground reference.
Power Supply	VSS_68	N22	Ground	Ground reference.
Power Supply	VSS_69	N23	Ground	Ground reference.
Power Supply	VSS_70	N24	Ground	Ground reference.
Power Supply	VSS_71	P3	Ground	Ground reference.
Power Supply	VSS_72	P8	Ground	Ground reference.
Power Supply	VSS_73	P9	Ground	Ground reference.
Power Supply	VSS_74	P10	Ground	Ground reference.
Power Supply	VSS_75	P11	Ground	Ground reference.
Power Supply	VSS_76	P12	Ground	Ground reference.
Power Supply	VSS_77	P13	Ground	Ground reference.
Power Supply	VSS_78	P14	Ground	Ground reference.

Power Supply	VSS_79	P15	Ground	Ground reference.
Power Supply	VSS_80	P16	Ground	Ground reference.
Power Supply	VSS_81	P17	Ground	Ground reference.
Power Supply	VSS_82	P18	Ground	Ground reference.
Power Supply	VSS_83	P19	Ground	Ground reference.
Power Supply	VSS_84	P23	Ground	Ground reference.
Power Supply	VSS_85	P24	Ground	Ground reference.
Power Supply	VSS_86	R8	Ground	Ground reference.
Power Supply	VSS_87	R9	Ground	Ground reference.
Power Supply	VSS_88	R10	Ground	Ground reference.
Power Supply	VSS_89	R11	Ground	Ground reference.
Power Supply	VSS_90	R12	Ground	Ground reference.
Power Supply	VSS_91	R13	Ground	Ground reference.
Power Supply	VSS_92	R14	Ground	Ground reference.
Power Supply	VSS_93	R15	Ground	Ground reference.
Power Supply	VSS_94	R16	Ground	Ground reference.
Power Supply	VSS_95	R17	Ground	Ground reference.
Power Supply	VSS_96	R18	Ground	Ground reference.
Power Supply	VSS_97	R19	Ground	Ground reference.
Power Supply	VSS_98	T8	Ground	Ground reference.
Power Supply	VSS_99	T9	Ground	Ground reference.
Power Supply	VSS_100	T10	Ground	Ground reference.
Power Supply	VSS_101	T11	Ground	Ground reference.
Power Supply	VSS_102	T12	Ground	Ground reference.
Power Supply	VSS_103	T13	Ground	Ground reference.
Power Supply	VSS_104	T14	Ground	Ground reference.
Power Supply	VSS_105	T15	Ground	Ground reference.
Power Supply	VSS_106	T16	Ground	Ground reference.
Power Supply	VSS_107	T17	Ground	Ground reference.
Power Supply	VSS_108	T18	Ground	Ground reference.
Power Supply	VSS_109	T19	Ground	Ground reference.
Power Supply	VSS_110	U6	Ground	Ground reference.
Power Supply	VSS_111	U7	Ground	Ground reference.
Power Supply	VSS_112	U8	Ground	Ground reference.
Power Supply	VSS_113	U9	Ground	Ground reference.
Power Supply	VSS_114	U10	Ground	Ground reference.
Power Supply	VSS_115	U11	Ground	Ground reference.
Power Supply	VSS_116	U12	Ground	Ground reference.
Power Supply	VSS_117	U13	Ground	Ground reference.
Power Supply	VSS_118	U14	Ground	Ground reference.
Power Supply	VSS_119	U15	Ground	Ground reference.
Power Supply	VSS_120	U16	Ground	Ground reference.
Power Supply	VSS_121	U17	Ground	Ground reference.
Power Supply	VSS_122	U18	Ground	Ground reference.
Power Supply	VSS_123	U19	Ground	Ground reference.
Power Supply	VSS_124	U20	Ground	Ground reference.
Power Supply	VSS_125	U21	Ground	Ground reference.
Power Supply	VSS_126	Y12	Ground	Ground reference.
Power Supply	VSS_127	Y16	Ground	Ground reference.
Power Supply	VSS_128	Y20	Ground	Ground reference.

Power Supply	VSS_129	AB6	Ground	Ground reference.
Power Supply	VSS_130	AB7	Ground	Ground reference.
Power Supply	VSS_131	AB8	Ground	Ground reference.
Power Supply	VSS_132	AB9	Ground	Ground reference.
Power Supply	VSS_133	AB10	Ground	Ground reference.
Power Supply	VSS_134	AB11	Ground	Ground reference.
Power Supply	VSS_135	AB12	Ground	Ground reference.
Power Supply	VSS_136	AB13	Ground	Ground reference.
Power Supply	VSS_137	AB14	Ground	Ground reference.
Power Supply	VSS_138	AB15	Ground	Ground reference.
Power Supply	VSS_139	AB16	Ground	Ground reference.
Power Supply	VSS_140	AB17	Ground	Ground reference.
Power Supply	VSS_141	AB18	Ground	Ground reference.
Power Supply	VSS_142	AB19	Ground	Ground reference.
Power Supply	VSS_143	AB20	Ground	Ground reference.
Power Supply	VSS_144	AB21	Ground	Ground reference.
Power Supply	VSS_145	AA12	Ground	Ground reference.
Power Supply	VSS_146	AA16	Ground	Ground reference.
Power Supply	VSS_147	AA20	Ground	Ground reference.
Power Supply	VSS_148	AC3	Ground	Ground reference.
Power Supply	VSS_149	AD5	Ground	Ground reference.
Power Supply	VSS_150	AD22	Ground	Ground reference.
Power Supply	VSS_151	AE1	Ground	Ground reference.
Power Supply	VSS_152	AE5	Ground	Ground reference.
Power Supply	VSS_153	AE12	Ground	Ground reference.
Power Supply	VSS_154	AE16	Ground	Ground reference.
Power Supply	VSS_155	AE20	Ground	Ground reference.
Power Supply	VSS_156	AE23	Ground	Ground reference.
Power Supply	VSS_157	AE26	Ground	Ground reference.
Power Supply	VSS_158	AF5	Ground	Ground reference.
Power Supply	VSS_159	AF12	Ground	Ground reference.
Power Supply	VSS_160	AF16	Ground	Ground reference.
Power Supply	VSS_161	AF20	Ground	Ground reference.
Power Supply	VSS_162	AF23	Ground	Ground reference.
Power Supply	VSS_163	AE4	Ground	Ground reference.
Power Supply	VSS_164	P22	Ground	Ground reference.
Power Supply	VSS_165	R22	Ground	Ground reference.
Power Supply	VSS_166	T22	Ground	Ground reference.
Power Supply	VSS_167	U22	Ground	Ground reference.
Power Supply	VSS_168	V22	Ground	Ground reference.
Power Supply	VSS_169	W22	Ground	Ground reference.
Power Supply	VSS_170	Y22	Ground	Ground reference.
Power Supply	VSS_171	AA22	Ground	Ground reference.
Power Supply	VSS_172	AB22	Ground	Ground reference.
Power Supply	VSS_173	AC22	Ground	Ground reference.
Power Supply	VSS_174	AD23	Ground	Ground reference.
Power Supply	VSS_175	AE24	Ground	Ground reference.
Power Supply	VSS_176	AF25	Ground	Ground reference.
Power Supply	VSS_177	AF24	Ground	Ground reference.
Power Supply	VSS_178	C6	Ground	Ground reference.

Power Supply	VSS_179	R26	Ground	Ground reference.
Reserved	Reserved_4	C11	I, PD, ST, 3V	Tie to VSS.
Reserved	Reserved_5	C18	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_6	C17	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_7	C16	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_8	C15	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_10	G23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_11	H23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_12	D14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_13	D13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_14	H4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_15	G4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_17	AE2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_18	AD3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_19	R24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_20	R23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_21	T23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_22	AE8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_23	AF8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_24	P4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_29	C10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_31	Y3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_32	Y2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_33	Y1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_34	W4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_35	W3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_36	W2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_37	V3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_38	V2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_39	V1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_40	U4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_41	U3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_50	B5	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_51	A5	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_52	B4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_53	A4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_54	B3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_55	A3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_56	B2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_57	A2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_58	C2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_59	C1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_60	D2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_61	D1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_62	E2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_63	E1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_64	F2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_65	F1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_66	G2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_67	G1	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_68	H2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_69	H1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_70	J2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_71	J1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_72	K2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_73	K1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_74	L2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_75	L1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_76	M2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_77	M1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_78	N2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_79	N1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_80	P2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_81	P1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_98	U2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_99	U1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_104	AA19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_105	Y19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_106	AF19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_107	AE19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_108	AE18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_109	AF18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_110	Y18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_111	AA18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_116	AE15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_117	AF15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_118	Y15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_119	AA15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_120	AA14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_121	Y14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_122	AF14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_123	AE14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_124	AE13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_125	AF13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_126	Y13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_127	AA13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_128	AA11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_129	Y11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_130	AF11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_131	AE11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_132	AE10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_133	AF10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_134	Y10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_135	AA10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_136	AA9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_137	Y9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_138	AF9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_139	AE9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_140	AA7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_141	Y7	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_142	AF7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_143	AE7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_144	AE6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_145	AF6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_146	Y6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_147	AA6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_148	R25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_150	AA25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_151	AA26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_152	AB24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_153	W26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_154	W24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_155	V25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_156	V23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_157	V26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_158	V24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_159	U25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_160	U23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_161	U26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_162	U24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_163	W23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_164	T26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_165	T25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_166	T24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_167	Y23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_168	Y24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_169	AA24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_170	Y25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_171	W25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_172	Y26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_173	AA23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_174	AE25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_175	AD25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_176	AD26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_177	AC26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_178	AC23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_179	AB25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_180	AB23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_181	AC24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_182	AB26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_183	AD24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_184	AC25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_186	T4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_187	T3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_188	T2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_189	T1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_190	R4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_191	C22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_192	C23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_201	C19	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_202	C20	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_203	C21	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_204	C24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_205	D3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_206	D6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_207	D7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_208	D8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_209	D9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_211	D12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_212	D15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_213	D22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_214	D23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_215	D24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_216	E3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_217	E24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_218	F3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_219	F13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_220	F14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_221	F24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_223	G14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_225	H14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_232	J14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_233	J15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_234	J16	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_235	J17	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_236	J18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_237	J19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_240	J8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_241	J9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_242	J10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_243	J11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_244	J12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_245	J13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_246	H13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_247	G13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_248	D10	I, PD, ST, 3V	Leave floating.
Serial CPU Interface	SI_Clk	AD1	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
Serial CPU Interface	SI_DI	AD2	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.

Serial CPU Interface	SI_DO	AC1	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
Serial CPU Interface	SI_nEn	AC2	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.
System Clock Interface	RefClk_N	AA8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.
System Clock Interface	RefClk_P	Y8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.

System Clock Interface	RefClk_Sel0	C12	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
System Clock Interface	RefClk_Sel1	C13	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
System Clock Interface	RefClk_Sel2	C14	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
Twisted Pair Interface	P0_D0N	L25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P0_D0P	L26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P0_D1N	M25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P0_D1P	M26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P0_D2N	N25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D2P	N26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P0_D3N	P25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D3P	P26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D0N	G25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P1_D0P	G26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P1_D1N	H25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P1_D1P	H26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P1_D2N	J25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D2P	J26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D3N	K25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D3P	K26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P2_D0N	C25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P2_D0P	C26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P2_D1N	D25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P2_D1P	D26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P2_D2N	E25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P2_D2P	E26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D3N	F25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D3P	F26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D0N	B22	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P3_D0P	A22	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Twisted Pair Interface	P3_D1N	B23	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P3_D1P	A23	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P3_D2N	B24	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D2P	A24	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D3N	B25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P3_D3P	A25	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D0N	B18	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P4_D0P	A18	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P4_D1N	B19	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P4_D1P	A19	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.

Twisted Pair Interface	P4_D2N	B20	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D2P	A20	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D3N	B21	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D3P	A21	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D0N	B14	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P5_D0P	A14	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P5_D1N	B15	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P5_D1P	A15	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P5_D2N	B16	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D2P	A16	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P5_D3N	B17	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D3P	A17	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D0N	B10	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P6_D0P	A10	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P6_D1N	B11	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P6_D1P	A11	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P6_D2N	B12	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D2P	A12	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3N	B13	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3P	A13	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P7_D0N	B6	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P7_D0P	A6	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P7_D1N	B7	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P7_D1P	A7	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P7_D2N	B8	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P7_D2P	A8	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D3N	B9	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D3P	A9	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

11 Pin Descriptions for VSC7421XJQ-02

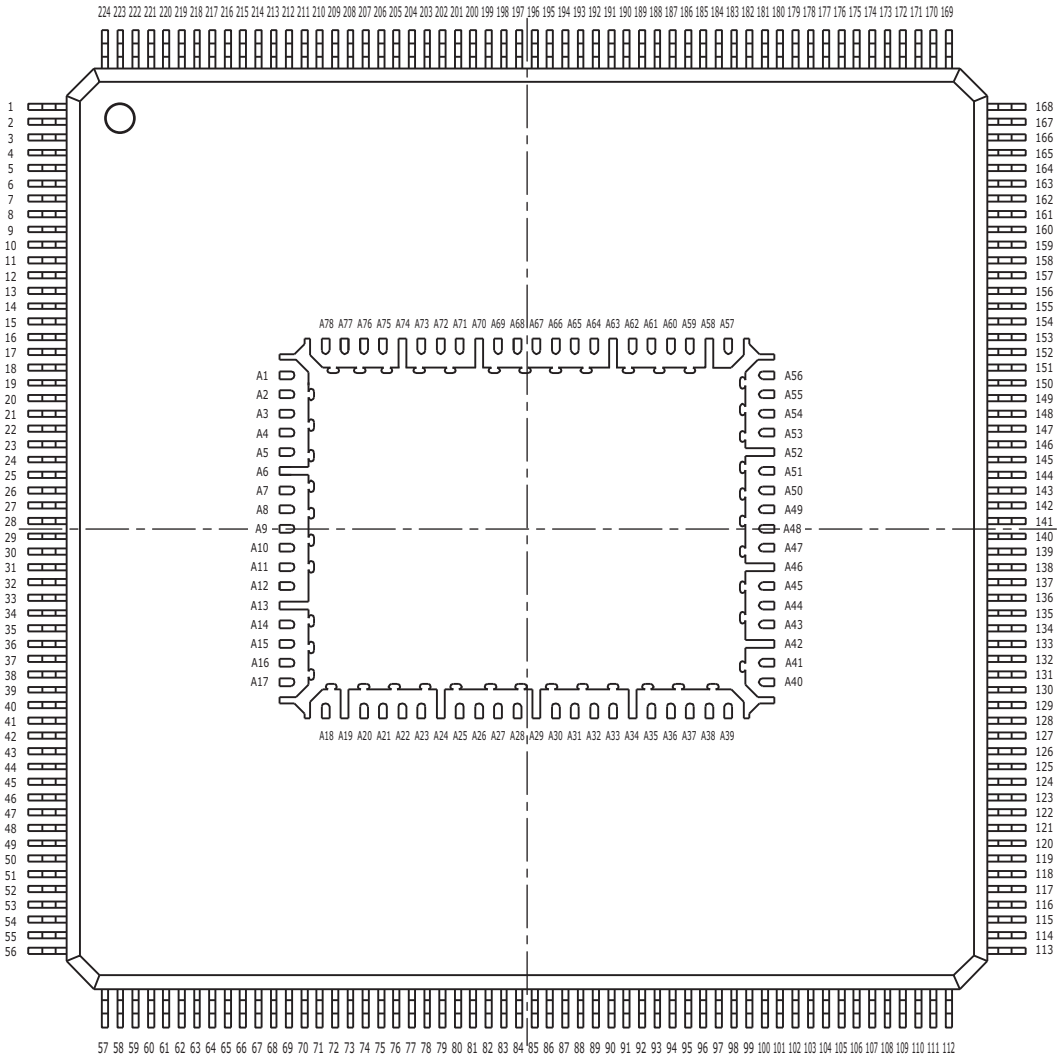
The VSC7421XJQ-02 device has 302 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

11.1 Pin Diagram for VSC7421XJQ-02

The following illustration shows the pin diagram for the VSC7421XJQ-02 device, as seen from the top view looking through the device.

Figure 73 • **Pin Diagram for VSC7421XJQ-02**



11.2 Pins by Function for VSC7421XJQ-02

This section contains the functional pin descriptions for the VSC7421XJQ-02 device. The following table lists the definitions for the pin type symbols.

Table 614 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

11.2.1 Analog Bias Signals

The following table lists the pins associated with the analog bias signals.

Table 615 • **Analog Bias Pins**

Name	Type	Description
SerDes_Rext_[1:0]	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Ref_filt_[2:0]	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Ref_rext_[2:0]	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.

11.2.2 Clock Circuits

The following table lists the pins associated with the system clock interface.

Table 616 • **System Clock Interface Pins**

Name	Type	Description
RefClk_Sel[2:0]	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to V_{DD_IO}. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
RefClk_P RefClk_N	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to V_{DD_A}. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.

11.2.3 General-Purpose Inputs and Outputs

The following table lists the pins associated with general-purpose inputs and outputs. The GPIO pins have an alternate function signal, which is mapped out in the following table. The overlaid functions are selected by software on a pin-by-pin basis. The MIIM slave interface is enabled depending on the VCORE_CFG settings and override the normal GPIO and alternate functions.

Table 617 • **GPIO Pin Mapping**

Name	Overlaid Function 1	Type	MIIM Slave Mode
GPIO_0	SIO_CLK	I/O, PU, ST, 3V	
GPIO_1	SIO_LD	I/O, PU, ST, 3V	
GPIO_2	SIO_DO	I/O, PU, ST, 3V	
GPIO_3	SIO_DI	I/O, PU, ST, 3V	
GPIO_4	TACHO	I/O, PU, ST, 3V	
GPIO_5	TWI_SCL	I/O, PU, ST, 3V	
GPIO_6	TWI_SDA	I/O, PU, ST, 3V	
GPIO_7	None	I/O, PU, ST, 3V	
GPIO_8	EXT_IRQ0	I/O, PU, ST, 3V	
GPIO_15	None	I/O, PU, ST, 3V	SLV_MDC
GPIO_16	None	I/O, PU, ST, 3V	SLV_MDIO

Table 617 • **GPIO Pin Mapping *(continued)***

Name	Overlaid Function 1	Type	MIIM Slave Mode
GPIO_29	PWM	I/O, PU, ST, 3V	
GPIO_30	UART_TX	I/O, PU, ST, 3V	
GPIO_31	UART_RX	I/O, PU, ST, 3V	

11.2.4 JTAG Interface

The following table lists the pins associated with the JTAG interface. The JTAG interface can be connected to the boundary scan TAP controller.

The JTAG signals are not 5 V tolerant.

Table 618 • **JTAG Interface Pins**

Name	Type	Description
JTAG_nTRST	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
JTAG_CLK	I, PU, ST, 3V	JTAG clock.
JTAG_TDI	I, PU, ST, 3V	JTAG test data in.
JTAG_TDO	OZ, 3V	JTAG test data out.
JTAG_TMS	I, PU, ST, 3V	JTAG test mode select.

11.2.5 MII Management Interface

The following table lists the pins associated with the MII Management interface.

Table 619 • **MII Management Interface Pins**

Name	Type	Description
MDIO	I/O	Management data input/output. MDIO is a bidirectional signal between a PHY and the device that transfers control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
MDC	O, 3V	Management data clock. MDC is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.

11.2.6 Miscellaneous Signals

The following table lists the pins associated with a particular interface or facility on the device.

Table 620 • **Miscellaneous Pins**

Name	Type	Description
nReset	I, PD, ST, 3V	Global device reset, active low.

Table 620 • **Miscellaneous Pins *(continued)***

Name	Type	Description
COMA_MODE	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
VCORE_CFG[2:0]	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
EXT_IRQ0(1)	I/O, PD, 3V	This pin interrupts inputs or outputs to the internal VCore-Ie CPU system or to an external processor. Signal polarity is programmable. See Figure 6, page 26.
Reserved_[6:8] Reserved_29	I, PD, ST, 3V	Tie to V_{DD_IO}.
Reserved_[4:5]	I, PD, ST, 3V	Tie to V_{SS}.
Reserved_[10:15] Reserved_[17:18] Reserved_[22:24]	I, PD, ST, 3V	Leave floating.

1. Available as an alternate function on the GPIO_8 pin.

11.2.7 Power Supplies and Ground

The following table lists the power supply and ground pins.

Table 621 • **Power Supply and Ground Pins**

Name	Type	Description
VDD	Power	1.0 V power supply voltage for core
VDD_A	Power	1.0 V power supply voltage for analog circuits
VDD_AL	Power	1.0 V power supply voltage for analog circuits for twisted pair interface
VDD_AH	Power	2.5 V power supply voltage for analog driver in twisted pair interface
VDD_IO	Power	2.5 V power supply for MII Management and miscellaneous I/Os
VDD_VS	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interfaces
VSS	Ground	Ground reference

11.2.8 Serial CPU Interface

The serial CPU interface (SI) can be used as a serial slave, master, or boot interface.

As a slave interface, it allows external CPUs to access internal registers. As a master interface, it allows the device to access external devices using a programmable protocol. The serial CPU interface also allows the internal VCore-Ie CPU system to boot from an attached serial memory device when the VCORE_CFG signals are set appropriately.

The following table lists the pins associated with the serial CPU interface (SI).

Table 622 • **Serial CPU Interface Pins**

Name	Type	Description
SI_Clk	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
SI_DI	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
SI_DO	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
SI_nEn	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.

11.2.9 Enhanced SerDes Interface

The following pins are associated with the Enhanced SerDes interface.

Table 623 • **Enhanced SerDes Interface Pins**

Name	Type	Description
SerDes_E[3:0]_RxP, N SerDes_E[3:0]_RxP, N	I, Diff, TD	Differential Enhanced SerDes data inputs.
SerDes_E[3:0]_TxP, N SerDes_E[3:0]_TxP, N	O, Diff	Differential Enhanced SerDes data outputs.

11.2.10 Twisted Pair Interface

The following pins are associated with the twisted pair interface. The PHYn_LED[1:0] LED control signals associated with the twisted pair interfaces are alternate functions on the GPIOs. For more information about the GPIO pin mapping, see Table 617, page 488.

Table 624 • **Twisted Pair Interface Pins**

Name	Type	Description
P0_D0P P1_D0P P2_D0P P3_D0P P4_D0P P5_D0P P6_D0P P7_D0P P8_D0P P9_D0P P10_D0P P11_D0P	A_{DIFF}	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Table 624 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D0N P1_D0N P2_D0N P3_D0N P4_D0N P5_D0N P6_D0N P7_D0N P8_D0N P9_D0N P10_D0N P11_D0N	A_{DIFF}	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
P0_D1P P1_D1P P2_D1P P3_D1P P4_D1P P5_D1P P6_D1P P7_D1P P8_D1P P9_D1P P10_D1P P11_D1P	A_{DIFF}	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
P0_D1N P1_D1N P2_D1N P3_D1N P4_D1N P5_D1N P6_D1N P7_D1N P8_D1N P9_D1N P10_D1N P11_D1N	A_{DIFF}	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
P0_D2P P1_D2P P2_D2P P3_D2P P4_D2P P5_D2P P6_D2P P7_D2P P8_D2P P9_D2P P10_D2P P11_D2P	A_{DIFF}	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Table 624 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D2N P1_D2N P2_D2N P3_D2N P4_D2N P5_D2N P6_D2N P7_D2N P8_D2N P9_D2N P10_D2N P11_D2N	A_{DIFF}	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
P0_D3P P1_D3P P2_D3P P3_D3P P4_D3P P5_D3P P6_D3P P7_D3P P8_D3P P9_D3P P10_D3P P11_D3P	A_{DIFF}	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
P0_D3N P1_D3N P2_D3N P3_D3N P4_D3N P5_D3N P6_D3N P7_D3N P8_D3N P9_D3N P10_D3N P11_D3N	A_{DIFF}	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

11.3 Pins by Number for VSC7421XJQ-02

This section provides a numeric list of the VSC7421XJQ-02 pins.

1	VDD_AL_1
2	P8_D3N
3	P8_D3P
4	P8_D2N
5	P8_D2P
6	P8_D1N
7	P8_D1P
8	P8_D0N
9	P8_D0P
10	P9_D3N
11	P9_D3P
12	P9_D2N
13	P9_D2P
14	P9_D1N
15	P9_D1P
16	P9_D0N
17	P9_D0P
18	Ref_filt_2
19	Ref_rext_2
20	VDD_AL_2
21	P10_D3N
22	P10_D3P
23	P10_D2N
24	P10_D2P
25	P10_D1N
26	P10_D1P
27	P10_D0N
28	P10_D0P
29	P11_D3N
30	P11_D3P
31	P11_D2N
32	P11_D2P
33	P11_D1N
34	P11_D1P
35	P11_D0N
36	P11_D0P
37	VDD_AL_3
38	GPIO_31
39	VDD_IO_1
40	GPIO_29
41	GPIO_16
42	GPIO_15
43	GPIO_8
44	GPIO_7
45	GPIO_5
46	GPIO_4
47	GPIO_3
48	SI_DO
49	GPIO_1
50	GPIO_0
51	SI_nEn
52	SI_DI
53	SI_Clk
54	MDC
55	MDIO
56	VDD_IO_2
57	VDD_1
58	VDD_2
59	VDD_3
60	VDD_A_1
61	VDD_VS_1
62	VDD_VS_2
63	VDD_A_2
64	VDD_A_3
65	Reserved_23
66	Reserved_22
67	VDD_IO_3
68	VDD_A_4
69	RefClk_N
70	RefClk_P
71	VDD_A_5
72	VDD_A_6
73	VDD_VS_3
74	VDD_A_7
75	VDD_VS_4
76	VDD_4
77	VDD_5
78	VDD_6
79	VDD_VS_5
80	VDD_A_8
81	VDD_VS_6
82	VDD_A_9
83	VDD_IO_4
84	VDD_VS_7
85	VDD_A_10
86	VDD_7
87	VDD_8
88	VDD_9
89	VDD_10
90	VDD_11
91	VDD_A_11
92	VDD_VS_8
93	VDD_A_12
94	VDD_VS_9
95	VDD_A_13
96	VDD_VS_10
97	VDD_VS_11
98	VDD_A_14
99	VDD_12
100	VDD_13
101	VDD_14
102	VDD_15
103	VDD_VS_12
104	VDD_A_15
105	VDD_16
106	SerDes_Rext_0
107	SerDes_Rext_1
108	VDD_IO_5
109	VDD_17
110	VDD_18

Pins by number *(continued)*

111 VDD_19	150 P2_D3N	189 P5_D1N
112 VDD_20	151 P2_D3P	190 P5_D1P
113 VDD_21	152 P2_D2N	191 P5_D0N
114 VDD_22	153 P2_D2P	192 P5_D0P
115 VDD_23	154 P2_D1N	193 Ref_filt_1
116 VDD_24	155 P2_D1P	194 Ref_rext_1
117 VDD_25	156 P2_D0N	195 P6_D3N
118 VDD_26	157 P2_D0P	196 P6_D3P
119 VDD_27	158 P3_D3N	197 P6_D2N
120 VDD_28	159 P3_D3P	198 P6_D2P
121 VDD_29	160 VDD_AL_10	199 P6_D1N
122 VDD_30	161 P3_D2N	200 P6_D1P
123 VDD_31	162 P3_D2P	201 VDD_AL_12
124 VDD_32	163 P3_D1N	202 P6_D0N
125 VDD_33	164 P3_D1P	203 P6_D0P
126 VDD_AL_4	165 P3_D0N	204 P7_D3N
127 VDD_AL_5	166 P3_D0P	205 P7_D3P
128 VDD_AL_6	167 Reserved_5	206 P7_D2N
129 VDD_AL_7	168 Reserved_6	207 P7_D2P
130 VDD_AL_8	169 Reserved_7	208 P7_D1N
131 P0_D3N	170 Reserved_8	209 P7_D1P
132 P0_D3P	171 JTAG_TRST	210 P7_D0N
133 VDD_AL_9	172 JTAG_DO	211 P7_D0P
134 P0_D2N	173 JTAG_TMS	212 Reserved_12
135 P0_D2P	174 JTAG_DI	213 Reserved_13
136 P0_D1N	175 JTAG_CLK	214 COMA_MODE
137 P0_D1P	176 P4_D3N	215 RefClk_Sel2
138 P0_D0N	177 P4_D3P	216 RefClk_Sel0
139 P0_D0P	178 P4_D2N	217 RefClk_Sel1
140 P1_D3N	179 P4_D2P	218 Reserved_4
141 P1_D3P	180 P4_D1N	219 Reserved_29
142 P1_D2N	181 P4_D1P	220 VCORE_CFG2
143 P1_D2P	182 P4_D0N	221 VCORE_CFG1
144 P1_D1N	183 VDD_AL_11	222 VCORE_CFG0
145 P1_D1P	184 P4_D0P	223 VDD_IO_21
146 P1_D0N	185 P5_D3N	224 nRESET
147 P1_D0P	186 P5_D3P	A1 Reserved_15
148 Ref_filt_0	187 P5_D2N	A2 VDD_AH_1
149 Ref_rext_0	188 P5_D2P	A3 VDD_AH_2

Pins by number *(continued)*

A4	VDD_AH_3
A5	VDD_AH_4
A6	VSS_1
A7	VDD_AH_5
A8	VDD_AH_6
A9	VDD_AH_7
A10	VDD_34
A11	Reserved_24
A12	GPIO_30
A13	VSS_2
A14	GPIO_6
A15	GPIO_2
A16	Reserved_18
A17	Reserved_17
A18	VSS_163
A19	VSS_3
A20	SerDes_E3_RxP
A21	SerDes_E3_RxN
A22	SerDes_E3_TxP
A23	SerDes_E3_TxN
A24	VSS_4
A25	SerDes_E2_TxN
A26	SerDes_E2_TxP
A27	SerDes_E2_RxN
A28	SerDes_E2_RxP
A29	VSS_5
A30	SerDes_E1_RxP
A31	SerDes_E1_RxN
A32	SerDes_E1_TxP
A33	SerDes_E1_TxN
A34	VSS_6
A35	SerDes_E0_TxN
A36	SerDes_E0_TxP
A37	SerDes_E0_RxN
A38	SerDes_E0_RxP
A39	VSS_7
A40	VSS_8
A41	VSS_9
A42	VSS_10
A43	VDD_35
A44	VDD_36
A45	VDD_37
A46	VSS_11
A47	VDD_AH_8
A48	VDD_AH_9
A49	VDD_AH_10
A50	VDD_AH_11
A51	VDD_AH_12
A52	VSS_12
A53	VDD_AH_13
A54	VDD_AH_14
A55	VDD_AH_15
A56	Reserved_10
A57	Reserved_11
A58	VSS_13
A59	VDD_IO_6
A60	VDD_IO_7
A61	VDD_38
A62	VDD_39
A63	VSS_14
A64	VDD_AH_16
A65	VDD_AH_17
A66	VDD_AH_18
A67	VDD_AH_19
A68	VDD_AH_20
A69	VDD_AH_21
A70	VSS_15
A71	VDD_IO_8
A72	VDD_40
A73	VDD_41
A74	VSS_16
A75	VDD_IO_9
A76	VDD_IO_10
A77	VDD_IO_11
A78	Reserved_14

11.4 Pins by Name for VSC7421XJQ-02

This section provides an alphabetical list of the VSC7421XJQ-02 pins.

COMA_MODE	214
GPIO_0	50
GPIO_1	49
GPIO_2	A15
GPIO_3	47
GPIO_4	46
GPIO_5	45
GPIO_6	A14
GPIO_7	44
GPIO_8	43
GPIO_15	42
GPIO_16	41
GPIO_29	40
GPIO_30	A12
GPIO_31	38
JTAG_CLK	175
JTAG_DI	174
JTAG_DO	172
JTAG_TMS	173
JTAG_TRST	171
MDC	54
MDIO	55
nRESET	224
P0_D0N	138
P0_D0P	139
P0_D1N	136
P0_D1P	137
P0_D2N	134
P0_D2P	135
P0_D3N	131
P0_D3P	132
P1_D0N	146
P1_D0P	147
P1_D1N	144
P1_D1P	145
P1_D2N	142
P1_D2P	143
P1_D3N	140
P1_D3P	141
P2_D0N	156
P2_D0P	157
P2_D1N	154
P2_D1P	155
P2_D2N	152
P2_D2P	153
P2_D3N	150
P2_D3P	151
P3_D0N	165
P3_D0P	166
P3_D1N	163
P3_D1P	164
P3_D2N	161
P3_D2P	162
P3_D3N	158
P3_D3P	159
P4_D0N	182
P4_D0P	184
P4_D1N	180
P4_D1P	181
P4_D2N	178
P4_D2P	179
P4_D3N	176
P4_D3P	177
P5_D0N	191
P5_D0P	192
P5_D1N	189
P5_D1P	190
P5_D2N	187
P5_D2P	188
P5_D3N	185
P5_D3P	186
P6_D0N	202
P6_D0P	203
P6_D1N	199
P6_D1P	200
P6_D2N	197
P6_D2P	198
P6_D3N	195
P6_D3P	196
P7_D0N	210
P7_D0P	211
P7_D1N	208
P7_D1P	209
P7_D2N	206
P7_D2P	207
P7_D3N	204
P7_D3P	205
P8_D0N	8
P8_D0P	9
P8_D1N	6
P8_D1P	7
P8_D2N	4
P8_D2P	5
P8_D3N	2
P8_D3P	3
P9_D0N	16
P9_D0P	17
P9_D1N	14
P9_D1P	15
P9_D2N	12
P9_D2P	13
P9_D3N	10
P9_D3P	11
P10_D0N	27
P10_D0P	28
P10_D1N	25
P10_D1P	26
P10_D2N	23
P10_D2P	24
P10_D3N	21

Pins by name *(continued)*

P10_D3P	22
P11_D0N	35
P11_D0P	36
P11_D1N	33
P11_D1P	34
P11_D2N	31
P11_D2P	32
P11_D3N	29
P11_D3P	30
Ref_filt_0	148
Ref_filt_1	193
Ref_filt_2	18
Ref_rext_0	149
Ref_rext_1	194
Ref_rext_2	19
RefClk_N	69
RefClk_P	70
RefClk_Sel0	216
RefClk_Sel1	217
RefClk_Sel2	215
Reserved_4	218
Reserved_5	167
Reserved_6	168
Reserved_7	169
Reserved_8	170
Reserved_10	A56
Reserved_11	A57
Reserved_12	212
Reserved_13	213
Reserved_14	A78
Reserved_15	A1
Reserved_17	A17
Reserved_18	A16
Reserved_22	66
Reserved_23	65
Reserved_24	A11
Reserved_29	219
SerDes_E0_RxN	A37
SerDes_E0_RxP	A38
SerDes_E0_TxN	A35
SerDes_E0_TxP	A36
SerDes_E1_RxN	A31
SerDes_E1_RxP	A30
SerDes_E1_TxN	A33
SerDes_E1_TxP	A32
SerDes_E2_RxN	A27
SerDes_E2_RxP	A28
SerDes_E2_TxN	A25
SerDes_E2_TxP	A26
SerDes_E3_RxN	A21
SerDes_E3_RxP	A20
SerDes_E3_TxN	A23
SerDes_E3_TxP	A22
SerDes_Rext_0	106
SerDes_Rext_1	107
SI_Clk	53
SI_DI	52
SI_DO	48
SI_nEn	51
VCORE_CFG0	222
VCORE_CFG1	221
VCORE_CFG2	220
VDD_1	57
VDD_2	58
VDD_3	59
VDD_4	76
VDD_5	77
VDD_6	78
VDD_7	86
VDD_8	87
VDD_9	88
VDD_10	89
VDD_11	90
VDD_12	99
VDD_13	100
VDD_14	101
VDD_15	102
VDD_16	105
VDD_17	109
VDD_18	110
VDD_19	111
VDD_20	112
VDD_21	113
VDD_22	114
VDD_23	115
VDD_24	116
VDD_25	117
VDD_26	118
VDD_27	119
VDD_28	120
VDD_29	121
VDD_30	122
VDD_31	123
VDD_32	124
VDD_33	125
VDD_34	A10
VDD_35	A43
VDD_36	A44
VDD_37	A45
VDD_38	A61
VDD_39	A62
VDD_40	A72
VDD_41	A73
VDD_A_1	60
VDD_A_2	63
VDD_A_3	64
VDD_A_4	68
VDD_A_5	71
VDD_A_6	72
VDD_A_7	74
VDD_A_8	80
VDD_A_9	82
VDD_A_10	85
VDD_A_11	91
VDD_A_12	93
VDD_A_13	95
VDD_A_14	98

Pins by name *(continued)*

VDD_A_15	104
VDD_AH_1	A2
VDD_AH_2	A3
VDD_AH_3	A4
VDD_AH_4	A5
VDD_AH_5	A7
VDD_AH_6	A8
VDD_AH_7	A9
VDD_AH_8	A47
VDD_AH_9	A48
VDD_AH_10	A49
VDD_AH_11	A50
VDD_AH_12	A51
VDD_AH_13	A53
VDD_AH_14	A54
VDD_AH_15	A55
VDD_AH_16	A64
VDD_AH_17	A65
VDD_AH_18	A66
VDD_AH_19	A67
VDD_AH_20	A68
VDD_AH_21	A69
VDD_AL_1	1
VDD_AL_2	20
VDD_AL_3	37
VDD_AL_4	126
VDD_AL_5	127
VDD_AL_6	128
VDD_AL_7	129
VDD_AL_8	130
VDD_AL_9	133
VDD_AL_10	160
VDD_AL_11	183
VDD_AL_12	201
VDD_IO_1	39
VDD_IO_2	56
VDD_IO_3	67
VDD_IO_4	83
VDD_IO_5	108
VDD_IO_6	A59
VDD_IO_7	A60
VDD_IO_8	A71
VDD_IO_9	A75
VDD_IO_10	A76
VDD_IO_11	A77
VDD_IO_21	223
VDD_VS_1	61
VDD_VS_2	62
VDD_VS_3	73
VDD_VS_4	75
VDD_VS_5	79
VDD_VS_6	81
VDD_VS_7	84
VDD_VS_8	92
VDD_VS_9	94
VDD_VS_10	96
VDD_VS_11	97
VDD_VS_12	103
VSS_1	A6
VSS_2	A13
VSS_3	A19
VSS_4	A24
VSS_5	A29
VSS_6	A34
VSS_7	A39
VSS_8	A40
VSS_9	A41
VSS_10	A42
VSS_11	A46
VSS_12	A52
VSS_13	A58
VSS_14	A63
VSS_15	A70
VSS_16	A74
VSS_163	A18

12 Pin Descriptions for VSC7421XJG-02

The VSC7421XJG-02 device has 672 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

12.1 Pin Identifications

The following table lists the definitions for the pin type symbols.

Table 625 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

12.2 Pin Diagram for VSC7421XJG-02

The following illustration shows the pin diagram for the VSC7421XJG-02 device, as seen from the top view looking through the device. For clarity, the device is shown in two halves, the top left and top right.

Figure 74 • **VSC7421XJG-02 Pin Diagram, Top Left**

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	#N/A	P8_D0P	P8_D1P	P8_D2P	P8_D3P	P7_D0P	P7_D1P	P7_D2P	P7_D3P	P6_D0P	P6_D1P	P6_D2P	P6_D3P
B	VSS_1	P8_D0N	P8_D1N	P8_D2N	P8_D3N	P7_D0N	P7_D1N	P7_D2N	P7_D3N	P6_D0N	P6_D1N	P6_D2N	P6_D3N
C	P9_D3P	P9_D3N	COMA_MODE	NRESET	VDD_IO_21	VSS_178	VCORE_CFG0	VCORE_CFG1	VCORE_CFG2	RESERVED_29	RESERVED_4	REFCLK_SEL0	REFCLK_SEL1
D	P9_D2P	P9_D2N	RESERVED_205	VDD_AH_1	VDD_AH_2	RESERVED_206	RESERVED_207	RESERVED_208	RESERVED_209	RESERVED_248	VDD_AH_4	RESERVED_211	RESERVED_13
E	P9_D1P	P9_D1N	RESERVED_216	VDD_AH_7	VDD_AH_8	VDD_IO_1	VDD_IO_2	VDD_AH_9	VDD_AL_1	VDD_AL_2	VDD_AH_10	VDD_AH_11	REF_REXT_1
F	P9_D0P	P9_D0N	RESERVED_218	VDD_AH_17	VDD_AH_18	VDD_IO_5	VDD_AH_3	VDD_AH_19	VDD_AL_5	VDD_AL_6	VDD_AH_20	VDD_AH_21	RESERVED_219
G	P10_D3P	P10_D3N	VSS_3	RESERVED_15	VSS_4	VDD_1	VDD_2	VDD_3	VDD_AL_9	VDD_AL_10	VDD_4	VDD_5	RESERVED_247
H	P10_D2P	P10_D2N	VSS_7	RESERVED_14	VSS_8	VDD_11	VDD_12	VDD_13	VDD_14	VDD_15	VDD_16	VDD_17	RESERVED_246
J	P10_D1P	P10_D1N	VDD_AH_27	VDD_AH_28	VDD_AL_13	VDD_AL_14	VDD_AL_15	RESERVED_240	RESERVED_241	RESERVED_242	RESERVED_243	RESERVED_244	RESERVED_245
K	P10_D0P	P10_D0N	VSS_11	REF_REXT_2	VDD_AL_19	VDD_AL_20	VDD_AL_21	VSS_12	VSS_13	VSS_14	VSS_15	VSS_16	VSS_17
L	P11_D3P	P11_D3N	VSS_25	REF_FILT_2	VSS_26	VDD_25	VDD_26	VSS_27	VSS_28	VSS_29	VSS_30	VSS_31	VSS_32
M	P11_D2P	P11_D2N	VDD_AH_31	VDD_AH_32	VDD_AH_33	VDD_29	VDD_30	VSS_41	VSS_42	VSS_43	VSS_44	VSS_45	VSS_46
N	P11_D1P	P11_D1N	VSS_53	VSS_54	VSS_55	VDD_33	VDD_34	VSS_56	VSS_57	VSS_58	VSS_59	VSS_60	VSS_61
P	P11_D0P	P11_D0N	VSS_71	RESERVED_24	VDD_IO_7	VDD_37	VDD_38	VSS_72	VSS_73	VSS_74	VSS_75	VSS_76	VSS_77
R	GPIO_31	GPIO_30	GPIO_29	RESERVED_190	VDD_IO_8	VDD_41	VDD_42	VSS_86	VSS_87	VSS_88	VSS_89	VSS_90	VSS_91
T	RESERVED_189	RESERVED_188	RESERVED_187	RESERVED_186	VDD_IO_9	VDD_45	VDD_46	VSS_98	VSS_99	VSS_100	VSS_101	VSS_102	VSS_103
U	RESERVED_99	RESERVED_98	RESERVED_41	RESERVED_40	VDD_IO_10	VSS_110	VSS_111	VSS_112	VSS_113	VSS_114	VSS_115	VSS_116	VSS_117
V	RESERVED_39	RESERVED_38	RESERVED_37	GPIO_16	VDD_IO_11	VDD_49	VDD_50	VDD_51	VDD_52	VDD_53	VDD_54	VDD_55	VDD_56
W	GPIO_15	RESERVED_36	RESERVED_35	RESERVED_34	VDD_IO_12	VDD_65	VDD_66	VDD_67	VDD_68	VDD_69	VDD_70	VDD_71	VDD_72
Y	RESERVED_33	RESERVED_32	RESERVED_31	GPIO_8	VDD_IO_13	RESERVED_146	RESERVED_141	REFCLK_P	SERDES_E3_TXP	RESERVED_134	RESERVED_129	VSS_126	SERDES_E2_TXP
AA	GPIO_7	GPIO_6	GPIO_5	GPIO_4	VDD_IO_14	RESERVED_147	RESERVED_140	REFCLK_N	SERDES_E3_TXN	RESERVED_135	RESERVED_128	VSS_145	SERDES_E2_TXN
AB	GPIO_3	GPIO_2	GPIO_1	GPIO_0	VDD_IO_15	VSS_129	VSS_130	VSS_131	VSS_132	VSS_133	VSS_134	VSS_135	VSS_136
AC	SI_DO	SI_NEN	VSS_148	VDD_IO_16	VDD_IO_17	VDD_A_1	VDD_A_2	VDD_A_3	VDD_A_4	VDD_A_5	VDD_A_6	VDD_A_7	VDD_A_8
AD	SI_CLK	SI_DI	RESERVED_18	VDD_IO_18	VSS_149	VDD_VS_1	VDD_VS_2	VDD_VS_3	VDD_VS_4	VDD_VS_5	VDD_VS_6	VDD_VS_7	VDD_VS_8
AE	VSS_151	RESERVED_17	VDD_IO_19	VSS_163	VSS_152	RESERVED_144	RESERVED_143	RESERVED_22	SERDES_E3_RXP	RESERVED_132	RESERVED_131	VSS_153	SERDES_E2_RXP
AF	#N/A	VDD_IO_20	MDIO	MDC	VSS_158	RESERVED_145	RESERVED_142	RESERVED_23	SERDES_E3_RXN	RESERVED_133	RESERVED_130	VSS_159	SERDES_E2_RXN

Figure 75 • **VSC7421XJG-02 Pin Diagram, Top Right**

14	15	16	17	18	19	20	21	22	23	24	25	26	
P5_D0P	P5_D1P	P5_D2P	P5_D3P	P4_D0P	P4_D1P	P4_D2P	P4_D3P	P3_D0P	P3_D1P	P3_D2P	P3_D3P	#N/A	A
P5_D0N	P5_D1N	P5_D2N	P5_D3N	P4_D0N	P4_D1N	P4_D2N	P4_D3N	P3_D0N	P3_D1N	P3_D2N	P3_D3N	VSS_2	B
REFCLK_SEL2	RESERVED_8	RESERVED_7	RESERVED_6	RESERVED_5	RESERVED_201	RESERVED_202	RESERVED_203	RESERVED_191	RESERVED_192	RESERVED_204	P2_D0N	P2_D0P	C
RESERVED_12	RESERVED_212	VDD_AH_5	JTAG_CLK	JTAG_DI	JTAG_DO	JTAG_TMS	JTAG_TRST	RESERVED_213	RESERVED_214	RESERVED_215	P2_D1N	P2_D1P	D
REF_FILT_1	VDD_AH_12	VDD_AH_13	VDD_AL_3	VDD_AL_4	VDD_AH_14	VDD_IO_3	VDD_IO_4	VDD_AH_15	VDD_AH_16	RESERVED_217	P2_D2N	P2_D2P	E
RESERVED_220	VDD_AH_22	VDD_AH_23	VDD_AL_7	VDD_AL_8	VDD_AH_24	VDD_AH_6	VDD_IO_6	VDD_AH_25	VDD_AH_26	RESERVED_221	P2_D3N	P2_D3P	F
RESERVED_223	VDD_6	VDD_7	VDD_AL_11	VDD_AL_12	VDD_8	VDD_9	VDD_10	VSS_5	RESERVED_10	VSS_6	P1_D0N	P1_D0P	G
RESERVED_225	VDD_18	VDD_19	VDD_20	VDD_21	VDD_22	VDD_23	VDD_24	VSS_9	RESERVED_11	VSS_10	P1_D1N	P1_D1P	H
RESERVED_232	RESERVED_233	RESERVED_234	RESERVED_235	RESERVED_236	RESERVED_237	VDD_AL_16	VDD_AL_17	VDD_AL_18	VDD_AH_29	VDD_AH_30	P1_D2N	P1_D2P	J
VSS_18	VSS_19	VSS_20	VSS_21	VSS_22	VSS_23	VDD_AL_22	VDD_AL_23	VDD_AL_24	REF_REXT_0	VSS_24	P1_D3N	P1_D3P	K
VSS_33	VSS_34	VSS_35	VSS_36	VSS_37	VSS_38	VDD_27	VDD_28	VSS_39	REF_FILT_0	VSS_40	P0_D0N	P0_D0P	L
VSS_47	VSS_48	VSS_49	VSS_50	VSS_51	VSS_52	VDD_31	VDD_32	VDD_AH_34	VDD_AH_35	VDD_AH_36	P0_D1N	P0_D1P	M
VSS_62	VSS_63	VSS_64	VSS_65	VSS_66	VSS_67	VDD_35	VDD_36	VSS_68	VSS_69	VSS_70	P0_D2N	P0_D2P	N
VSS_78	VSS_79	VSS_80	VSS_81	VSS_82	VSS_83	VDD_39	VDD_40	VSS_164	VSS_84	VSS_85	P0_D3N	P0_D3P	P
VSS_92	VSS_93	VSS_94	VSS_95	VSS_96	VSS_97	VDD_43	VDD_44	VSS_165	RESERVED_20	RESERVED_19	RESERVED_148	VSS_179	R
VSS_104	VSS_105	VSS_106	VSS_107	VSS_108	VSS_109	VDD_47	VDD_48	VSS_166	RESERVED_21	RESERVED_166	RESERVED_165	RESERVED_164	T
VSS_118	VSS_119	VSS_120	VSS_121	VSS_122	VSS_123	VSS_124	VSS_125	VSS_167	RESERVED_160	RESERVED_162	RESERVED_159	RESERVED_161	U
VDD_57	VDD_58	VDD_59	VDD_60	VDD_61	VDD_62	VDD_63	VDD_64	VSS_168	RESERVED_156	RESERVED_158	RESERVED_155	RESERVED_157	V
VDD_73	VDD_74	VDD_75	VDD_76	VDD_77	VDD_78	VDD_79	VDD_80	VSS_169	RESERVED_163	RESERVED_154	RESERVED_171	RESERVED_153	W
RESERVED_121	RESERVED_118	VSS_127	SERDES_E1_TXP	RESERVED_110	RESERVED_105	VSS_128	SERDES_E0_TXP	VSS_170	RESERVED_167	RESERVED_168	RESERVED_170	RESERVED_172	Y
RESERVED_120	RESERVED_119	VSS_146	SERDES_E1_TXN	RESERVED_111	RESERVED_104	VSS_147	SERDES_E0_TXN	VSS_171	RESERVED_173	RESERVED_169	RESERVED_150	RESERVED_151	AA
VSS_137	VSS_138	VSS_139	VSS_140	VSS_141	VSS_142	VSS_143	VSS_144	VSS_172	RESERVED_180	RESERVED_152	RESERVED_179	RESERVED_182	AB
VDD_A_9	VDD_A_10	VDD_A_11	VDD_A_12	VDD_A_13	VDD_A_14	VDD_A_15	VDD_A_16	VSS_173	RESERVED_178	RESERVED_181	RESERVED_184	RESERVED_177	AC
VDD_VS_9	VDD_VS_10	VDD_VS_11	VDD_VS_12	VDD_VS_13	VDD_VS_14	VDD_VS_15	VDD_VS_16	VSS_150	VSS_174	RESERVED_183	RESERVED_175	RESERVED_176	AD
RESERVED_123	RESERVED_116	VSS_154	SERDES_E1_RXP	RESERVED_108	RESERVED_107	VSS_155	SERDES_E0_RXP	SERDES_REXT_0	VSS_156	VSS_175	RESERVED_174	VSS_157	AE
RESERVED_122	RESERVED_117	VSS_160	SERDES_E1_RXN	RESERVED_109	RESERVED_106	VSS_161	SERDES_E0_RXN	SERDES_REXT_1	VSS_162	VSS_177	VSS_176	#N/A	AF

12.3 Pins by Function for VSC7421XJG-02

This section contains the functional pin descriptions for the VSC7421XJG-02 device.

Functional Group	Name	Number	Type	Description
Analog Bias	Ref_filt_0	L23	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_1	E14	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_2	L4	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_rext_0	K23	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	Ref_rext_1	E13	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	Ref_rext_2	K4	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	SerDes_Rext_0	AE22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Analog Bias	SerDes_Rext_1	AF22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Enhanced SerDes Interface	SerDes_E0_RxN	AF21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_RxP	AE21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_TxN	AA21	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E0_TxP	Y21	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E1_RxN	AF17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_RxP	AE17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_TxN	AA17	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E1_TxP	Y17	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E2_RxN	AF13	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E2_RxP	AE13	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E2_TxN	AA13	O, Diff	Differential Enhanced SerDes data outputs.

Enhanced SerDes Interface	SerDes_E2_TxP	Y13	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E3_RxN	AF9	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E3_RxP	AE9	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E3_TxN	AA9	O, Diff	Differential Enhanced SerDes data outputs.
Enhanced SerDes Interface	SerDes_E3_TxP	Y9	O, Diff	Differential Enhanced SerDes data outputs.
General Purpose I/O	GPIO_0	AB4	I/O, PU, ST, 3V	Overlaid function 1: SIO_CLK.
General Purpose I/O	GPIO_1	AB3	I/O, PU, ST, 3V	Overlaid function 1: SIO_LD.
General Purpose I/O	GPIO_2	AB2	I/O, PU, ST, 3V	Overlaid function 1: SIO_DO.
General Purpose I/O	GPIO_3	AB1	I/O, PU, ST, 3V	Overlaid function 1: SIO_DI.
General Purpose I/O	GPIO_4	AA4	I/O, PU, ST, 3V	Overlaid function 1: TACHO.
General Purpose I/O	GPIO_5	AA3	I/O, PU, ST, 3V	Overlaid function 1: TWI_SCL.
General Purpose I/O	GPIO_6	AA2	I/O, PU, ST, 3V	Overlaid function 1: TWI_SDA.
General Purpose I/O	GPIO_7	AA1	I/O, PU, ST, 3V	General-purpose input/output.
General Purpose I/O	GPIO_8	Y4	I/O, PU, ST, 3V	Overlaid function 1: EXT_IRQ0.
General Purpose I/O	GPIO_15	W1	I/O, PU, ST, 3V	MIIM slave mode: SLV_MDC.
General Purpose I/O	GPIO_16	V4	I/O, PU, ST, 3V	MIIM slave mode: SLV_MDIO.
General Purpose I/O	GPIO_29	R3	I/O, PU, ST, 3V	Overlaid function 1: PWM.
General Purpose I/O	GPIO_30	R2	I/O, PU, ST, 3V	Overlaid function 1: UART_TX.
General Purpose I/O	GPIO_31	R1	I/O, PU, ST, 3V	Overlaid function 1: UART_RX.
JTAG Interface	JTAG_CLK	D17	I, PU, ST, 3V	JTAG clock.
JTAG Interface	JTAG_DI	D18	I, PU, ST, 3V	JTAG test data in.
JTAG Interface	JTAG_DO	D19	OZ, 3V	JTAG test data out.
JTAG Interface	JTAG_TMS	D20	I, PU, ST, 3V	JTAG test mode select.
JTAG Interface	JTAG_TRST	D21	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
MII Management Interface	MDC	AF4	O, 3V	Management data clock. MDC is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.
MII Management Interface	MDIO	AF3	I/O	Management data input/output. MDIO is a bidirectional signal between a PHY and the device that transfers control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.

Miscellaneous	COMA_MODE	C3	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
Miscellaneous	nRESET	C4	I, PD, ST, 3V	Global device reset, active low.
Miscellaneous	VCORE_CFG0	C7	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Miscellaneous	VCORE_CFG1	C8	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Miscellaneous	VCORE_CFG2	C9	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Power Supply	VDD_1	G6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_2	G7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_3	G8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_4	G11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_5	G12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_6	G15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_7	G16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_8	G19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_9	G20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_10	G21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_11	H6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_12	H7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_13	H8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_14	H9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_15	H10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_16	H11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_17	H12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_18	H15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_19	H16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_20	H17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_21	H18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_22	H19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_23	H20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_24	H21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_25	L6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_26	L7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_27	L20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_28	L21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_29	M6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_30	M7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_31	M20	Power	1.0 V power supply voltage for core.

Power Supply	VDD_32	M21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_33	N6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_34	N7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_35	N20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_36	N21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_37	P6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_38	P7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_39	P20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_40	P21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_41	R6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_42	R7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_43	R20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_44	R21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_45	T6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_46	T7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_47	T20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_48	T21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_49	V6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_50	V7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_51	V8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_52	V9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_53	V10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_54	V11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_55	V12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_56	V13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_57	V14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_58	V15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_59	V16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_60	V17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_61	V18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_62	V19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_63	V20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_64	V21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_65	W6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_66	W7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_67	W8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_68	W9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_69	W10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_70	W11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_71	W12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_72	W13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_73	W14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_74	W15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_75	W16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_76	W17	Power	1.0 V power supply voltage for core.

Power Supply	VDD_77	W18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_78	W19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_79	W20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_80	W21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_A_1	AC6	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_2	AC7	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_3	AC8	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_4	AC9	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_5	AC10	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_6	AC11	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_7	AC12	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_8	AC13	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_9	AC14	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_10	AC15	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_11	AC16	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_12	AC17	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_13	AC18	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_14	AC19	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_15	AC20	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_16	AC21	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_AH_1	D4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_2	D5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_3	F7	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_4	D11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_5	D16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_6	F20	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_7	E4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_8	E5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_9	E8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.

Power Supply	VDD_AH_10	E11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_11	E12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_12	E15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_13	E16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_14	E19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_15	E22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_16	E23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_17	F4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_18	F5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_19	F8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_20	F11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_21	F12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_22	F15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_23	F16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_24	F19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_25	F22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_26	F23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_27	J3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_28	J4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_29	J23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_30	J24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_31	M3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_32	M4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_33	M5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_34	M22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_35	M23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_36	M24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AL_1	E9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.

Power Supply	VDD_AL_2	E10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_3	E17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_4	E18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_5	F9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_6	F10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_7	F17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_8	F18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_9	G9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_10	G10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_11	G17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_12	G18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_13	J5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_14	J6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_15	J7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_16	J20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_17	J21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_18	J22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_19	K5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_20	K6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_21	K7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_22	K20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_23	K21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_24	K22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_IO_1	E6	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_2	E7	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_3	E20	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_4	E21	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_5	F6	Power	2.5 V power supply for MII Management and miscellaneous I/Os.

Power Supply	VDD_IO_6	F21	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_7	P5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_8	R5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_9	T5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_10	U5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_11	V5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_12	W5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_13	Y5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_14	AA5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_15	AB5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_16	AC4	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_17	AC5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_18	AD4	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_19	AE3	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_20	AF2	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_IO_21	C5	Power	2.5 V power supply for MII Management and miscellaneous I/Os.
Power Supply	VDD_VS_1	AD6	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_2	AD7	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_3	AD8	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_4	AD9	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_5	AD10	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_6	AD11	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_7	AD12	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_8	AD13	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_9	AD14	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_10	AD15	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_11	AD16	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_12	AD17	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.

Power Supply	VDD_VS_13	AD18	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_14	AD19	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_15	AD20	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VDD_VS_16	AD21	Power	1.0 V or 1.2 V power supply for SerDes and Enhanced SerDes interface.
Power Supply	VSS_1	B1	Ground	Ground reference.
Power Supply	VSS_2	B26	Ground	Ground reference.
Power Supply	VSS_3	G3	Ground	Ground reference.
Power Supply	VSS_4	G5	Ground	Ground reference.
Power Supply	VSS_5	G22	Ground	Ground reference.
Power Supply	VSS_6	G24	Ground	Ground reference.
Power Supply	VSS_7	H3	Ground	Ground reference.
Power Supply	VSS_8	H5	Ground	Ground reference.
Power Supply	VSS_9	H22	Ground	Ground reference.
Power Supply	VSS_10	H24	Ground	Ground reference.
Power Supply	VSS_11	K3	Ground	Ground reference.
Power Supply	VSS_12	K8	Ground	Ground reference.
Power Supply	VSS_13	K9	Ground	Ground reference.
Power Supply	VSS_14	K10	Ground	Ground reference.
Power Supply	VSS_15	K11	Ground	Ground reference.
Power Supply	VSS_16	K12	Ground	Ground reference.
Power Supply	VSS_17	K13	Ground	Ground reference.
Power Supply	VSS_18	K14	Ground	Ground reference.
Power Supply	VSS_19	K15	Ground	Ground reference.
Power Supply	VSS_20	K16	Ground	Ground reference.
Power Supply	VSS_21	K17	Ground	Ground reference.
Power Supply	VSS_22	K18	Ground	Ground reference.
Power Supply	VSS_23	K19	Ground	Ground reference.
Power Supply	VSS_24	K24	Ground	Ground reference.
Power Supply	VSS_25	L3	Ground	Ground reference.
Power Supply	VSS_26	L5	Ground	Ground reference.
Power Supply	VSS_27	L8	Ground	Ground reference.
Power Supply	VSS_28	L9	Ground	Ground reference.
Power Supply	VSS_29	L10	Ground	Ground reference.
Power Supply	VSS_30	L11	Ground	Ground reference.
Power Supply	VSS_31	L12	Ground	Ground reference.
Power Supply	VSS_32	L13	Ground	Ground reference.
Power Supply	VSS_33	L14	Ground	Ground reference.
Power Supply	VSS_34	L15	Ground	Ground reference.
Power Supply	VSS_35	L16	Ground	Ground reference.
Power Supply	VSS_36	L17	Ground	Ground reference.
Power Supply	VSS_37	L18	Ground	Ground reference.
Power Supply	VSS_38	L19	Ground	Ground reference.

Power Supply	VSS_39	L22	Ground	Ground reference.
Power Supply	VSS_40	L24	Ground	Ground reference.
Power Supply	VSS_41	M8	Ground	Ground reference.
Power Supply	VSS_42	M9	Ground	Ground reference.
Power Supply	VSS_43	M10	Ground	Ground reference.
Power Supply	VSS_44	M11	Ground	Ground reference.
Power Supply	VSS_45	M12	Ground	Ground reference.
Power Supply	VSS_46	M13	Ground	Ground reference.
Power Supply	VSS_47	M14	Ground	Ground reference.
Power Supply	VSS_48	M15	Ground	Ground reference.
Power Supply	VSS_49	M16	Ground	Ground reference.
Power Supply	VSS_50	M17	Ground	Ground reference.
Power Supply	VSS_51	M18	Ground	Ground reference.
Power Supply	VSS_52	M19	Ground	Ground reference.
Power Supply	VSS_53	N3	Ground	Ground reference.
Power Supply	VSS_54	N4	Ground	Ground reference.
Power Supply	VSS_55	N5	Ground	Ground reference.
Power Supply	VSS_56	N8	Ground	Ground reference.
Power Supply	VSS_57	N9	Ground	Ground reference.
Power Supply	VSS_58	N10	Ground	Ground reference.
Power Supply	VSS_59	N11	Ground	Ground reference.
Power Supply	VSS_60	N12	Ground	Ground reference.
Power Supply	VSS_61	N13	Ground	Ground reference.
Power Supply	VSS_62	N14	Ground	Ground reference.
Power Supply	VSS_63	N15	Ground	Ground reference.
Power Supply	VSS_64	N16	Ground	Ground reference.
Power Supply	VSS_65	N17	Ground	Ground reference.
Power Supply	VSS_66	N18	Ground	Ground reference.
Power Supply	VSS_67	N19	Ground	Ground reference.
Power Supply	VSS_68	N22	Ground	Ground reference.
Power Supply	VSS_69	N23	Ground	Ground reference.
Power Supply	VSS_70	N24	Ground	Ground reference.
Power Supply	VSS_71	P3	Ground	Ground reference.
Power Supply	VSS_72	P8	Ground	Ground reference.
Power Supply	VSS_73	P9	Ground	Ground reference.
Power Supply	VSS_74	P10	Ground	Ground reference.
Power Supply	VSS_75	P11	Ground	Ground reference.
Power Supply	VSS_76	P12	Ground	Ground reference.
Power Supply	VSS_77	P13	Ground	Ground reference.
Power Supply	VSS_78	P14	Ground	Ground reference.
Power Supply	VSS_79	P15	Ground	Ground reference.
Power Supply	VSS_80	P16	Ground	Ground reference.
Power Supply	VSS_81	P17	Ground	Ground reference.
Power Supply	VSS_82	P18	Ground	Ground reference.
Power Supply	VSS_83	P19	Ground	Ground reference.

Power Supply	VSS_84	P23	Ground	Ground reference.
Power Supply	VSS_85	P24	Ground	Ground reference.
Power Supply	VSS_86	R8	Ground	Ground reference.
Power Supply	VSS_87	R9	Ground	Ground reference.
Power Supply	VSS_88	R10	Ground	Ground reference.
Power Supply	VSS_89	R11	Ground	Ground reference.
Power Supply	VSS_90	R12	Ground	Ground reference.
Power Supply	VSS_91	R13	Ground	Ground reference.
Power Supply	VSS_92	R14	Ground	Ground reference.
Power Supply	VSS_93	R15	Ground	Ground reference.
Power Supply	VSS_94	R16	Ground	Ground reference.
Power Supply	VSS_95	R17	Ground	Ground reference.
Power Supply	VSS_96	R18	Ground	Ground reference.
Power Supply	VSS_97	R19	Ground	Ground reference.
Power Supply	VSS_98	T8	Ground	Ground reference.
Power Supply	VSS_99	T9	Ground	Ground reference.
Power Supply	VSS_100	T10	Ground	Ground reference.
Power Supply	VSS_101	T11	Ground	Ground reference.
Power Supply	VSS_102	T12	Ground	Ground reference.
Power Supply	VSS_103	T13	Ground	Ground reference.
Power Supply	VSS_104	T14	Ground	Ground reference.
Power Supply	VSS_105	T15	Ground	Ground reference.
Power Supply	VSS_106	T16	Ground	Ground reference.
Power Supply	VSS_107	T17	Ground	Ground reference.
Power Supply	VSS_108	T18	Ground	Ground reference.
Power Supply	VSS_109	T19	Ground	Ground reference.
Power Supply	VSS_110	U6	Ground	Ground reference.
Power Supply	VSS_111	U7	Ground	Ground reference.
Power Supply	VSS_112	U8	Ground	Ground reference.
Power Supply	VSS_113	U9	Ground	Ground reference.
Power Supply	VSS_114	U10	Ground	Ground reference.
Power Supply	VSS_115	U11	Ground	Ground reference.
Power Supply	VSS_116	U12	Ground	Ground reference.
Power Supply	VSS_117	U13	Ground	Ground reference.
Power Supply	VSS_118	U14	Ground	Ground reference.
Power Supply	VSS_119	U15	Ground	Ground reference.
Power Supply	VSS_120	U16	Ground	Ground reference.
Power Supply	VSS_121	U17	Ground	Ground reference.
Power Supply	VSS_122	U18	Ground	Ground reference.
Power Supply	VSS_123	U19	Ground	Ground reference.
Power Supply	VSS_124	U20	Ground	Ground reference.
Power Supply	VSS_125	U21	Ground	Ground reference.
Power Supply	VSS_126	Y12	Ground	Ground reference.
Power Supply	VSS_127	Y16	Ground	Ground reference.
Power Supply	VSS_128	Y20	Ground	Ground reference.

Power Supply	VSS_129	AB6	Ground	Ground reference.
Power Supply	VSS_130	AB7	Ground	Ground reference.
Power Supply	VSS_131	AB8	Ground	Ground reference.
Power Supply	VSS_132	AB9	Ground	Ground reference.
Power Supply	VSS_133	AB10	Ground	Ground reference.
Power Supply	VSS_134	AB11	Ground	Ground reference.
Power Supply	VSS_135	AB12	Ground	Ground reference.
Power Supply	VSS_136	AB13	Ground	Ground reference.
Power Supply	VSS_137	AB14	Ground	Ground reference.
Power Supply	VSS_138	AB15	Ground	Ground reference.
Power Supply	VSS_139	AB16	Ground	Ground reference.
Power Supply	VSS_140	AB17	Ground	Ground reference.
Power Supply	VSS_141	AB18	Ground	Ground reference.
Power Supply	VSS_142	AB19	Ground	Ground reference.
Power Supply	VSS_143	AB20	Ground	Ground reference.
Power Supply	VSS_144	AB21	Ground	Ground reference.
Power Supply	VSS_145	AA12	Ground	Ground reference.
Power Supply	VSS_146	AA16	Ground	Ground reference.
Power Supply	VSS_147	AA20	Ground	Ground reference.
Power Supply	VSS_148	AC3	Ground	Ground reference.
Power Supply	VSS_149	AD5	Ground	Ground reference.
Power Supply	VSS_150	AD22	Ground	Ground reference.
Power Supply	VSS_151	AE1	Ground	Ground reference.
Power Supply	VSS_152	AE5	Ground	Ground reference.
Power Supply	VSS_153	AE12	Ground	Ground reference.
Power Supply	VSS_154	AE16	Ground	Ground reference.
Power Supply	VSS_155	AE20	Ground	Ground reference.
Power Supply	VSS_156	AE23	Ground	Ground reference.
Power Supply	VSS_157	AE26	Ground	Ground reference.
Power Supply	VSS_158	AF5	Ground	Ground reference.
Power Supply	VSS_159	AF12	Ground	Ground reference.
Power Supply	VSS_160	AF16	Ground	Ground reference.
Power Supply	VSS_161	AF20	Ground	Ground reference.
Power Supply	VSS_162	AF23	Ground	Ground reference.
Power Supply	VSS_163	AE4	Ground	Ground reference.
Power Supply	VSS_164	P22	Ground	Ground reference.
Power Supply	VSS_165	R22	Ground	Ground reference.
Power Supply	VSS_166	T22	Ground	Ground reference.
Power Supply	VSS_167	U22	Ground	Ground reference.
Power Supply	VSS_168	V22	Ground	Ground reference.
Power Supply	VSS_169	W22	Ground	Ground reference.
Power Supply	VSS_170	Y22	Ground	Ground reference.
Power Supply	VSS_171	AA22	Ground	Ground reference.
Power Supply	VSS_172	AB22	Ground	Ground reference.
Power Supply	VSS_173	AC22	Ground	Ground reference.

Power Supply	VSS_174	AD23	Ground	Ground reference.
Power Supply	VSS_175	AE24	Ground	Ground reference.
Power Supply	VSS_176	AF25	Ground	Ground reference.
Power Supply	VSS_177	AF24	Ground	Ground reference.
Power Supply	VSS_178	C6	Ground	Ground reference.
Power Supply	VSS_179	R26	Ground	Ground reference.
Reserved	Reserved_4	C11	I, PD, ST, 3V	Tie to VSS.
Reserved	Reserved_5	C18	I, PD, ST, 3V	Tie to VSS.
Reserved	Reserved_6	C17	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_7	C16	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_8	C15	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_10	G23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_11	H23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_12	D14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_13	D13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_14	H4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_15	G4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_17	AE2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_18	AD3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_19	R24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_20	R23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_21	T23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_22	AE8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_23	AF8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_24	P4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_29	C10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_31	Y3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_32	Y2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_33	Y1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_34	W4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_35	W3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_36	W2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_37	V3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_38	V2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_39	V1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_40	U4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_41	U3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_98	U2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_99	U1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_104	AA19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_105	Y19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_106	AF19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_107	AE19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_108	AE18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_109	AF18	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_110	Y18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_111	AA18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_116	AE15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_117	AF15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_118	Y15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_119	AA15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_120	AA14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_121	Y14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_122	AF14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_123	AE14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_128	AA11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_129	Y11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_130	AF11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_131	AE11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_132	AE10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_133	AF10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_134	Y10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_135	AA10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_140	AA7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_141	Y7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_142	AF7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_143	AE7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_144	AE6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_145	AF6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_146	Y6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_147	AA6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_148	R25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_150	AA25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_151	AA26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_152	AB24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_153	W26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_154	W24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_155	V25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_156	V23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_157	V26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_158	V24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_159	U25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_160	U23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_161	U26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_162	U24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_163	W23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_164	T26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_165	T25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_166	T24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_167	Y23	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_168	Y24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_169	AA24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_170	Y25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_171	W25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_172	Y26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_173	AA23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_174	AE25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_175	AD25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_176	AD26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_177	AC26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_178	AC23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_179	AB25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_180	AB23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_181	AC24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_182	AB26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_183	AD24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_184	AC25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_186	T4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_187	T3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_188	T2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_189	T1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_190	R4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_191	C22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_192	C23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_201	C19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_202	C20	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_203	C21	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_204	C24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_205	D3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_206	D6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_207	D7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_208	D8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_209	D9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_211	D12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_212	D15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_213	D22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_214	D23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_215	D24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_216	E3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_217	E24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_218	F3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_219	F13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_220	F14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_221	F24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_223	G14	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_225	H14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_232	J14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_233	J15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_234	J16	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_235	J17	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_236	J18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_237	J19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_240	J8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_241	J9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_242	J10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_243	J11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_244	J12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_245	J13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_246	H13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_247	G13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_248	D10	I, PD, ST, 3V	Leave floating.
Serial CPU Interface	SI_Clk	AD1	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
Serial CPU Interface	SI_DI	AD2	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
Serial CPU Interface	SI_DO	AC1	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
Serial CPU Interface	SI_nEn	AC2	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.

System Clock Interface	RefClk_N	AA8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.
System Clock Interface	RefClk_P	Y8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.
System Clock Interface	RefClk_Sel0	C12	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
System Clock Interface	RefClk_Sel1	C13	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.

System Clock Interface	RefClk_Sel2	C14	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
Twisted Pair Interface	P0_D0N	L25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P0_D0P	L26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P0_D1N	M25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P0_D1P	M26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P0_D2N	N25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P0_D2P	N26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D3N	P25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D3P	P26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D0N	G25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P1_D0P	G26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P1_D1N	H25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P1_D1P	H26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P1_D2N	J25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D2P	J26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D3N	K25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D3P	K26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D0N	C25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P2_D0P	C26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P2_D1N	D25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P2_D1P	D26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P2_D2N	E25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D2P	E26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D3N	F25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P2_D3P	F26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D0N	B22	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P3_D0P	A22	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P3_D1N	B23	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P3_D1P	A23	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P3_D2N	B24	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P3_D2P	A24	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D3N	B25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D3P	A25	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D0N	B18	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P4_D0P	A18	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P4_D1N	B19	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P4_D1P	A19	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P4_D2N	B20	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D2P	A20	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D3N	B21	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D3P	A21	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D0N	B14	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P5_D0P	A14	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P5_D1N	B15	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P5_D1P	A15	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P5_D2N	B16	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D2P	A16	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D3N	B17	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P5_D3P	A17	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D0N	B10	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P6_D0P	A10	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P6_D1N	B11	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P6_D1P	A11	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P6_D2N	B12	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P6_D2P	A12	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3N	B13	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3P	A13	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D0N	B6	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P7_D0P	A6	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P7_D1N	B7	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P7_D1P	A7	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P7_D2N	B8	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D2P	A8	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D3N	B9	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D3P	A9	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D0N	B2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P8_D0P	A2	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P8_D1N	B3	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P8_D1P	A3	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P8_D2N	B4	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D2P	A4	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D3N	B5	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P8_D3P	A5	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D0N	F2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P9_D0P	F1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P9_D1N	E2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P9_D1P	E1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P9_D2N	D2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P9_D2P	D1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D3N	C2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D3P	C1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D0N	K2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P10_D0P	K1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P10_D1N	J2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.

Twisted Pair Interface	P10_D1P	J1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P10_D2N	H2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D2P	H1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D3N	G2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D3P	G1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D0N	P2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.

Twisted Pair Interface	P11_D0P	P1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P11_D1N	N2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
Twisted Pair Interface	P11_D1P	N1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P11_D2N	M2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D2P	M1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D3N	L2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P11_D3P	L1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

13 Pin Descriptions for VSC7422XJQ-02

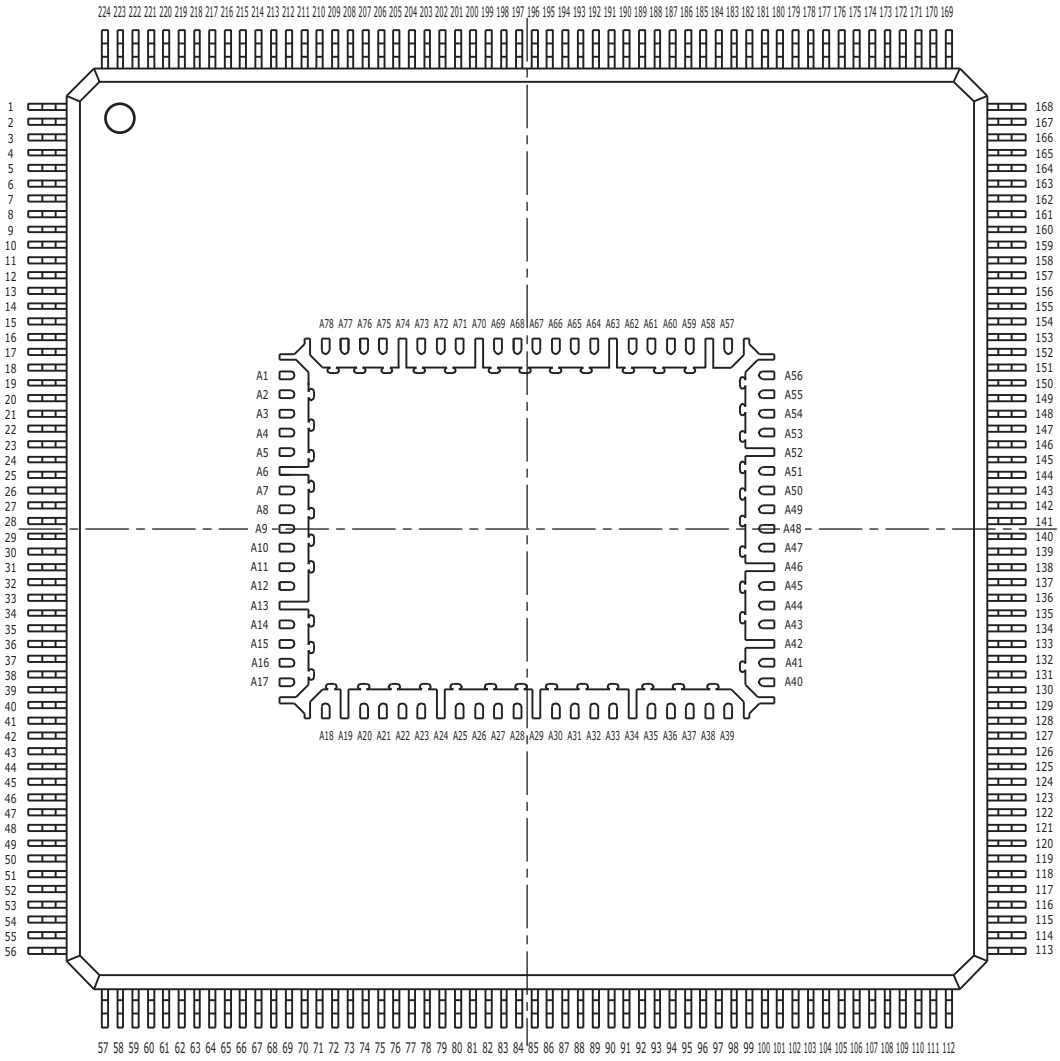
The VSC7422XJQ-02 device has 302 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

13.1 Pin Diagram for VSC7422XJQ-02

The following illustration shows the pin diagram for the VSC7422XJQ-02 device, as seen from the top view looking through the device.

Figure 76 • **Pin Diagram for VSC7422XJQ-02**



13.2 Pins by Function for VSC7422XJQ-02

This section contains the functional pin descriptions for the VSC7422XJQ-02 device. The following table lists the definitions for the pin type symbols.

Table 626 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

13.2.1 Analog Bias Signals

The following table lists the pins associated with the analog bias signals.

Table 627 • **Analog Bias Pins**

Name	Type	Description
SerDes_Rext_[1:0]	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Ref_filt_[2:0]	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Ref_rext_[2:0]	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.

13.2.2 Clock Circuits

The following table lists the pins associated with the system clock interface.

Table 628 • **System Clock Interface Pins**

Name	Type	Description
RefClk_Sel[2:0]	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to V_{DD_IO}. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
RefClk_P RefClk_N	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to V_{DD_A}. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.

13.2.3 General-Purpose Inputs and Outputs

The following table lists the pins associated with general-purpose inputs and outputs. The GPIO pins have an alternate function signal, which is mapped out in the following table. The overlaid functions are selected by software on a pin-by-pin basis. The MIIM slave interface is enabled depending on the VCORE_CFG settings and override the normal GPIO and alternate functions.

Table 629 • **GPIO Pin Mapping**

Name	Overlaid Function 1	Type	MIIM Slave Mode
GPIO_0	SIO_CLK	I/O, PU, ST, 3V	
GPIO_1	SIO_LD	I/O, PU, ST, 3V	
GPIO_2	SIO_DO	I/O, PU, ST, 3V	
GPIO_3	SIO_DI	I/O, PU, ST, 3V	
GPIO_4	TACHO	I/O, PU, ST, 3V	
GPIO_5	TWI_SCL	I/O, PU, ST, 3V	
GPIO_6	TWI_SDA	I/O, PU, ST, 3V	
GPIO_7	None	I/O, PU, ST, 3V	
GPIO_8	EXT_IRQ0	I/O, PU, ST, 3V	
GPIO_15	None	I/O, PU, ST, 3V	SLV_MDC
GPIO_16	None	I/O, PU, ST, 3V	SLV_MDIO

Table 629 • **GPIO Pin Mapping *(continued)***

Name	Overlaid Function 1	Type	MIIM Slave Mode
GPIO_29	PWM	I/O, PU, ST, 3V	
GPIO_30	UART_TX	I/O, PU, ST, 3V	
GPIO_31	UART_RX	I/O, PU, ST, 3V	

13.2.4 JTAG Interface

The following table lists the pins associated with the JTAG interface. The JTAG interface can be connected to the boundary scan TAP controller.

The JTAG signals are not 5 V tolerant.

Table 630 • **JTAG Interface Pins**

Name	Type	Description
JTAG_nTRST	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
JTAG_CLK	I, PU, ST, 3V	JTAG clock.
JTAG_TDI	I, PU, ST, 3V	JTAG test data in.
JTAG_TDO	OZ, 3V	JTAG test data out.
JTAG_TMS	I, PU, ST, 3V	JTAG test mode select.

13.2.5 MII Management Interface

The following table lists the pins associated with the MII Management interface.

Table 631 • **MII Management Interface Pins**

Name	Type	Description
MDIO	I/O, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
MDC	O, 3V	Management data clock. MDC is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.

13.2.6 Miscellaneous Signals

The following table lists the pins associated with a particular interface or facility on the device.

Table 632 • **Miscellaneous Pins**

Name	Type	Description
nReset	I, PD, ST, 3V	Global device reset, active low.

Table 632 • **Miscellaneous Pins *(continued)***

Name	Type	Description
COMA_MODE	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
VCORE_CFG[2:0]	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
EXT_IRQ0(1)	I/O PD, 3V	This pin interrupts inputs or outputs to the internal VCore-Ie CPU system or to an external processor. Signal polarity is programmable. See Figure 6, page 26.
Reserved_5 Reserved_[7:8] Reserved_29	I, PD, ST, 3V	Tie to V_{DD_IO}.
Reserved_4 Reserved_6	I, PD, ST, 3V	Tie to V_{SS}.
Reserved_[10:15] Reserved_[17:18] Reserved_[22:24]	I, PD, ST, 3V	Leave floating.

1. Available as an alternate function on the GPIO_8 pin.

13.2.7 Power Supplies and Ground

The following table lists the power supply and ground pins.

Table 633 • **Power Supply and Ground Pins**

Name	Type	Description
VDD	Power	1.0 V power supply voltage for core
VDD_A	Power	1.0 V power supply voltage for analog circuits
VDD_AL	Power	1.0 V power supply voltage for analog circuits for twisted pair interface
VDD_AH	Power	2.5 V power supply voltage for analog driver in twisted pair interface
VDD_IO	Power	2.5 V power supply for MII Management, and miscellaneous I/Os
VDD_VS	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces
VSS	Ground	Ground reference

13.2.8 Serial CPU Interface

The serial CPU interface (SI) can be used as a serial slave, master, or boot interface.

As a slave interface, it allows external CPUs to access internal registers. As a master interface, it allows the device to access external devices using a programmable protocol. The serial CPU interface also allows the internal VCore-Ie CPU system to boot from an attached serial memory device when the VCORE_CFG signals are set appropriately.

The following table lists the pins associated with the serial CPU interface (SI).

Table 634 • **Serial CPU Interface Pins**

Name	Type	Description
SI_Clk	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
SI_DI	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
SI_DO	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
SI_nEn	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.

13.2.9 Enhanced SerDes Interface

The following pins are associated with the Enhanced SerDes interface.

Table 635 • **Enhanced SerDes Interface Pins**

Name	Type	Description
SerDes_E[3:0]_RxP, N SerDes_E[3:0]_RxP, N	I, Diff, TD	Differential Enhanced SerDes data inputs.
SerDes_E[3:0]_TxP, N SerDes_E[3:0]_TxP, N	O, Diff	Differential Enhanced SerDes data outputs.

13.2.10 Twisted Pair Interface

The following pins are associated with the twisted pair interface. The PHYn_LED[1:0] LED control signals associated with the twisted pair interfaces are alternate functions on the GPIOs. For more information about the GPIO pin mapping, see Table 629, page 539.

Table 636 • **Twisted Pair Interface Pins**

Name	Type	Description
P0_D0P P1_D0P P2_D0P P3_D0P P4_D0P P5_D0P P6_D0P P7_D0P P8_D0P P9_D0P P10_D0P P11_D0P	A_{DIFF}	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Table 636 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D0N P1_D0N P2_D0N P3_D0N P4_D0N P5_D0N P6_D0N P7_D0N P8_D0N P9_D0N P10_D0N P11_D0N	A_{DIFF}	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
P0_D1P P1_D1P P2_D1P P3_D1P P4_D1P P5_D1P P6_D1P P7_D1P P8_D1P P9_D1P P10_D1P P11_D1P	A_{DIFF}	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
P0_D1N P1_D1N P2_D1N P3_D1N P4_D1N P5_D1N P6_D1N P7_D1N P8_D1N P9_D1N P10_D1N P11_D1N	A_{DIFF}	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
P0_D2P P1_D2P P2_D2P P3_D2P P4_D2P P5_D2P P6_D2P P7_D2P P8_D2P P9_D2P P10_D2P P11_D2P	A_{DIFF}	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Table 636 • **Twisted Pair Interface Pins *(continued)***

Name	Type	Description
P0_D2N P1_D2N P2_D2N P3_D2N P4_D2N P5_D2N P6_D2N P7_D2N P8_D2N P9_D2N P10_D2N P11_D2N	A_{DIFF}	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
P0_D3P P1_D3P P2_D3P P3_D3P P4_D3P P5_D3P P6_D3P P7_D3P P8_D3P P9_D3P P10_D3P P11_D3P	A_{DIFF}	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
P0_D3N P1_D3N P2_D3N P3_D3N P4_D3N P5_D3N P6_D3N P7_D3N P8_D3N P9_D3N P10_D3N P11_D3N	A_{DIFF}	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).

13.3 Pins by Number for VSC7422XJQ-02

This section provides a numeric list of the VSC7422XJQ-02 pins.

1	VDD_AL_1
2	P8_D3N
3	P8_D3P
4	P8_D2N
5	P8_D2P
6	P8_D1N
7	P8_D1P
8	P8_D0N
9	P8_D0P
10	P9_D3N
11	P9_D3P
12	P9_D2N
13	P9_D2P
14	P9_D1N
15	P9_D1P
16	P9_D0N
17	P9_D0P
18	Ref_filt_2
19	Ref_rext_2
20	VDD_AL_2
21	P10_D3N
22	P10_D3P
23	P10_D2N
24	P10_D2P
25	P10_D1N
26	P10_D1P
27	P10_D0N
28	P10_D0P
29	P11_D3N
30	P11_D3P
31	P11_D2N
32	P11_D2P
33	P11_D1N
34	P11_D1P
35	P11_D0N
36	P11_D0P
37	VDD_AL_3
38	GPIO_31
39	VDD_IO_1
40	GPIO_29
41	GPIO_16
42	GPIO_15
43	GPIO_8
44	GPIO_7
45	GPIO_5
46	GPIO_4
47	GPIO_3
48	SI_DO
49	GPIO_1
50	GPIO_0
51	SI_nEn
52	SI_DI
53	SI_Clk
54	MDC
55	MDIO
56	VDD_IO_2
57	VDD_1
58	VDD_2
59	VDD_3
60	VDD_A_1
61	VDD_VS_1
62	VDD_VS_2
63	VDD_A_2
64	VDD_A_3
65	Reserved_23
66	Reserved_22
67	VDD_IO_3
68	VDD_A_4
69	RefClk_N
70	RefClk_P
71	VDD_A_5
72	VDD_A_6
73	VDD_VS_3
74	VDD_A_7
75	VDD_VS_4
76	VDD_4
77	VDD_5
78	VDD_6
79	VDD_VS_5
80	VDD_A_8
81	VDD_VS_6
82	VDD_A_9
83	VDD_IO_4
84	VDD_VS_7
85	VDD_A_10
86	VDD_7
87	VDD_8
88	VDD_9
89	VDD_10
90	VDD_11
91	VDD_A_11
92	VDD_VS_8
93	VDD_A_12
94	VDD_VS_9
95	VDD_A_13
96	VDD_VS_10
97	VDD_VS_11
98	VDD_A_14
99	VDD_12
100	VDD_13
101	VDD_14
102	VDD_15
103	VDD_VS_12
104	VDD_A_15
105	VDD_16
106	SerDes_Rext_0
107	SerDes_Rext_1
108	VDD_IO_5
109	VDD_17
110	VDD_18

Pins by number *(continued)*

111 VDD_19	150 P2_D3N	189 P5_D1N
112 VDD_20	151 P2_D3P	190 P5_D1P
113 VDD_21	152 P2_D2N	191 P5_D0N
114 VDD_22	153 P2_D2P	192 P5_D0P
115 VDD_23	154 P2_D1N	193 Ref_filt_1
116 VDD_24	155 P2_D1P	194 Ref_rext_1
117 VDD_25	156 P2_D0N	195 P6_D3N
118 VDD_26	157 P2_D0P	196 P6_D3P
119 VDD_27	158 P3_D3N	197 P6_D2N
120 VDD_28	159 P3_D3P	198 P6_D2P
121 VDD_29	160 VDD_AL_10	199 P6_D1N
122 VDD_30	161 P3_D2N	200 P6_D1P
123 VDD_31	162 P3_D2P	201 VDD_AL_12
124 VDD_32	163 P3_D1N	202 P6_D0N
125 VDD_33	164 P3_D1P	203 P6_D0P
126 VDD_AL_4	165 P3_D0N	204 P7_D3N
127 VDD_AL_5	166 P3_D0P	205 P7_D3P
128 VDD_AL_6	167 Reserved_5	206 P7_D2N
129 VDD_AL_7	168 Reserved_6	207 P7_D2P
130 VDD_AL_8	169 Reserved_7	208 P7_D1N
131 P0_D3N	170 Reserved_8	209 P7_D1P
132 P0_D3P	171 JTAG_TRST	210 P7_D0N
133 VDD_AL_9	172 JTAG_DO	211 P7_D0P
134 P0_D2N	173 JTAG_TMS	212 Reserved_12
135 P0_D2P	174 JTAG_DI	213 Reserved_13
136 P0_D1N	175 JTAG_CLK	214 COMA_MODE
137 P0_D1P	176 P4_D3N	215 RefClk_Sel2
138 P0_D0N	177 P4_D3P	216 RefClk_Sel0
139 P0_D0P	178 P4_D2N	217 RefClk_Sel1
140 P1_D3N	179 P4_D2P	218 Reserved_4
141 P1_D3P	180 P4_D1N	219 Reserved_29
142 P1_D2N	181 P4_D1P	220 VCORE_CFG2
143 P1_D2P	182 P4_D0N	221 VCORE_CFG1
144 P1_D1N	183 VDD_AL_11	222 VCORE_CFG0
145 P1_D1P	184 P4_D0P	223 VDD_IO_21
146 P1_D0N	185 P5_D3N	224 nRESET
147 P1_D0P	186 P5_D3P	A1 Reserved_15
148 Ref_filt_0	187 P5_D2N	A2 VDD_AH_1
149 Ref_rext_0	188 P5_D2P	A3 VDD_AH_2

Pins by number *(continued)*

A4	VDD_AH_3
A5	VDD_AH_4
A6	VSS_1
A7	VDD_AH_5
A8	VDD_AH_6
A9	VDD_AH_7
A10	VDD_34
A11	Reserved_24
A12	GPIO_30
A13	VSS_2
A14	GPIO_6
A15	GPIO_2
A16	Reserved_18
A17	Reserved_17
A18	VSS_163
A19	VSS_3
A20	SerDes_E3_RxP
A21	SerDes_E3_RxN
A22	SerDes_E3_TxP
A23	SerDes_E3_TxN
A24	VSS_4
A25	SerDes_E2_TxN
A26	SerDes_E2_TxP
A27	SerDes_E2_RxN
A28	SerDes_E2_RxP
A29	VSS_5
A30	SerDes_E1_RxP
A31	SerDes_E1_RxN
A32	SerDes_E1_TxP
A33	SerDes_E1_TxN
A34	VSS_6
A35	SerDes_E0_TxN
A36	SerDes_E0_TxP
A37	SerDes_E0_RxN
A38	SerDes_E0_RxP
A39	VSS_7
A40	VSS_8
A41	VSS_9
A42	VSS_10
A43	VDD_35
A44	VDD_36
A45	VDD_37
A46	VSS_11
A47	VDD_AH_8
A48	VDD_AH_9
A49	VDD_AH_10
A50	VDD_AH_11
A51	VDD_AH_12
A52	VSS_12
A53	VDD_AH_13
A54	VDD_AH_14
A55	VDD_AH_15
A56	Reserved_10
A57	Reserved_11
A58	VSS_13
A59	VDD_IO_6
A60	VDD_IO_7
A61	VDD_38
A62	VDD_39
A63	VSS_14
A64	VDD_AH_16
A65	VDD_AH_17
A66	VDD_AH_18
A67	VDD_AH_19
A68	VDD_AH_20
A69	VDD_AH_21
A70	VSS_15
A71	VDD_IO_8
A72	VDD_40
A73	VDD_41
A74	VSS_16
A75	VDD_IO_9
A76	VDD_IO_10
A77	VDD_IO_11
A78	Reserved_14

13.4 Pins by Name for VSC7422XJQ-02

This section provides an alphabetical list of the VSC7422XJQ-02 pins.

COMA_MODE	214
GPIO_0	50
GPIO_1	49
GPIO_2	A15
GPIO_3	47
GPIO_4	46
GPIO_5	45
GPIO_6	A14
GPIO_7	44
GPIO_8	43
GPIO_15	42
GPIO_16	41
GPIO_29	40
GPIO_30	A12
GPIO_31	38
JTAG_CLK	175
JTAG_DI	174
JTAG_DO	172
JTAG_TMS	173
JTAG_TRST	171
MDC	54
MDIO	55
nRESET	224
P0_D0N	138
P0_D0P	139
P0_D1N	136
P0_D1P	137
P0_D2N	134
P0_D2P	135
P0_D3N	131
P0_D3P	132
P1_D0N	146
P1_D0P	147
P1_D1N	144
P1_D1P	145
P1_D2N	142
P1_D2P	143
P1_D3N	140
P1_D3P	141
P2_D0N	156
P2_D0P	157
P2_D1N	154
P2_D1P	155
P2_D2N	152
P2_D2P	153
P2_D3N	150
P2_D3P	151
P3_D0N	165
P3_D0P	166
P3_D1N	163
P3_D1P	164
P3_D2N	161
P3_D2P	162
P3_D3N	158
P3_D3P	159
P4_D0N	182
P4_D0P	184
P4_D1N	180
P4_D1P	181
P4_D2N	178
P4_D2P	179
P4_D3N	176
P4_D3P	177
P5_D0N	191
P5_D0P	192
P5_D1N	189
P5_D1P	190
P5_D2N	187
P5_D2P	188
P5_D3N	185
P5_D3P	186
P6_D0N	202
P6_D0P	203
P6_D1N	199
P6_D1P	200
P6_D2N	197
P6_D2P	198
P6_D3N	195
P6_D3P	196
P7_D0N	210
P7_D0P	211
P7_D1N	208
P7_D1P	209
P7_D2N	206
P7_D2P	207
P7_D3N	204
P7_D3P	205
P8_D0N	8
P8_D0P	9
P8_D1N	6
P8_D1P	7
P8_D2N	4
P8_D2P	5
P8_D3N	2
P8_D3P	3
P9_D0N	16
P9_D0P	17
P9_D1N	14
P9_D1P	15
P9_D2N	12
P9_D2P	13
P9_D3N	10
P9_D3P	11
P10_D0N	27
P10_D0P	28
P10_D1N	25
P10_D1P	26
P10_D2N	23
P10_D2P	24
P10_D3N	21

Pins by name *(continued)*

P10_D3P	22
P11_D0N	35
P11_D0P	36
P11_D1N	33
P11_D1P	34
P11_D2N	31
P11_D2P	32
P11_D3N	29
P11_D3P	30
Ref_filt_0	148
Ref_filt_1	193
Ref_filt_2	18
Ref_rext_0	149
Ref_rext_1	194
Ref_rext_2	19
RefClk_N	69
RefClk_P	70
RefClk_Sel0	216
RefClk_Sel1	217
RefClk_Sel2	215
Reserved_4	218
Reserved_5	167
Reserved_6	168
Reserved_7	169
Reserved_8	170
Reserved_10	A56
Reserved_11	A57
Reserved_12	212
Reserved_13	213
Reserved_14	A78
Reserved_15	A1
Reserved_17	A17
Reserved_18	A16
Reserved_22	66
Reserved_23	65
Reserved_24	A11
Reserved_29	219
SerDes_E0_RxN	A37
SerDes_E0_RxP	A38
SerDes_E0_TxN	A35
SerDes_E0_TxP	A36
SerDes_E1_RxN	A31
SerDes_E1_RxP	A30
SerDes_E1_TxN	A33
SerDes_E1_TxP	A32
SerDes_E2_RxN	A27
SerDes_E2_RxP	A28
SerDes_E2_TxN	A25
SerDes_E2_TxP	A26
SerDes_E3_RxN	A21
SerDes_E3_RxP	A20
SerDes_E3_TxN	A23
SerDes_E3_TxP	A22
SerDes_Rext_0	106
SerDes_Rext_1	107
SI_Clk	53
SI_DI	52
SI_DO	48
SI_nEn	51
VCORE_CFG0	222
VCORE_CFG1	221
VCORE_CFG2	220
VDD_1	57
VDD_2	58
VDD_3	59
VDD_4	76
VDD_5	77
VDD_6	78
VDD_7	86
VDD_8	87
VDD_9	88
VDD_10	89
VDD_11	90
VDD_12	99
VDD_13	100
VDD_14	101
VDD_15	102
VDD_16	105
VDD_17	109
VDD_18	110
VDD_19	111
VDD_20	112
VDD_21	113
VDD_22	114
VDD_23	115
VDD_24	116
VDD_25	117
VDD_26	118
VDD_27	119
VDD_28	120
VDD_29	121
VDD_30	122
VDD_31	123
VDD_32	124
VDD_33	125
VDD_34	A10
VDD_35	A43
VDD_36	A44
VDD_37	A45
VDD_38	A61
VDD_39	A62
VDD_40	A72
VDD_41	A73
VDD_A_1	60
VDD_A_2	63
VDD_A_3	64
VDD_A_4	68
VDD_A_5	71
VDD_A_6	72
VDD_A_7	74
VDD_A_8	80
VDD_A_9	82
VDD_A_10	85
VDD_A_11	91
VDD_A_12	93
VDD_A_13	95
VDD_A_14	98

Pins by name *(continued)*

VDD_A_15	104
VDD_AH_1	A2
VDD_AH_2	A3
VDD_AH_3	A4
VDD_AH_4	A5
VDD_AH_5	A7
VDD_AH_6	A8
VDD_AH_7	A9
VDD_AH_8	A47
VDD_AH_9	A48
VDD_AH_10	A49
VDD_AH_11	A50
VDD_AH_12	A51
VDD_AH_13	A53
VDD_AH_14	A54
VDD_AH_15	A55
VDD_AH_16	A64
VDD_AH_17	A65
VDD_AH_18	A66
VDD_AH_19	A67
VDD_AH_20	A68
VDD_AH_21	A69
VDD_AL_1	1
VDD_AL_2	20
VDD_AL_3	37
VDD_AL_4	126
VDD_AL_5	127
VDD_AL_6	128
VDD_AL_7	129
VDD_AL_8	130
VDD_AL_9	133
VDD_AL_10	160
VDD_AL_11	183
VDD_AL_12	201
VDD_IO_1	39
VDD_IO_2	56
VDD_IO_3	67
VDD_IO_4	83
VDD_IO_5	108
VDD_IO_6	A59
VDD_IO_7	A60
VDD_IO_8	A71
VDD_IO_9	A75
VDD_IO_10	A76
VDD_IO_11	A77
VDD_IO_21	223
VDD_VS_1	61
VDD_VS_2	62
VDD_VS_3	73
VDD_VS_4	75
VDD_VS_5	79
VDD_VS_6	81
VDD_VS_7	84
VDD_VS_8	92
VDD_VS_9	94
VDD_VS_10	96
VDD_VS_11	97
VDD_VS_12	103
VSS_1	A6
VSS_2	A13
VSS_3	A19
VSS_4	A24
VSS_5	A29
VSS_6	A34
VSS_7	A39
VSS_8	A40
VSS_9	A41
VSS_10	A42
VSS_11	A46
VSS_12	A52
VSS_13	A58
VSS_14	A63
VSS_15	A70
VSS_16	A74
VSS_163	A18

14 Pin Descriptions for VSC7422XJG-02

The VSC7422XJG-02 device has 672 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

14.1 Pin Identifications

The following table lists the definitions for the pin type symbols.

Table 637 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ABIAS	Analog bias	Analog bias pin.
DIFF	Differential	Differential signal pair.
I	Input	Input signal.
O	Output	Output signal.
I/O	Bidirectional	Bidirectional input or output signal.
A	Analog input	Analog input for sensing variable voltage levels.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
3V		3.3 V-tolerant.
O	Output	Output signal.
OZ	3-state output	Output.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.
TD	Termination differential	Internal differential termination.

14.2 Pin Diagram for VSC7422XJG-02

The following illustration shows the pin diagram for the VSC7422XJG-02 device, as seen from the top view looking through the device. For clarity, the device is shown in two halves, the top left and top right.

Figure 77 • **VSC7422XJG-02 Pin Diagram, Top Left**

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	#N/A	P8_D0P	P8_D1P	P8_D2P	P8_D3P	P7_D0P	P7_D1P	P7_D2P	P7_D3P	P6_D0P	P6_D1P	P6_D2P	P6_D3P
B	VSS_1	P8_D0N	P8_D1N	P8_D2N	P8_D3N	P7_D0N	P7_D1N	P7_D2N	P7_D3N	P6_D0N	P6_D1N	P6_D2N	P6_D3N
C	P9_D3P	P9_D3N	COMA_MODE	nRESET	VDD_IO_21	VSS_178	VCORE_CFG0	VCORE_CFG1	VCORE_CFG2	Reserved_29	Reserved_4	RefClk_Sel0	RefClk_Sel1
D	P9_D2P	P9_D2N	Reserved_205	VDD_AH_1	VDD_AH_2	Reserved_206	Reserved_207	Reserved_208	Reserved_209	Reserved_248	VDD_AH_4	Reserved_211	Reserved_13
E	P9_D1P	P9_D1N	Reserved_216	VDD_AH_7	VDD_AH_8	VDD_IO_1	VDD_IO_2	VDD_AH_9	VDD_AL_1	VDD_AL_2	VDD_AH_10	VDD_AH_11	Ref_rext_1
F	P9_D0P	P9_D0N	Reserved_218	VDD_AH_17	VDD_AH_18	VDD_IO_5	VDD_AH_3	VDD_AH_19	VDD_AL_5	VDD_AL_6	VDD_AH_20	VDD_AH_21	Reserved_219
G	P10_D3P	P10_D3N	VSS_3	Reserved_15	VSS_4	VDD_1	VDD_2	VDD_3	VDD_AL_9	VDD_AL_10	VDD_4	VDD_5	Reserved_247
H	P10_D2P	P10_D2N	VSS_7	Reserved_14	VSS_8	VDD_11	VDD_12	VDD_13	VDD_14	VDD_15	VDD_16	VDD_17	Reserved_246
J	P10_D1P	P10_D1N	VDD_AH_27	VDD_AH_28	VDD_AL_13	VDD_AL_14	VDD_AL_15	Reserved_240	Reserved_241	Reserved_242	Reserved_243	Reserved_244	Reserved_245
K	P10_D0P	P10_D0N	VSS_11	Ref_rext_2	VDD_AL_19	VDD_AL_20	VDD_AL_21	VSS_12	VSS_13	VSS_14	VSS_15	VSS_16	VSS_17
L	P11_D3P	P11_D3N	VSS_25	Ref_filt_2	VSS_26	VDD_25	VDD_26	VSS_27	VSS_28	VSS_29	VSS_30	VSS_31	VSS_32
M	P11_D2P	P11_D2N	VDD_AH_31	VDD_AH_32	VDD_AH_33	VDD_29	VDD_30	VSS_41	VSS_42	VSS_43	VSS_44	VSS_45	VSS_46
N	P11_D1P	P11_D1N	VSS_53	VSS_54	VSS_55	VDD_33	VDD_34	VSS_56	VSS_57	VSS_58	VSS_59	VSS_60	VSS_61
P	P11_D0P	P11_D0N	VSS_71	Reserved_24	VDD_IO_7	VDD_37	VDD_38	VSS_72	VSS_73	VSS_74	VSS_75	VSS_76	VSS_77
R	GPIO_31	GPIO_30	GPIO_29	Reserved_190	VDD_IO_8	VDD_41	VDD_42	VSS_86	VSS_87	VSS_88	VSS_89	VSS_90	VSS_91
T	Reserved_189	Reserved_188	Reserved_187	Reserved_186	VDD_IO_9	VDD_45	VDD_46	VSS_98	VSS_99	VSS_100	VSS_101	VSS_102	VSS_103
U	Reserved_99	Reserved_98	Reserved_41	Reserved_40	VDD_IO_10	VSS_110	VSS_111	VSS_112	VSS_113	VSS_114	VSS_115	VSS_116	VSS_117
V	Reserved_39	Reserved_38	Reserved_37	GPIO_16	VDD_IO_11	VDD_49	VDD_50	VDD_51	VDD_52	VDD_53	VDD_54	VDD_55	VDD_56
W	GPIO_15	Reserved_36	Reserved_35	Reserved_34	VDD_IO_12	VDD_65	VDD_66	VDD_67	VDD_68	VDD_69	VDD_70	VDD_71	VDD_72
Y	Reserved_33	Reserved_32	Reserved_31	GPIO_8	VDD_IO_13	Reserved_146	Reserved_141	RefClk_P	SerDes_E3_TxP	Reserved_134	Reserved_129	VSS_126	SerDes_E2_TxP
AA	GPIO_7	GPIO_6	GPIO_5	GPIO_4	VDD_IO_14	Reserved_147	Reserved_140	RefClk_N	SerDes_E3_TxN	Reserved_135	Reserved_128	VSS_145	SerDes_E2_TxN
AB	GPIO_3	GPIO_2	GPIO_1	GPIO_0	VDD_IO_15	VSS_129	VSS_130	VSS_131	VSS_132	VSS_133	VSS_134	VSS_135	VSS_136
AC	SI_DO	SI_nEn	VSS_148	VDD_IO_16	VDD_IO_17	VDD_A_1	VDD_A_2	VDD_A_3	VDD_A_4	VDD_A_5	VDD_A_6	VDD_A_7	VDD_A_8
AD	SI_Clk	SI_DI	Reserved_18	VDD_IO_18	VSS_149	VDD_VS_1	VDD_VS_2	VDD_VS_3	VDD_VS_4	VDD_VS_5	VDD_VS_6	VDD_VS_7	VDD_VS_8
AE	VSS_151	Reserved_17	VDD_IO_19	VSS_163	VSS_152	Reserved_144	Reserved_143	Reserved_22	SerDes_E3_RxP	Reserved_132	Reserved_131	VSS_153	SerDes_E2_RxP
AF	#N/A	VDD_IO_20	MDIO	MDC	VSS_158	Reserved_145	Reserved_142	Reserved_23	SerDes_E3_RxN	Reserved_133	Reserved_130	VSS_159	SerDes_E2_RxN

Figure 78 • **VSC7422XJG-02 Pin Diagram, Top Right**

14	15	16	17	18	19	20	21	22	23	24	25	26	
P5_D0P	P5_D1P	P5_D2P	P5_D3P	P4_D0P	P4_D1P	P4_D2P	P4_D3P	P3_D0P	P3_D1P	P3_D2P	P3_D3P	#N/A	A
P5_D0N	P5_D1N	P5_D2N	P5_D3N	P4_D0N	P4_D1N	P4_D2N	P4_D3N	P3_D0N	P3_D1N	P3_D2N	P3_D3N	VSS_2	B
RefClk_Sel2	Reserved_8	Reserved_7	Reserved_6	Reserved_5	Reserved_201	Reserved_202	Reserved_203	Reserved_191	Reserved_192	Reserved_204	P2_D0N	P2_D0P	C
Reserved_12	Reserved_212	VDD_AH_5	JTAG_CLK	JTAG_DI	JTAG_DO	JTAG_TMS	JTAG_TRST	Reserved_213	Reserved_214	Reserved_215	P2_D1N	P2_D1P	D
Ref_filt_1	VDD_AH_12	VDD_AH_13	VDD_AL_3	VDD_AL_4	VDD_AH_14	VDD_IO_3	VDD_IO_4	VDD_AH_15	VDD_AH_16	Reserved_217	P2_D2N	P2_D2P	E
Reserved_220	VDD_AH_22	VDD_AH_23	VDD_AL_7	VDD_AL_8	VDD_AH_24	VDD_AH_6	VDD_IO_6	VDD_AH_25	VDD_AH_26	Reserved_221	P2_D3N	P2_D3P	F
Reserved_223	VDD_6	VDD_7	VDD_AL_11	VDD_AL_12	VDD_8	VDD_9	VDD_10	VSS_5	Reserved_10	VSS_6	P1_D0N	P1_D0P	G
Reserved_225	VDD_18	VDD_19	VDD_20	VDD_21	VDD_22	VDD_23	VDD_24	VSS_9	Reserved_11	VSS_10	P1_D1N	P1_D1P	H
Reserved_232	Reserved_233	Reserved_234	Reserved_235	Reserved_236	Reserved_237	VDD_AL_16	VDD_AL_17	VDD_AL_18	VDD_AH_29	VDD_AH_30	P1_D2N	P1_D2P	J
VSS_18	VSS_19	VSS_20	VSS_21	VSS_22	VSS_23	VDD_AL_22	VDD_AL_23	VDD_AL_24	Ref_rext_0	VSS_24	P1_D3N	P1_D3P	K
VSS_33	VSS_34	VSS_35	VSS_36	VSS_37	VSS_38	VDD_27	VDD_28	VSS_39	Ref_filt_0	VSS_40	P0_D0N	P0_D0P	L
VSS_47	VSS_48	VSS_49	VSS_50	VSS_51	VSS_52	VDD_31	VDD_32	VDD_AH_34	VDD_AH_35	VDD_AH_36	P0_D1N	P0_D1P	M
VSS_62	VSS_63	VSS_64	VSS_65	VSS_66	VSS_67	VDD_35	VDD_36	VSS_68	VSS_69	VSS_70	P0_D2N	P0_D2P	N
VSS_78	VSS_79	VSS_80	VSS_81	VSS_82	VSS_83	VDD_39	VDD_40	VSS_164	VSS_84	VSS_85	P0_D3N	P0_D3P	P
VSS_92	VSS_93	VSS_94	VSS_95	VSS_96	VSS_97	VDD_43	VDD_44	VSS_165	Reserved_20	Reserved_19	Reserved_148	VSS_179	R
VSS_104	VSS_105	VSS_106	VSS_107	VSS_108	VSS_109	VDD_47	VDD_48	VSS_166	Reserved_21	Reserved_166	Reserved_165	Reserved_164	T
VSS_118	VSS_119	VSS_120	VSS_121	VSS_122	VSS_123	VSS_124	VSS_125	VSS_167	Reserved_160	Reserved_162	Reserved_159	Reserved_161	U
VDD_57	VDD_58	VDD_59	VDD_60	VDD_61	VDD_62	VDD_63	VDD_64	VSS_168	Reserved_156	Reserved_158	Reserved_155	Reserved_157	V
VDD_73	VDD_74	VDD_75	VDD_76	VDD_77	VDD_78	VDD_79	VDD_80	VSS_169	Reserved_163	Reserved_154	Reserved_171	Reserved_153	W
Reserved_121	Reserved_118	VSS_127	SerDes_E1_TxP	Reserved_110	Reserved_105	VSS_128	SerDes_E0_TxP	VSS_170	Reserved_167	Reserved_168	Reserved_170	Reserved_172	Y
Reserved_120	Reserved_119	VSS_146	SerDes_E1_TxN	Reserved_111	Reserved_104	VSS_147	SerDes_E0_TxN	VSS_171	Reserved_173	Reserved_169	Reserved_150	Reserved_151	AA
VSS_137	VSS_138	VSS_139	VSS_140	VSS_141	VSS_142	VSS_143	VSS_144	VSS_172	Reserved_180	Reserved_152	Reserved_179	Reserved_182	AB
VDD_A_9	VDD_A_10	VDD_A_11	VDD_A_12	VDD_A_13	VDD_A_14	VDD_A_15	VDD_A_16	VSS_173	Reserved_178	Reserved_181	Reserved_184	Reserved_177	AC
VDD_VS_9	VDD_VS_10	VDD_VS_11	VDD_VS_12	VDD_VS_13	VDD_VS_14	VDD_VS_15	VDD_VS_16	VSS_150	VSS_174	Reserved_183	Reserved_175	Reserved_176	AD
Reserved_123	Reserved_116	VSS_154	SerDes_E1_RxP	Reserved_108	Reserved_107	VSS_155	SerDes_E0_RxP	SerDes_Rext_0	VSS_156	VSS_175	Reserved_174	VSS_157	AE
Reserved_122	Reserved_117	VSS_160	SerDes_E1_RxN	Reserved_109	Reserved_106	VSS_161	SerDes_E0_RxN	SerDes_Rext_1	VSS_162	VSS_177	VSS_176	#N/A	AF

14.3 Pins by Function for VSC7422XJG-02

This section contains the functional pin descriptions for the VSC7422XJG-02 device.

Functional Group	Name	Number	Type	Description
Analog Bias	Ref_filt_0	L23	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_1	E14	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_filt_2	L4	A	Reference filter. Connect a 1.0 µF external capacitor between each pin and ground.
Analog Bias	Ref_rext_0	K23	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	Ref_rext_1	E13	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.

Analog Bias	Ref_rext_2	K4	A	Reference external resistor. Connect a 2.0 kΩ (1%) resistor between each pin and ground.
Analog Bias	SerDes_Rext_0	AE22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Analog Bias	SerDes_Rext_1	AF22	A	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SerDes_Rext_1 and SerDes_Rext_0.
Enhanced SerDes Interface	SerDes_E0_RxN	AF21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_RxP	AE21	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E0_TxN	AA21	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E0_TxP	Y21	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E1_RxN	AF17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_RxP	AE17	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E1_TxN	AA17	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E1_TxP	Y17	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E2_RxN	AF13	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E2_RxP	AE13	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E2_TxN	AA13	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E2_TxP	Y13	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E3_RxN	AF9	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E3_RxP	AE9	I, Diff, TD	Differential Enhanced SerDes data inputs.
Enhanced SerDes Interface	SerDes_E3_TxN	AA9	O, Diff	Differential Enhanced SerDes data outputs
Enhanced SerDes Interface	SerDes_E3_TxP	Y9	O, Diff	Differential Enhanced SerDes data outputs
General Purpose I/O	GPIO_0	AB4	I/O, PU, ST, 3V	Overlaid function 1: SIO_CLK.
General Purpose I/O	GPIO_1	AB3	I/O, PU, ST, 3V	Overlaid function 1: SIO_LD.
General Purpose I/O	GPIO_2	AB2	I/O, PU, ST, 3V	Overlaid function 1: SIO_DO.
General Purpose I/O	GPIO_3	AB1	I/O, PU, ST, 3V	Overlaid function 1: SIO_DI.
General Purpose I/O	GPIO_4	AA4	I/O, PU, ST, 3V	Overlaid function 1: TACHO.
General Purpose I/O	GPIO_5	AA3	I/O, PU, ST, 3V	Overlaid function 1: TWI_SCL.
General Purpose I/O	GPIO_6	AA2	I/O, PU, ST, 3V	Overlaid function 1: TWI_SDA.
General Purpose I/O	GPIO_7	AA1	I/O, PU, ST, 3V	General-purpose input/output.
General Purpose I/O	GPIO_8	Y4	I/O, PU, ST, 3V	Overlaid function 1: EXT_IRQ0.
General Purpose I/O	GPIO_15	W1	I/O, PU, ST, 3V	MIIM slave mode: SLV_MDC.
General Purpose I/O	GPIO_16	V4	I/O, PU, ST, 3V	MIIM slave mode: SLV_MDIO.
General Purpose I/O	GPIO_29	R3	I/O, PU, ST, 3V	Overlaid function 1: PWM.
General Purpose I/O	GPIO_30	R2	I/O, PU, ST, 3V	Overlaid function 1: UART_TX.
General Purpose I/O	GPIO_31	R1	I/O, PU, ST, 3V	Overlaid function 1: UART_RX.
JTAG Interface	JTAG_CLK	D17	I, PU, ST, 3V	JTAG clock.
JTAG Interface	JTAG_DI	D18	I, PU, ST, 3V	JTAG test data in.
JTAG Interface	JTAG_DO	D19	OZ, 3V	JTAG test data out.
JTAG Interface	JTAG_TMS	D20	I, PU, ST, 3V	JTAG test mode select.
JTAG Interface	JTAG_TRST	D21	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.

MII Management Interface	MDC	AF4	O, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
MII Management Interface	MDIO	AF3	I/O, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the device.
Miscellaneous	COMA_MODE	C3	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered-down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. Additionally, this signal is used to synchronize the operation of multiple devices on the same printed circuit board to provide visual synchronization for LEDs driven from the separate devices.
Miscellaneous	nRESET	C4	I, PD, ST, 3V	Global device reset, active low.
Miscellaneous	VCORE_CFG0	C7	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Miscellaneous	VCORE_CFG1	C8	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Miscellaneous	VCORE_CFG2	C9	I, PD, ST, 3V	Configuration signals for controlling the VCore-Ie CPU functions.
Power Supply	VDD_1	G6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_2	G7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_3	G8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_4	G11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_5	G12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_6	G15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_7	G16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_8	G19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_9	G20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_10	G21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_11	H6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_12	H7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_13	H8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_14	H9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_15	H10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_16	H11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_17	H12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_18	H15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_19	H16	Power	1.0 V power supply voltage for core.

Power Supply	VDD_20	H17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_21	H18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_22	H19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_23	H20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_24	H21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_25	L6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_26	L7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_27	L20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_28	L21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_29	M6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_30	M7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_31	M20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_32	M21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_33	N6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_34	N7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_35	N20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_36	N21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_37	P6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_38	P7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_39	P20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_40	P21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_41	R6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_42	R7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_43	R20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_44	R21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_45	T6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_46	T7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_47	T20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_48	T21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_49	V6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_50	V7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_51	V8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_52	V9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_53	V10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_54	V11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_55	V12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_56	V13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_57	V14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_58	V15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_59	V16	Power	1.0 V power supply voltage for core.
Power Supply	VDD_60	V17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_61	V18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_62	V19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_63	V20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_64	V21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_65	W6	Power	1.0 V power supply voltage for core.
Power Supply	VDD_66	W7	Power	1.0 V power supply voltage for core.
Power Supply	VDD_67	W8	Power	1.0 V power supply voltage for core.
Power Supply	VDD_68	W9	Power	1.0 V power supply voltage for core.
Power Supply	VDD_69	W10	Power	1.0 V power supply voltage for core.
Power Supply	VDD_70	W11	Power	1.0 V power supply voltage for core.
Power Supply	VDD_71	W12	Power	1.0 V power supply voltage for core.
Power Supply	VDD_72	W13	Power	1.0 V power supply voltage for core.
Power Supply	VDD_73	W14	Power	1.0 V power supply voltage for core.
Power Supply	VDD_74	W15	Power	1.0 V power supply voltage for core.
Power Supply	VDD_75	W16	Power	1.0 V power supply voltage for core.

Power Supply	VDD_76	W17	Power	1.0 V power supply voltage for core.
Power Supply	VDD_77	W18	Power	1.0 V power supply voltage for core.
Power Supply	VDD_78	W19	Power	1.0 V power supply voltage for core.
Power Supply	VDD_79	W20	Power	1.0 V power supply voltage for core.
Power Supply	VDD_80	W21	Power	1.0 V power supply voltage for core.
Power Supply	VDD_A_1	AC6	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_2	AC7	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_3	AC8	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_4	AC9	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_5	AC10	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_6	AC11	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_7	AC12	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_8	AC13	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_9	AC14	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_10	AC15	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_11	AC16	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_12	AC17	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_13	AC18	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_14	AC19	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_15	AC20	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_A_16	AC21	Power	1.0 V power supply voltage for analog circuits.
Power Supply	VDD_AH_1	D4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_2	D5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_3	F7	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_4	D11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_5	D16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_6	F20	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_7	E4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_8	E5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_9	E8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.

Power Supply	VDD_AH_10	E11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_11	E12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_12	E15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_13	E16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_14	E19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_15	E22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_16	E23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_17	F4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_18	F5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_19	F8	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_20	F11	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_21	F12	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_22	F15	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_23	F16	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_24	F19	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_25	F22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_26	F23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_27	J3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_28	J4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_29	J23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_30	J24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_31	M3	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_32	M4	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_33	M5	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_34	M22	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_35	M23	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AH_36	M24	Power	2.5 V power supply voltage for analog driver in twisted pair interface.
Power Supply	VDD_AL_1	E9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.

Power Supply	VDD_AL_2	E10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_3	E17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_4	E18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_5	F9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_6	F10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_7	F17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_8	F18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_9	G9	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_10	G10	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_11	G17	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_12	G18	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_13	J5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_14	J6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_15	J7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_16	J20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_17	J21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_18	J22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_19	K5	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_20	K6	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_21	K7	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_22	K20	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_23	K21	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_AL_24	K22	Power	1.0 V power supply voltage for analog circuits for twisted pair interface.
Power Supply	VDD_IO_1	E6	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_2	E7	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_3	E20	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_4	E21	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_5	F6	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.

Power Supply	VDD_IO_6	F21	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_7	P5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_8	R5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_9	T5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_10	U5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_11	V5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_12	W5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_13	Y5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_14	AA5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_15	AB5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_16	AC4	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_17	AC5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_18	AD4	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_19	AE3	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_20	AF2	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_IO_21	C5	Power	2.5 V power supply for MII Management, and miscellaneous I/Os.
Power Supply	VDD_VS_1	AD6	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_2	AD7	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_3	AD8	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_4	AD9	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_5	AD10	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_6	AD11	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_7	AD12	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_8	AD13	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_9	AD14	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_10	AD15	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_11	AD16	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_12	AD17	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.

Power Supply	VDD_VS_13	AD18	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_14	AD19	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_15	AD20	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VDD_VS_16	AD21	Power	1.0 V or 1.2 V power supply for Enhanced SerDes interfaces.
Power Supply	VSS_1	B1	Ground	Ground reference.
Power Supply	VSS_2	B26	Ground	Ground reference.
Power Supply	VSS_3	G3	Ground	Ground reference.
Power Supply	VSS_4	G5	Ground	Ground reference.
Power Supply	VSS_5	G22	Ground	Ground reference.
Power Supply	VSS_6	G24	Ground	Ground reference.
Power Supply	VSS_7	H3	Ground	Ground reference.
Power Supply	VSS_8	H5	Ground	Ground reference.
Power Supply	VSS_9	H22	Ground	Ground reference.
Power Supply	VSS_10	H24	Ground	Ground reference.
Power Supply	VSS_11	K3	Ground	Ground reference.
Power Supply	VSS_12	K8	Ground	Ground reference.
Power Supply	VSS_13	K9	Ground	Ground reference.
Power Supply	VSS_14	K10	Ground	Ground reference.
Power Supply	VSS_15	K11	Ground	Ground reference.
Power Supply	VSS_16	K12	Ground	Ground reference.
Power Supply	VSS_17	K13	Ground	Ground reference.
Power Supply	VSS_18	K14	Ground	Ground reference.
Power Supply	VSS_19	K15	Ground	Ground reference.
Power Supply	VSS_20	K16	Ground	Ground reference.
Power Supply	VSS_21	K17	Ground	Ground reference.
Power Supply	VSS_22	K18	Ground	Ground reference.
Power Supply	VSS_23	K19	Ground	Ground reference.
Power Supply	VSS_24	K24	Ground	Ground reference.
Power Supply	VSS_25	L3	Ground	Ground reference.
Power Supply	VSS_26	L5	Ground	Ground reference.
Power Supply	VSS_27	L8	Ground	Ground reference.
Power Supply	VSS_28	L9	Ground	Ground reference.
Power Supply	VSS_29	L10	Ground	Ground reference.
Power Supply	VSS_30	L11	Ground	Ground reference.
Power Supply	VSS_31	L12	Ground	Ground reference.
Power Supply	VSS_32	L13	Ground	Ground reference.
Power Supply	VSS_33	L14	Ground	Ground reference.
Power Supply	VSS_34	L15	Ground	Ground reference.
Power Supply	VSS_35	L16	Ground	Ground reference.
Power Supply	VSS_36	L17	Ground	Ground reference.
Power Supply	VSS_37	L18	Ground	Ground reference.
Power Supply	VSS_38	L19	Ground	Ground reference.
Power Supply	VSS_39	L22	Ground	Ground reference.
Power Supply	VSS_40	L24	Ground	Ground reference.
Power Supply	VSS_41	M8	Ground	Ground reference.
Power Supply	VSS_42	M9	Ground	Ground reference.
Power Supply	VSS_43	M10	Ground	Ground reference.
Power Supply	VSS_44	M11	Ground	Ground reference.
Power Supply	VSS_45	M12	Ground	Ground reference.
Power Supply	VSS_46	M13	Ground	Ground reference.
Power Supply	VSS_47	M14	Ground	Ground reference.
Power Supply	VSS_48	M15	Ground	Ground reference.

Power Supply	VSS_49	M16	Ground	Ground reference.
Power Supply	VSS_50	M17	Ground	Ground reference.
Power Supply	VSS_51	M18	Ground	Ground reference.
Power Supply	VSS_52	M19	Ground	Ground reference.
Power Supply	VSS_53	N3	Ground	Ground reference.
Power Supply	VSS_54	N4	Ground	Ground reference.
Power Supply	VSS_55	N5	Ground	Ground reference.
Power Supply	VSS_56	N8	Ground	Ground reference.
Power Supply	VSS_57	N9	Ground	Ground reference.
Power Supply	VSS_58	N10	Ground	Ground reference.
Power Supply	VSS_59	N11	Ground	Ground reference.
Power Supply	VSS_60	N12	Ground	Ground reference.
Power Supply	VSS_61	N13	Ground	Ground reference.
Power Supply	VSS_62	N14	Ground	Ground reference.
Power Supply	VSS_63	N15	Ground	Ground reference.
Power Supply	VSS_64	N16	Ground	Ground reference.
Power Supply	VSS_65	N17	Ground	Ground reference.
Power Supply	VSS_66	N18	Ground	Ground reference.
Power Supply	VSS_67	N19	Ground	Ground reference.
Power Supply	VSS_68	N22	Ground	Ground reference.
Power Supply	VSS_69	N23	Ground	Ground reference.
Power Supply	VSS_70	N24	Ground	Ground reference.
Power Supply	VSS_71	P3	Ground	Ground reference.
Power Supply	VSS_72	P8	Ground	Ground reference.
Power Supply	VSS_73	P9	Ground	Ground reference.
Power Supply	VSS_74	P10	Ground	Ground reference.
Power Supply	VSS_75	P11	Ground	Ground reference.
Power Supply	VSS_76	P12	Ground	Ground reference.
Power Supply	VSS_77	P13	Ground	Ground reference.
Power Supply	VSS_78	P14	Ground	Ground reference.
Power Supply	VSS_79	P15	Ground	Ground reference.
Power Supply	VSS_80	P16	Ground	Ground reference.
Power Supply	VSS_81	P17	Ground	Ground reference.
Power Supply	VSS_82	P18	Ground	Ground reference.
Power Supply	VSS_83	P19	Ground	Ground reference.
Power Supply	VSS_84	P23	Ground	Ground reference.
Power Supply	VSS_85	P24	Ground	Ground reference.
Power Supply	VSS_86	R8	Ground	Ground reference.
Power Supply	VSS_87	R9	Ground	Ground reference.
Power Supply	VSS_88	R10	Ground	Ground reference.
Power Supply	VSS_89	R11	Ground	Ground reference.
Power Supply	VSS_90	R12	Ground	Ground reference.
Power Supply	VSS_91	R13	Ground	Ground reference.
Power Supply	VSS_92	R14	Ground	Ground reference.
Power Supply	VSS_93	R15	Ground	Ground reference.
Power Supply	VSS_94	R16	Ground	Ground reference.
Power Supply	VSS_95	R17	Ground	Ground reference.
Power Supply	VSS_96	R18	Ground	Ground reference.
Power Supply	VSS_97	R19	Ground	Ground reference.
Power Supply	VSS_98	T8	Ground	Ground reference.
Power Supply	VSS_99	T9	Ground	Ground reference.
Power Supply	VSS_100	T10	Ground	Ground reference.
Power Supply	VSS_101	T11	Ground	Ground reference.
Power Supply	VSS_102	T12	Ground	Ground reference.
Power Supply	VSS_103	T13	Ground	Ground reference.
Power Supply	VSS_104	T14	Ground	Ground reference.

Power Supply	VSS_105	T15	Ground	Ground reference.
Power Supply	VSS_106	T16	Ground	Ground reference.
Power Supply	VSS_107	T17	Ground	Ground reference.
Power Supply	VSS_108	T18	Ground	Ground reference.
Power Supply	VSS_109	T19	Ground	Ground reference.
Power Supply	VSS_110	U6	Ground	Ground reference.
Power Supply	VSS_111	U7	Ground	Ground reference.
Power Supply	VSS_112	U8	Ground	Ground reference.
Power Supply	VSS_113	U9	Ground	Ground reference.
Power Supply	VSS_114	U10	Ground	Ground reference.
Power Supply	VSS_115	U11	Ground	Ground reference.
Power Supply	VSS_116	U12	Ground	Ground reference.
Power Supply	VSS_117	U13	Ground	Ground reference.
Power Supply	VSS_118	U14	Ground	Ground reference.
Power Supply	VSS_119	U15	Ground	Ground reference.
Power Supply	VSS_120	U16	Ground	Ground reference.
Power Supply	VSS_121	U17	Ground	Ground reference.
Power Supply	VSS_122	U18	Ground	Ground reference.
Power Supply	VSS_123	U19	Ground	Ground reference.
Power Supply	VSS_124	U20	Ground	Ground reference.
Power Supply	VSS_125	U21	Ground	Ground reference.
Power Supply	VSS_126	Y12	Ground	Ground reference.
Power Supply	VSS_127	Y16	Ground	Ground reference.
Power Supply	VSS_128	Y20	Ground	Ground reference.
Power Supply	VSS_129	AB6	Ground	Ground reference.
Power Supply	VSS_130	AB7	Ground	Ground reference.
Power Supply	VSS_131	AB8	Ground	Ground reference.
Power Supply	VSS_132	AB9	Ground	Ground reference.
Power Supply	VSS_133	AB10	Ground	Ground reference.
Power Supply	VSS_134	AB11	Ground	Ground reference.
Power Supply	VSS_135	AB12	Ground	Ground reference.
Power Supply	VSS_136	AB13	Ground	Ground reference.
Power Supply	VSS_137	AB14	Ground	Ground reference.
Power Supply	VSS_138	AB15	Ground	Ground reference.
Power Supply	VSS_139	AB16	Ground	Ground reference.
Power Supply	VSS_140	AB17	Ground	Ground reference.
Power Supply	VSS_141	AB18	Ground	Ground reference.
Power Supply	VSS_142	AB19	Ground	Ground reference.
Power Supply	VSS_143	AB20	Ground	Ground reference.
Power Supply	VSS_144	AB21	Ground	Ground reference.
Power Supply	VSS_145	AA12	Ground	Ground reference.
Power Supply	VSS_146	AA16	Ground	Ground reference.
Power Supply	VSS_147	AA20	Ground	Ground reference.
Power Supply	VSS_148	AC3	Ground	Ground reference.
Power Supply	VSS_149	AD5	Ground	Ground reference.
Power Supply	VSS_150	AD22	Ground	Ground reference.
Power Supply	VSS_151	AE1	Ground	Ground reference.
Power Supply	VSS_152	AE5	Ground	Ground reference.
Power Supply	VSS_153	AE12	Ground	Ground reference.
Power Supply	VSS_154	AE16	Ground	Ground reference.
Power Supply	VSS_155	AE20	Ground	Ground reference.
Power Supply	VSS_156	AE23	Ground	Ground reference.
Power Supply	VSS_157	AE26	Ground	Ground reference.
Power Supply	VSS_158	AF5	Ground	Ground reference.
Power Supply	VSS_159	AF12	Ground	Ground reference.
Power Supply	VSS_160	AF16	Ground	Ground reference.

Power Supply	VSS_161	AF20	Ground	Ground reference.
Power Supply	VSS_162	AF23	Ground	Ground reference.
Power Supply	VSS_163	AE4	Ground	Ground reference.
Power Supply	VSS_164	P22	Ground	Ground reference.
Power Supply	VSS_165	R22	Ground	Ground reference.
Power Supply	VSS_166	T22	Ground	Ground reference.
Power Supply	VSS_167	U22	Ground	Ground reference.
Power Supply	VSS_168	V22	Ground	Ground reference.
Power Supply	VSS_169	W22	Ground	Ground reference.
Power Supply	VSS_170	Y22	Ground	Ground reference.
Power Supply	VSS_171	AA22	Ground	Ground reference.
Power Supply	VSS_172	AB22	Ground	Ground reference.
Power Supply	VSS_173	AC22	Ground	Ground reference.
Power Supply	VSS_174	AD23	Ground	Ground reference.
Power Supply	VSS_175	AE24	Ground	Ground reference.
Power Supply	VSS_176	AF25	Ground	Ground reference.
Power Supply	VSS_177	AF24	Ground	Ground reference.
Power Supply	VSS_178	C6	Ground	Ground reference.
Power Supply	VSS_179	R26	Ground	Ground reference.
Reserved	Reserved_4	C11	I, PD, ST, 3V	Tie to VSS.
Reserved	Reserved_5	C18	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_6	C17	I, PD, ST, 3V	Tie to VSS.
Reserved	Reserved_7	C16	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_8	C15	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_10	G23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_11	H23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_12	D14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_13	D13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_14	H4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_15	G4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_17	AE2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_18	AD3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_19	R24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_20	R23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_21	T23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_22	AE8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_23	AF8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_24	P4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_29	C10	I, PD, ST, 3V	Tie to VDD_IO.
Reserved	Reserved_31	Y3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_32	Y2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_33	Y1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_34	W4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_35	W3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_36	W2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_37	V3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_38	V2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_39	V1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_40	U4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_41	U3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_98	U2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_99	U1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_104	AA19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_105	Y19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_106	AF19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_107	AE19	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_108	AE18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_109	AF18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_110	Y18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_111	AA18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_116	AE15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_117	AF15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_118	Y15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_119	AA15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_120	AA14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_121	Y14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_122	AF14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_123	AE14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_128	AA11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_129	Y11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_130	AF11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_131	AE11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_132	AE10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_133	AF10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_134	Y10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_135	AA10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_140	AA7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_141	Y7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_142	AF7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_143	AE7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_144	AE6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_145	AF6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_146	Y6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_147	AA6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_148	R25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_150	AA25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_151	AA26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_152	AB24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_153	W26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_154	W24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_155	V25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_156	V23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_157	V26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_158	V24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_159	U25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_160	U23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_161	U26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_162	U24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_163	W23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_164	T26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_165	T25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_166	T24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_167	Y23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_168	Y24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_169	AA24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_170	Y25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_171	W25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_172	Y26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_173	AA23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_174	AE25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_175	AD25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_176	AD26	I, PD, ST, 3V	Leave floating.

Reserved	Reserved_177	AC26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_178	AC23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_179	AB25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_180	AB23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_181	AC24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_182	AB26	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_183	AD24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_184	AC25	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_186	T4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_187	T3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_188	T2	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_189	T1	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_190	R4	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_191	C22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_192	C23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_201	C19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_202	C20	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_203	C21	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_204	C24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_205	D3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_206	D6	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_207	D7	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_208	D8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_209	D9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_211	D12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_212	D15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_213	D22	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_214	D23	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_215	D24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_216	E3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_217	E24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_218	F3	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_219	F13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_220	F14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_221	F24	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_223	G14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_225	H14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_232	J14	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_233	J15	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_234	J16	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_235	J17	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_236	J18	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_237	J19	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_240	J8	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_241	J9	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_242	J10	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_243	J11	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_244	J12	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_245	J13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_246	H13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_247	G13	I, PD, ST, 3V	Leave floating.
Reserved	Reserved_248	D10	I, PD, ST, 3V	Leave floating.

Serial CPU Interface	SI_Clk	AD1	I/O, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.
Serial CPU Interface	SI_DI	AD2	I, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
Serial CPU Interface	SI_DO	AC1	OZ, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.
Serial CPU Interface	SI_nEn	AC2	I/O, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-Ie CPU system. Released when booting is completed.
System Clock Interface	RefClk_N	AA8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.
System Clock Interface	RefClk_P	Y8	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.

System Clock Interface	RefClk_Sel0	C12	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
System Clock Interface	RefClk_Sel1	C13	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
System Clock Interface	RefClk_Sel2	C14	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
Twisted Pair Interface	P0_D0N	L25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P0_D0P	L26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Twisted Pair Interface	P0_D1N	M25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P0_D1P	M26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P0_D2N	N25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D2P	N26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D3N	P25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P0_D3P	P26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P1_D0N	G25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P1_D0P	G26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P1_D1N	H25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P1_D1P	H26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P1_D2N	J25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D2P	J26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P1_D3N	K25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P1_D3P	K26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D0N	C25	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P2_D0P	C26	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P2_D1N	D25	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P2_D1P	D26	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.

Twisted Pair Interface	P2_D2N	E25	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D2P	E26	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D3N	F25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P2_D3P	F26	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D0N	B22	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P3_D0P	A22	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Twisted Pair Interface	P3_D1N	B23	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P3_D1P	A23	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P3_D2N	B24	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D2P	A24	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D3N	B25	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P3_D3P	A25	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P4_D0N	B18	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P4_D0P	A18	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P4_D1N	B19	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P4_D1P	A19	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P4_D2N	B20	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D2P	A20	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P4_D3N	B21	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P4_D3P	A21	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D0N	B14	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P5_D0P	A14	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P5_D1N	B15	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P5_D1P	A15	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.

Twisted Pair Interface	P5_D2N	B16	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D2P	A16	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D3N	B17	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P5_D3P	A17	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D0N	B10	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P6_D0P	A10	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Twisted Pair Interface	P6_D1N	B11	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P6_D1P	A11	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P6_D2N	B12	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D2P	A12	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3N	B13	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P6_D3P	A13	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P7_D0N	B6	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P7_D0P	A6	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P7_D1N	B7	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P7_D1P	A7	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P7_D2N	B8	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D2P	A8	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P7_D3N	B9	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P7_D3P	A9	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D0N	B2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P8_D0P	A2	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P8_D1N	B3	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P8_D1P	A3	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.

Twisted Pair Interface	P8_D2N	B4	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D2P	A4	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D3N	B5	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P8_D3P	A5	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D0N	F2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P9_D0P	F1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.

Twisted Pair Interface	P9_D1N	E2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P9_D1P	E1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P9_D2N	D2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D2P	D1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D3N	C2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P9_D3P	C1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P10_D0N	K2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P10_D0P	K1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P10_D1N	J2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P10_D1P	J1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
Twisted Pair Interface	P10_D2N	H2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D2P	H1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).

Twisted Pair Interface	P10_D3N	G2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P10_D3P	G1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D0N	P2	ADIFF	Tx/Rx channel A negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
Twisted Pair Interface	P11_D0P	P1	ADIFF	Tx/Rx channel A positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
Twisted Pair Interface	P11_D1N	N2	ADIFF	Tx/Rx channel B negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6
Twisted Pair Interface	P11_D1P	N1	ADIFF	Tx/Rx channel B positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.

Twisted Pair Interface	P11_D2N	M2	ADIFF	Tx/Rx channel C negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D2P	M1	ADIFF	Tx/Rx channel C positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D3N	L2	ADIFF	Tx/Rx channel D negative signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes).
Twisted Pair Interface	P11_D3P	L1	ADIFF	Tx/Rx channel D positive signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mbps mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes).

15 Package Information

VSC7420XJQ-02, VSC7421XJQ-02, VSC7422XJQ-02, VSC7420XJQ-04, VSC7421XJQ-04, and VSC7422XJQ-04 are packaged in a lead-free (Pb-free), 302-pin, plastic thin quad flat package (TQFP) with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height.

VSC7420XJG-02, VSC7421XJG-02, VSC7422XJG-02, VSC7420XJG-04, VSC7421XJG-04, and VSC7422XJG-04 are packaged in a lead-free (Pb-free), 672-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height.

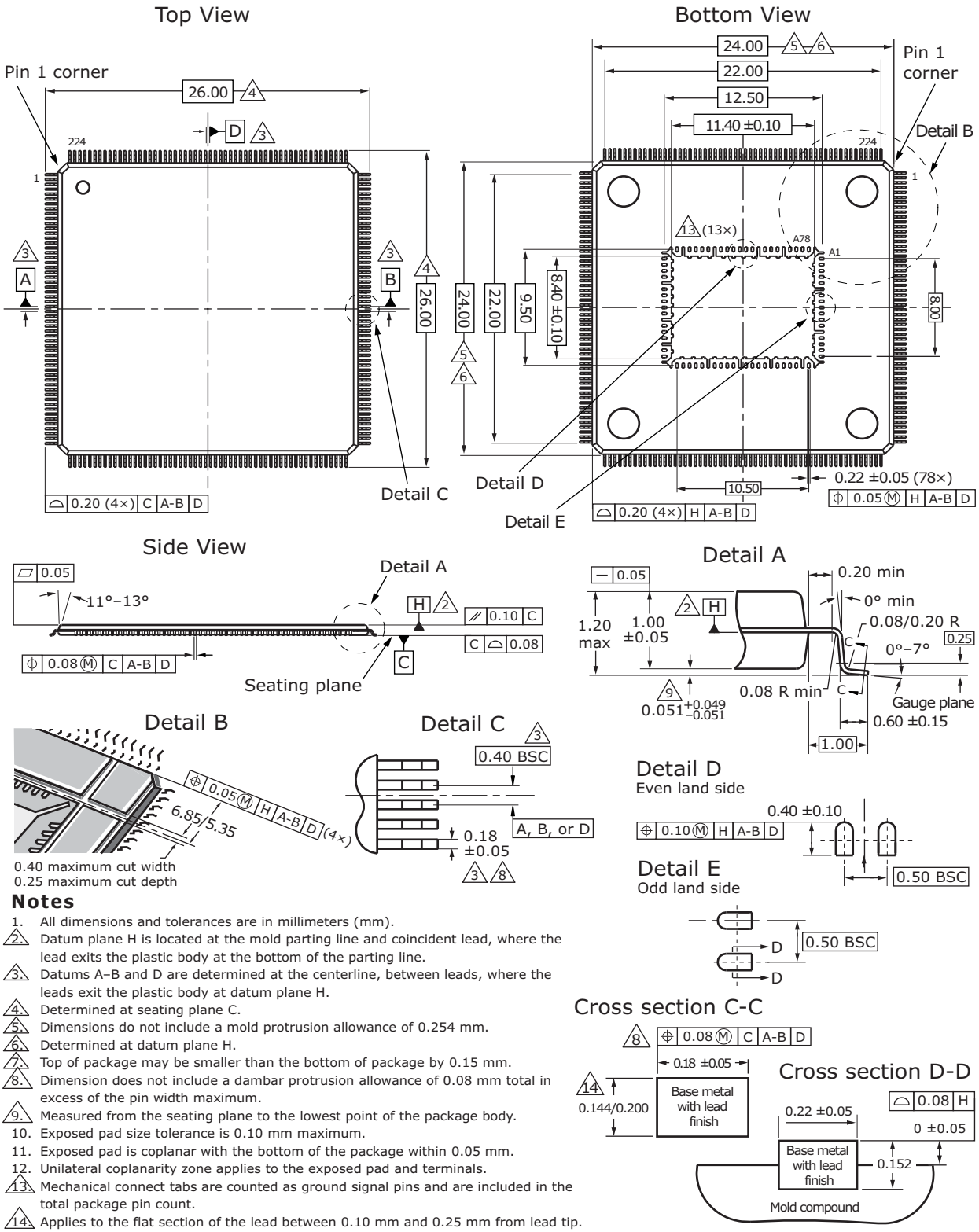
Lead-free products comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawings, thermal specifications, and moisture sensitivity rating for the VSC7420XJQ-02, VSC7421XJQ-02, VSC7422XJQ-02, VSC7420XJQ-04, VSC7421XJQ-04, VSC7422XJQ-04, VSC7420XJG-02, VSC7421XJG-02, VSC7422XJG-02, VSC7420XJG-04, VSC7421XJG-04, and VSC7422XJG-04 devices.

15.1 Package Drawing

The following illustrations show the package drawings for the VSC7420XJQ-02, VSC7421XJQ-02, VSC7422XJQ-02, VSC7420XJQ-04, VSC7421XJQ-04, VSC7422XJQ-04, VSC7420XJG-02, VSC7421XJG-02, VSC7422XJG-02, VSC7420XJG-04, VSC7421XJG-04, and VSC7422XJG-04 devices. The drawings contain the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

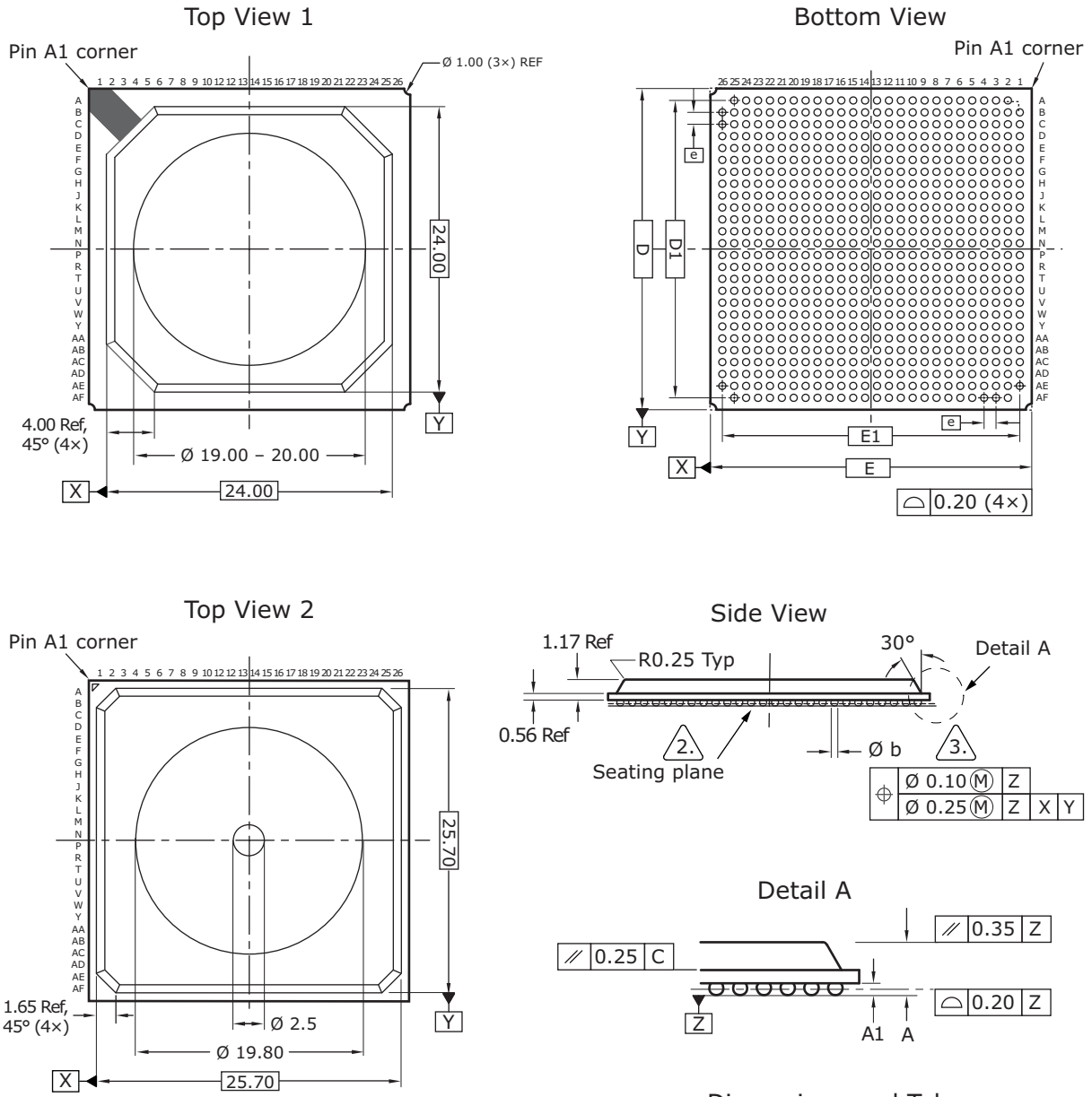
Figure 79 • **Package Drawing TQFP**



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Datum plane H is located at the mold parting line and coincident lead, where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and D are determined at the centerline, between leads, where the leads exit the plastic body at datum plane H.
4. Determined at seating plane C.
5. Dimensions do not include a mold protrusion allowance of 0.254 mm.
6. Determined at datum plane H.
7. Top of package may be smaller than the bottom of package by 0.15 mm.
8. Dimension does not include a dambar protrusion allowance of 0.08 mm total in excess of the pin width maximum.
9. Measured from the seating plane to the lowest point of the package body.
10. Exposed pad size tolerance is 0.10 mm maximum.
11. Exposed pad is coplanar with the bottom of the package within 0.05 mm.
12. Unilateral coplanarity zone applies to the exposed pad and terminals.
13. Mechanical connect tabs are counted as ground signal pins and are included in the total package pin count.
14. Applies to the flat section of the lead between 0.10 mm and 0.25 mm from lead tip.

Figure 80 • **Package Drawing BGA**



Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A	2.10	2.23	2.44
A1	0.40	0.50	0.60
D		27.00	
E		27.00	
D1		25.00	
E1		25.00	
e		1.00	
3. b	0.50	0.60	0.70

Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Radial true position is represented by typical values.
5. Top view 1 and top view 2 reflect one of two packages customers can expect to receive.

15.2 Thermal Specifications

Thermal specifications for these devices are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are

modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for these devices, see the JESD51-1 standard.

Table 638 • **Thermal Resistances TQFP**

Symbol	°C/W	Parameter
θ_{JCtop}	5.13	Die junction to package case top
θ_{JB}	7.86	Die junction to printed circuit board
θ_{JA}	15.39	Die junction to ambient
θ_{JMA} at 1 m/s	11.53	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	9.34	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using QFP packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

Table 639 • **Thermal Resistances BGA**

Symbol	°C/W	Parameter
θ_{JCtop}	3.27	Die junction to package case top
θ_{JB}	6.03	Die junction to printed circuit board
θ_{JA}	12.14	Die junction to ambient
θ_{JMA} at 1 m/s	9.42	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	8	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using BGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

15.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

16 Design Guidelines

This section provides information about design guidelines for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

16.1 Power Supplies

The following guidelines apply to designing power supplies for use with the VSC7420-02, VSC7421-02, and VSC7422-02 devices:

- Make at least one unbroken ground plane (GND).
- Use the power and ground plane combination as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the separation between the planes. Typical values with a 0.25 mm (0.01 inch) separation are 100 pF/in2. This capacitance is more effective than a capacitor of equivalent value, because the planes have no inductance or Equivalent Series Resistance (ESR).
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances in a configuration that maintains the integrity of the plane. Groups of vias spaced close together often overlap clearances. This can form a large slot in the plane. As a result, return currents are forced around the slot, which increases the loop area and EMI emissions. Signals should never be placed on a ground plane, because the resulting slot forces return currents around the slot.
- Vias connecting power planes to the supply and ground balls must be at least 0.25 mm (0.010 inch) in diameter, preferably with no thermal relief and plated closed with copper or solder. Use separate (or even multiple) vias for each supply and ground ball.

16.2 Power Supply Decoupling

Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended capacitors are as follows:

- For bulk decoupling, use 10 µF high capacity and low ESR capacitors or equivalent, distributed across the board.
- For high-frequency decoupling, use 0.1 µF high frequency (for example, X7R) ceramic capacitors placed on the side of the PCB closest to the plane being decoupled, and as close as possible to the power ball. A larger value in the same housing unit produces even better results.
- Use surface-mounted components for lower lead inductance and pad capacitance. Smaller form factor components are best (that is, 0402 is better than 0603).

16.3 Reference Clock

The device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements of this interface. For more information, see Reference Clock, page 421.

16.3.1 Single-Ended RefClk Input

An external resistor network is required to use a single-ended reference clock. The network limits the amplitude and adjusts the center of the swing.

The following illustrations show configurations for a single-ended reference clock.

Figure 81 • **2.5 V CMOS Single-Ended RefClk Input Resistor Network**

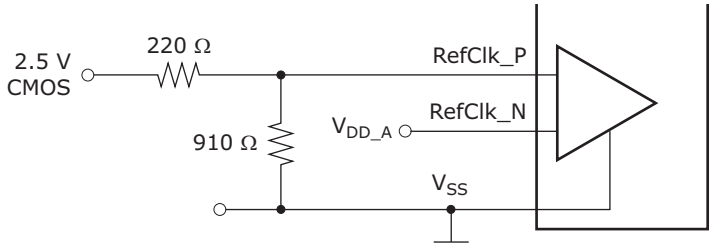
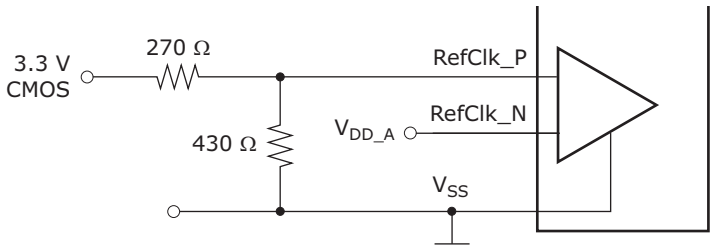


Figure 82 • **3.3 V CMOS Single-Ended RefClk Input Resistor Network**



16.4 Interfaces

This section provides general recommendations for all interfaces and information related to the specific interfaces on the device.

16.4.1 General Recommendations

High-speed signals require excellent frequency and phase response up to the third harmonic. The best design would provide excellent frequency and phase response up to the seventh harmonic. The following recommendations can improve signal quality and minimize transmission distances:

Keep traces as short as possible. Initial component placement should be considered very carefully.

- The impedance of the traces must match the impedance of the termination resistors, connectors, and cable. This reduces reflections due to impedance mismatches.
- Differential impedance must be maintained in a 100 Ω differential application. Routing two 50 Ω traces is not adequate. The two traces must be separated by enough distance to maintain differential impedance. When routing differential pairs, keep the two trace lengths identical. Differences in trace lengths translate directly into signal skew. Note that the differential impedance may be affected when separations occur.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.
- Do not group all the passive components together. The pads of the components add capacitance to the traces. At the frequencies encountered, this can result in unwanted reductions in impedance. Use surface-mounted 0603 components to reduce this effect.
- Eliminate or reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from other traces.
- Keep signal traces away from other signals that might capacitively couple noise into the signals. A good rule of thumb is to keep the traces apart by ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the high-speed transmitter and receiver signals.
- Using grounded guard traces is typically not effective for improving signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout, but remove them prior to design completion. This has the benefit of enforcing keep-out areas around sensitive high-speed signals so that vias and other traces are not accidentally placed incorrectly.
- When signals in a differential pair are mismatched, the result is a common-mode current. In a well-designed system, common-mode currents should make up less than one percent of the total differential currents. Mode currents represent a primary source of EMI emissions. To reduce common-mode currents, route differential traces so that their lengths are the same. For example, a

5-mm (0.2-inch) length mismatch between differential signals having the rise and fall times of 200 ps results in the common-mode current being up to 18% of the differential current.

Note Care must be taken when choosing proper components (such as the termination resistors) in the designing of the layout of a printed circuit board, because of the high application frequency. The use of surface-mount components is highly recommended to minimize parasitic inductance and lead length of the termination resistor.

Matching the impedance of the PCB traces, connectors, and balanced interconnect media is also highly recommended. Impedance variations along the entire interconnect path must be minimized, because they degrade the signal path and may cause reflections of the signal.

16.4.2 SGMII Interface

The SGMII interface consists of a Tx and Rx differential pair operating at 1250 Mbps.

The SGMII signals can be routed on any PCB trace layer with the following constraints:

- The Tx output signals in a pair should have matched electrical lengths.
- The Rx input signals in a pair should have matched electrical lengths.
- SGMII Tx and Rx pairs must be routed as 100 Ω differential traces with ground plane as reference.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.
- AC-coupling of Tx and Rx may be needed, depending on the PHY. If AC-coupled, the inputs are self-biased.
- To reduce the crosstalk between pairs or other PCB lines, it is recommended that the spacing on each side of the pair be larger than four times the track width.

16.4.3 Serial Interface

If the serial CPU interface is not used, all input signals can be left floating.

The SI bus consists of the SI_Clk clock signal, the SI_DO and SI_DI data signals, and the SI_nCS0 device select signal.

When routing the SI_Clk signal, be sure to create clean edges. If the SI bus is connected to more than one slave device, route it in a daisy-chain configuration with no stubs. Terminate the SI_Clk signal properly to avoid reflections and double clocking.

If it is not possible (or desirable) to route the bus in a daisy-chain configuration, the SI_Clk signal should be buffered and routed in a star topology from the buffers. Each buffered clock should be terminated at its source.

The SI tristates the SI_Clk and SI_DO signals prior to deasserting the SI_nCS0 signal. This makes it possible to implement CPOL/CPHA as 0/0 or 1/1, if the attached SI devices require it, using termination resistors. If the attached devices support both types of CPOL/CPHA, SI_Clk and SI_DO must still have pull resistors to one of the I/O supply rails to prevent spurious clocks being seen when the signals are tristated.

16.4.4 Enhanced SerDes Interface

The Enhanced SerDes interface can be used for fiber connections, backplanes, or direct coupler cable connections, such as the CX4 cable.

The Enhanced SerDes interface can operate in several modes. The physical signal bit rate is between 125 Mbps to 6.25 Mbps.

The inputs are self-biased and have internal AC-coupling. In some modes, the interface requires external AC-coupling, because of the input DC voltage limitation. If external AC-coupling capacitors are required, it is recommended to use small form factor components, such as 0603. The small form factor minimizes impedance mismatch by the AC-coupling capacitors, because the size of the form factor approximately matches the trace width commonly used for these signals.

The Enhanced SerDes interface can be directly connected to either 1 Gbps or 2.5 Gbps SFP modules. For these applications, external AC-coupling capacitors are not required, because the SFP module already includes capacitors.

The following table lists the AC-coupling requirements for common Enhanced SerDes connections.

Table 640 • **Enhanced SerDes Interface Coupling Requirements**

Enhanced SerDes Connection	Mode	External AC-Coupling Requirement
SFP modules	SFP	Not required
SGMII PHY	SGMII	Required(1)
Enhanced SerDes device	Enhanced SerDes	Required

1. AC-coupling is not required with direct connection to the VSC8512 PHY device.

The Enhanced SerDes interface signals must be routed as a differential pair, with a 100 Ω differential characteristic impedance. The differential intrapair skew must be below 5 ps in the PCB trace.

To minimize crosstalk between transmitter and receiver, equal drive strength is recommended in both devices in a link.

To minimize crosstalk between differential pairs, the characteristic differential impedance of the signals must be determined only by the distance to the reference plane and the intra-pair coupling and not the distance to the neighboring traces. To separate the transmitter and receiver signals to minimize crosstalk, it is recommended to route the transmitter and receiver signals on as many different PCB layers as feasible.

16.4.5 Two-Wire Serial Interface

The two-wire serial interface is capable of suppressing small amplitude glitches less than 5 ns in duration, which is less than the 50 ns duration often quoted for similar interfaces. Because the two-wire serial implementation uses Schmitt-triggered inputs, the VSC7420-02, VSC7421-02, and VSC7422-02 devices have a greater tolerance to low amplitude noise. For glitch-free operation, select the proper pull-up resistor value to ensure that the transition time through the input switching region is less than 5 ns given the line's total capacitive load. For capacitive loads up to 40 pF, a pull-up resistor of 510 Ω or less ensures glitch-free operation for noise levels up to 700 mV peak-to-peak.

17 Design Considerations

This section provides information about the design considerations for the VSC7420-02, VSC7421-02, and VSC7422-02 devices.

17.1 10BASE-T mode unable to re-establish link

10BASE-T mode is unable to re-establish link with the following devices if the link drops while sending data: SparX-III™ and Caracal™ family of switches, VSC8512-02, VSC8522-02, VSC8522-12, VSC8504, VSC8552, VSC8572, and VSC8574. No issue is observed for other link partner devices. The probability of this error occurring is low except in a test environment.

The workaround is to contact Microsemi for the current API software release.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100054.

17.2 Software script for link performance

Software script is required for improved link performance. PHY ports may exhibit suboptimal performance. Contact Microsemi for a script to be applied during system initialization.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100034.

17.3 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages. This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100036.

17.4 Clause 45 register 7.60

Clause 45, register 7.60, bit 10 reads back as a logic 1. This is a reserved bit in the standard and should be ignored by software.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100037.

17.5 Clause 45 register 3.22

Clause 45, register 3.22 is cleared upon read only when extended page access register (register 31) is set to 0. This register cannot be read when page access register is set to a value other than 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.22.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100038.

17.6 Clause 45 register 3.1

Clause 45, register 3.1, Rx and Tx LPI received bits are cleared upon read only when extended page access register (register 31) is set to 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.1.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100039.

17.7 Clause 45 register address post-increment

Clause 45 register address post-increment only works when reading registers and only when the extended page access register (register 31) is set to 0. The estimated impact is low, as there are very few Clause 45 registers in a Gigabit PHY, and they can be addressed individually.

The workaround is to access Clause 45 registers individually.

This item was previously published in the VSC7420-02, VSC7421-02, and VSC7422-02 *Errata revision 1.0* as EA100040.

18 Ordering Information

The devices are offered with two operating temperature ranges. The range for VSC7420-02, VSC7421-02, and VSC7422-02 is 0 °C ambient to 125 °C junction. The range for VSC7420-04, VSC7421-04, and VSC7422-04 is –40 °C ambient to 125 °C junction.

VSC7420XJQ-02, VSC7421XJQ-02, VSC7422XJQ-02, VSC7420XJQ-04, VSC7421XJQ-04, and VSC7422XJQ-04 are packaged in a lead-free (Pb-free), 302-pin, plastic thin quad flat package (TQFP) with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height.

VSC7420XJG-02, VSC7421XJG-02, VSC7422XJG-02, VSC7420XJG-04, VSC7421XJG-04, and VSC7422XJG-04 are packaged in a lead-free (Pb-free), 672-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height.

Lead-free products comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information.

Table 641 • **Ordering Information: TQFP Package**

Part Order Number	Description
VSC7420XJQ-02	10-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7420XJQ-04	10-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.
VSC7421XJQ-02	16-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7421XJQ-04	16-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.
VSC7422XJQ-02	26-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7422XJQ-04	26-port Gigabit Ethernet switch Lead-free, 302-pin plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.

Table 642 • **Ordering Information: BGA Package**

Part Order Number	Description
VSC7420XJG-02	10-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7420XJG-04	10-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.
VSC7421XJG-02	16-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7421XJG-04	16-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.
VSC7422XJG-02	26-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC7422XJG-04	26-port Gigabit Ethernet switch Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.36 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.

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