



**THE DATASHEET OF
PSMN0R7-25YLDX**





PSMN0R7-25YLD

N-channel 25 V, 0.72 mΩ, 300 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

25 July 2017

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- 100% Avalanche tested at $I_{(AS)} = 190$ A
- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 μ A leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 150 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$		-	-	25	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	158	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	0.76	0.92	mΩ

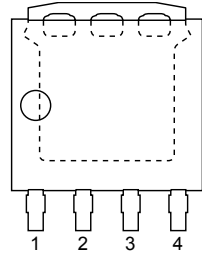
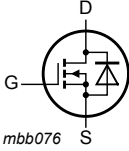
N-channel 25 V, 0.72 mΩ, 300 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	-	11.9	-	nC

[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	Gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN0R7-25YLD	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56); 4 leads	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN0R7-25YLD	0D725L

8. Limiting values

Table 5. Limiting values

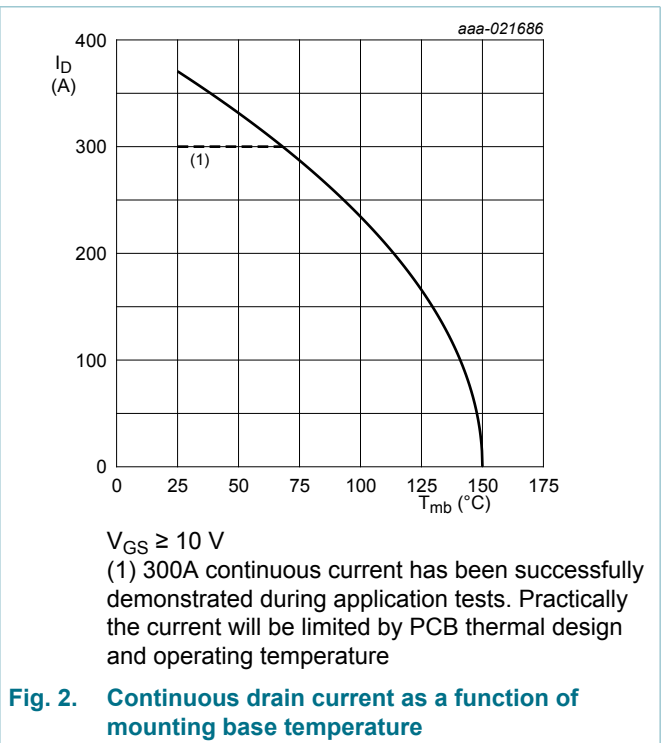
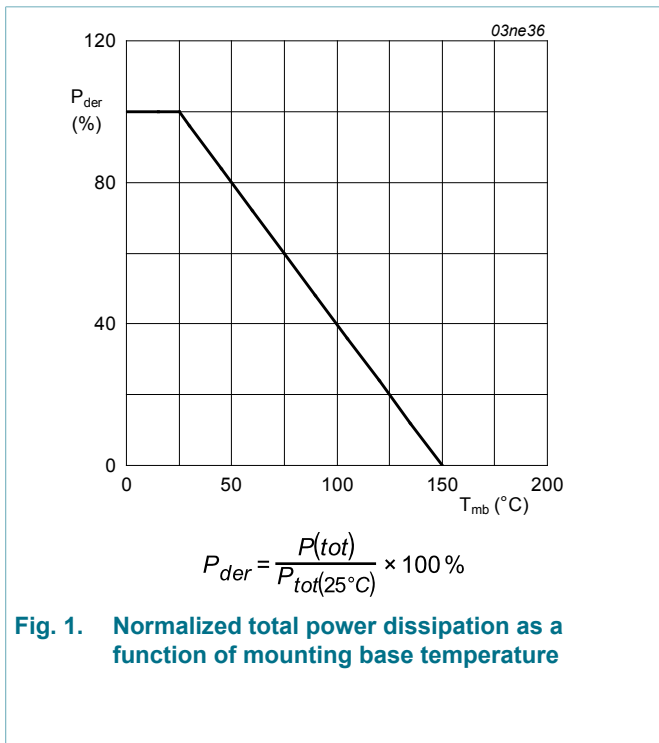
In accordance with the Absolute Maximum Rating System (IEC 60134).

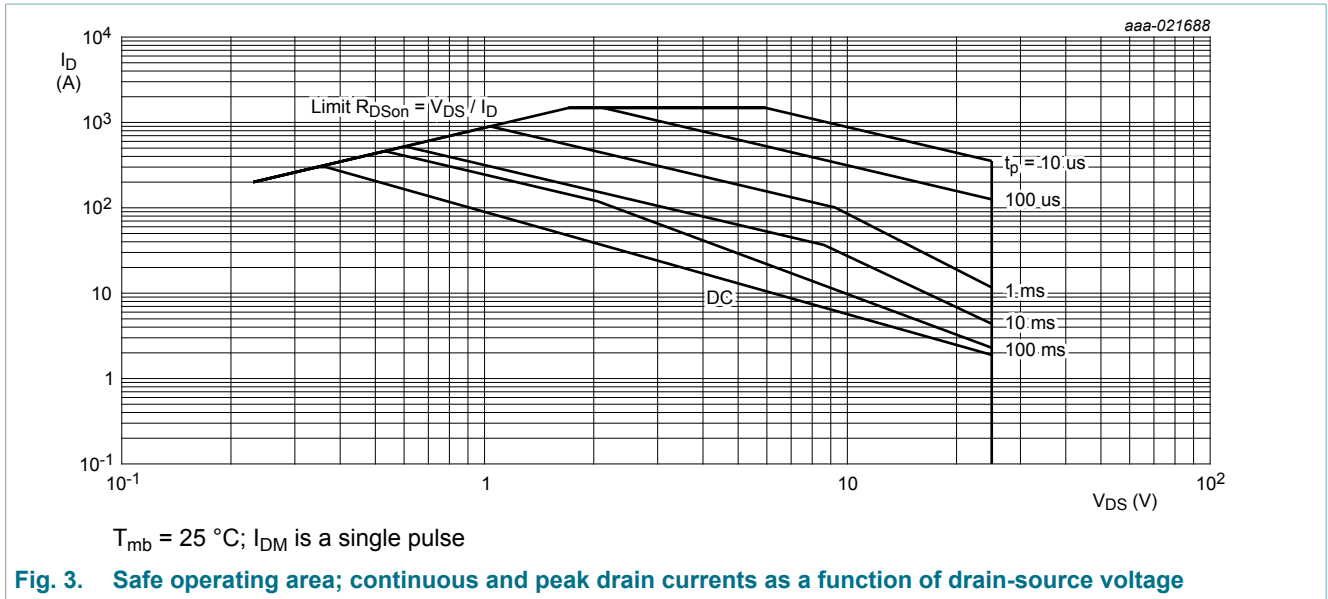
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V

N-channel 25 V, 0.72 mΩ, 300 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	158	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	300	A
		V _{GS} = 10 V; T _{mb} = 100 °C		-	235	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1482	A
T _{stg}	storage temperature			-55	150	°C
T _j	junction temperature			-55	150	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	132	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1482	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 300 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 36 μs		-	174	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 25 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	190	A

- [1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature
- [2] Protected by 100% test

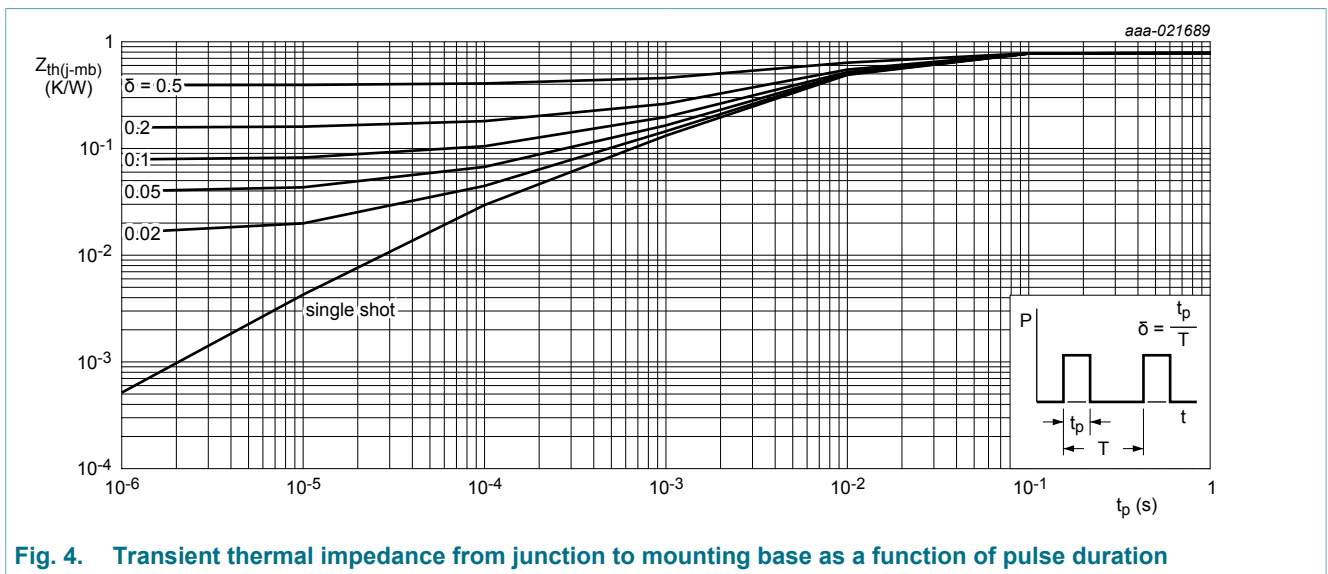




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.59	0.79	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W



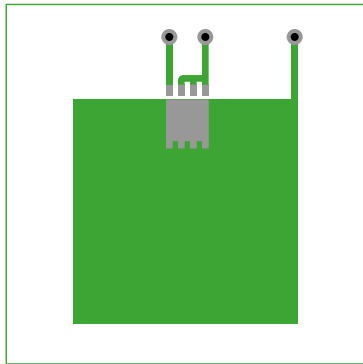


Fig. 5. PCB layout for thermal impedance junction to ambient 1" square pad; FR4 Board; 2oz copper

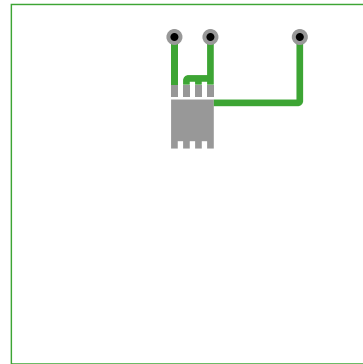


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.66	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-5.1	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	68.5	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	0.76	0.92	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	1.47	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	0.57	0.72	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	1.15	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.35	-	Ω

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 12 ; Fig. 13	-	110.2	-	nC	
		I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13	-	50.9	-	nC	
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	45.8	-	nC	
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13	-	18.8	-	nC	
Q _{GS(th)}	pre-threshold gate-source charge		-	11.9	-	nC	
Q _{GS(th-pl)}	post-threshold gate-source charge		-	6.9	-	nC	
Q _{GD}	gate-drain charge		-	11.9	-	nC	
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 12 V; Fig. 12 ; Fig. 13	-	2.6	-	V	
C _{iss}	input capacitance	V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 14	-	8320	-	pF	
C _{oss}	output capacitance		-	2982	-	pF	
C _{rss}	reverse transfer capacitance		-	522	-	pF	
t _{d(on)}	turn-on delay time		V _{DS} = 12 V; R _L = 0.6 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω	-	42.2	-	ns
t _r	rise time		-	48.3	-	ns	
t _{d(off)}	turn-off delay time		-	53.1	-	ns	
t _f	fall time		-	38.2	-	ns	
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 12 V; f = 1 MHz; T _j = 25 °C	-	54	-	nC	
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 15	-	0.77	1.2	V	
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 12 V; Fig. 16	-	57.7	-	ns	
Q _r	recovered charge		[1]	-	83.2	-	nC
t _a	reverse recovery rise time		-	-	30.5	-	ns
t _b	reverse recovery fall time		-	-	27.2	-	ns
S	softness factor		-	-	0.9	-	

[1] includes capacitive recovery

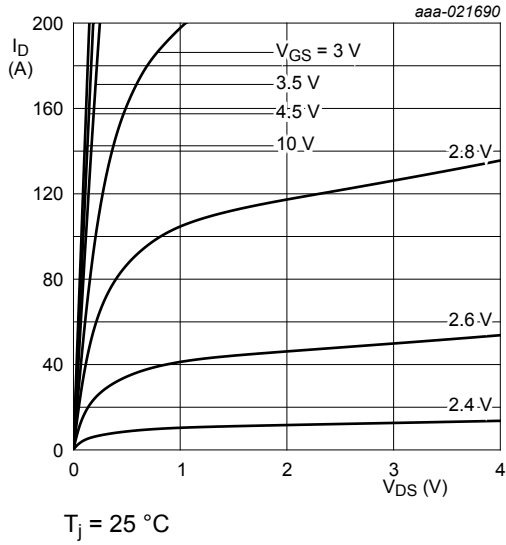


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

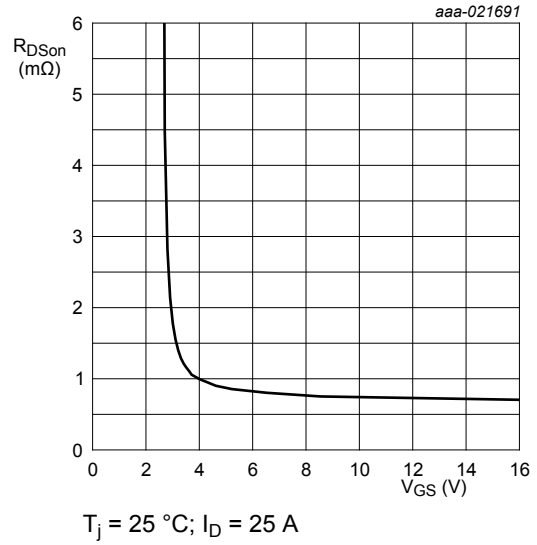


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

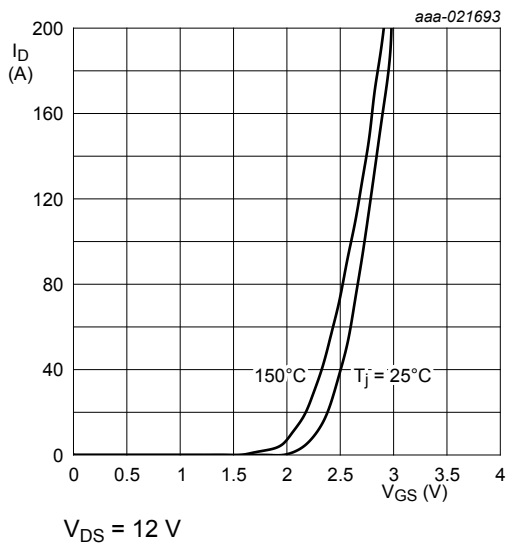


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

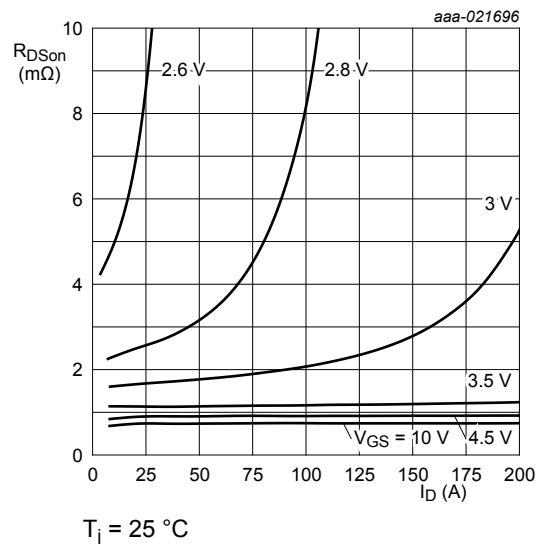
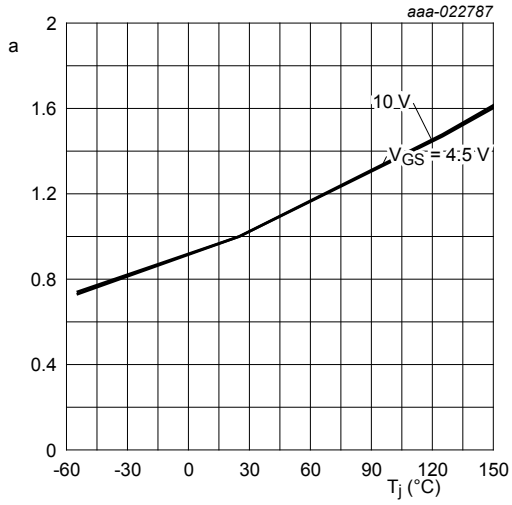
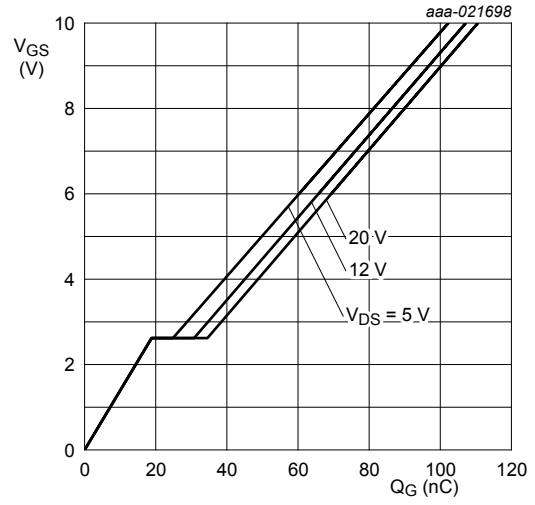


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig. 12. Gate-source voltage as a function of gate charge; typical values

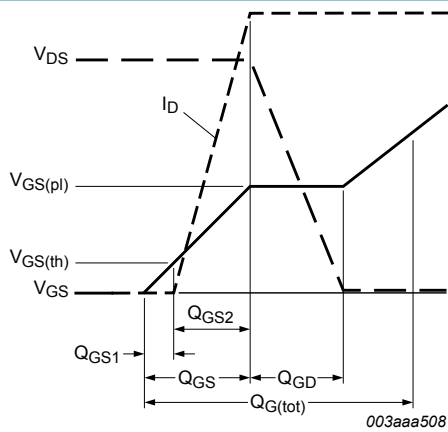
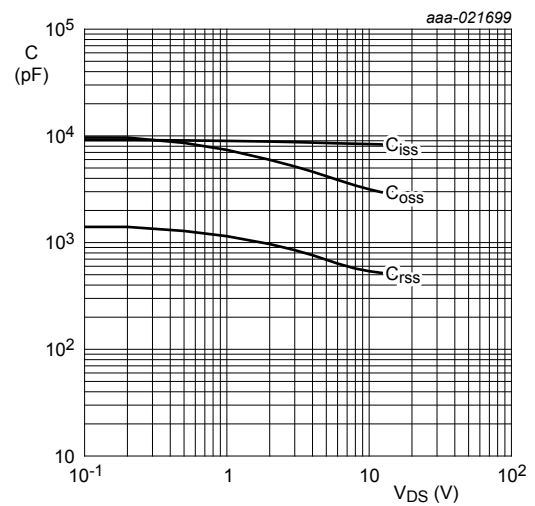


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

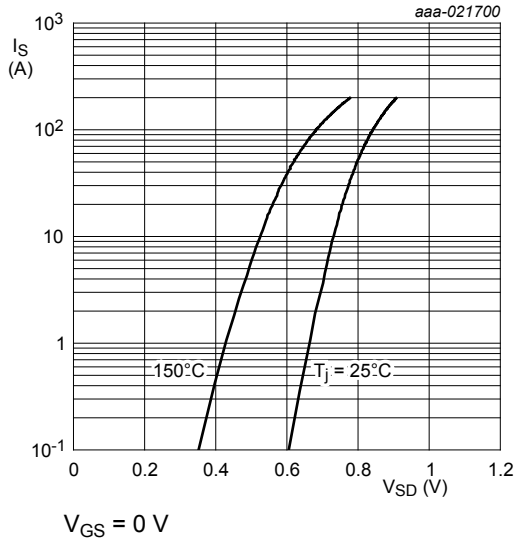


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

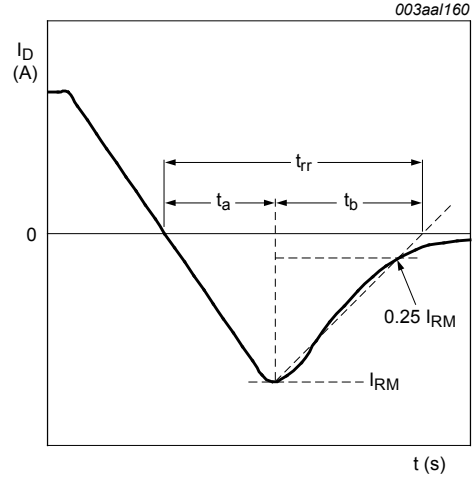


Fig. 16. Reverse recovery timing definition

11. Package outline

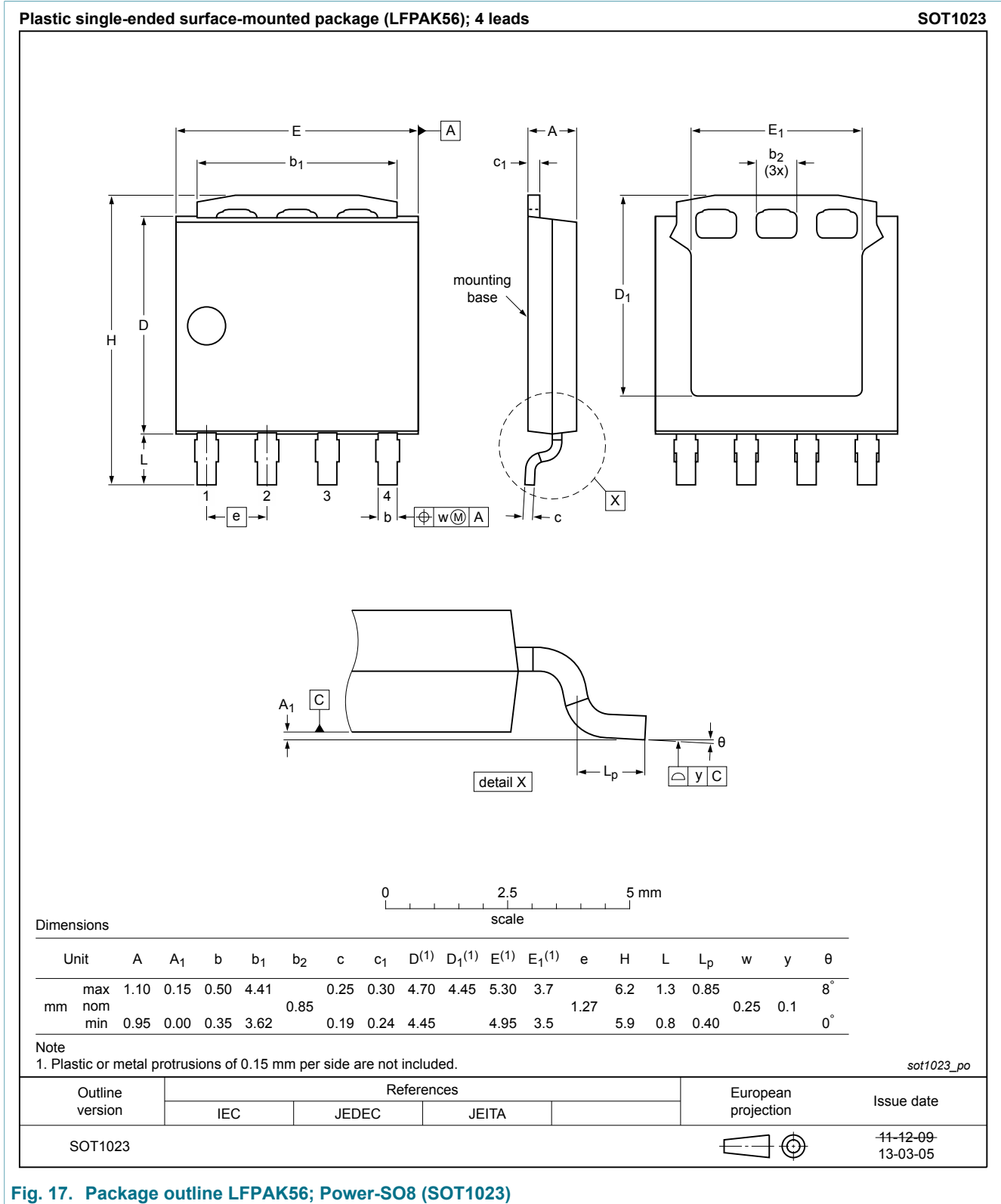


Fig. 17. Package outline LPAK56; Power-SO8 (SOT1023)

12. Soldering

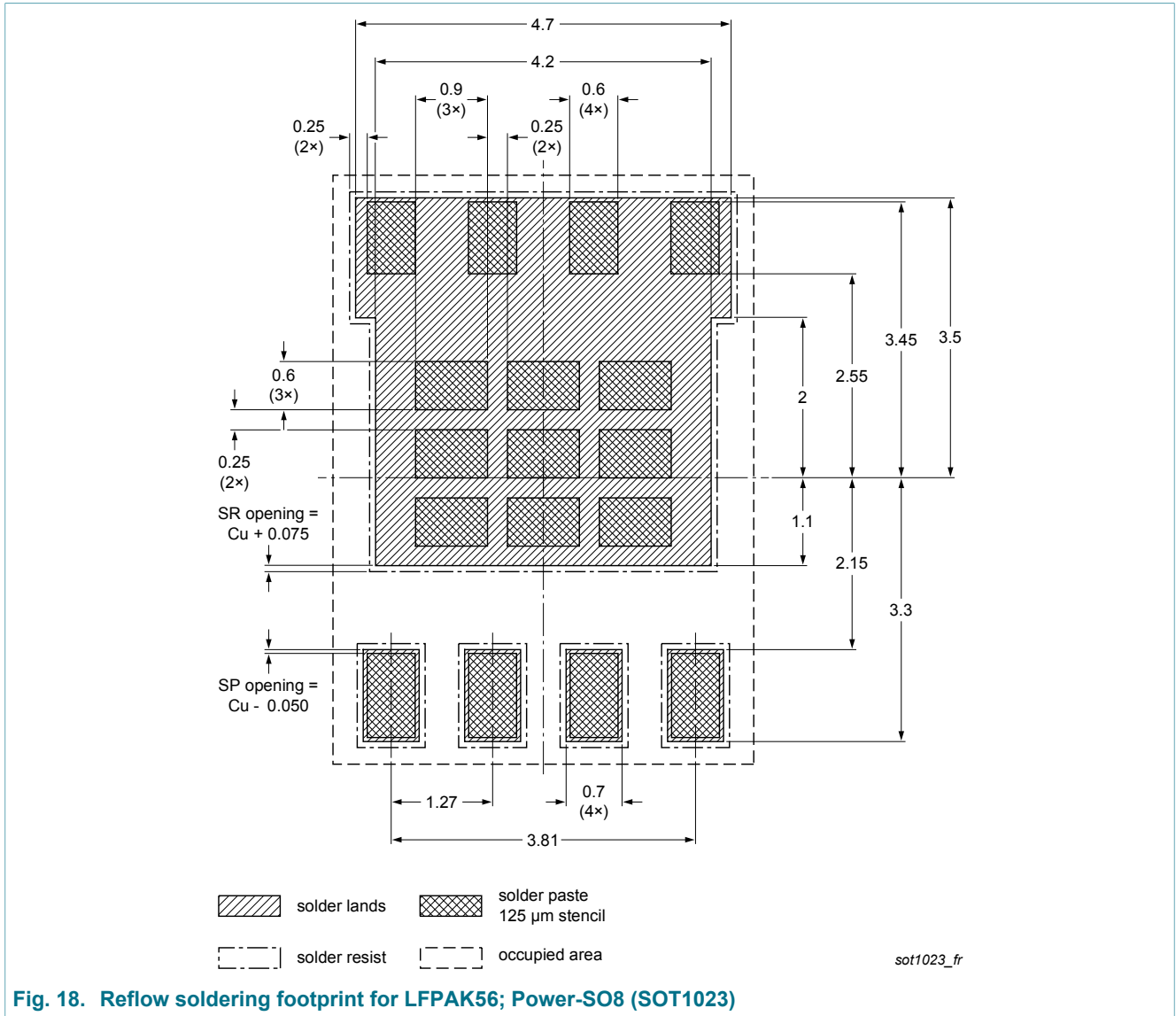


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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14. Contents



1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	10
12. Soldering.....	11
13. Legal information.....	12

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