



**THE DATASHEET OF
MP6401DGT-18AD3-LF-Z**



DESCRIPTION

The MP6401 combines a low-dropout linear regulator with an integrated reset circuit. It operates from a 2.5V to 5.5V input voltage and regulates the output voltage with 2% accuracy at 1.8V, 2.5V, 3.3V or adjustable value. It delivers up to 300mA of load current. By combining an LDO linear regulator with a reset circuit, these products can reduce cost and save space in compact portable devices such as cell phones, smart phones, PDAs, PMPs, and portable GPS devices.

The MP6401 provides a push-pull, active-low that asserts when the regulator output voltage drops below the microprocessor supply threshold (-7.5% or -12.5% of nominal output voltage). Four reset delay time, 3.125ms, 25ms, 200ms and 1580ms can be selected. The MP6401 is available in 3mmx3mm TQFN8, 2mmx2mm TQFN6 and TSOT packages and is specified for operation from -40°C to 85°C.

FEATURES

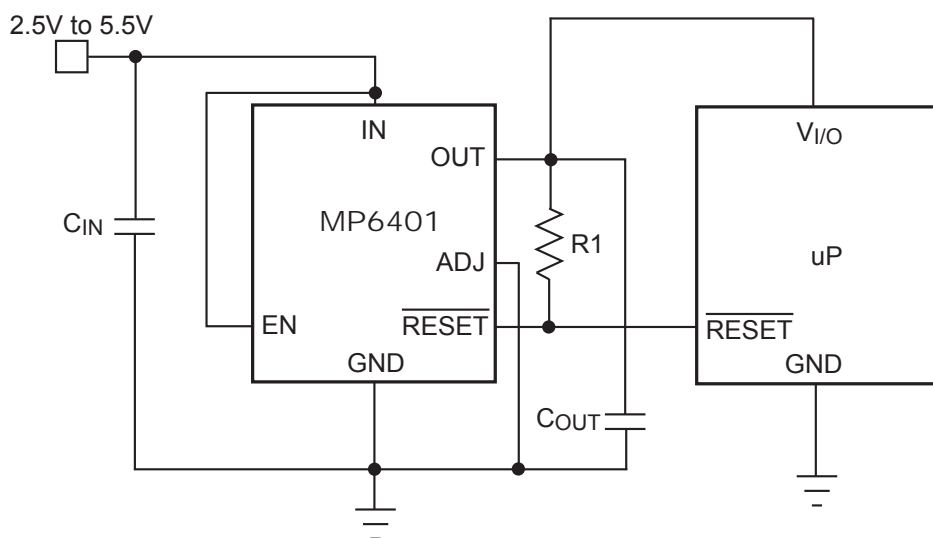
- Low Quiescent Current of 80µA for Battery Powered Equipment
- Low 114mV Dropout at 300mA Output
- ±2% Accurate Output Voltage
- Fixed Output Voltage Options of 1.8V, 2.5V or 3.3V
- Adjustable Output Voltage from 1.229V to 5V Using an External Resistor Divider
- 15µV_{RMS} Ultra Low Noise Output
- PSRR: 57dB at 1kHz
- Input Reverse Current, Thermal and Short-Circuit Protection
- Microprocessor Reset with Four Delay time Options
- Push-Pull $\overline{\text{RESET}}$

APPLICATIONS

- Smart Phone and Cell Phone
- Portable GPS Devices
- Wireless Devices
- PDA and PMP

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TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number* | Package | Top Marking | Free Air Temperature (T _A) |
|-----------------|-----------------|-----------------|--|
| MP6401DQT-18AD3 | TQFN8 (3mmx3mm) | 7T | -40°C to +85°C |
| MP6401DQT-18BD3 | | 8T | |
| MP6401DQT-25AD3 | | 5T | |
| MP6401DQT-25BD3 | | 6T | |
| MP6401DQT-33BD3 | | 4T | |
| MP6401DGT-18AD3 | | TQFN6 (2mmx2mm) | |
| MP6401DGT-18BD3 | 8T | | |
| MP6401DGT-25AD3 | 5T | | |
| MP6401DGT-25BD3 | 6T | | |
| MP6401DGT-33BD3 | 4T | | |
| MP6401DJ-18AD3 | TSOT23-6 | | |
| MP6401DJ-18BD3 | | 8T | |
| MP6401DJ-25AD3 | | 5T | |
| MP6401DJ-25BD3 | | 6T | |
| MP6401DJ-33BD3 | | 4T | |

* For other versions, contact factory for availability.

Note:

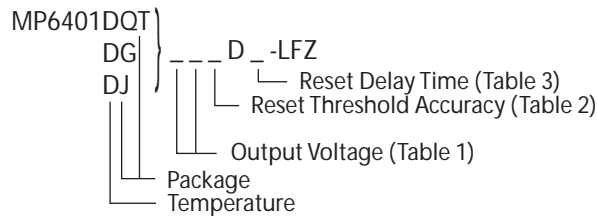


Table 1—Output Voltage Suffix Guide

| Suffix | Output Voltage |
|--------|----------------|
| 18 | 1.8 |
| 25 | 2.5 |
| 33 | 3.3 |

Table 2—Reset Threshold Accuracy

| Suffix | Vout Reset Threshold (%) |
|--------|--------------------------|
| A | -7.5% |
| B | -12.5% |

Table 3—Reset Delay Time Guide

| Suffix | Typical Reset Delay Time (ms) |
|--------|-------------------------------|
| D1 | 3.125 |
| D2 | 25 |
| D3 | 200 |
| D4 | 1580 |

PACKAGE REFERENCE

| | | |
|--------------------------|--------------------------|------------------------|
| <p>TOP VIEW</p> | <p>TOP VIEW</p> | <p>TOP VIEW</p> |
| TQFN8 (3mm x 3mm) | TQFN6 (2mm x 2mm) | TSOT23-6 |

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|-----------------|
| IN, EN, OUT | -0.3V to + 6 V |
| ADJ | -0.3V to 6V |
| RESET | -0.3V to 6V |
| Continuous Power Dissipation. (T _A = +25°C) ⁽²⁾ | |
| TQFN8 (3mm x 3mm) | 2.6W |
| TQFN6 (2mm x 2mm) | 1.56W |
| TSOT | 0.57W |
| Junction Temperature | 150°C |
| Lead Temperature | 260°C |
| Storage Temperature | -65°C to +150°C |

Recommended Operating Conditions ⁽³⁾

| | |
|---|-----------------|
| Supply Voltage V _{IN} | 2.5V to 5.5V |
| Operating Junct. Temp (T _J) | -40°C to +125°C |

Thermal Resistance ⁽⁴⁾

| | θ_{JA} | θ_{JC} |
|-------------------------|---------------|---------------|
| TQFN8 (3mm x 3mm) | 48 | 11 ... °C/W |
| TQFN6 (2mm x 2mm) | 80 | 16 ... °C/W |
| TSOT | 220 | 110 .. °C/W |

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150°C(TYP) and disengages at T_J=130°C(TYP)
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

$V_{IN} = (V_{OUT} + 0.5V)$ or $+2.5V$, whichever is greater, $C_{OUT} = 3.3\mu F$. Typical Value at $T_A = +25^\circ C$ unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|-------------------|--|-------------|----------|-------------|---------------|
| Input Supply Range | V_{IN} | | 2.5 | | 5.5 | V |
| Input Undervoltage Lockout | V_{UVLO} | V_{IN} falling | 1.85 | 2.05 | 2.2 | V |
| Hysteresis of UVLO | V_{HYS} | | | 190 | | mV |
| Supply Current (Ground Current) | I_Q | $I_{OUT} = 0$ | | 80 | 155 | μA |
| Shutdown Supply Current | I_{SHDN} | $T_A = +25^\circ C$ | | 0.1 | 1 | μA |
| Regulation Circuit | | | | | | |
| Output Current | | | 300 | | | mA |
| Output Voltage Accuracy (Fixed Output Voltage) | | $1mA \leq I_{OUT} \leq 300mA$ | -2 | | +2 | % |
| Adjustable Output Voltage Range | | | V_{ADJ} | | 5 | V |
| ADJ Reference Voltage | V_{ADJ} | | 1.205 | 1.229 | 1.253 | V |
| ADJ Threshold | | | | 250 | | mV |
| ADJ Input Leakage Current | I_{ADJ} | $V_{ADJ} = 0, +1.2V$ | | ± 20 | ± 100 | nA |
| Dropout Voltage (Fixed Output Voltage) ⁽⁵⁾ | ΔV_{DO} | $V_{OUT} = +3.3V, I_{OUT} = 300mA$ | | 114 | 220 | mV |
| Short Current Limit | | $V_{IN} \geq 2.5V$ | | 375 | | mA |
| In Regulation Current Limit | | $V_{IN} \geq 2.5V$ | | 500 | | mA |
| Input Reverse Leakage Current (OUT to IN Leakage Current) | | $V_{IN} = 4V, V_{OUT} = 5V, EN$ deasserted, $T_A = +25^\circ C$ | | 0.01 | 1 | μA |
| EN Input Low Voltage | V_{IL} | | | | $0.3V_{IN}$ | V |
| EN Input High Voltage | V_{IH} | | $0.7V_{IN}$ | | | V |
| EN Input Current | | $EN = V_{IN}$ or GND, $T_A = +25^\circ C$ | -1 | 0.1 | +1 | μA |
| Thermal-Shutdown Temperature | T_{SHDN} | | | 150 | | $^\circ C$ |
| Thermal-Shutdown Hysteresis | ΔT_{SHDN} | | | 20 | | $^\circ C$ |
| Line Regulation | | $V_{OUT} = 1.5V, 2.5V \leq V_{IN} \leq 5.5V, I_{OUT} = 10mA$ | | 0.02 | | %/V |
| Load Regulation | | $V_{OUT} = 1.5V, V_{IN} = 2.5V, 1mA \leq I_{OUT} \leq 150mA$ | | 0.1 | | % |
| Output Voltage Noise | | 10Hz to 100kHz, $C_{IN} = 0.1\mu F, I_{OUT} = 100mA, V_{OUT} = 1.5V$ | | 15 | | μV_{RMS} |
| Reset Circuit | | | | | | |
| V_{OUT} Reset Threshold | V_{THOUT} | MP6401__ - __ AD_ | 90 | 92.5 | 95 | % V_{OUT} |
| | | MP6401__ - __ BD_ | 85 | 87.5 | 90 | |
| V_{OUT} to Reset Delay | | | | 30 | | μs |
| Reset Delay Time | T_d | D1 | 2.2 | 3.125 | 4.0 | ms |
| | | D2 | 17.5 | 25 | 32.5 | |
| | | D3 | 140 | 200 | 260 | |
| | | D4 | 1106 | 1580 | 2054 | |

ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN} = (V_{OUT} + 0.5V)$ or +2.5V, whichever is greater, $C_{OUT} = 3.3\mu F$. Typical Value at $T_A = +25^\circ C$ unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------------|----------|---|--------------|-----|-----|------|
| RESET Output Voltage Push-Pull | V_{OL} | $V_{OUT} \geq 1.0V$, $I_{SINK} = 50\mu A$, RESET asserted | | | 0.3 | V |
| | | $V_{OUT} \geq 1.5V$, $I_{SINK} = 3.2mA$, RESET asserted | | | 0.4 | |
| | V_{OH} | $V_{OUT} \geq 2.0V$, $I_{SOURCE} = 500\mu A$, RESET deasserted | $0.8V_{OUT}$ | | | |

Notes:

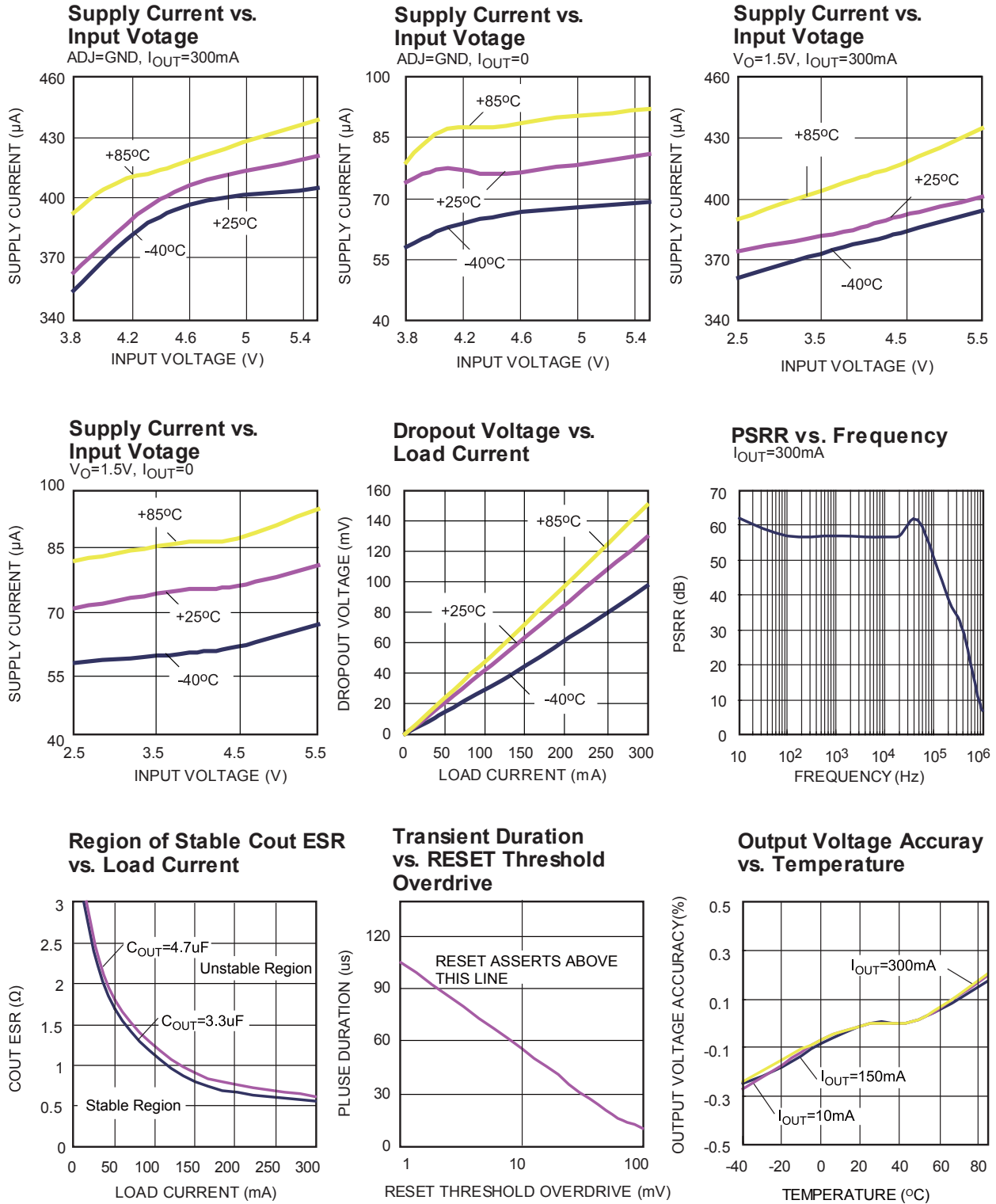
5) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

PIN FUNCTIONS

| TQFN8 Pin # | TQFN6 Pin# | TSOT Pin# | Name | Description |
|----------------|---------------|--------------|---------------------------|--|
| 1 | 1 | 3 | IN | Supply input pin. |
| 2 | | | | |
| 3 | 2 | 2 | GND | Ground. |
| 4 | 3 | 1 | EN | Enable (Active High). Connect EN to IN generally. Don't float EN pin. |
| 5 | 4 | 6 | $\overline{\text{RESET}}$ | Push-pull $\overline{\text{RESET}}$. It asserts when the OUT voltage drops below its threshold. When OUT voltage recover, $\overline{\text{RESET}}$ deasserts after a fix delay time (four options). |
| 6 | 5 | 5 | ADJ | Mode selector input. When ADJ is connected to the tap of an external resistor divider from the OUT to GND, the OUT voltage is adjustable. When ADJ is connected to GND, a preset output voltage is selected. |
| 7 | 6 | 4 | OUT | Regulator output pin. |
| 8 | | | | |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{OUT}=3.3\mu F$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$, Typical values are at $T_A=+25^{\circ}C$, unless otherwise noted.

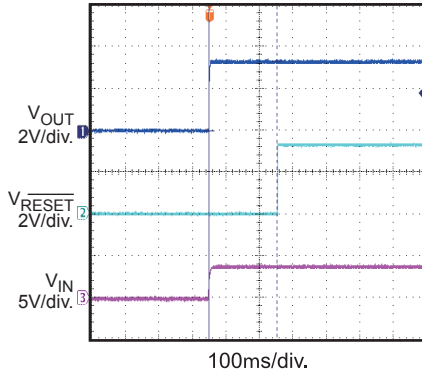


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

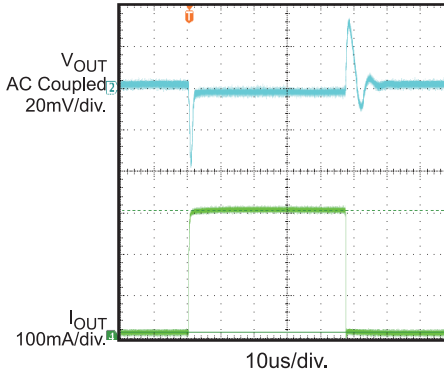
$V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{OUT}=3.3\mu F$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$, Typical values are at $T_A=+25^{\circ}C$, unless otherwise noted.

Start-up through V_{IN}

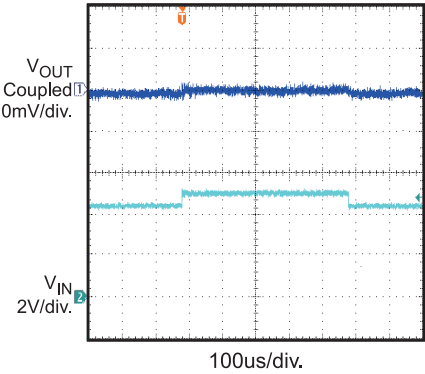
$V_{IN} = 3.8V, I_{OUT} = 0$


Load-Transient Response

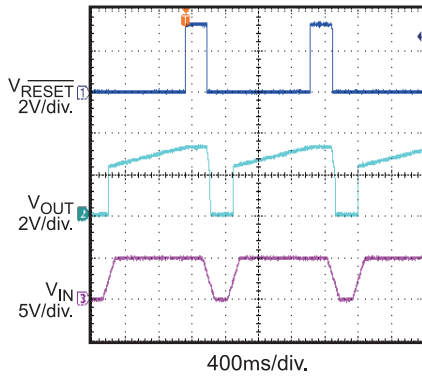
$I_{OUT} = 10mA$ to $300mA$

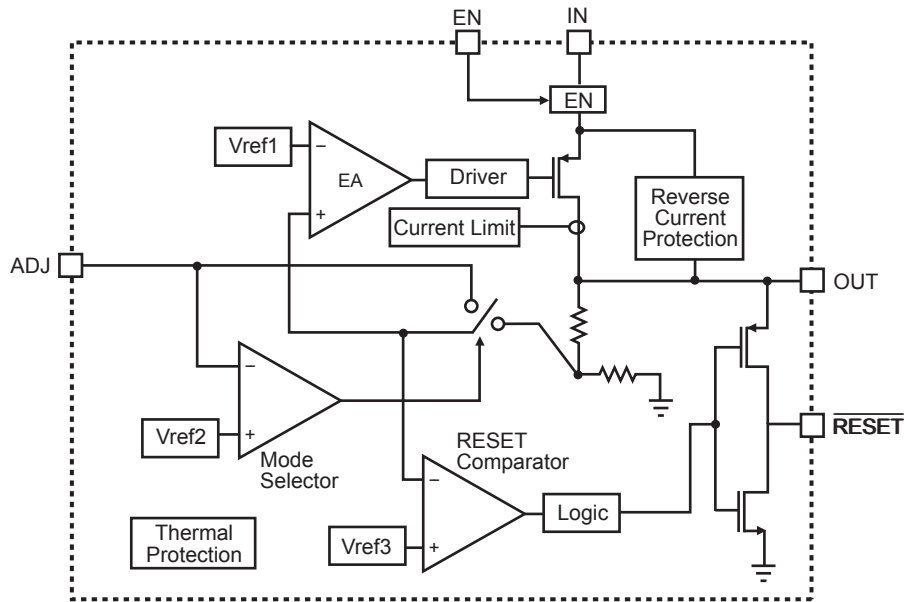

Line-Transient Response

$V_{IN} = 4.5V$ to $5V, I_{OUT} = 10mA$


Reset Response To V_{IN} Rising

$ADJ=GND, I_{OUT} = 0$



BLOCK DIAGRAM

Figure 1—MP6401 Block Diagram

TIMING DIAGRAM

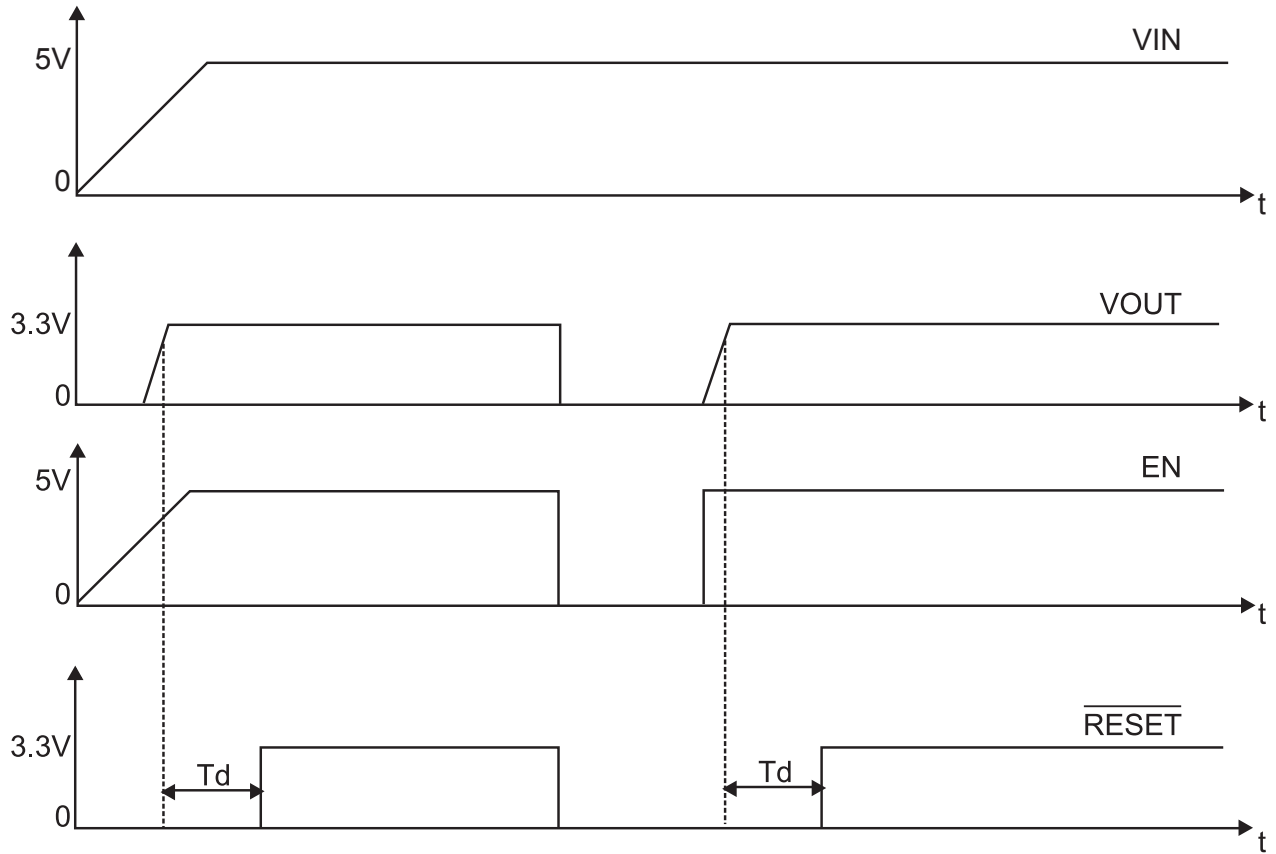


Figure 2—RESET Timing Diagram

OPERATION

The MP6401 integrates a low noise, low dropout, low quiescent current linear regulator and a microprocessor reset circuit. It operates from a 2.5V to 5.5V input voltage and regulates the fixed output voltage with 2% accuracy at 1.8V, 2.5V, 3.3V or adjustable value. The MP6401 can supply to 300mA of load current. The internal reset circuit is used to monitor the regulator output voltage. The $\overline{\text{RESET}}$ asserts when the regulator output voltage drops below the standard microprocessor supply threshold.

Linear Regulator

The MP6401 can output a fixed voltage (1.8V, 2.5V, 3.3V options) or adjustable voltage which ranges from 1.25V to 5V with 2.0% accuracy by operating from a +2.5V to +5.5V input. The MP6401 can supply up to 300mA of load current. When ADJ is connected to GND, a fixed output voltage is selected. Connecting ADJ pin to the tap of external resistor divider from the OUT to GND, adjustable output voltage is selected. The typical ADJ connection is shown in Fig 3.

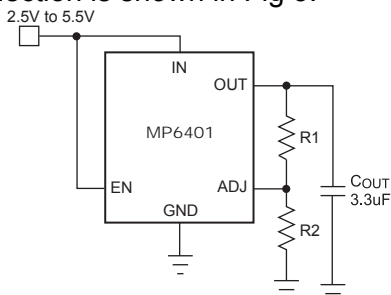


Figure 3—Output Voltage Adjusted with Resistor Divider

Reset Function

The reset circuit monitors the OUT voltage. $\overline{\text{RESET}}$ asserts while OUT voltage falls below its threshold. Two OUT voltage thresholds (-7.5% and -12.5%) are available. The power-up, power-down, and brownout conditions will make $\overline{\text{RESET}}$ asserted. So MP6401 monitor circuit could right control the microprocessor. $\overline{\text{RESET}}$ asserts when the input and output voltage below their thresholds. $\overline{\text{RESET}}$ asserts when EN is a low logic. When the assert trigger condition is removed, $\overline{\text{RESET}}$ will deassert after a fixed delay time. Four options of reset delay-time (see Table 3) can be selected.

EN Shutdown

The MP6401 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off and the supply current is reduced. Generally, the EN pin should be tied to IN to keep the regulator output always on. Do not float the EN pin.

Reverse Leakage Protection

An internal circuit monitors V_{IN} and V_{OUT} to control the reverse leakage current from OUT to IN. While V_{IN} decreases lower than V_{OUT} and EN still hold logic high, the monitor circuit turns off the pass element and its parasitic diode. Typically the reverse leakage current through pass element decreases to 0.1uA. $\overline{\text{RESET}}$ deasserts until V_{IN} returns greater than V_{OUT} and V_{OUT} is higher than its preset threshold.

MP6401 also can work with backup battery at OUT after input power supply is removed as shown in Fig 4. When input power supply is removed, $\overline{\text{RESET}}$ asserts. The backup battery will power the device through two external diodes and typically the current from OUT to ground is 40uA. So, the power supply removing does not erase RAM content if the voltage of backup battery is greater than memory's standby specification. The backup battery can be replaced by a super-cap, while the diode connected with battery is changed to a current-limiting resistor.

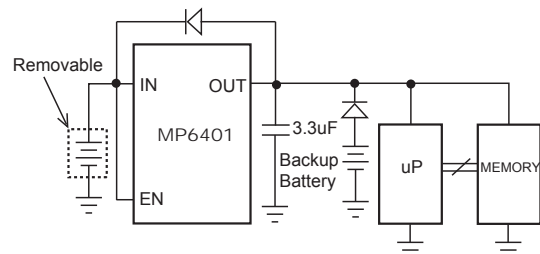


Figure 4— Maintain Memory with Backup Battery

Current Limit

The MP6401 includes a current limit structure which monitors and controls pass element gate voltage limiting the guaranteed maximum output current to 500mA.

Thermal Shutdown

Thermal protection turns off the pass element when the junction temperature exceeds +150°C, allowing to cool the IC. When the IC's junction temperature drops by 20°C, the pass element will be turned on again. Thermal protection limits total power dissipation on the MP6401. For reliable operation, junction temperature should be limited to 125 °C maximum.

APPLICATION INFORMATION

Adjustable Regulator Output

The OUT voltage of MP6401 has two modes available (fixed and adjustable output voltage). When ADJ pin is connected to GND, the regulator works in fixed voltage mode. The regulator output voltage will equal to preset voltage (1.8V, 2.5V or 3.3V options). In fixed voltage mode, the impedance between ADJ and ground should always be less than 50kΩ. Generally, ADJ is connected directly to ground.

When the ADJ pin is connected to the tap of an external resistor divider, the regulator works in adjustable voltage mode as shown in Fig 3. The output voltage is selected by resistor divider, thus

$$V_{OUT} = 1.229 \times \frac{R_1 + R_2}{R_2}$$

In adjustable voltage mode, R_2 equal to 13kΩ is recommended as a good tradeoff among stability, accuracy and high-frequency PSRR. R_2 should be not greater than 100kΩ.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_D (MAX) = (T_J (MAX) - T_A) / \theta_{JA}$$

Where $(T_J (MAX) - T_A)$ is the temperature difference between the junction and the ambient environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the GND pin of MP6401 to ground using a large pad or ground plane helps to channel heat away.

Output Capacitor Selection

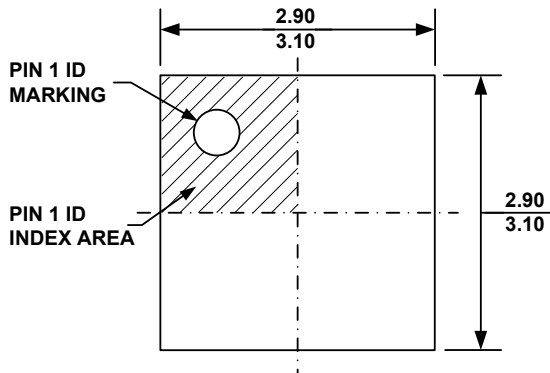
The MP6401 is designed specifically to work with very low ESR ceramic output capacitor 3.3uF (min). For performance consideration, a large ceramic capacitor such as 10uF is better. X7R or X5R capacitor dielectric is recommended.

OUT Voltage Transient Immunity

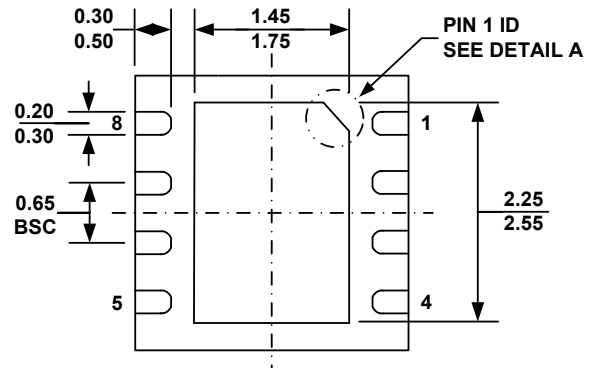
The MP6401 can be immune to OUT pin short negative transient. Typically, the immune duration is 60us with 10mV overdriving. A shorter negative transient can not make the \overline{RESET} output assert.

PACKAGE INFORMATION

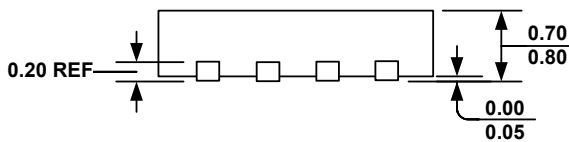
TQFN8 (3mm x 3mm)



TOP VIEW

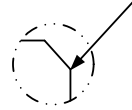


BOTTOM VIEW

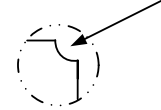


SIDE VIEW

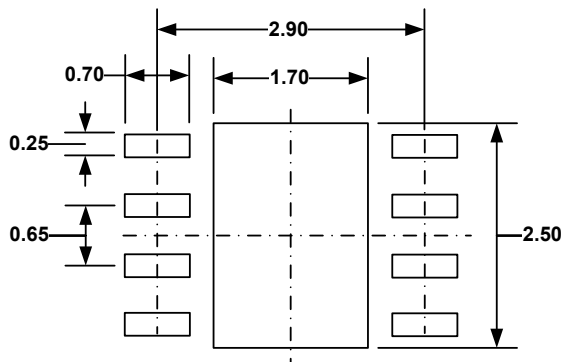
PIN 1 ID OPTION A
0.30x45° TYP.



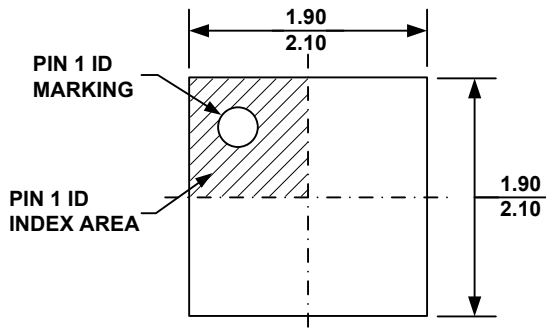
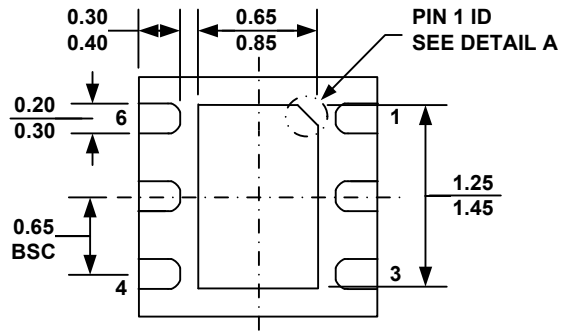
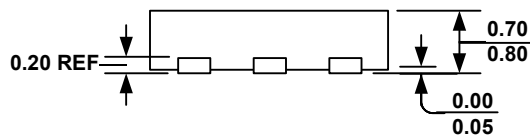
PIN 1 ID OPTION B
R0.20 TYP.

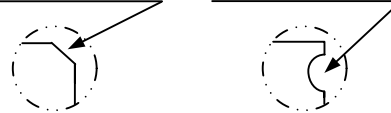
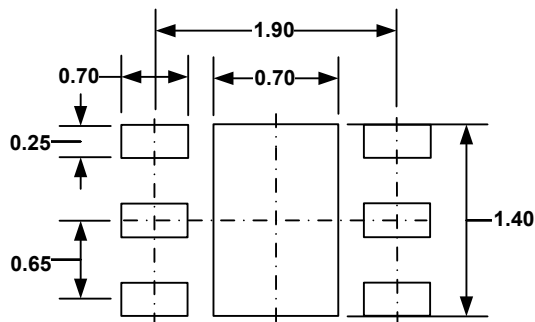


DETAIL A

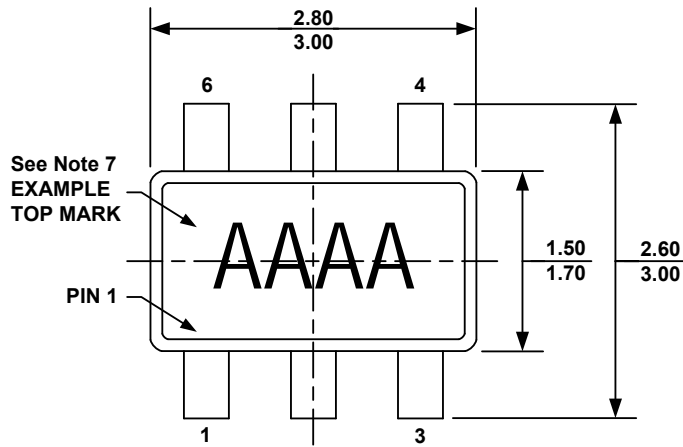
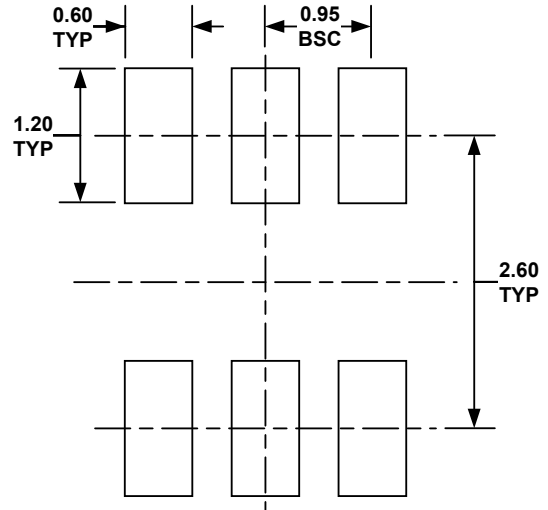
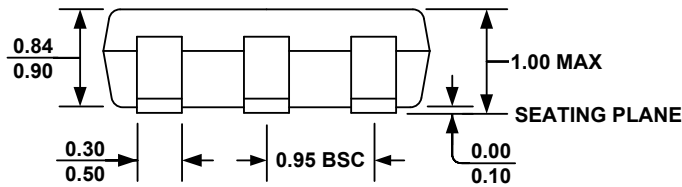
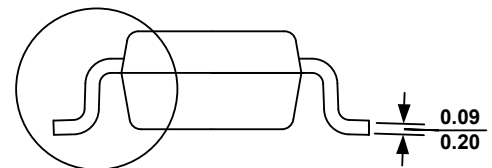
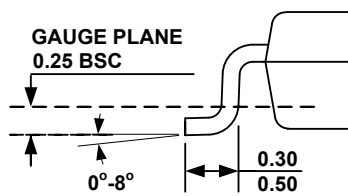


RECOMMENDED LAND PATTERN

TQFN6 (2mm x 2mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW
PIN 1 ID OPTION A
 0.30x45° TYP.

PIN 1 ID OPTION B
 R0.20 TYP.

DETAIL A

RECOMMENDED LAND PATTERN
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-229, VARIATION WCCC.
- 5) DRAWING IS NOT TO SCALE.



TSOT23-6

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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