THE DATASHEET OF

TMP1075DSGT

TMP1075 Temperature Sensor With I²C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout

1 Features

- Temperature accuracy:
  - ±0.25°C (typical) from −55°C to 125°C
  - ±1°C (maximum) from −40 °C to 110°C
  - ±2°C (maximum) from −55°C to 125°C
- Low power consumption:
  - 2.7µA Average current
  - 0.37µA Shutdown current
- Supply range options from: 1.62V to 5.5V
- Temperature independent of supply
- Digital interface: SMBus, I²C
- Software compatibility with industry standard LM75 and TMP75
- Can coexist in I³C mixed fast mode bus
- Resolution: 12 Bits
- Supports up to 32 I2C addresses
- ALERT pin function
- NIST traceability

2 Applications

- Power-supply temperature monitoring
- Connected peripherals & printers
- PC and notebooks
- Mobile phones
- Battery management
- Enterprise machine
- Thermostat
- Wireless environmental sensor and HVAC
- Electro mechanical device temperature

3 Description

The TMP1075 is the most accurate and lowest power replacement to the industry standard LM75 and TMP75 digital temperature sensors. Available in SOIC-8, VSSOP-8, WSON-8, and SOT563-6 packages, the TMP1075 offers pin-to-pin and software compatibility to quickly upgrade any existing xx75 design. The TMP1075 additional new packages are a 2.0mm × 2.0mm DFN and a 1.6mm × 1.6mm SOT563-6 reducing the printed circuit board (PCB) footprint by 82% and 89% compared to the SOIC package, respectively.

The TMP1075 has a ±1°C accuracy over a wide temperature range and offers an on-chip 12-bit analog-to-digital converter (ADC) providing a temperature resolution of 0.0625°C.

Compatible with two-wire SMBus and I²C interfaces, the TMP1075 support up to 32 device addresses and provides SMBus Reset and Alert function.

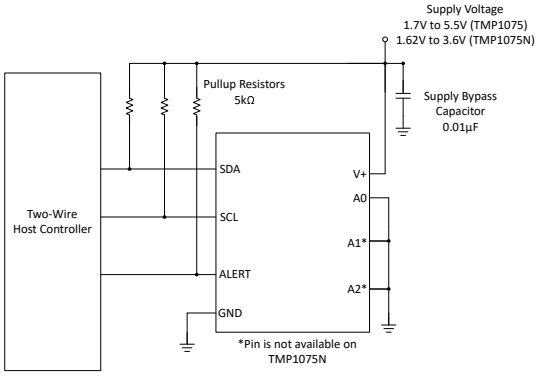
The TMP1075 D, DGK, and DSG packages are specified for operation over a temperature range of −55°C to 125°C and the TMP1075N DRL package is specified over the −40°C to 125°C temperature range.

The TMP1075 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards.

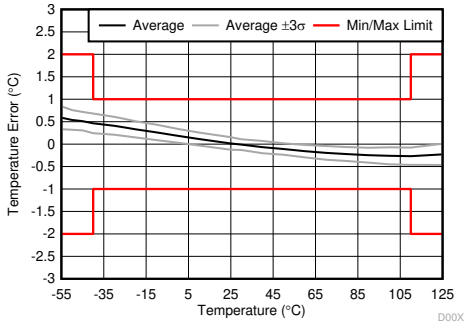
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP1075	VSSOP (DGK, 8)	3.00mm × 4.90mm
	SOIC (D, 8)	4.90mm × 6.00mm
	WSON (DSG, 8)	2.00mm × 2.00mm
	SOT563 (DRL, 6)(3)	1.60mm × 1.60mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Available as the TMP1075N orderable.



Simplified Schematic



DGK and D packages

Temperature Accuracy

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4 Device Comparison

Table 4-1 lists the key specification and feature differences between the different TMP1075 packages.

Table 4-1. Package Feature and Spec Comparison

SPEC/FEATURE	TMP1075			TMP1075N
	D	DGK	DSG	DRL
Supply Voltage	1.7 V to 5.5 V	1.7 V to 5.5 V	1.7 V to 5.5 V	1.62 V to 3.6 V
Temperature Range	–55°C to 125°C	–55°C to 125°C	–55°C to 125°C	–40°C to 125°C
Body Size	4.90 mm × 3.91 mm	3.00 mm × 3.00 mm	2.00 mm × 2.00 mm	1.60 mm × 1.20 mm
Accuracy	±1.0°C: –40°C to +110°C ±2.0°C: –55°C to 125°C	±1.0°C: –40°C to +110°C ±2.0°C: –55°C to 125°C	±1.0°C: –40°C to +75°C ±2.0°C: –55°C to 125°C	±1.0°C: –10°C to +60°C ±2.0°C: –40°C to 125°C
I2C Addresses	32	32	32	4
Conversion Rate Settings	Yes	Yes	Yes	No
Device ID	Yes	Yes	Yes	No

5 Pin Configuration and Functions

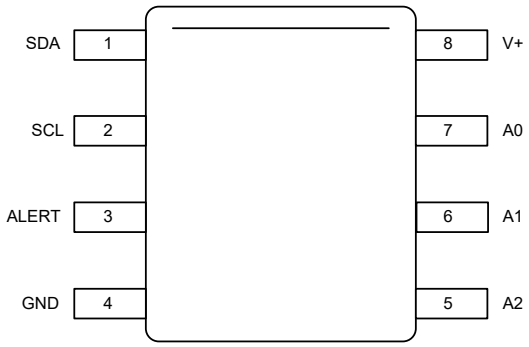


Figure 5-1. D Package 8-Pin SOIC Top View

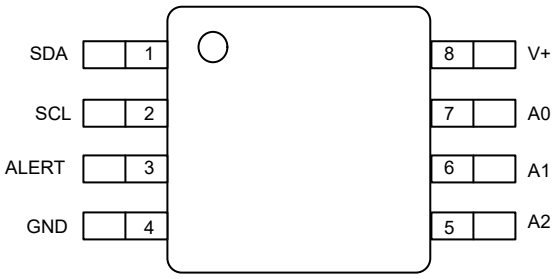


Figure 5-2. DGK Package 8-Pin VSSOP Top View

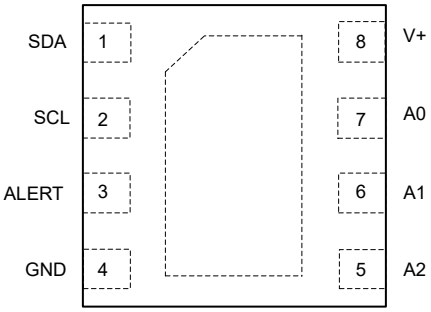
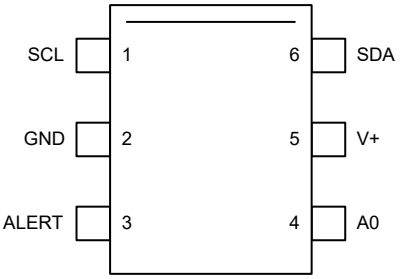


Figure 5-3. DSG Package 8-Pin WSON Top View



1. Pin 1 is determined by orienting the package marking as indicated in the diagram.
2. Referred to as the TMP1075N orderable throughout the document.

Figure 5-4. DRL Package 6-Pin SOT563 Top View

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SOIC / VSSOP / WSON	SOT563		
A0	7	4	I	Address select A0: Connect to GND, V+, SDA, or SCL
A1	6	—	I	Address select A1: Connect to GND, V+, SDA, or SCL
A2	5	—	I	Address select A2: Connect to GND or V+
ALERT	3	3	O	Overtemperature alert; Open-drain output that requires a pullup resistor
GND	4	2	—	Ground
SCL	2	1	I	Serial clock
SDA	1	6	I/O	Serial data. Open-drain output that requires a pullup resistor
V+	8	5	I	Supply voltage, 1.7 V to 5.5 V (TMP1075); 1.62 V to 3.6 V (TMP1075N)

(1) I = Input, O = Output, I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply, V+	TMP1075		6.5	V
	TMP1075N		4	
Input voltage SCL, SDA, A1, A0	TMP1075	–0.3	6.5	V
Input voltage SCL, SDA, A0	TMP1075N	–0.3	4	V
Input voltage ALERT	TMP1075N		(V+)+0.3 and ≤4	V
Input voltage A2 pin	TMP1075	–0.3	(V+) + 0.3	V
Operating temperature		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–60	130	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	TMP1075	1.7		5.5	V
	TMP1075N	1.62	3.3	3.6	V
Operating free-air temperature, T_A	TMP1075	–55		125	°C
	TMP1075N	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TMP1075 DGK (VSSOP) 8 PINS	TMP1075 D (SOIC) 8 PINS	TMP1075 DSG (WSON) 8 PINS	TMP1075N DRL (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.5	130.4	87.4	240.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82	76.9	111.1	96.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	124.4	72.3	54	124.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.9	32	9.8	4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	122.6	71.9	54.4	123.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	28.1	—	°C/W
M_T	Thermal mass	16.6	64.2	5.0	—	mJ/°C

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics:TMP1075

at T_A = –55°C to +125°C and V+ = 1.7 V to 5.5 V (unless noted); typical specification are at T_A = 25°C and V+=3.3 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT							
	Range			–55		125	°C
	Accuracy (temperature error)	DGK, D	–40°C to 110°C		±0.25	±1	°C
			–55°C to 125°C		±0.25	±2	
		DSG	–40°C to 75°C		±0.25	±1	°C
			–55°C to 125°C		±0.25	±2	°C
	Accuracy (temperature error) vs supply		PSRR			±0.03	°C/V
	Resolution		1 LSB (12 bit)		0.0625		°C
	Repeatability[1]		25°C, V+= 3.3 V[2]		0.0625		°C
	Long-term drift[3]		500 hours at 150°C, 5.5 V		0.0625		°C
DIGITAL INPUT/OUTPUT							
	Input capacitance				5		pF
V_{IH}	High-level input logic			0.7(V+)			V
V_{IL}	Low-level input logic					0.3(V+)	V
I_{IN}	Leakage input current			–0.25	0	0.25	µA
	Input voltage hysteresis		SCL and SDA pins		600		mV
V_{OL}	Low-level output logic		I_{OL} = -3 mA, SDA and ALERT pins	0	0.15	0.4	V
	ADC Conversion time		one-shot mode	4.5	5.5	7	ms
T_C	Conversion Time		R1 = 0, R0 = 0 (default)		27.5		ms
			R1 = 0, R0 = 1		55		
			R1 = 1, R0 = 0		110		
			R1 = 1, R0 = 1		220		
	Reset time		The time between reset until ADC conversion start		0.3		ms
	Conversion Rate Variation			–10	0	10	%
POWER SUPPLY							
	Operating voltage range			1.7	3.3	5.5	V

at T_A = –55°C to +125°C and V+ = 1.7 V to 5.5 V (unless noted); typical specification are at T_A = 25°C and V+=3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current (serial bus inactive)	R1 = 0, R0 = 0 (default)		10	20	µA
		R1 = 0, R0 = 1		5.5	9	µA
		R1 = 1, R0 = 0		4	6	
		R1 = 1, R0 = 1		2.7	4	
		During 5.5 ms active conversion		52	85	µA
I_{SD}	Shutdown current	Serial bus active, SCL frequency = 400 kHz, A0=A1=A2=GND		13		µA
		Serial bus inactive, A0=A1=A2=SCL=SDA=V+, 25°C		0.37	0.65	µA
		Serial bus inactive, A0=A1=A2=SCL=SDA=V+		0.37	3.5	µA
	Power supply thresholds	Supply rising, Power-on Reset		1.22		V
		Supply failing, Brown-out Detect		1.1		

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) One-shot mode setup, 1 sample per minute for 24 hours.
(3) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C.

6.6 Electrical Characteristics: TMP1075N

At T_A = 25 °C and V+ = 1.62 to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR						
	Temperature Operating Range		-40		125	°C
T_{ERR}	Temperature accuracy	-10 °C to 60 °C		0.25	±1	°C
		-40 °C to 125°C		0.5	±2	
PSR	DC power supply rejection			0.2	0.5	°C/V
T_{RES}	Temperature resolution	Including sign bit		12		Bits
		LSB		62.5		m°C
t_{CONV}	Conversion time			10	15	ms
DIGITAL INPUT/OUTPUT						
C_{IN}	Input capacitance			3		pF
V_{IH}	Input logic high level		0.7 × V+		3.6	V
V_{IL}	Input logic low level				0.3 × V+	V
I_{IN}	Input leakage current	0 V< V+ < 3.6 V			1	µA
V_{OL}	Output low level	SDA, ALERT (V+ > 2 V, I_{OL} = 3 mA)	0		0.4	V
V_{OL}	Output low level	SDA, ALERT (V+ < 2 V, I_{OL} = 3 mA)	0		0.2 x V+	V
POWER SUPPLY						
V+	Operating supply range		1.62		3.6	V
I_{DD_AVG}	Average current consumption	Serial bus inactive		4.8	7.5	µA
		Serial bus active, SCL frequency = 400 kHz		10		
		Serial bus active, SCL frequency = 2.85 MHz		40		
I_{DD_SD}	Shutdown current	Serial bus inactive		0.15	0.35	µA
		Serial bus active, SCL frequency = 400 kHz		5.5		µA
		Serial bus active, SCL frequency = 2.85 MHz		35		µA

6.7 Timing Requirements:TMP1075

minimum and maximum specifications are over –55°C to 125°C and V+ = 1.7 V to 5.5 V (unless otherwise noted)(1)

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time(2)	0		0	130	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock low period	1300		250		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
$t_{(VDAT)}$	Data valid time (data response time)(3)		900		130	ns
t_{FDA}	Data fall time		300		100	ns
t_R	Clock rise time		300		40	ns
t_F	Clock fall time		300		40	ns
$t_{timeout}$	Timeout (SCL = SDA = GND)	20	30	20	30	ms
t_{RC}	Clock/ data rise time for SCL = 100 kHz		1000			ns

(1) The host and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

6.8 Timing Requirements: TMP1075N

minimum and maximum specifications are over –40°C to 125°C and V+ = 1.62 V to 3.6 V (unless otherwise noted)(1)

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency		0.001	0.4	0.001	2.85	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions		600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time(2)		100	900	25	105	ns
$t_{(SUDAT)}$	Data setup time		100		25		ns
$t_{(LOW)}$	SCL clock low period		1300		210		ns
$t_{(HIGH)}$	SCL clock high period		600		60		ns
t_{FD}	Data fall time			300		80	ns
t_{RD}	Data rise time			300			
		SCLK ≤100 kHz		1000			
t_{RC}	Clock rise time			300		40	ns
t_{FC}	Clock fall time			300		40	ns
$t_{timeout}$	Timeout (SCL = SDA = GND)		30	40	30	40	ms

(1) The host and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{LPF}	Spike filter for I^3C compatibility	SCL= 12.5 MHz		50		ns

6.10 Timing Diagrams

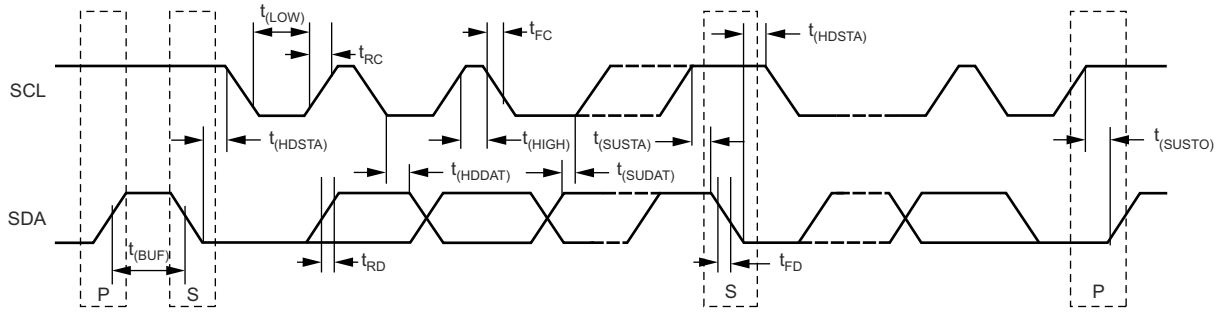


Figure 6-1. Two-Wire Timing Diagram

6.11 Typical Characteristics

at T_A = 25°C, V+ = 3.3 V, and apply to D, DGK, and DSG packages (unless otherwise noted)

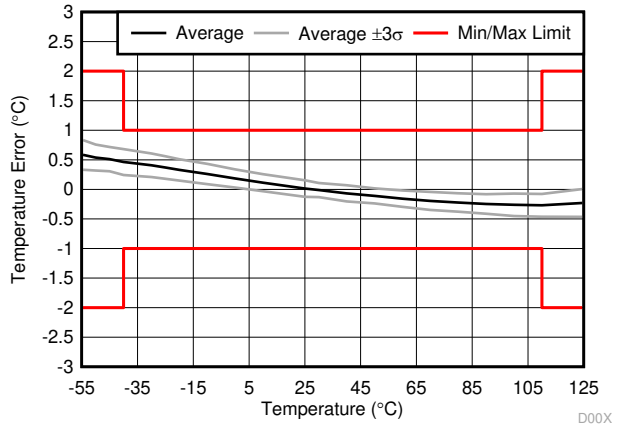


Figure 6-2. DGK & D Temperature Error vs. Temperature

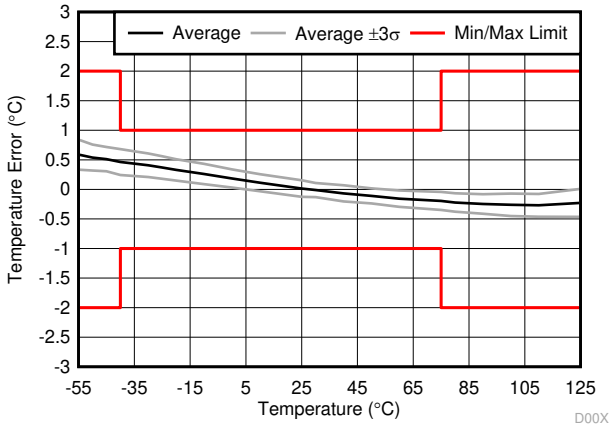


Figure 6-3. DSG Temperature Error vs. Temperature

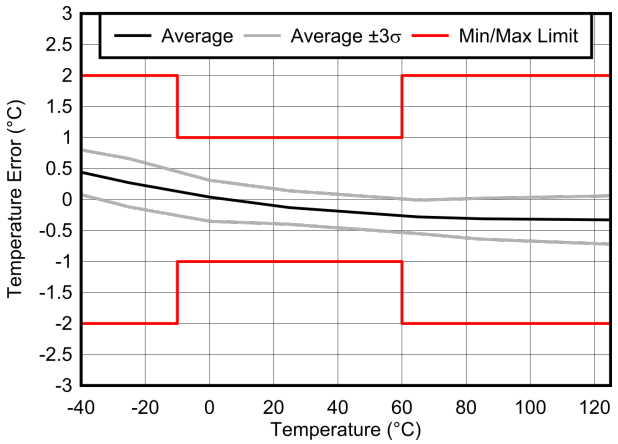


Figure 6-4. TMP1075NDRL Temperature Error vs. Temperature

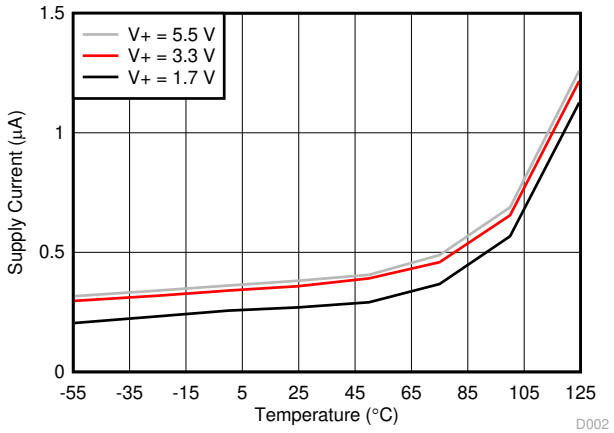


Figure 6-5. Shutdown Current vs. Temperature

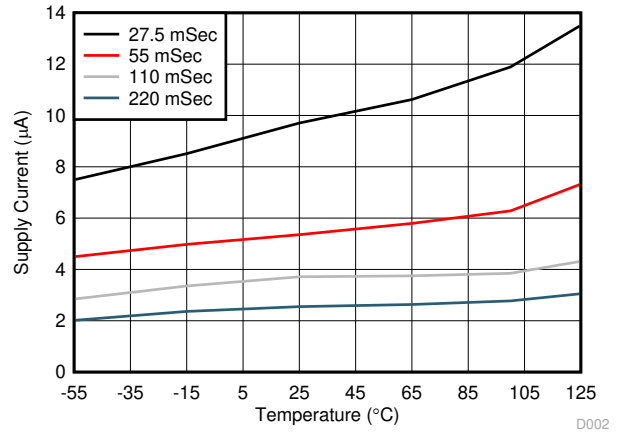


Figure 6-6. Average Current vs. Conversion Rates and Temperature

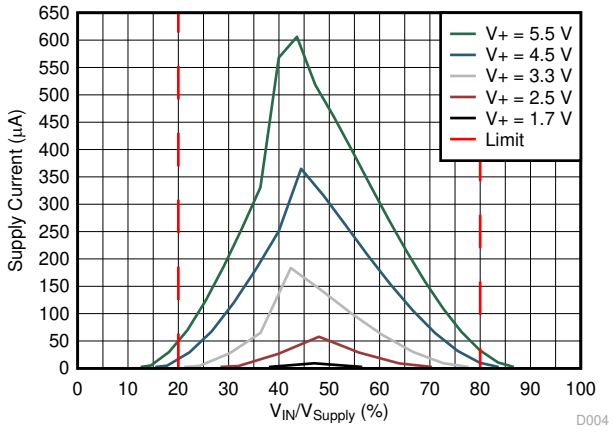


Figure 6-7. Supply Current vs. Input Cell Voltage

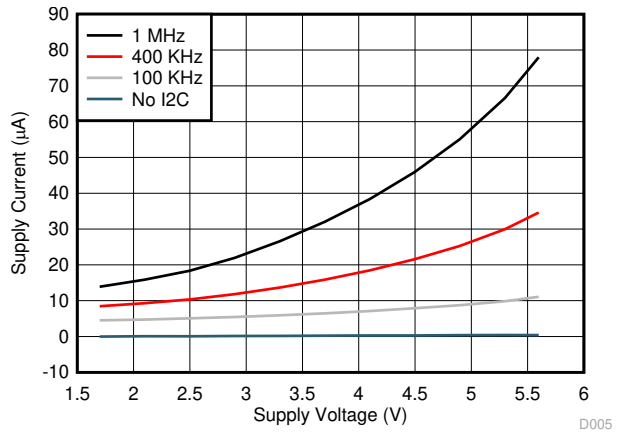


Figure 6-8. Supply Current vs. I²C Bus Clock and Supply Voltage in Shutdown Mode

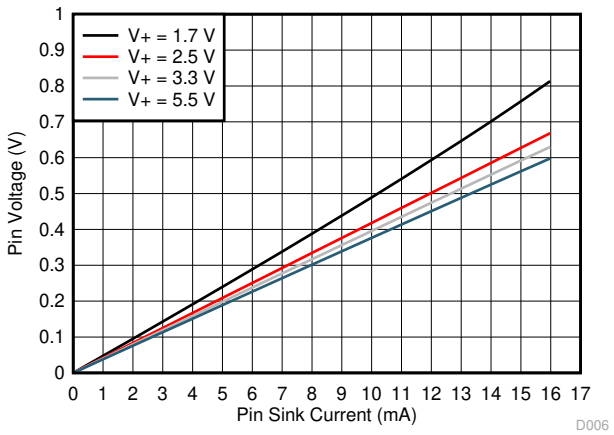


Figure 6-9. ALERT Pin Output Voltage vs. Sink Current

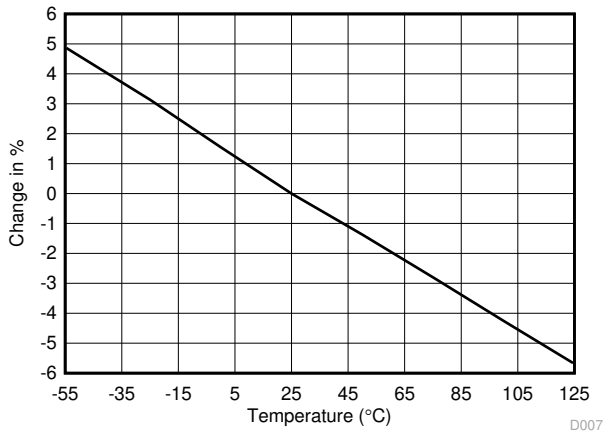


Figure 6-10. Sampling Period Change vs. Temperature (1.7 V to 5.5 V)

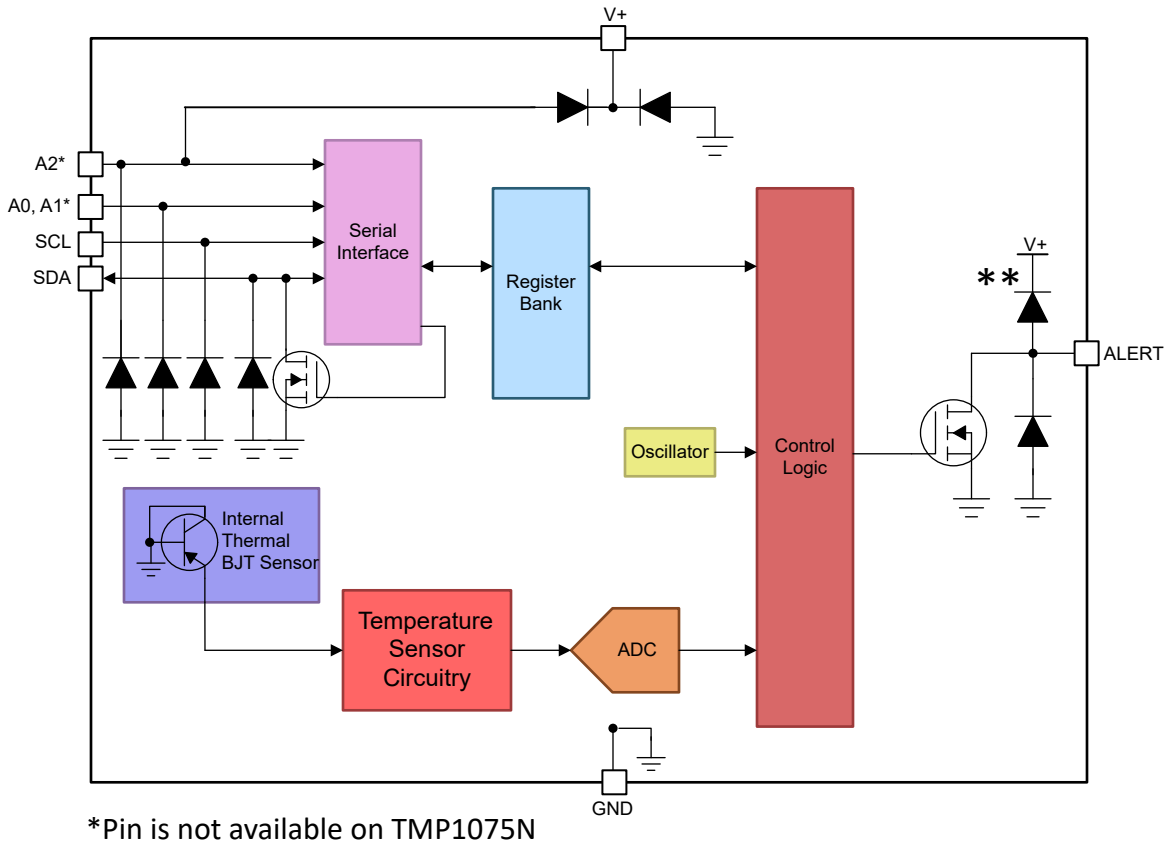
7 Detailed Description

7.1 Overview

The TMP1075 device is a digital temperature sensor that is designed for thermal management and thermal protection applications. The TMP1075 is a SMBus and is I^2C interface-compatible. The device is also capable of coexisting in an I^3C bus when in Mixed Fast Mode. The TMP1075 non-N orderables are specified over a temperature range of −55°C to 125°C and the TMP1075N orderable is specified over the −40°C to 125°C temperature range. Figure 7-1 shows an internal block diagram of TMP1075 device.

The temperature sensor thermal path runs through the package leads as well as the plastic package. The leads provide the primary thermal path due to the lower thermal resistance of the metal.

7.2 Functional Block Diagram



*Pin is not available on TMP1075N
** ESD Diode only in TMP1075N

Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only temperature register. Which is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data. However, only the first 12 MSBs are used to indicate temperature while the remaining 4 LSB are set to zero. Table 7-1 lists the data format for the temperature. Negative numbers are represented in binary two's-complement format. After power-up or reset, the temperature register reads 0°C until the first conversion is complete.

Table 7-1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
127.9375	0111 1111 1111 0000	7FF0
100	0110 0100 0000 0000	6400
80	0101 0000 0000 0000	5000
75	0100 1011 0000 0000	4B00
50	0011 0010 0000 0000	3200
25	0001 1001 0000 0000	1900
0.25	0000 0000 0100 0000	0040
0.0625	0000 0000 0001 0000	0010
0	0000 0000 0000 0000	0000
–0.0625	1111 1111 1111 0000	FFF0
–0.25	1111 1111 1100 0000	FFC0
–25	1110 0111 0000 0000	E700
–50	1100 1110 0000 0000	CE00
–128	1000 000 0000 0000	8000

7.3.2 I^2C and SMBus Serial Interface

The TMP1075 operates as a target device on the two-wire, SMBus and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O line SDA and SCL input pin. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP1075 supports the transmission protocol for fast mode up to 400 kHz and high-speed mode up to 2.56 MHz. All data bytes are transmitted MSB first.

7.3.2.1 Bus Overview

The device that initiates the data transfer is called a host, and the devices controlled by the host are the target. The bus must be controlled by a host device that generates the SCL that controls the bus access and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. This is indicated by the host pulling the data line SDA from a high to low logic level when SCL is high. All target devices on the bus shift in the device address byte on the rising edge of the clock with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the device being addressed responds to the host by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the host generates a STOP condition indicated by pulling SDA from low to high logic level when SCL is high.

7.3.2.2 Serial Bus Address

To communicate with the TMP1075, the host must first address devices through an address byte. The device address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP1075 features three address pins to allow up to 32 devices (TMP1075N: 4) to be addressed on a single bus interface. Table 7-2 and Table 7-3 describe the pin logic levels used to configure the TMP1075 I2C address. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

Table 7-2. TMP1075 Address Pins State

A2	A1	A0	7-BIT ADDRESS	A2	A1	A0	7-BIT ADDRESS
0	0	SDA	1000000	0	SDA	SDA	1010000
0	0	SCL	1000001	0	SDA	SCL	1010001
0	1	SDA	1000010	0	SCL	SDA	1010010
0	1	SCL	1000011	0	SCL	SCL	1010011
1	0	SDA	1000100	1	SDA	SDA	1010100
1	0	SCL	1000101	1	SDA	SCL	1010101
1	1	SDA	1000110	1	SCL	SDA	1010110
1	1	SCL	1000111	1	SCL	SCL	1010111
0	0	0	1001000	0	SDA	0	1011000
0	0	1	1001001	0	SDA	1	1011001
0	1	0	1001010	0	SCL	0	1011010
0	1	1	1001011	0	SCL	1	1011011
1	0	0	1001100	1	SDA	0	1011100
1	0	1	1001101	1	SDA	1	1011101
1	1	0	1001110	1	SCL	0	1011110
1	1	1	1001111	1	SCL	1	1011111

Table 7-3. TMP1075N Address Pins State

A0	7-BIT ADDRESS
0	1001000
1	1001001
SDA	1001010
SCL	1001011

7.3.2.3 Pointer Register

Figure 7-2 shows the internal register structure of the TMP1075, and Table 7-5 lists the pointer addresses of the register map. Table 7-4 shows that the register map reset value of the pointer register is 00h.

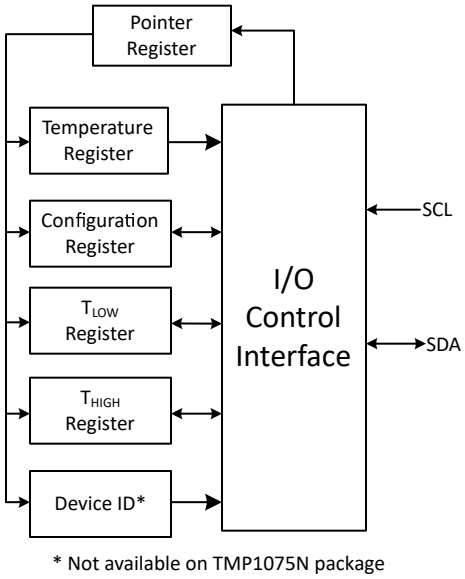


Figure 7-2. Internal Register Structure

7.3.2.3.1 Pointer Register Byte [reset = 00h]

Table 7-4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	Register Bits			

7.3.2.4 Writing and Reading to the TMP1075

Accessing a particular register on the TMP1075 device is accomplished by writing the appropriate value to the pointer register. After Reset, the register value is set to zero. The value for the pointer register is the first byte transferred after the device address byte with the R/W bit low. Every write operation to the TMP1075 requires a value for the pointer register (see Figure 7-3).

When reading from the TMP1075 device, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a device address byte with the R/ $\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The host can then generate a START condition and send the device address byte with the R/ $\overline{W}$ bit high to initiate the read command. See Figure 7-5 for details of this sequence. If repeated reads from the same register are desired, the pointer register bytes do not have to be continually sent because the TMP1075 remembers the pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first.

7.3.2.5 Operation Mode

The TMP1075 can operate as a receiver or transmitter. As a target device, the TMP1075 never drives the SCL line.

7.3.2.5.1 Receiver Mode

The first byte transmitted by the host is the device address with the R/$\overline{W}$ bit low. The TMP1075 then acknowledges reception of a valid address. The next byte transmitted by the host is the pointer register. The TMP1075 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP1075 acknowledges reception of each data byte. The host can terminate data transfer by generating a START or STOP condition.

7.3.2.5.2 Transmitter Mode

The first byte is transmitted by the host and is the device address, with the R/$\overline{W}$ bit high. The target device acknowledges reception of a valid device address. The next byte is transmitted by the device and is the most significant byte of the register indicated by the Pointer register. The host acknowledges reception of the data byte. The next byte transmitted by the device is the least significant byte. The host acknowledges reception of the data byte. The host can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

7.3.2.6 SMBus Alert Function

The TMP1075 supports the SMBus Alert function. When the TMP1075 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP1075 can be connected as an SMBus Alert signal. When a host senses that an alert condition is present on the ALERT line, the host sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP1075 is active, the devices acknowledge the SMBus Alert command and respond by returning the device address on the SDA line. The eighth bit (LSB) of the device address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the alert condition. This bit is equal to POL if the temperature is greater than or equal to T_{HIGH}. This bit is equal to $\overline{POL}$ if the temperature is less than T_{LOW}. See Figure 7-8 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the device address portion of the SMBus Alert command determines which device clears the alert status. If the TMP1075 wins the arbitration, the ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP1075 loses the arbitration, the ALERT pin remains active.

7.3.2.7 General Call- Reset Function

The TMP1075 responds to the two-wire general call address (0000 000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000 110, the TMP1075 resets the internal registers to the power-up reset values.

7.3.2.8 High-Speed Mode (HS)

For the two-wire bus to operate at frequencies above 400 kHz, the host device must issue an HS mode host code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1075 device does not acknowledge this byte, but the device does switch the input filters on the SDA and SCL and the output filters on the SDA to operate in HS mode. After the HS mode host code is issued, the host transmits a two-wire device address to initiate a data transfer operation. The bus continues to operate in HS mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP1075 switches the input and output filters back to fast-mode operation.

7.3.2.9 Coexists in I^3C Mixed Fast Mode

A bus with both I^3C and I^2C interfaces is referred to as a mixed fast mode with clock speeds up to 12.5 MHz. For the TMP1075, which is an I^2C device, to coexist in the same bus, the device incorporated a spike suppression filter of 50 ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I^3C devices.

7.3.2.10 Time-Out Function

The TMP1075 resets the serial interface if SCL is held low by the host or SDA is held low by the TMP1075 for 25 ms (TMP1075N: 30 ms) (typical) between a START and STOP condition. The TMP1075 releases the SDA bus and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained.

7.3.3 Timing Diagrams

The TMP1075 is two-wire SMBus and I^2C interface-compatible. Figure 7-3 to Figure 7-8 describe the various operations on the TMP1075. The following list provides bus definitions.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the host device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a host receive, the termination of the data transfer can be signaled by the host generating a Not-Acknowledge on the last byte that is transmitted by the target device.

7.3.4 Two-Wire Timing Diagrams

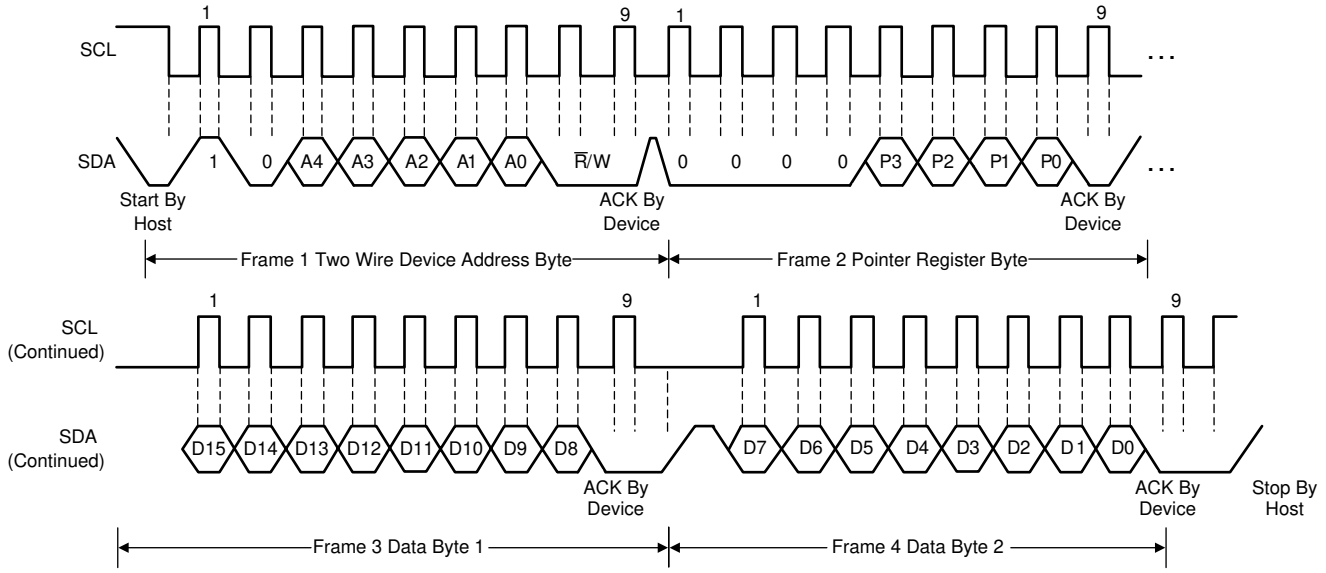


Figure 7-3. Two-Wire Timing Diagram for Write Word Format

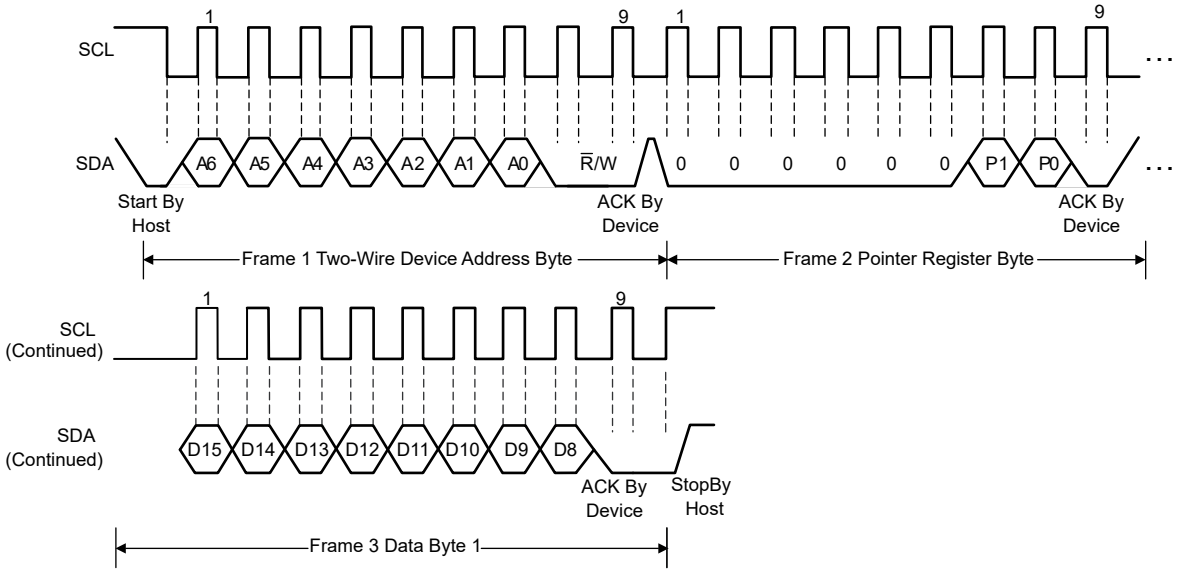


Figure 7-4. Two-Wire Timing Diagram for Write Single Byte Format

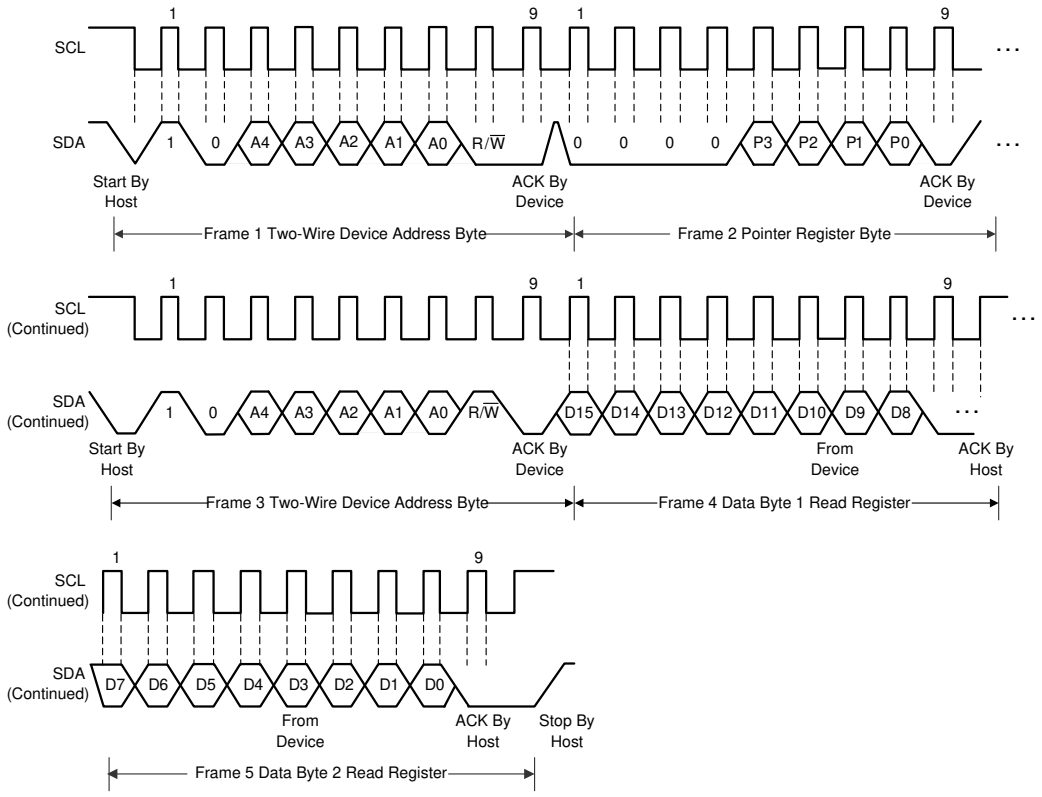


Figure 7-5. Two-Wire Timing Diagram for Read Word Format

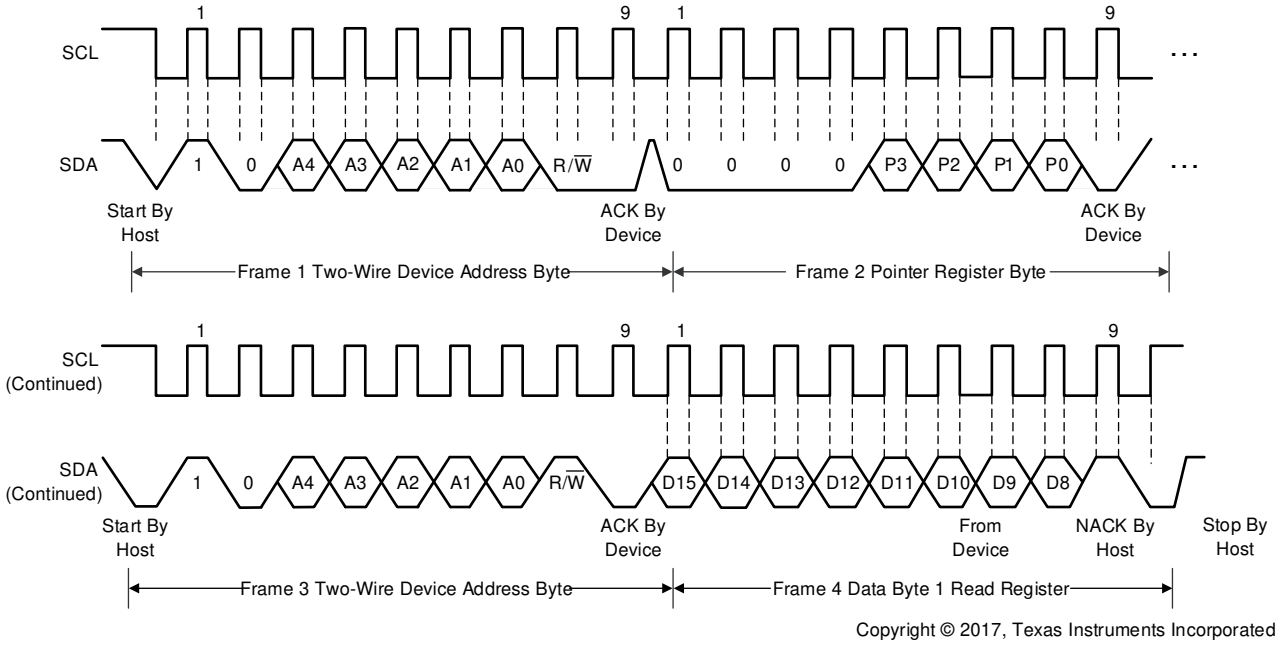


Figure 7-6. Two-Wire Timing Diagram for Read Single Byte Format

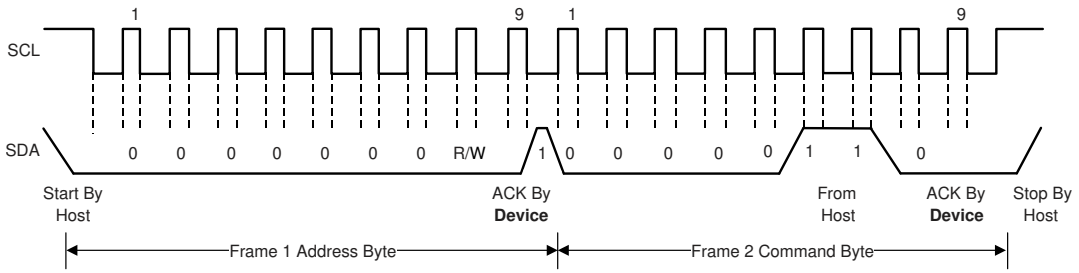


Figure 7-7. General-Call Reset Command Timing Diagram

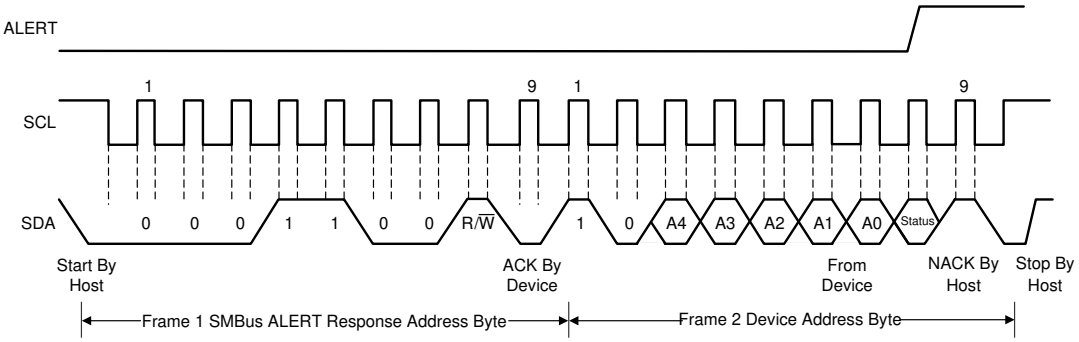


Figure 7-8. Timing Diagram for SMBus Alert

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

Shutdown mode (SD) of the TMP1075 device allows the user to conserve power by shutting down all device circuitry except the serial interface, which significantly reduces the current consumption. SD is initiated when the SD bit in the configuration register is set to 1. When SD is equal to 0, the device stays in continuous conversion mode.

7.4.2 One-Shot Mode (OS)

The TMP1075 features a one-shot mode (OS) temperature measurement. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP1075 when continuous temperature monitoring is not required.

When the configuration register is read, the OS bit always reads 0 on TMP1075 non-N orderables. On the TMP1075N orderable, the OS bit reads back 0 during the one-shot conversion and 1 after the conversion cycle.

7.4.3 Continuous Conversion Mode (CC)

When the device is operating in continuous conversion mode (SD=0), every conversion cycle consists of an active conversion, followed by a standby (see Figure 7-9). The device consumes a higher current during an active conversion, and lower current during standby. Active conversion time is 5.5 ms (TMP1075N: 10 ms) before the part goes in standby. Table 7-8 shows the list of conversion cycle configured using [R1:R0] bits in the configuration register.

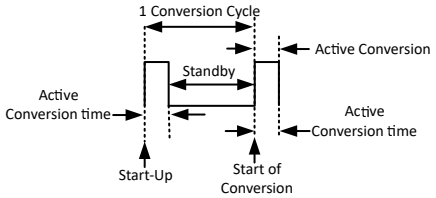


Figure 7-9. Conversion Rate Diagram

7.4.4 Thermostat Mode (TM)

The thermostat mode bit indicates whether ALERT pin operates in comparator mode (TM = 0) or interrupt mode (TM = 1). ALERT pin mode is controlled by TM (bit 9) of the configuration register. Any write to the TM bit changes the ALERT pin to a none active condition, clears the faults count, and clears the alert interrupt history on the TMP1075 non-N orderables. The ALERT pin can be disabled in both comparator and interrupt modes if both limit registers are set to the rail values T_{LOW} = –128°C and T_{HIGH} = +127.9375°C on the TMP1075 non-N orderables.

7.4.4.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of Fault Queue bits [F1:F0]. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of system noise. The SMBus Alert response function is ignored in the comparator mode.

7.4.4.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the device starts to compare temperature readings with the high limit register value. The ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of conversions as set by the Fault Queue bits [F1:F0]. The ALERT pin remains active until the pin is cleared by one of three events: a read of any register, a successful SMBus Alert response, or a shutdown command. After the ALERT pin is cleared, the device starts to compare temperature readings with the T_{LOW}. The ALERT pin becomes active again only when the temperature drops below T_{LOW} for a consecutive number of conversions as set by the Fault Queue bits. The ALERT pin remains active until cleared by any of the same three clearing events. After the ALERT pin is cleared by one of the events, the cycle repeats and the device resumes to compare the temperature to T_{HIGH}. The interrupt mode history is cleared by a change in the TM=0 bit, setting the device to SD mode, or resetting the device on the TMP1075 non-N orderables.

7.4.4.3 Polarity Mode (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. Figure 7-10 shows the operation of the ALERT pin in various modes.

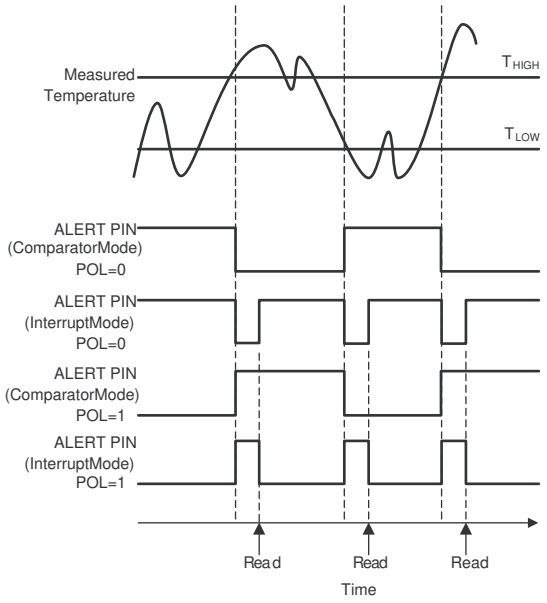


Figure 7-10. Output Transfer Function Diagrams

7.5 Register Map

Table 7-5. TMP1075 Register Map

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	0000h	TEMP	Temperature result register	Go
01h	R/W	00FFh	CFGR	Configuration register	Go
02h	R/W	4B00h	LLIM	Low limit register	Go
03h	R/W	5000h	HLIM	High limit register	Go
0Fh(1)	R	7500h	DIEID	Device ID register	Go

(1) Device ID register not available on TMP1075N

Note

TMP1075 Configuration register supports single byte read and write for software compatibility with xx75 standard temperature sensors.

7.5.1 Register Descriptions

Table 7-6. TMP1075 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.1 Temperature Register (address = 00h) [default reset = 0000h]

The temperature register of the TMP1075 is a 12-bit, read-only register that stores the result of the most recent conversion (see Figure 7-11). Data is represented in binary two's complement format. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset, the temperature register value is 0°C until the first conversion is complete.

Figure 7-11. Temperature Register

15	14	13	12	11	10	9	8
T11	T10	T9	T8	T7	T6	T5	T4
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
T3	T2	T1	T0	0	0	0	0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 7-7. Temperature Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	T[11:0]	R	000h	12-bit, read-only register that stores the most recent temperature conversion results.
3:0	—	R	0h	Not used

7.5.1.2 Configuration Register (address = 01h) [default reset = 00FFh (60A0h TMP1075N)]

The configuration register is an 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. Figure 7-12 shows the format of the configuration register for the TMP1075, followed by a breakdown of the register bits. The power-up or reset value of the configuration register are all bits equal to 00FFh (TMP1075N: 60A0h). Only single byte writes and reads must be used when pointing to the configuration register for proper operation on the TMP1075N orderable.

Figure 7-12. Configuration Register: TMP1075

15	14	13	12	11	10	9	8
OS	R1	R0	F1	F0	POL	TM	SD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Figure 7-13. Configuration Register: TMP1075N

15	14	13	12	11	10	9	8
OS	R1	R0	F1	F0	POL	TM	SD
R/W-0	R-1	R-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
1	0	x	0	0	0	0	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 7-8. Configuration Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	OS	R/W	0	One-shot conversion mode. Writing 1, starts a single temperature conversion. Read returns 0.
14:13	R[1:0]	R/W R (TMP1075N)	0 11 (TMP1075N)	Conversion rate setting when device is in continuous conversion mode 00: 27.5 ms conversion rate 01: 55 ms conversion rate 10: 110 ms conversion rate 11: 220 ms conversion rate (250 ms TMP1075N)
12:11	F[1:0]	R/W	0	Consecutive fault measurements to trigger the alert function 00: 1 fault 01: 2 faults 10: 3 faults (4 faults TMP1075N) 11: 4 faults (6 faults TMP1075N)
10	POL	R/W	0	Polarity of the output pin 0: Active low ALERT pin 1: Active high ALERT pin
9	TM	R/W	0	Selects the function of the ALERT pin 0: ALERT pin functions in comparator mode 1: ALERT pin functions in interrupt mode
8	SD	R/W	0	Sets the device in shutdown mode to conserve power 0: Device is in continuous conversion 1: Device is in shutdown mode
7:0	—	R/W	FFh A0h (TMP1075N)	Not used Reserved on TMP1075N package

Note

The configuration register supports single-byte read and write over I^2C bus to verify software compatibility with other xx75 standard temperature sensors like TMP75 and LM75. When a single byte write is performed, the data byte on the I^2C bus updates the register bits 15-8. Similarly when a single byte read is performed, the data bits 15-8 is transferred over the I^2C bus.

7.5.1.3 Low Limit Register (address = 02h) [default reset = 4B00h]

The register is configured as a 12-bit, read/write register and data is represented in two's complement format. Figure 7-14 shows the layout for T_{LOW} is the same as the temperature register. The default reset value is 4B00h and corresponds to 75°C.

Figure 7-14. Low Limit Register

15	14	13	12	11	10	9	8
L11	L10	L9	L8	L7	L6	L5	L4
R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
7	6	5	4	3	2	1	0
L3	L2	L1	L0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-9. Low Limit Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	L[11:0]	R/W	4B0h	12-bit, read-write register that stores the low limit for comparison with temperature results.
3:0	—	R/W	0h	Not used

7.5.1.4 High Limit Register (address = 03h) [default reset = 5000h]

The register is configured as a 12-bit, read/write register and data is represented in two's complement format. Figure 7-15 show the layout for T_{HIGH} is the same as the temperature register. The default reset value is 5000h and corresponds to 80°C.

Figure 7-15. High Limit Register

15	14	13	12	11	10	9	8
H11	H10	H9	H8	H7	H6	H5	H4
R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
H3	H2	H1	H0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-10. High Limit Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:4	H[11:0]	R/W	500h	12-bit, read-write register that stores the high limit for comparison with temperature results.
3:0	—	R/W	0h	Not used

7.5.1.5 Device ID Register (address = 0Fh) [default reset = 7500]

Figure 7-16 shows this read-only register reads the device ID, and this register only available on the TMP1075 non-N orderables.

Figure 7-16. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R-0	R-1	R-1	R-1	R-0	R-1	R-0	R-1
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 7-11. Device ID Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	DID[15:0]	R/W	7500h	16-bit, read-only register that stores the die ID for the device. The MSB reads the static value 75h to indicate the device name for TMP1075

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMP1075 can measure the PCB temperature of the location where the user mounts the device. The TMP1075 features two-wire SMBus and I^2C interface compatibility, with the TMP1075 allowing up to 32 (TMP1075N: 4) devices on one bus. The TMP1075 requires a pullup resistor on the SDA pin, and if needed, on the SCL and ALERT pins. A 0.01-µF bypass capacitor is also required (see Figure 8-1).

8.2 Typical Application

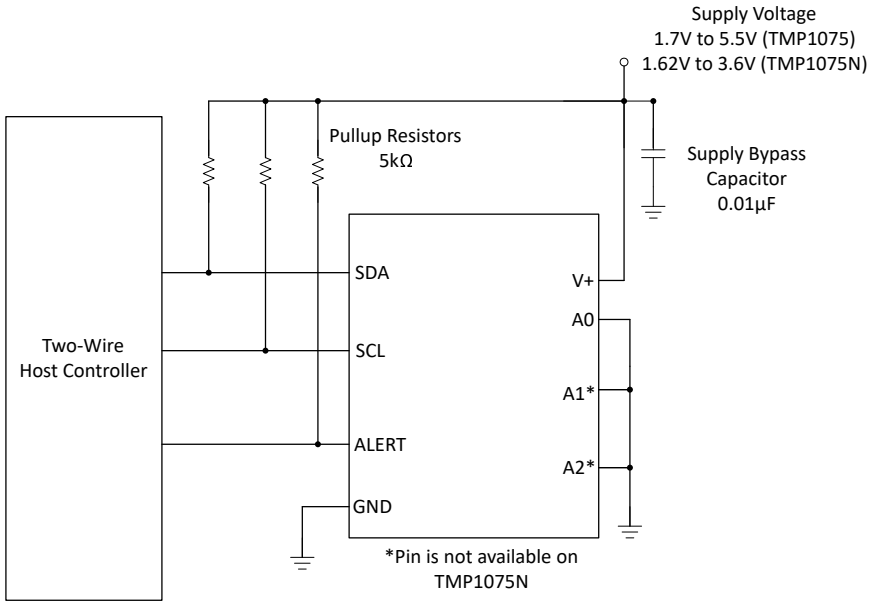


Figure 8-1. Typical Connections

8.2.1 Design Requirements

The recommended value for the pullup resistor is 5 kΩ. In some applications, the pullup resistor can be lower or higher than 5 kΩ, but the maximum current through the pullup current is recommended to not exceed 3 mA on the SCL and SDA pins. The SCL, SDA, A0, and A1, lines can be pulled up to a supply that is higher than V+. The ALERT line can be pulled up to a supply higher than V+ on the TMP1075 non-N orderables. The A2 pin can only be connected to GND or V+. When the ALERT pin is not used, the pin can either be connected GND or left floating.

8.2.2 Detailed Design Procedure

Place the TMP1075 device in close proximity to the heat source that must be monitored with a proper layout for good thermal coupling. This placement verifies that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.2.1 Migrating From the xx75 Device Family

The TMP1075 is designed specifically to be a pin-to-pin compatible replacement with xx75 family of devices. This includes considerations for software compatibility. The two byte registers of the TMP1075 dynamically support single byte read or write, meaning that replacing older xx75 standard temperature sensors do not require any updates to existing code.

8.2.3 Application Curve

For application curves, see Table 8-1:

Table 8-1. Table of Graphs

FIGURE	TITLE
Figure 6-10	Sampling Period Change vs. Temperature (1.7 V to 5.5 V)

8.3 Power Supply Recommendations

The TMP1075 D, DGK, and DSG packages operate with a power supply in the range of 1.7 V to 5.5 V (TMP1075N DRL package operates from 1.62 V to 3.6 V). A power-supply bypass capacitor is required for precision and stability. Place this power-supply bypass capacitor as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

For minimizing device self-heating and improving temperature precision, TI recommends to:

- Use the minimum supply voltage rail available
- Avoid communication over I^2C bus during ADC conversion
- Use one-shot mode to minimize power consumption
- Set I^2C signal levels V_{IL} close to ground and V_{IH} above 90% of V+
- Maintain the I2C bus signals positive edge less than 1 µs by using a pullup resistor < 10 kΩ
- Connect the address pins A_0 and A_1 to either ground or V+

8.4 Layout

8.4.1 Layout Guidelines

Place the power-supply bypass capacitor as close to the supply and ground pins as possible. The recommended value of this bypass capacitor is 0.01 µF. Pullup the open-drain output pins SDA and ALERT through 5-kΩ pullup resistors. The SCL requires a pullup resistor only if the microprocessor output is open drain.

8.4.2 Layout Example

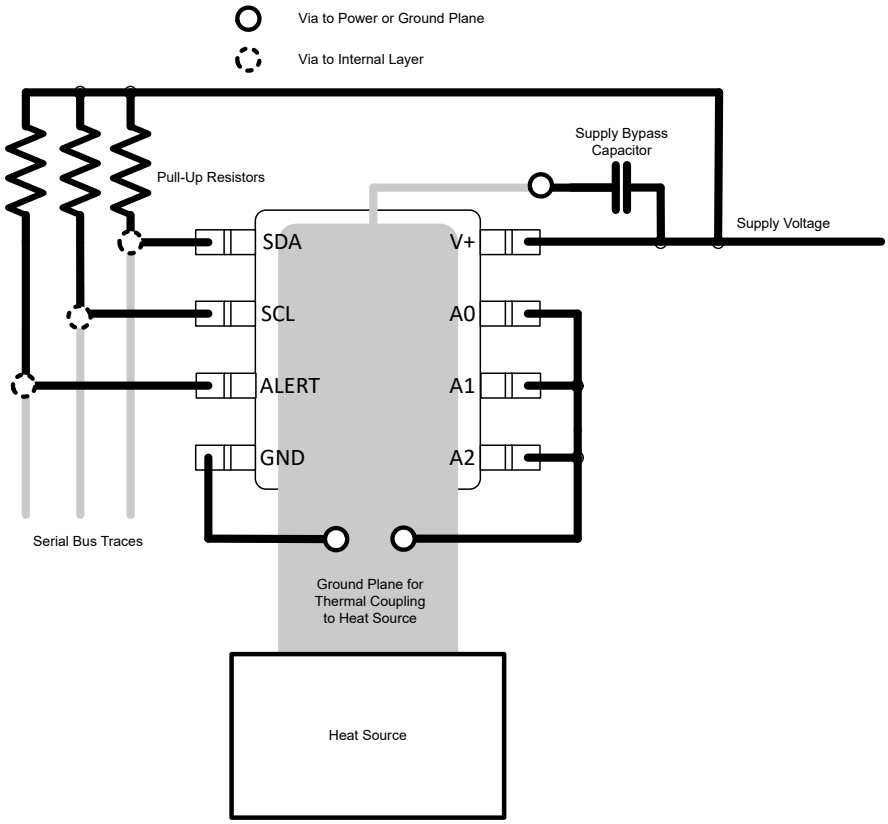


Figure 8-2. Layout Example (D Package)

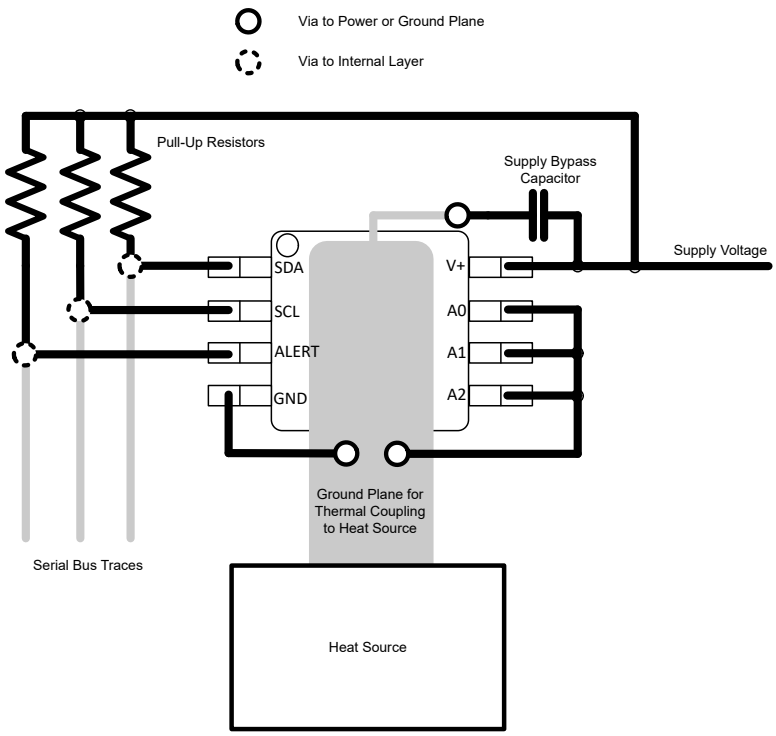


Figure 8-3. Layout Example (DGK Package)

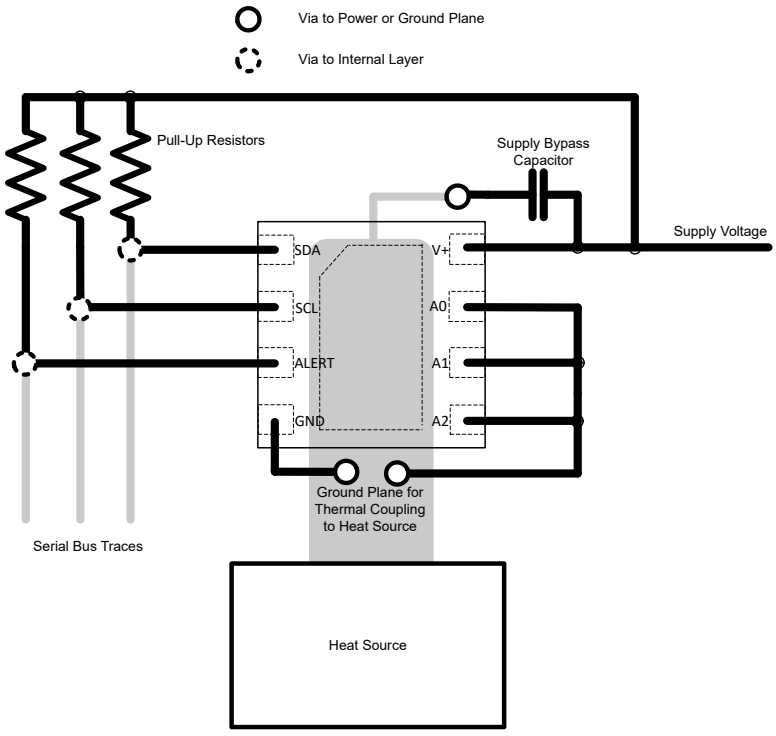


Figure 8-4. Layout Example (DSG Package)

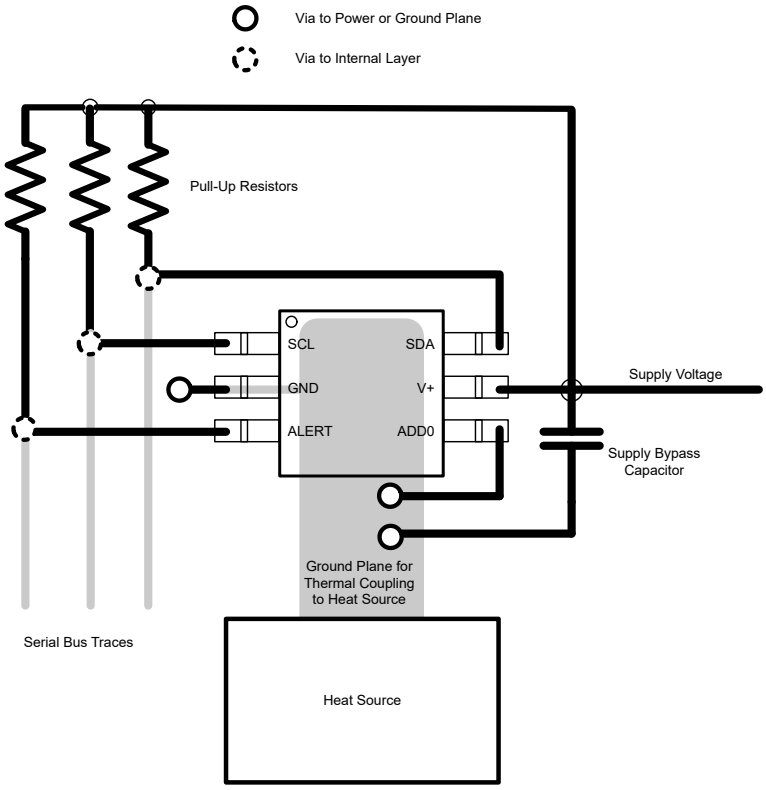


Figure 8-5. Layout Example (DRL Package)

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP102 Low-Power Digital Temperature Sensor With SMBus and Two-Wire Serial Interface in SOT563*, data sheet
- Texas Instruments, *TMP112x High-Accuracy, Low-Power, Digital Temperature Sensors With SMBus and TwoWire Serial Interface in SOT563*, data sheet
- Texas Instruments, *TMP110 Ultra-Small, ±1.0°C Accurate, I2C Digital Temperature Sensor for Cost-Sensitive Systems*, data sheet
- Texas Instruments, *TMP LM 75 Comparison Common FAQs*, application note
-

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2021) to Revision F (June 2024)	Page
• Changed all instances of legacy terminology to controller and target where I2C is mentioned	1
• Updated the number format for tables, figures, and cross-references throughout the document	1
• Changed the "Conversion time" for TMP1075N throughout the document	1
• Changed the shutdown and average current for TMP1075N throughout the document	1
• Changed DRL package *Thermal Information* section	6
• Changed "Conversion time" for TMP1075N in *Electrical Characteristics* table	7
• Changed Average current consumption for TMP1075N in *Electrical Characteristics* table	7
• Changed Shutdown current for TMP1075N in *Electrical Characteristics* table	7
• Added Two-Wire Timing Diagram	9

- Changed conversion rate of TMP1075N from 35 ms to 250 ms 22

Changes from Revision D (October 2019) to Revision E (August 2021) **Page**

- Added TMP1075N features to list..... 1
- Added typical accuracy specification to features list..... 1
- Added the SOT563 (TMP1075N orderable) package..... 1
- Added Device Comparison Section..... 3
- Added figures for different package options..... 4
- Added column for TMP1075N pin numbers..... 4
- Added TMP1075N Specifications..... 5
- Added *TMP1075NDRL Temperature Error vs. Temperature* graph 10
- Added TMP1075N information in Overview Section..... 12
- Changed the *Functional Block Diagram* to apply to TMP1075N..... 12
- Added number of I2C addresses available on TMP1075N to Serial Bus Address Section. 14
- Added table for TMP1075N address options. 14
- Updated internal register structure figure to apply to TMP1075N..... 14
- Added typical specification for TMP1075N timeout 16
- Added clarification on timeout function to include SCL..... 16
- Removed redundant information to accurate describe all packages..... 19
- Added TMP1075N OS bit behavior..... 19
- Added TMP1075N Continuous Conversion Mode information..... 19
- Updated Conversion Rate Diagram to reflect all TMP1075 and TMP1075N..... 19
- Clarified what TM bit behavior for TMP1075 and TMP1075N 20
- Added table note to indicate Device ID register is not available on TMP1075N..... 21
- Added TMP1075N configuration register information 22
- Updated text to indicate that device ID register does not apply to TMP1075N..... 24
- Added number of I2C addresses available on TMP1075N..... 24
- Changed Typical Connections figure to apply to TMP1075N..... 25
- Removed redundant Application Curve section..... 25
- Updated text to include TMP1075N information..... 25
- Updated Migrating From the xx75 Device Family section to specify TMP1075 compatible packages 25
- Included TMP1075N information to Power Supply Recommendations..... 26
- Added figures to the *Layout Example* section for each package..... 26

Changes from Revision C (January 2019) to Revision D (October 2019) **Page**

- Added software compatibility to feature list..... 1
- Updated pointer register to be part of the serial interface description..... 14
- Updated the register map table to new format..... 21
- Added access type codes for register bits..... 21
- Updated temperature register format and bit definition table..... 21
- Changed configuration register format and bit definition table 22
- Updated low limit register format and bit definition table 23
- Updated high limit register format and bit definition table 23
- Updated device ID register format and bit definition table 24

Changes from Revision B (December 2018) to Revision C (January 2019) **Page**

- Changed TMP1075DSG package moved from Preview to Production Data..... 1
- Changed min/max limit from 1.5°C to 1°C in the *Temperature Accuracy (DGK & D)* graph..... 1
- Changed min/max limit from 1.5°C to 1°C in the *DGK & D Temperature Error vs. Temperature* graph..... 10

- Added *DSG Temperature Error vs. Temperature* graph 10

Changes from Revision A (June 2018) to Revision B (December 2018) **Page**

- Added TMP1075DSG package 1
- Updated description section of the data sheet and added a *Description (continued)* section..... 1
- Added TMP1075 configuration register support for single byte read and write..... 22
- Added Software support section for migrating from xx75 to TMP1075 25

Changes from Revision * (March 2018) to Revision A (June 2018) **Page**

- Changed the TMP1075DGK orderable status from Advanced Information to Production Data..... 1
- Added SOIC and DFN packages..... 1
- Changed the *Functional Block Diagram* 12
- Changed *Digital Temperature Output* cross-reference from: *Temperature Register (0x00)* to: *Temperature Data Format* 13
- Changed the *Temperature Data Format* table 13
- Changed and renamed the *Address Pins and Slave Addresses for the TMP1075* table to *Address Pins State* 14
- Changed the *Two-Wire Timing Diagrams* section 17
- Added content to the *Device Functional Modes* section 19

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP1075DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-55 to 125	1075	Samples
TMP1075DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1075	Samples
TMP1075DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1AE	Samples
TMP1075NDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N75	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

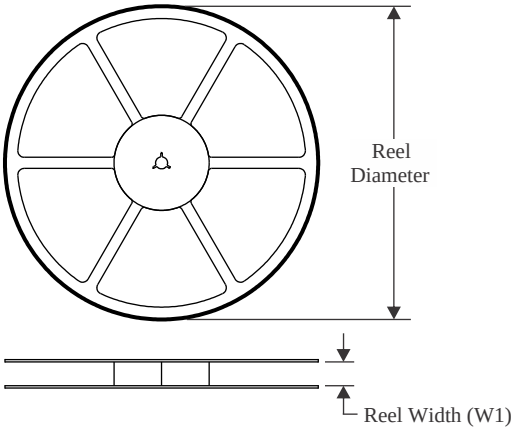
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

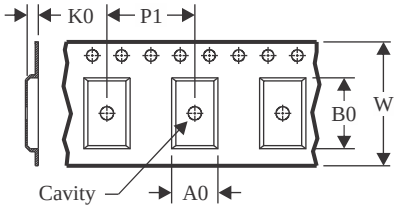
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

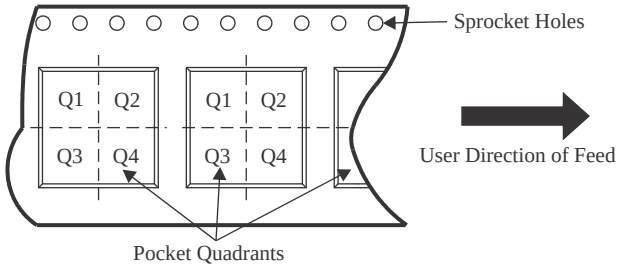


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

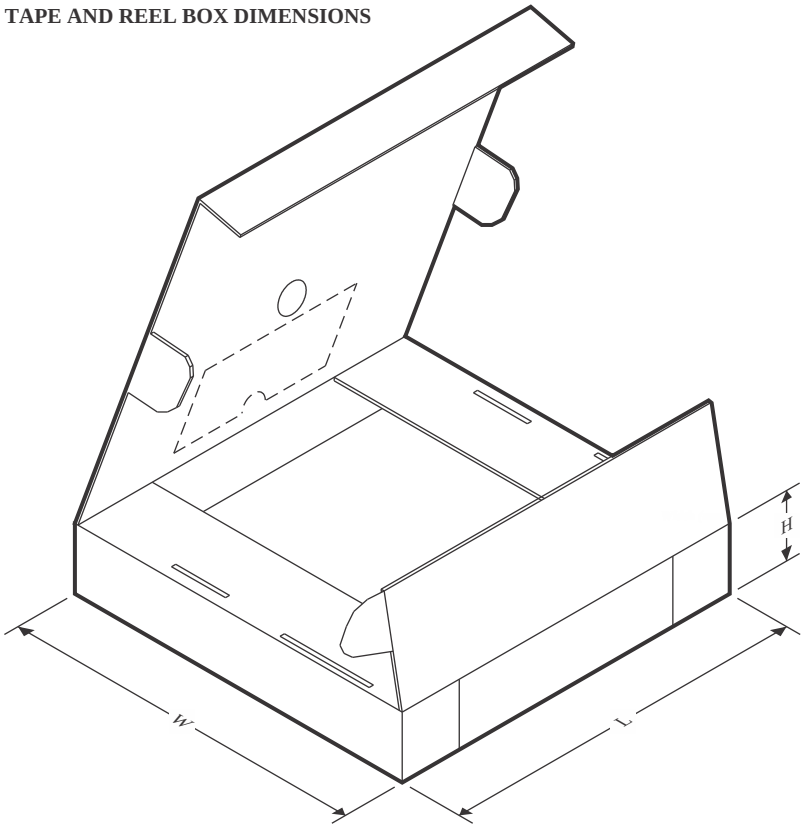
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

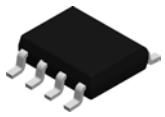
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP1075DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP1075DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP1075DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TMP1075NDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP1075DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP1075DR	SOIC	D	8	2500	356.0	356.0	35.0
TMP1075DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TMP1075NDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

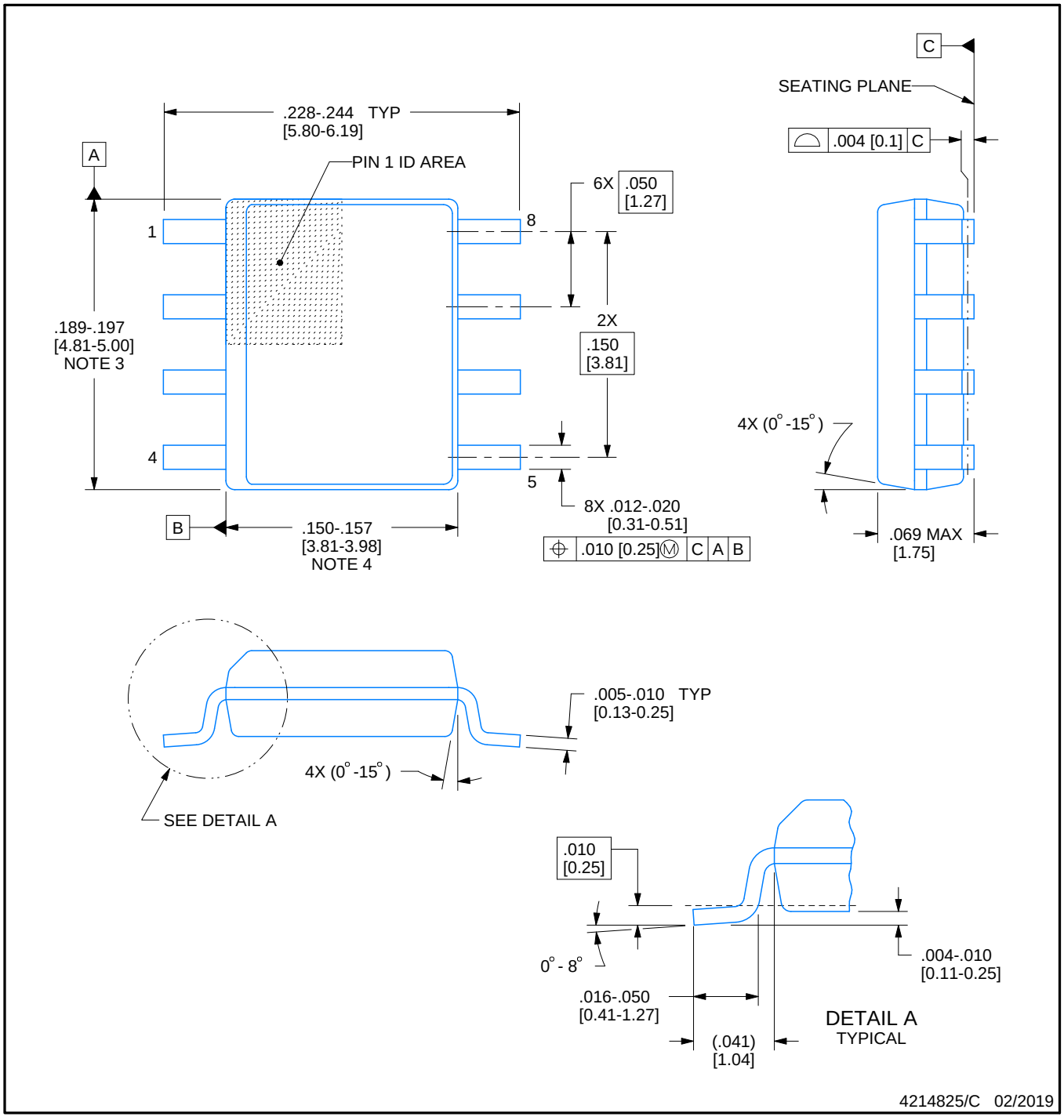


PACKAGE OUTLINE

D0008A

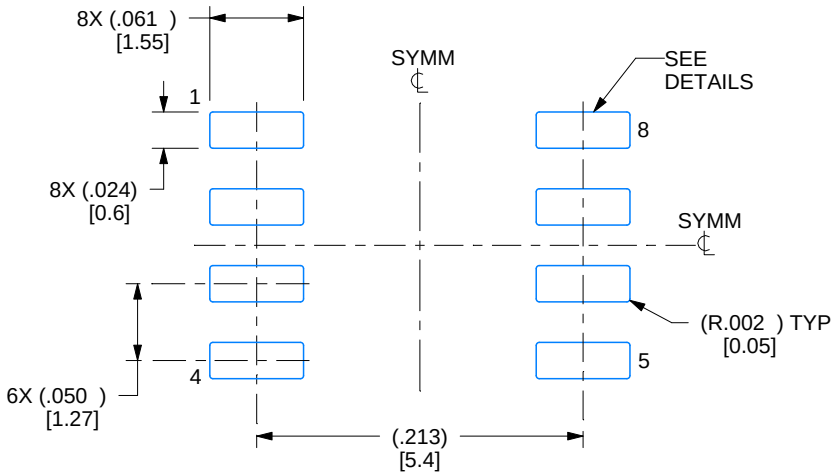
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

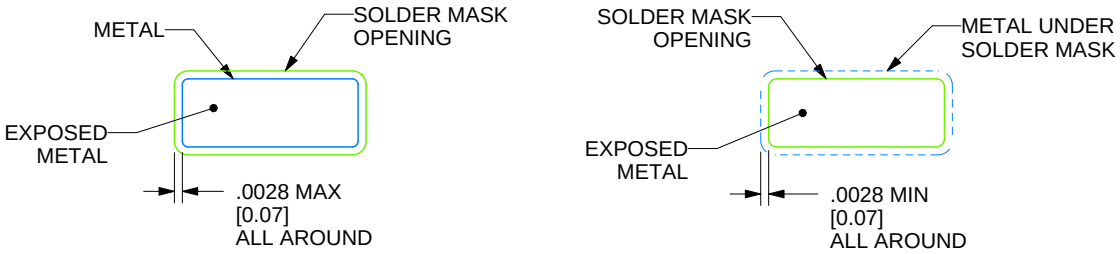


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

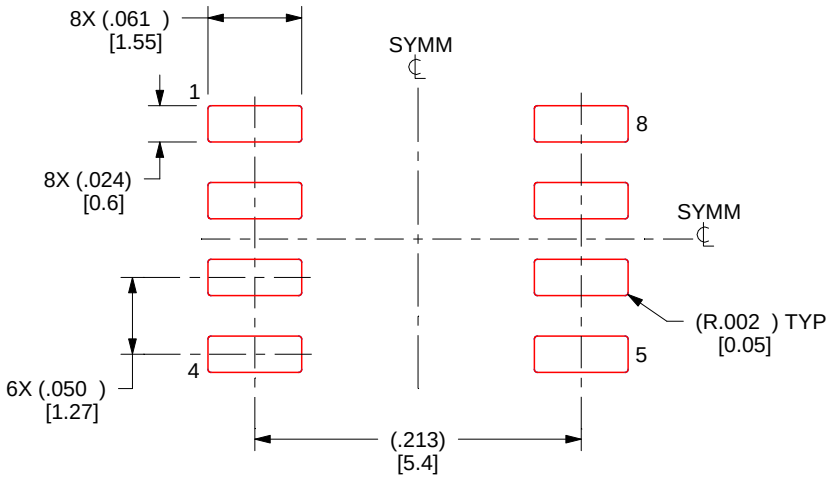
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

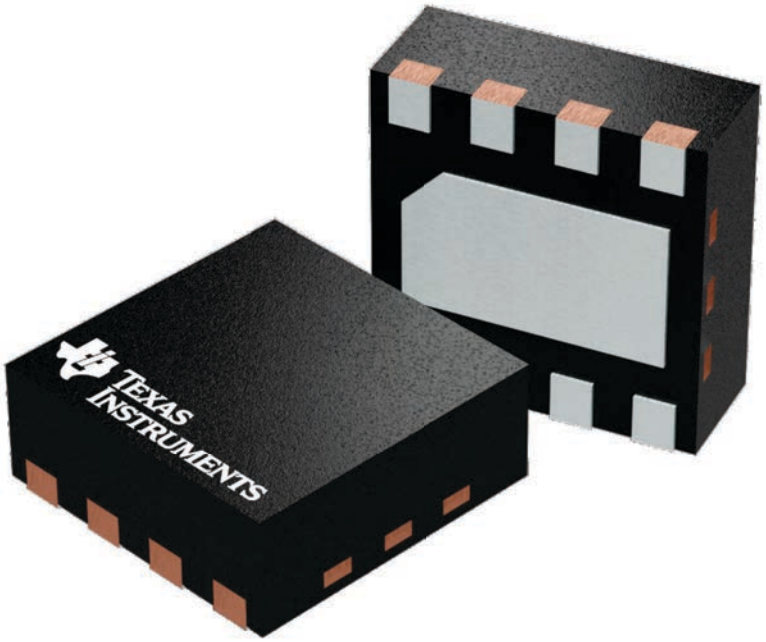
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



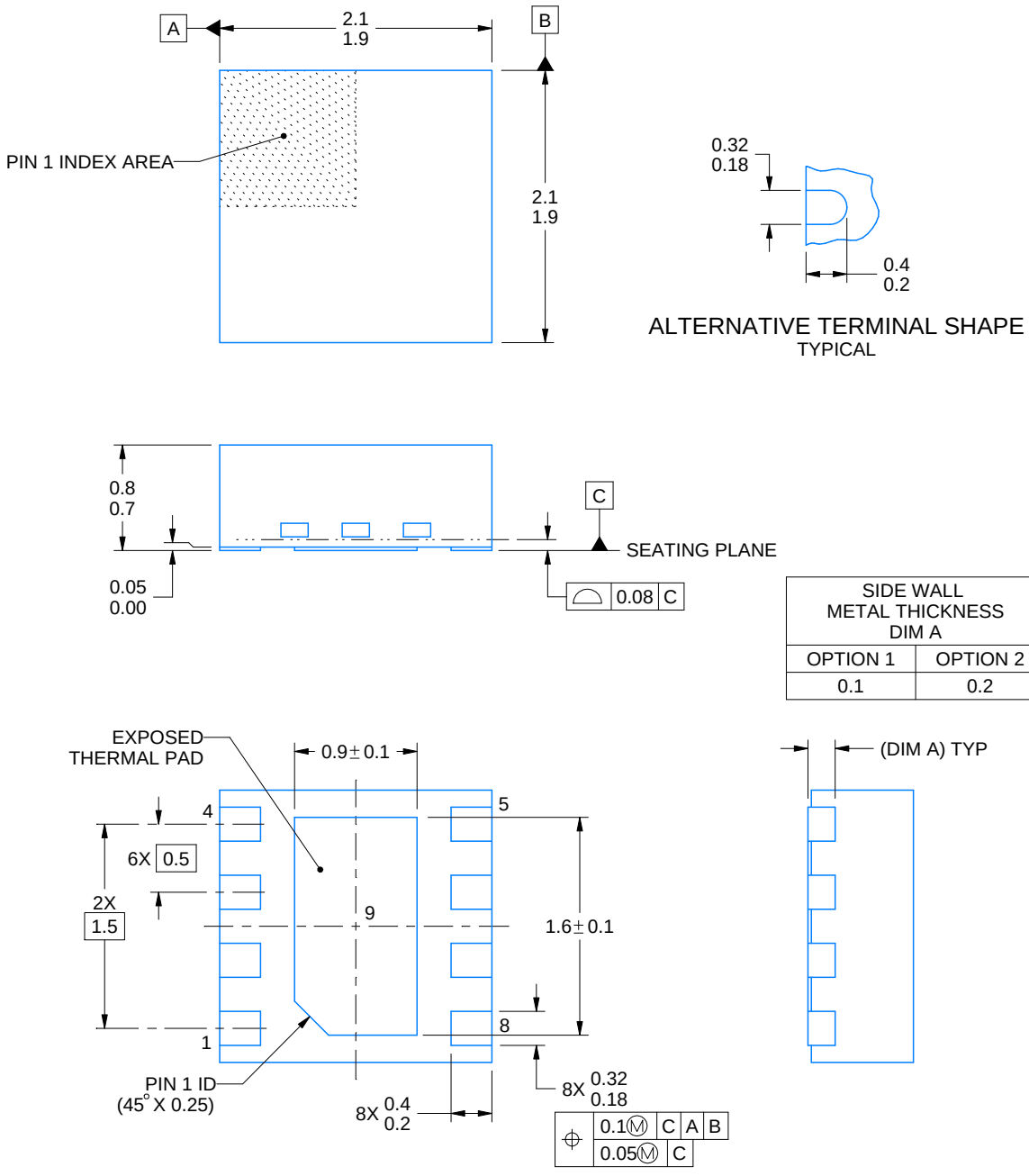
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

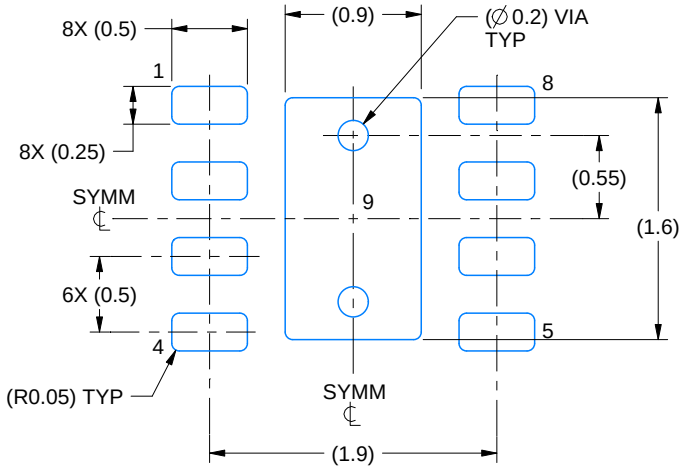
PLASTIC SMALL OUTLINE - NO LEAD



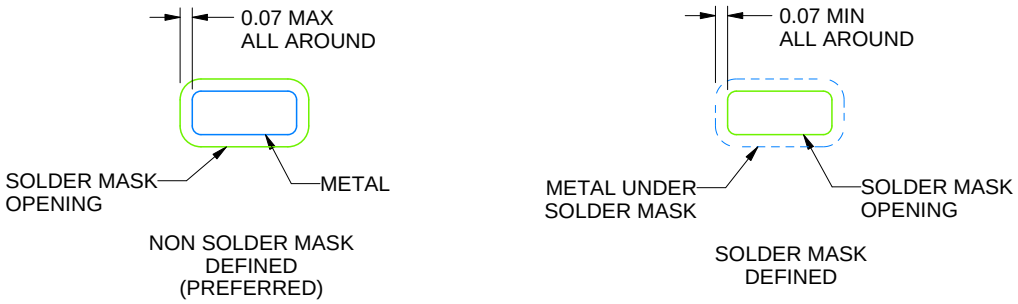
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

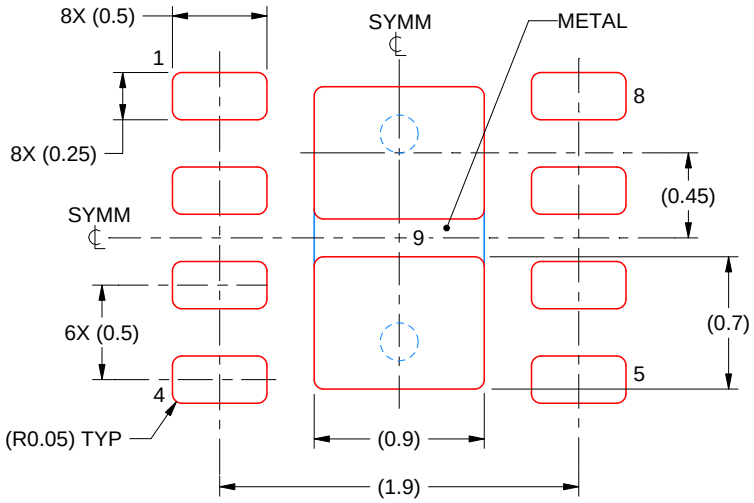


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

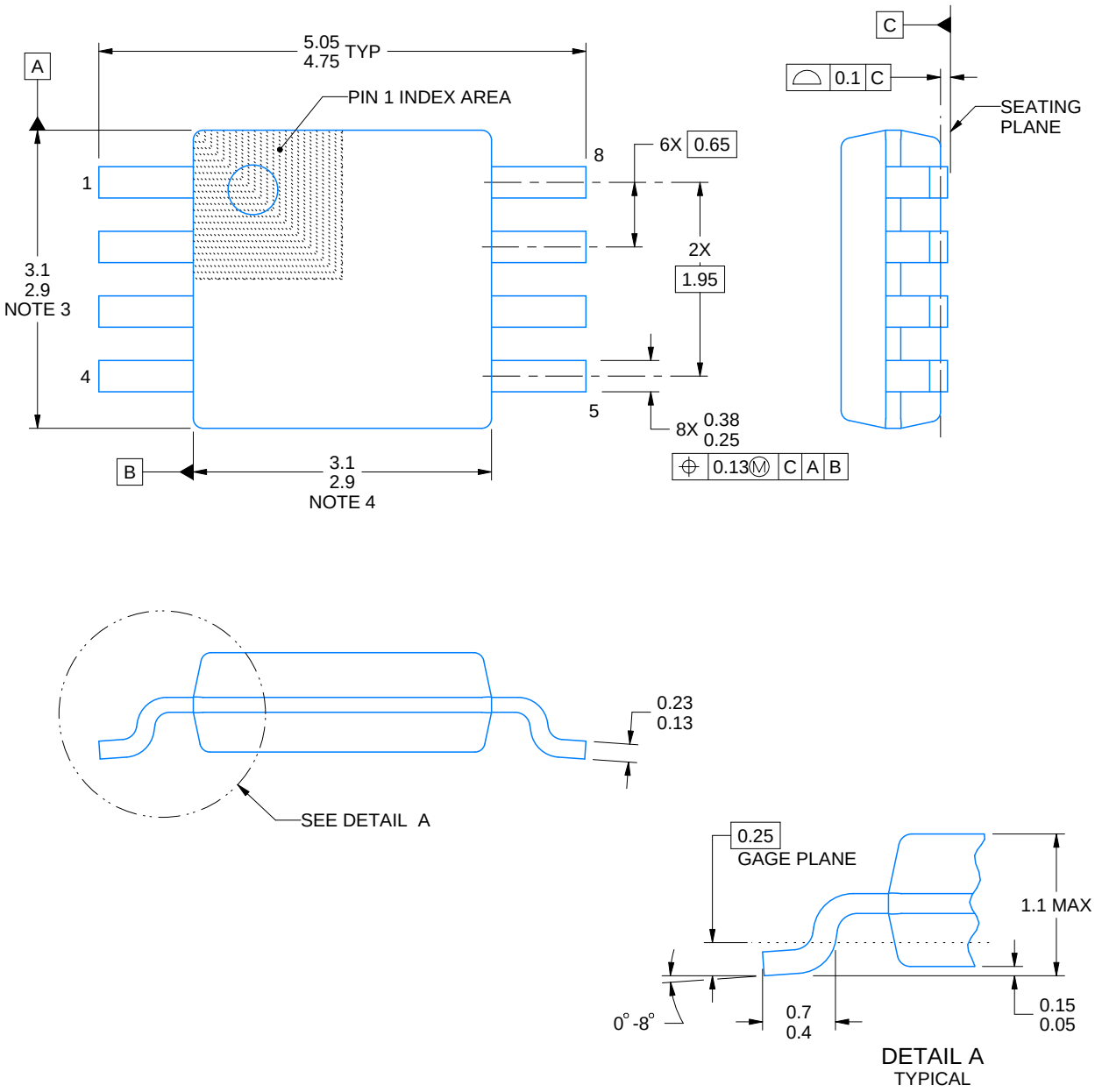
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

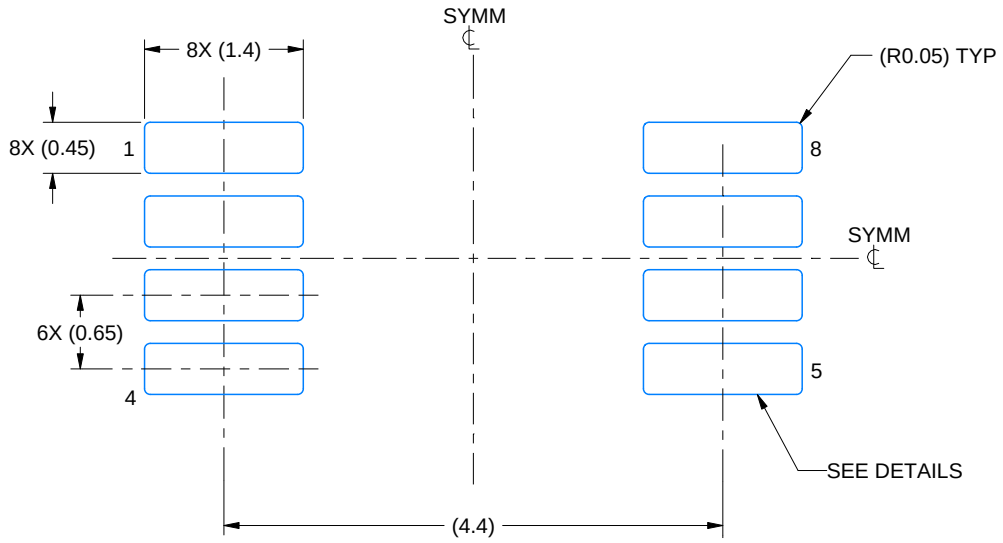
SMALL OUTLINE PACKAGE



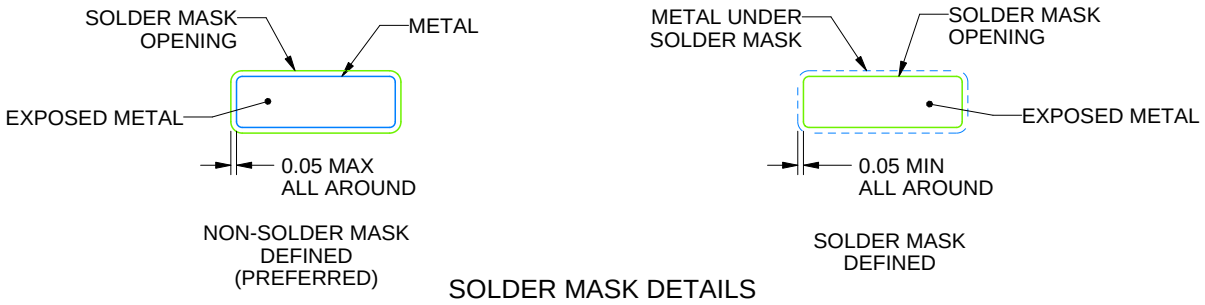
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

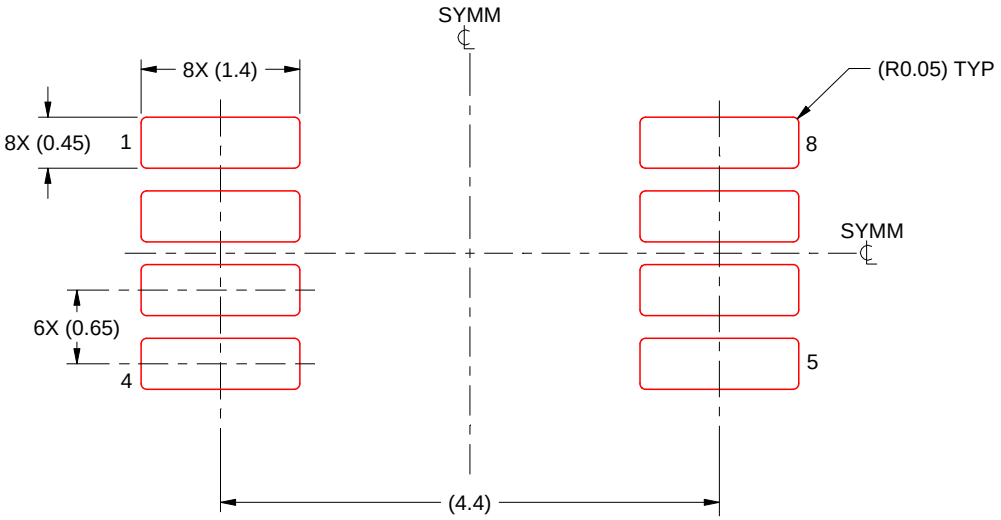


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

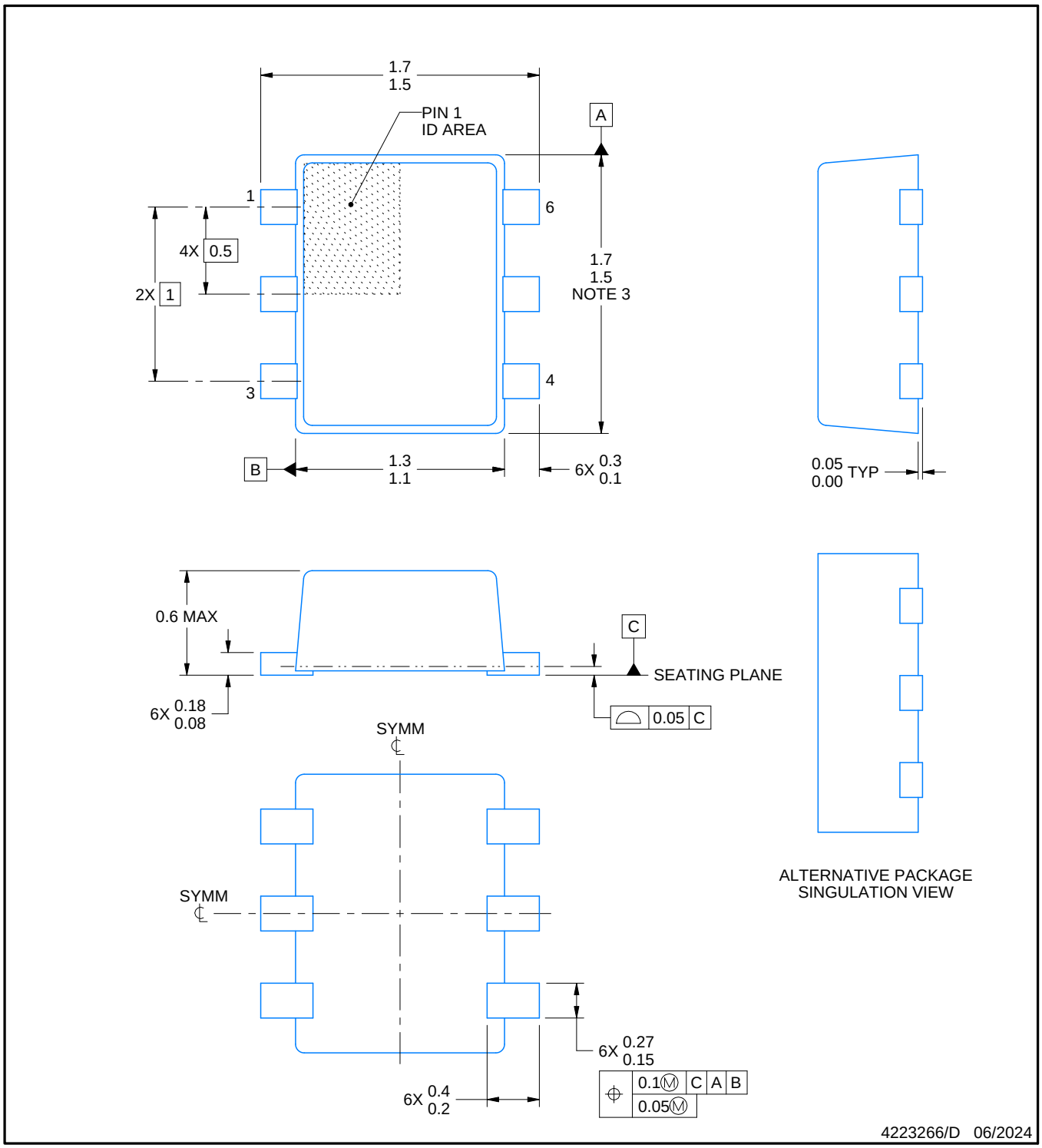


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



NOTES:

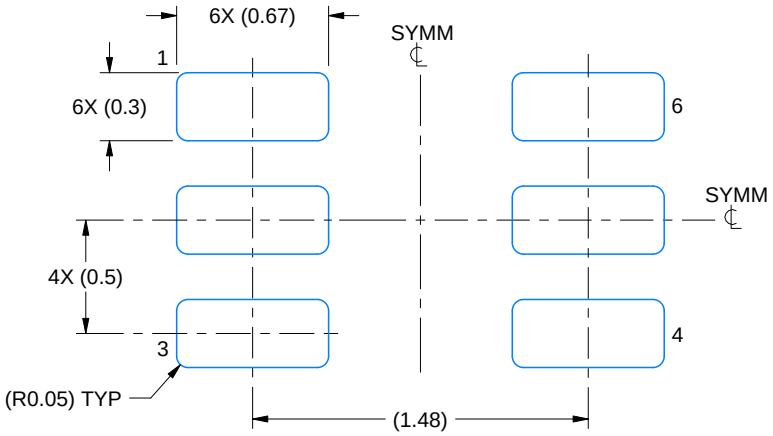
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

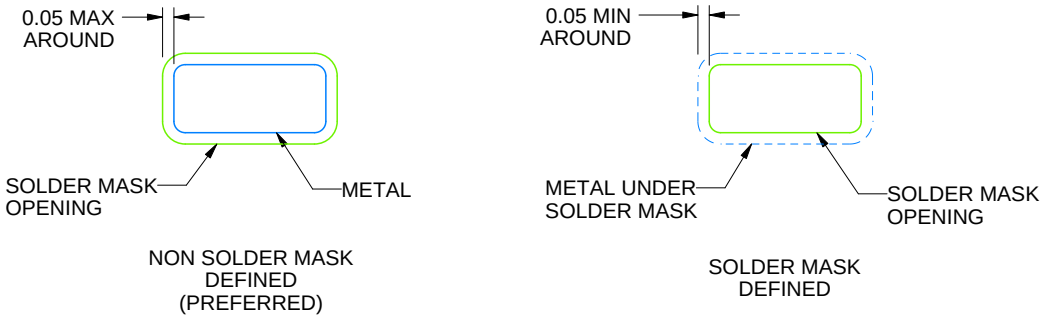
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/D 06/2024

NOTES: (continued)

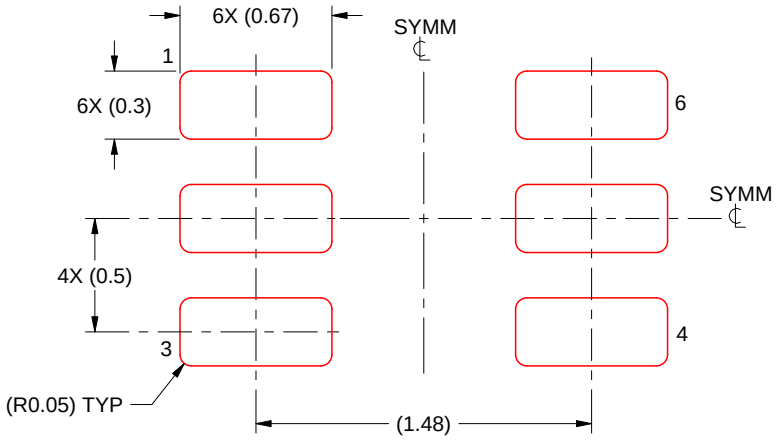
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/D 06/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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