



**THE DATASHEET OF  
IPA80R1K0CEXKSA2**



## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ CE

800V CoolMOS™ CE Power Transistor  
IPA80R1K0CE

## Data Sheet

Rev. 2.1  
Final

## 1 Description

CoolMOS™ CE is a revolutionary technology for high voltage power MOSFETs. The high voltage capability combines safety with performance and ruggedness to allow stable designs at highest efficiency level. CoolMOS™ 800V CE comes with selected package choice offering the benefit of reduced system costs and higher power density designs.

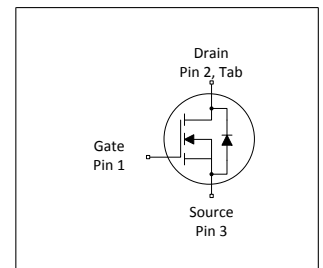
### Features

- High voltage technology
- Extreme  $dv/dt$  rated
- High peak current capability
- Low gate charge
- Low effective capacitances
- Pb-free plating, RoHS Compliant, Halogen free mold compound
- Qualified for consumer grade applications

### Applications

LED Lighting for retrofit applications in QR Flyback topology

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_j=25^\circ\text{C}$	800	V
$R_{DS(on),max}$	950	$m\Omega$
$Q_{g,typ}$	31	nC
$I_{D,pulse}$	18	A
$E_{oss}@400V$	2.4	$\mu\text{J}$
Body diode $di/dt$	400	$A/\mu\text{s}$

Type / Ordering Code	Package	Marking	Related Links
IPA80R1K0CE	PG-TO 220 FullPAK	8R1K0CE	see Appendix A

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## 2 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	5.7 3.6	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	230	mJ	$I_D=1.6\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.20	mJ	$I_D=1.6\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, repetitive	$I_{AR}$	-	-	1.60	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots640\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	32	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	5.7	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	4	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	400	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage for TO-220FP	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max} < 150^\circ\text{C}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

### 3 Thermal characteristics

**Table 3 Thermal characteristics TO-220 FullPAK**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	3.9	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

## 4 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V, I_D=0.25mA$
Gate threshold voltage	$V_{(GS)th}$	2.1	3.0	3.9	V	$V_{DS}=V_{GS}, I_D=0.25mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	10	$\mu A$	$V_{DS}=800, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=800, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.83	0.95	$\Omega$	$V_{GS}=10V, I_D=3.6A, T_j=25^\circ C$ $V_{GS}=10V, I_D=3.6A, T_j=150^\circ C$
Gate resistance	$R_G$	-	1.2	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	785	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	33	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	26	-	pF	$V_{GS}=0V, V_{DS}=0\dots 480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	69	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots 480V$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=5.7A,$ $R_G=15\Omega; \text{see table 9}$
Rise time	$t_r$	-	15	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=5.7A,$ $R_G=15\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	72	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=5.7A,$ $R_G=15\Omega; \text{see table 9}$
Fall time	$t_f$	-	8	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=5.7A,$ $R_G=15\Omega; \text{see table 9}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	4	-	nC	$V_{DD}=640V, I_D=5.7A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	15	-	nC	$V_{DD}=640V, I_D=5.7A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	31	-	nC	$V_{DD}=640V, I_D=5.7A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=640V, I_D=5.7A, V_{GS}=0 \text{ to } 10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1	-	V	$V_{GS}=0V, I_F=5.7A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	520	-	ns	$V_R=400V, I_F=5.7A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	5	-	$\mu C$	$V_R=400V, I_F=5.7A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	18	-	A	$V_R=400V, I_F=5.7A, di_F/dt=100A/\mu s$ ; see table 8

### 5 Electrical characteristics diagrams

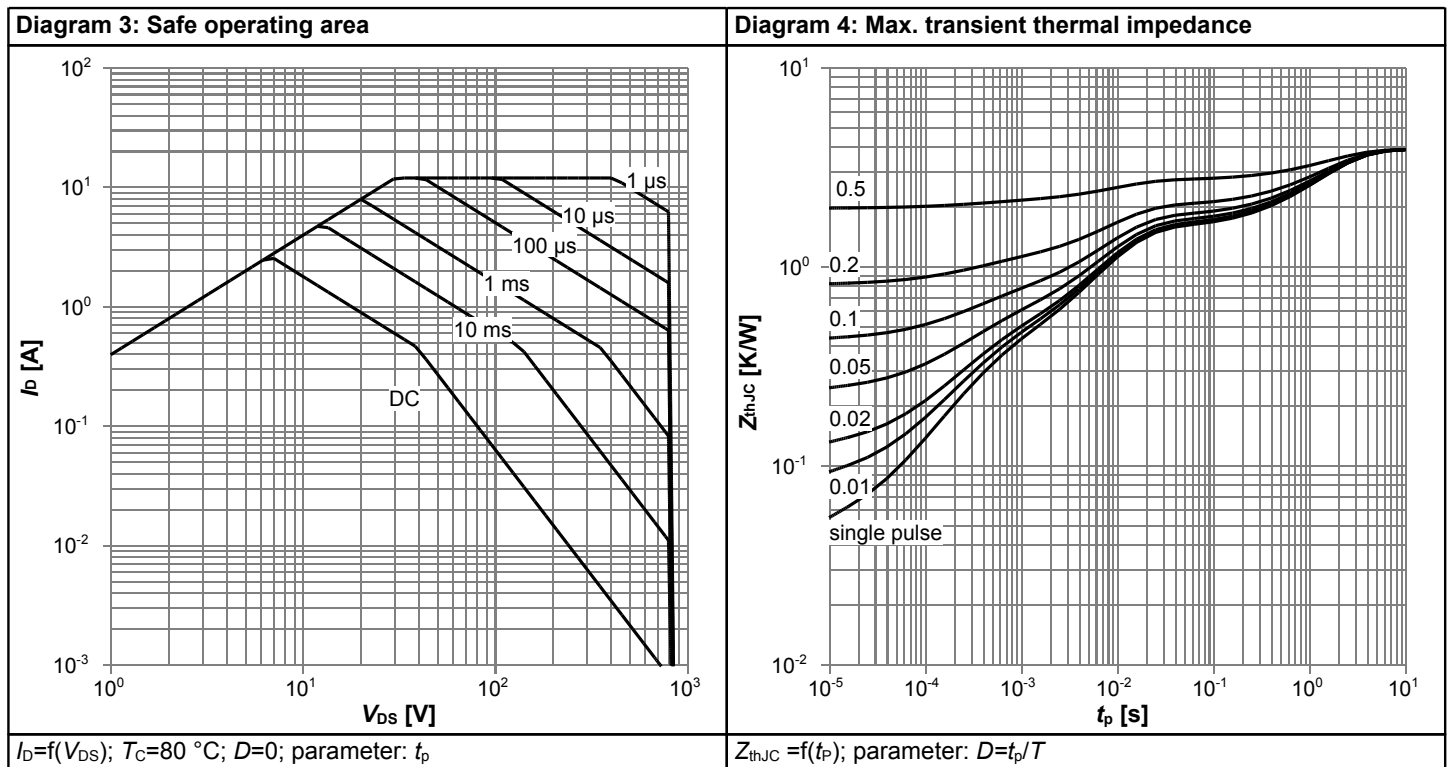
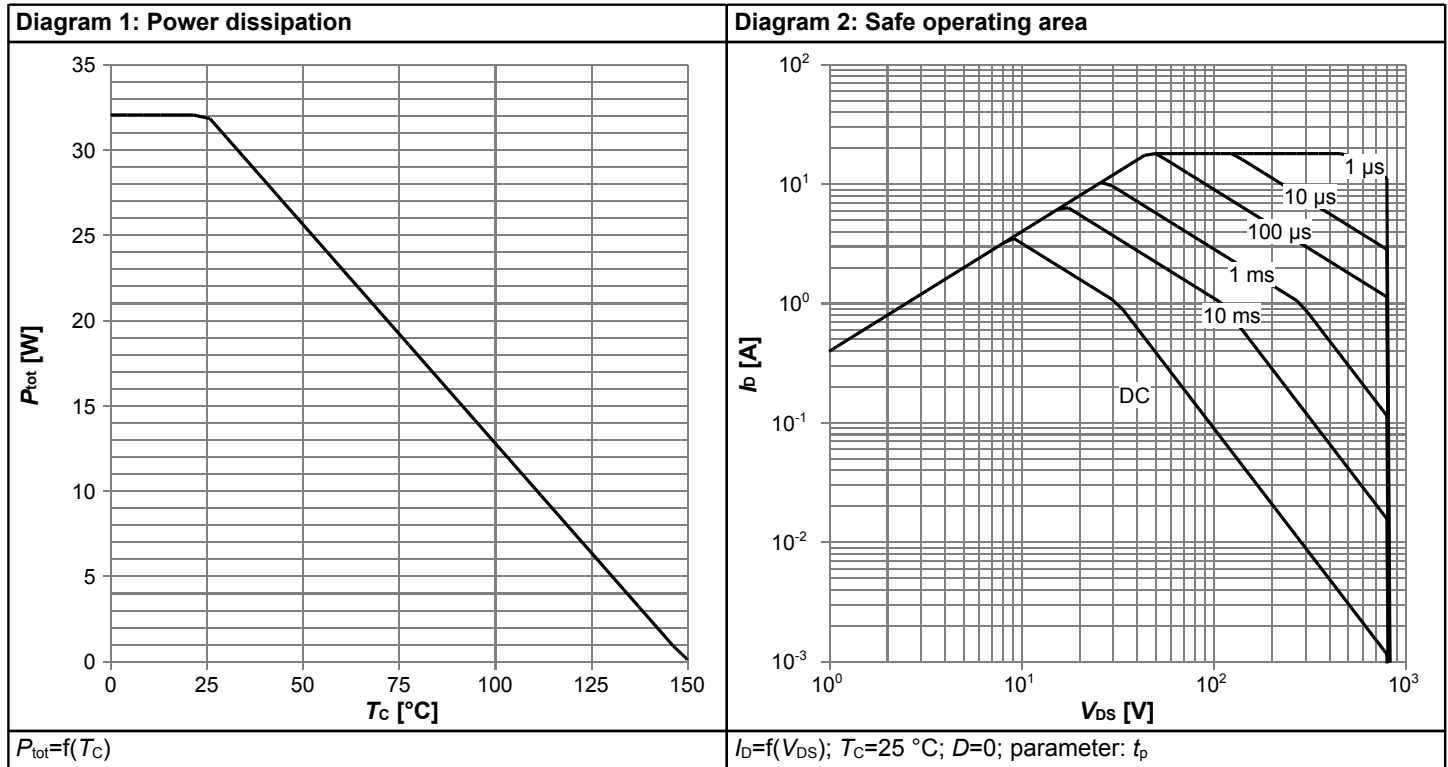
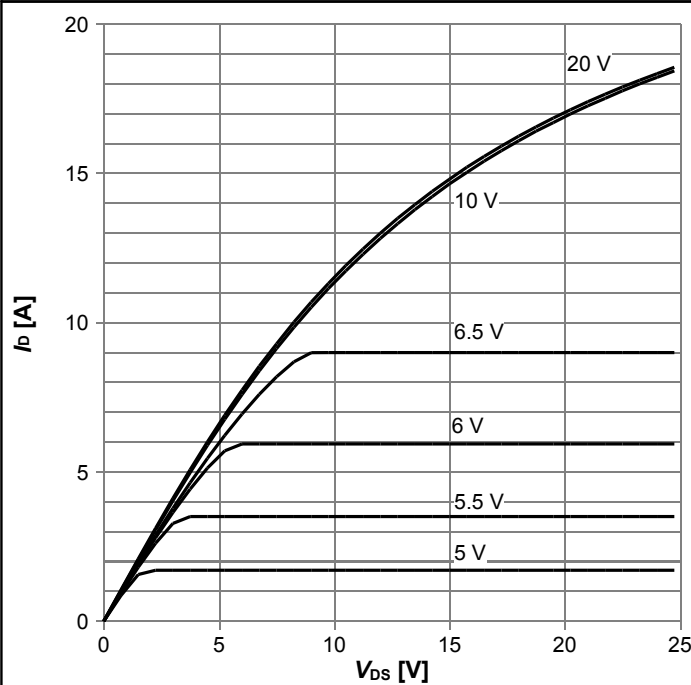
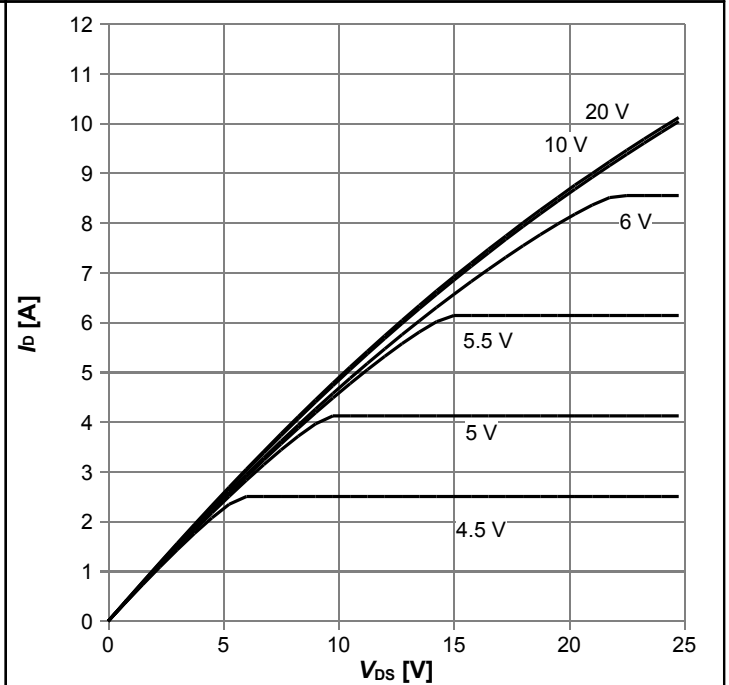


Diagram 5: Typ. output characteristics



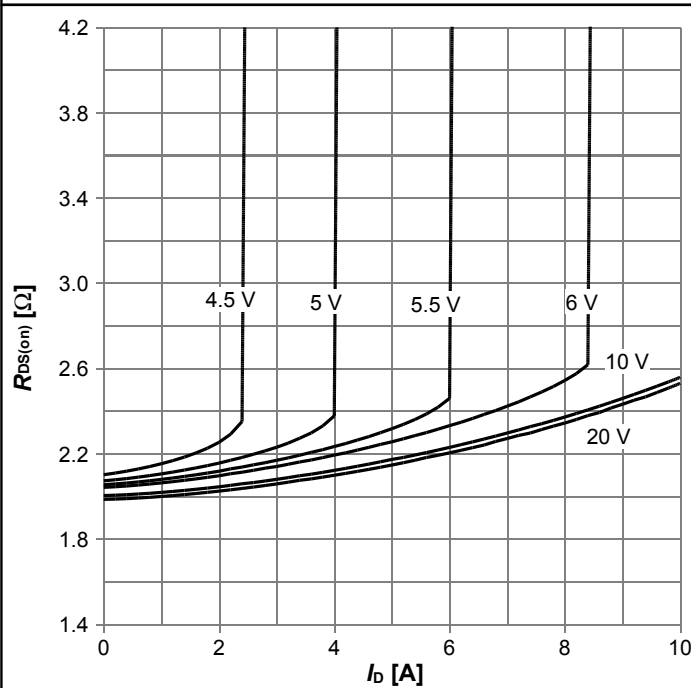
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}; t_p=10\text{ }\mu\text{s};$  parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



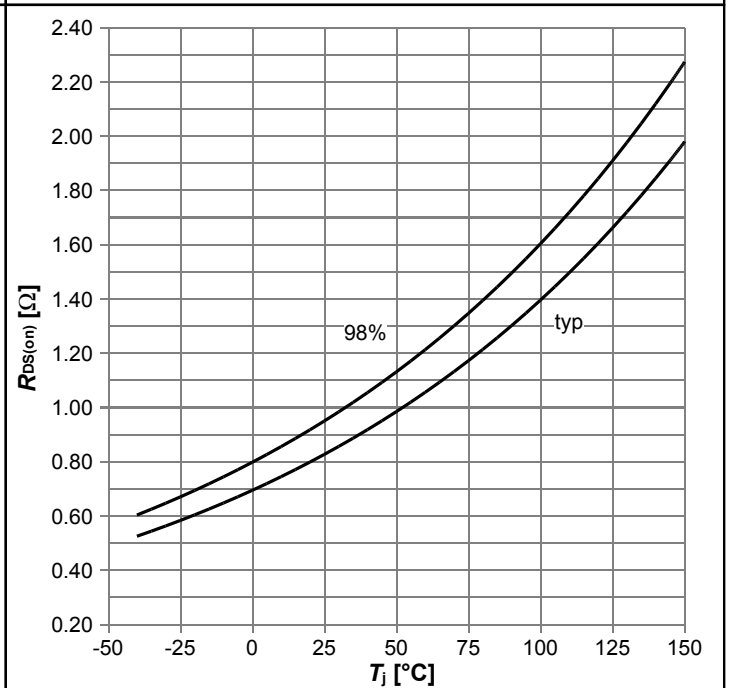
$I_D=f(V_{DS}); T_j=150\text{ }^\circ\text{C}; t_p=10\text{ }\mu\text{s};$  parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D); T_j=150\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



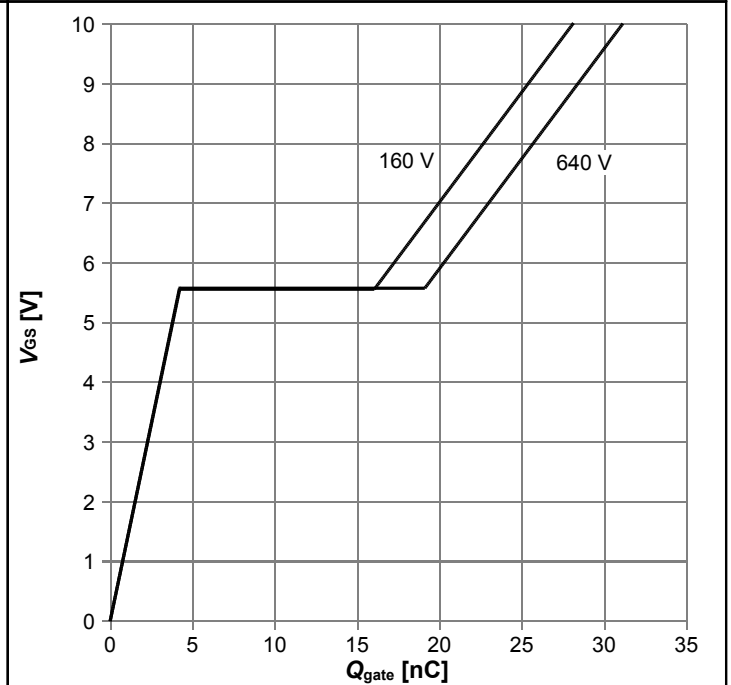
$R_{DS(on)}=f(T_j); I_D=3.6\text{ A}; V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



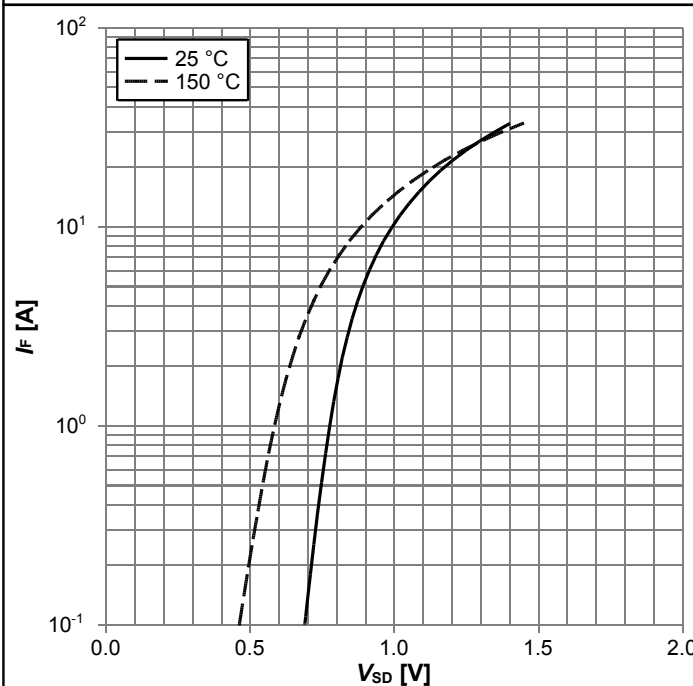
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



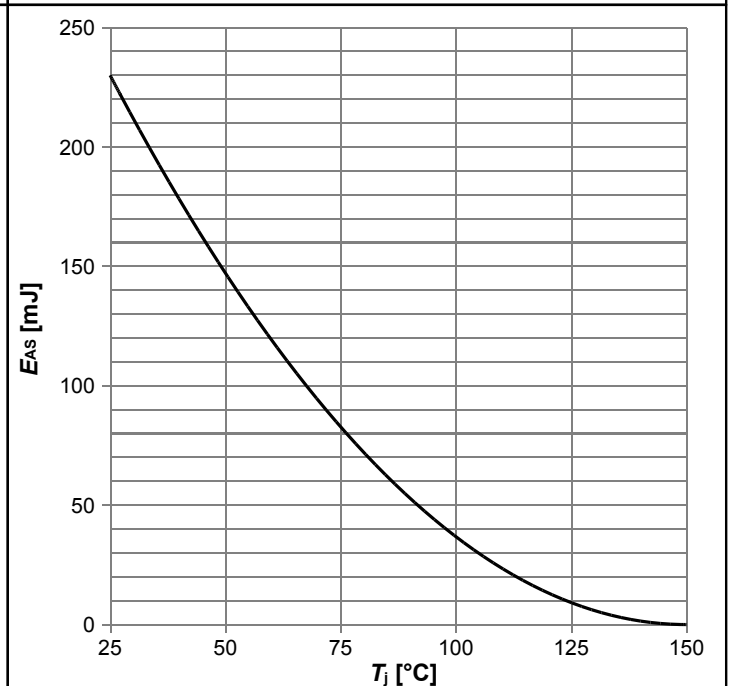
$V_{GS} = f(Q_{gate}); I_D = 5.7 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



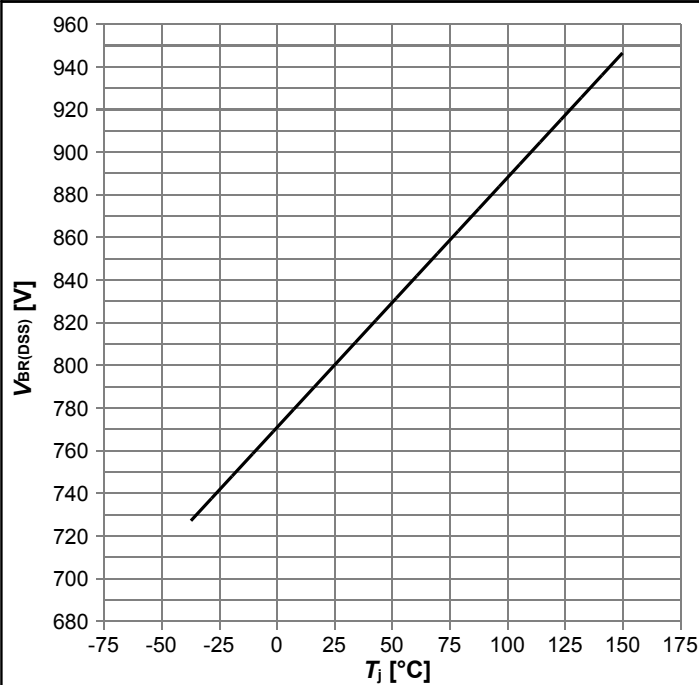
$I_F = f(V_{SD}); t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 12: Avalanche energy



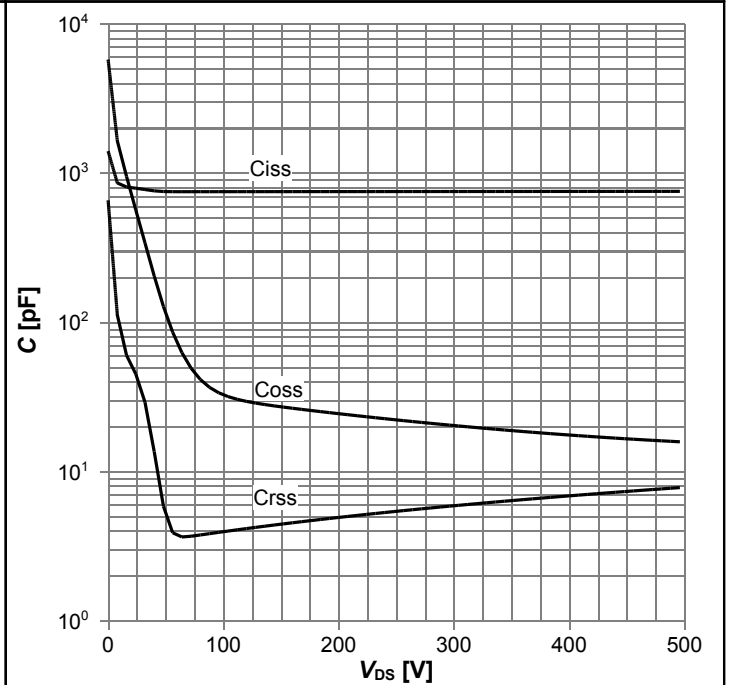
$E_{AS} = f(T_j); I_D = 1.6 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



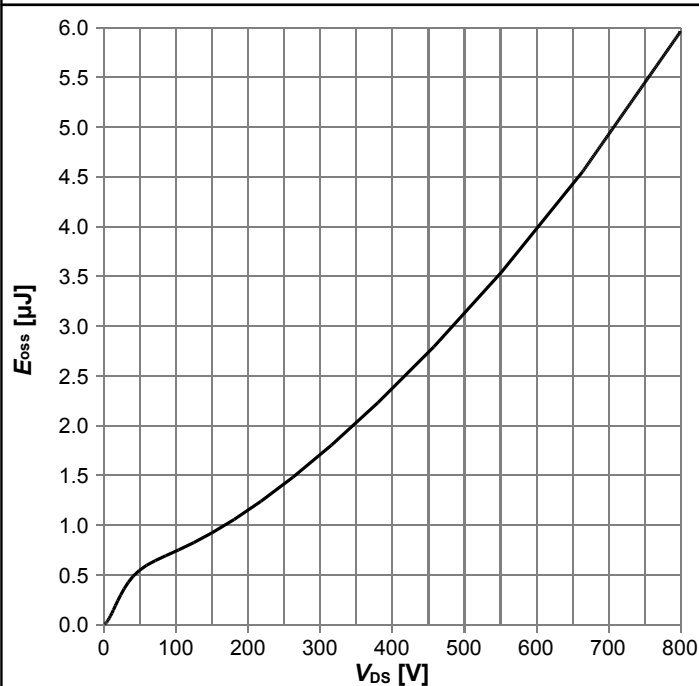
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 6 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p> <math>t_{rr} = t_F + t_S</math>  <math>Q_r = Q_F + Q_S</math> </p>

**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform



## 8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA80R1K0CE

Revision: 2015-06-23, Rev. 2.1

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version
2.1	2015-06-23	Continuous current Id update

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