



THE DATASHEET OF UC3524DTR



ADVANCED REGULATING PULSE WIDTH MODULATORS

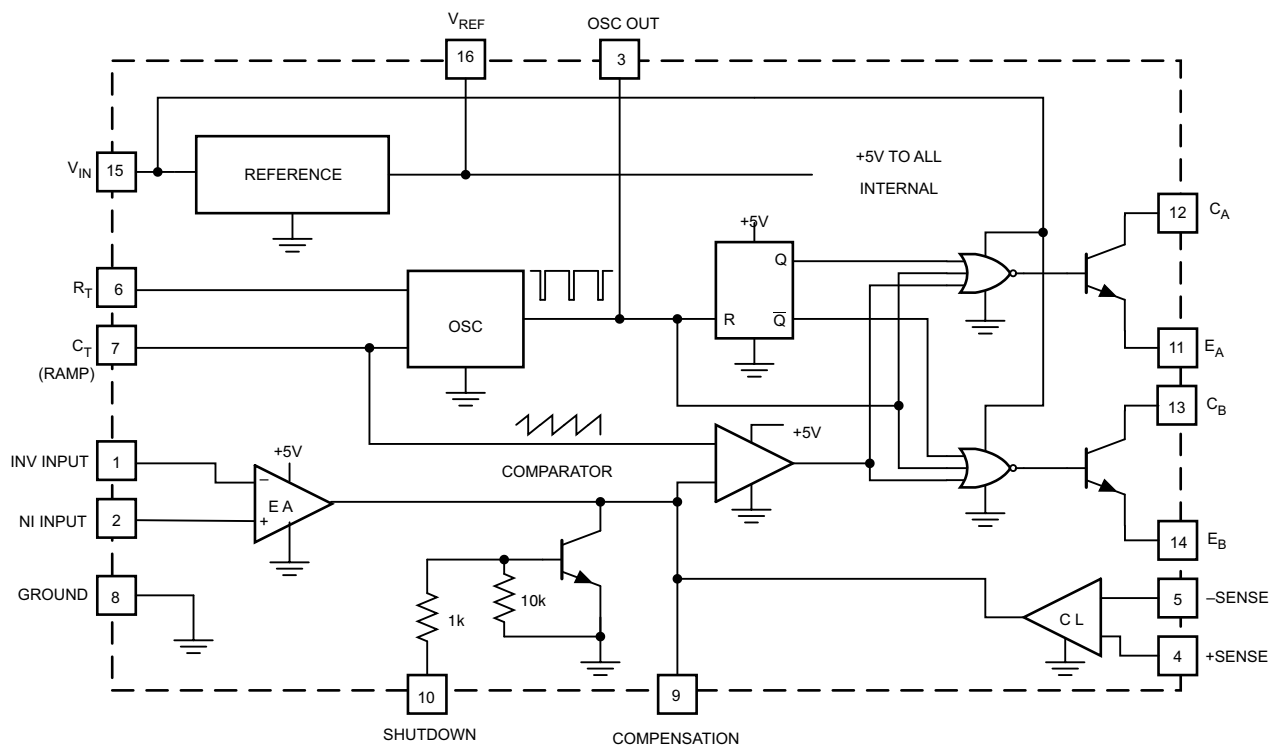
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current . . . 8 mA Typical
- Interchangeable With SG1524, SG2524 and SG3524, Respectively

DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to 125°C . The UC2524 and UC3524 are designed for operation from -25°C to 85°C and 0°C to 70°C , respectively.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

these specifications apply for $T_A = -55^\circ\text{C}$ to 125°C for the UC1524, -25°C to 85°C for the UC2524, and 0°C to 70°C for the UC3524, $V_{IN} = 20\text{ V}$, and $f = 20\text{ kHz}$, $T_A = T_J$, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8\text{ V to }40\text{ V}$		10	20		10	30	mV
Load regulation	$I_L = 0\text{ mA to }20\text{ mA}$		20	50		20	50	mV
Ripple rejection	$f = 120\text{ Hz}$, $T_J = 25^\circ\text{C}$		66			66		dB
Short circuit current limit	$V_{REF} = 0$, $T_J = 25^\circ\text{C}$		100			100		mA
Temperature stability	Over operating temperature range		0.3%	1%		0.3%	1%	
Long term stability	$T_J = 125^\circ\text{C}$, $t = 1000\text{ Hrs}$		20			20		mV
OSCILLATOR SECTION								
Maximum frequency	$C_T = 1\text{ nF}$, $R_T = 2\text{ k}\Omega$		300			300		kHz
Initial accuracy	R_T and C_T constant		5%			5%		
Voltage stability	$V_{IN} = 8\text{ V to }40\text{ V}$, $T_J = 25^\circ\text{C}$			1%			1%	
Temperature stability	Over operating temperature range			5%			5%	
Output amplitude	Pin 3, $T_J = 25^\circ\text{C}$		3.5			3.5		V
Output pulse width	$C_T = 0.01\text{ mfd}$, $T_J = 25^\circ\text{C}$		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	$V_{CM} = 2.5\text{ V}$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5\text{ V}$		2	10		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_J = 25^\circ\text{C}$	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	$T_J = 25^\circ\text{C}$		70			70		dB
Small signal bandwidth	$A_V = 0\text{ dB}$, $T_J = 25^\circ\text{C}$		3			3		MHz
Output voltage	$T_J = 25^\circ\text{C}$	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty-cycle	% Each output on	0%		45%	0%		45%	
Input threshold	Zero duty-cycle		1			1		V
	Maximum duty-cycle		3.5			3.5		
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2 V with error amplifier set for maximum out, $T_J = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/ $^\circ\text{C}$
Common mode voltage	$T_J = -55^\circ\text{C to }85^\circ\text{C}$ for the $-1\text{ V to }1\text{ V}$ limit	-1		1	-1		1	V
	$T_J = 25^\circ\text{C}$	-0.3		1				
OUTPUT SECTION (EACH OUTPUT)								
Collector-emitter voltage		40			40			V
Collector leakage current	$V_{CE} = 40\text{ V}$		0.1	50		0.1	50	μA
Saturation voltage	$I_C = 50\text{ mA}$		1	2		1	2	V
Emitter output voltage	$V_{IN} = 20\text{ V}$	17	18		17	18		V
Rise Time	$R_C = 2\text{ k}\Omega$, $T_J = 25^\circ\text{C}$		0.2			0.2		μs
Fall Time	$R_C = 2\text{ k}\Omega$, $T_J = 25^\circ\text{C}$		0.1			0.1		μs
Total standby current (Note)	$V_{IN} = 40\text{ V}$		8	10		8	10	mA

PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T), R_T establishes a constant charging current for C_T . This results in a linear voltage ramp at C_T , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5 V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering

flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

TYPICAL CHARACTERISTICS

**OPEN-LOOP VOLTAGE AMPLIFICATION
 OF ERROR AMPLIFIER
 VS
 FREQUENCY**

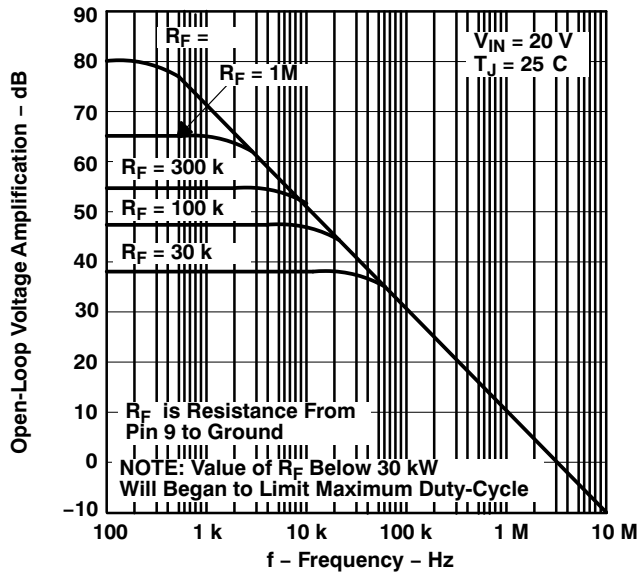


Figure 1.

**OSCILLATOR FREQUENCY
 VS
 TIMING COMPONENTS**

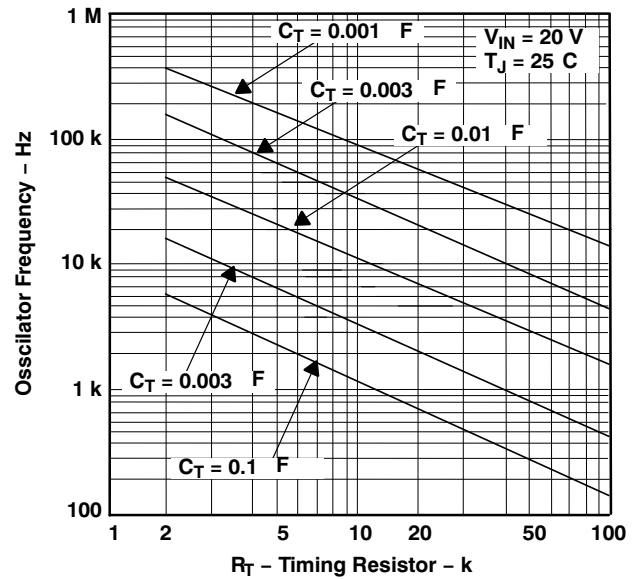


Figure 2.

**OUTPUT DEAD TIME
 VS
 TIMING CAPACITANCE VALUE**

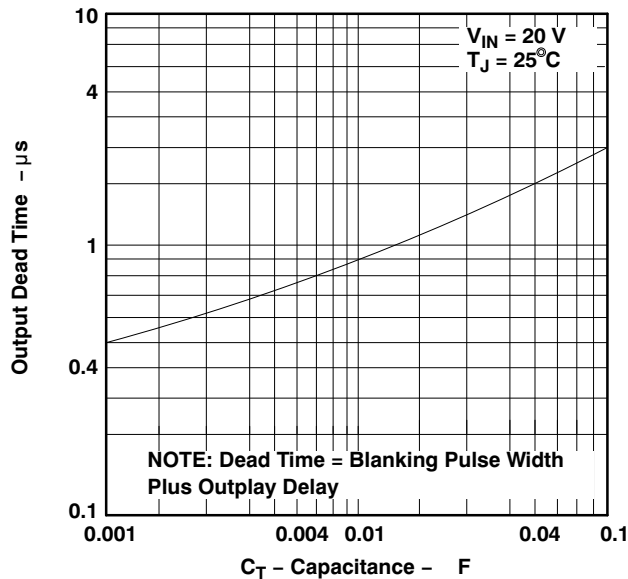


Figure 3.

**OUTPUT SATURATION VOLTAGE
 VS
 LOAD CURRENT**

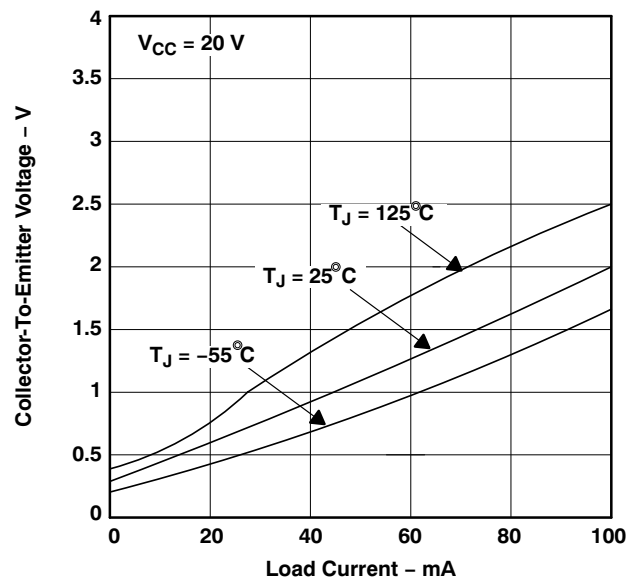


Figure 4.

APPLICATION INFORMATION

OSCILLATOR

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

$$f = \frac{1.18}{R_T C_T} \quad (1)$$

where

R_T is in $k\Omega$

C_T is in μF

f is in kHz

Practical values of C_T fall between 1 nF and 100 nF. Practical values of R_T fall between 1.8 $k\Omega$ and 100 $k\Omega$. This results in a frequency range typically from 120 Hz to 500 kHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T . If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 5.

SYNCHRONOUS OPERATIONS

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 $k\Omega$. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T terminal.

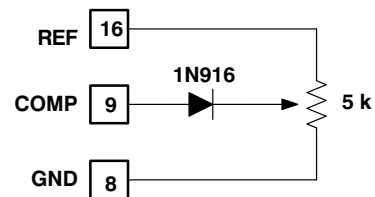


Figure 5. Error Amplifier Clamp

The other R_T terminals can be left open or shorted to V_{REF} . Minimum lead lengths should be used between the C_T terminals.

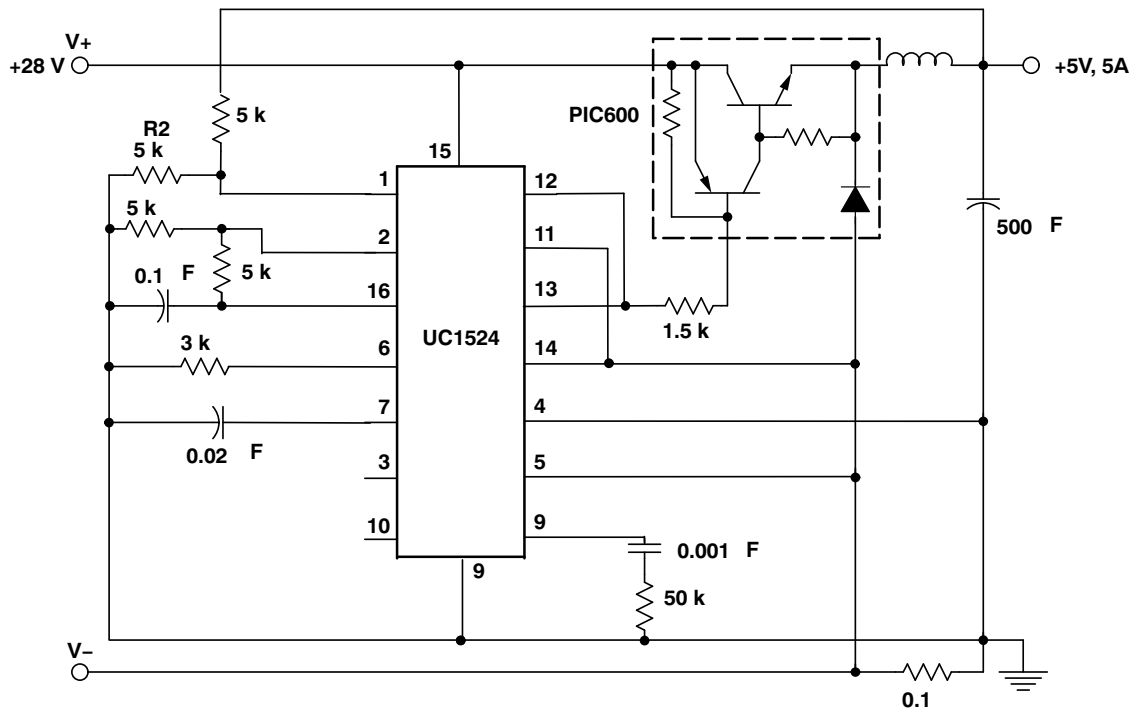


Figure 6. Single-Ended LC Switching Regulator Circuit

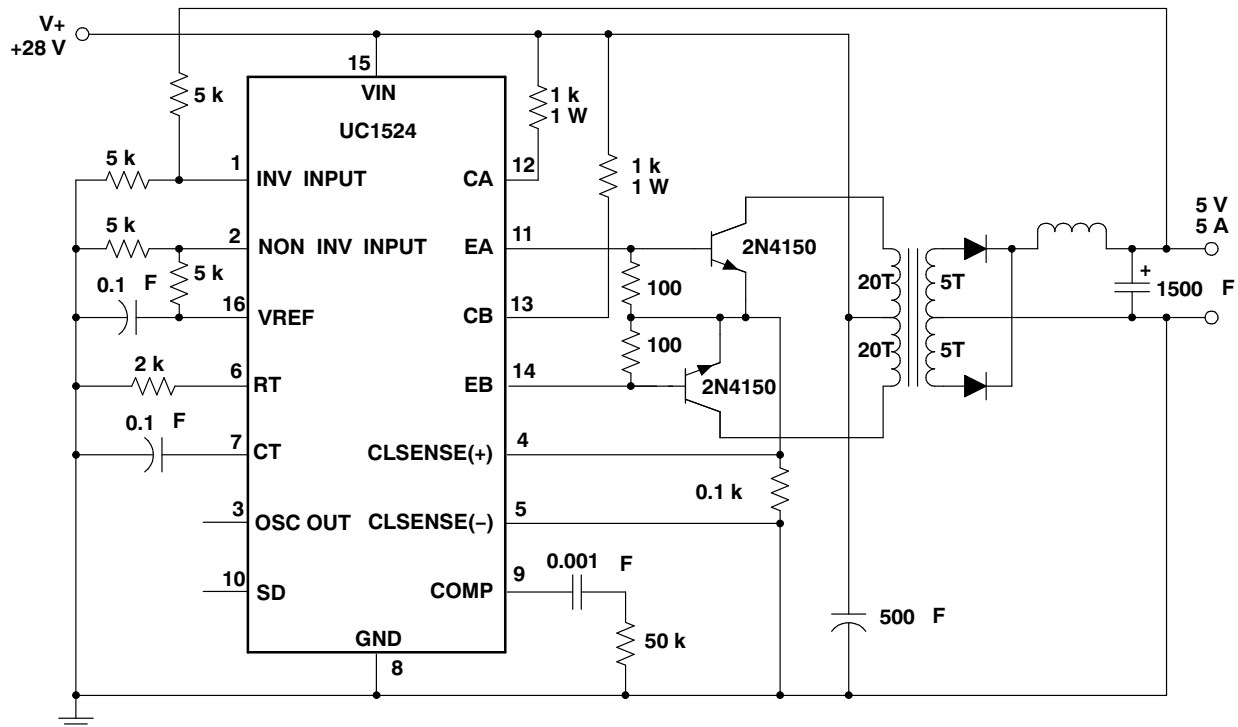


Figure 7. Push-Pull Transformer Coupled Circuit

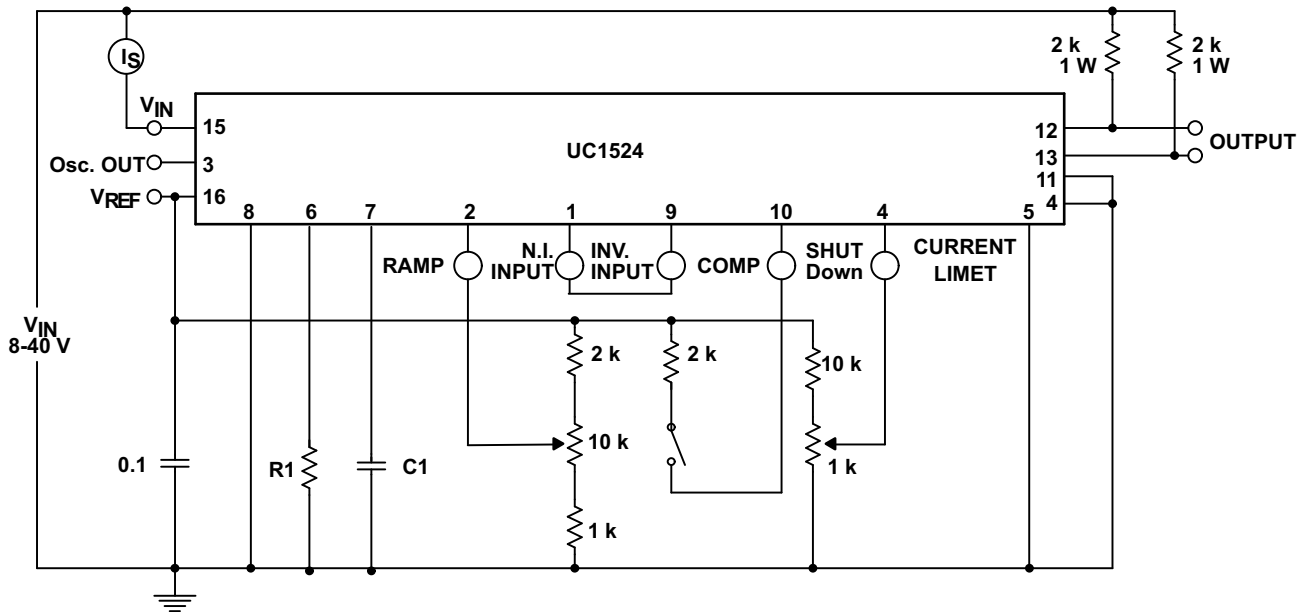


Figure 8. Open Loop Test Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC1524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1524J/80937	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1524J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2524DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2524N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2524NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3524D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UC3524DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UC3524DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UC3524DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UC3524DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC3524N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3524NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

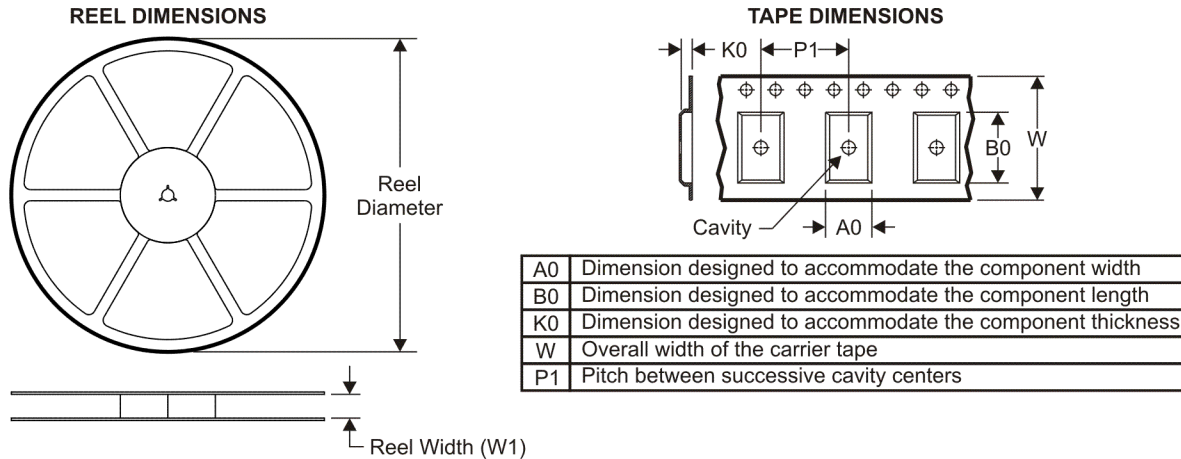
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2524DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3524DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UC3524DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2524DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3524DTR	SOIC	D	16	2500	346.0	346.0	33.0
UC3524DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

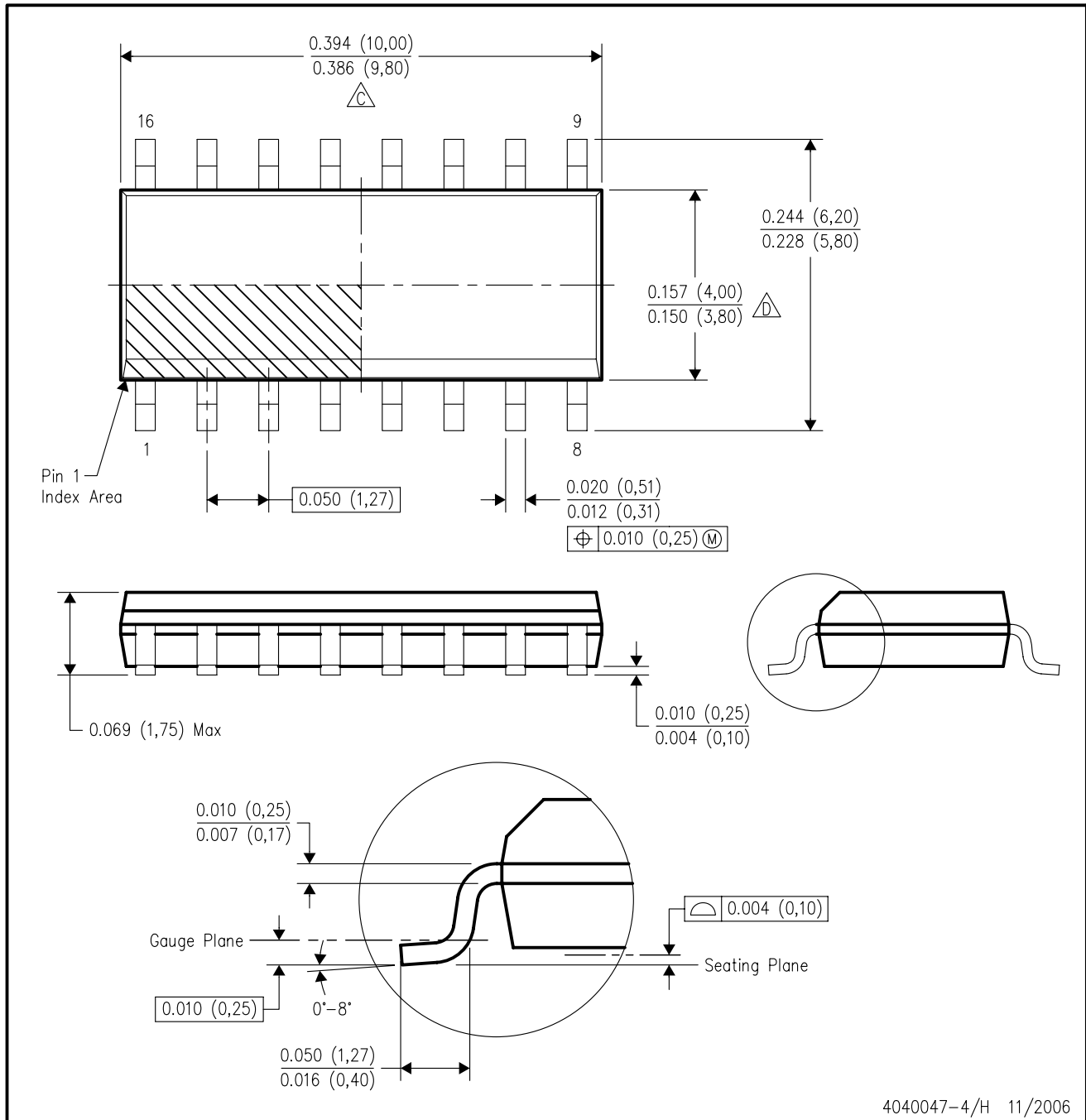


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

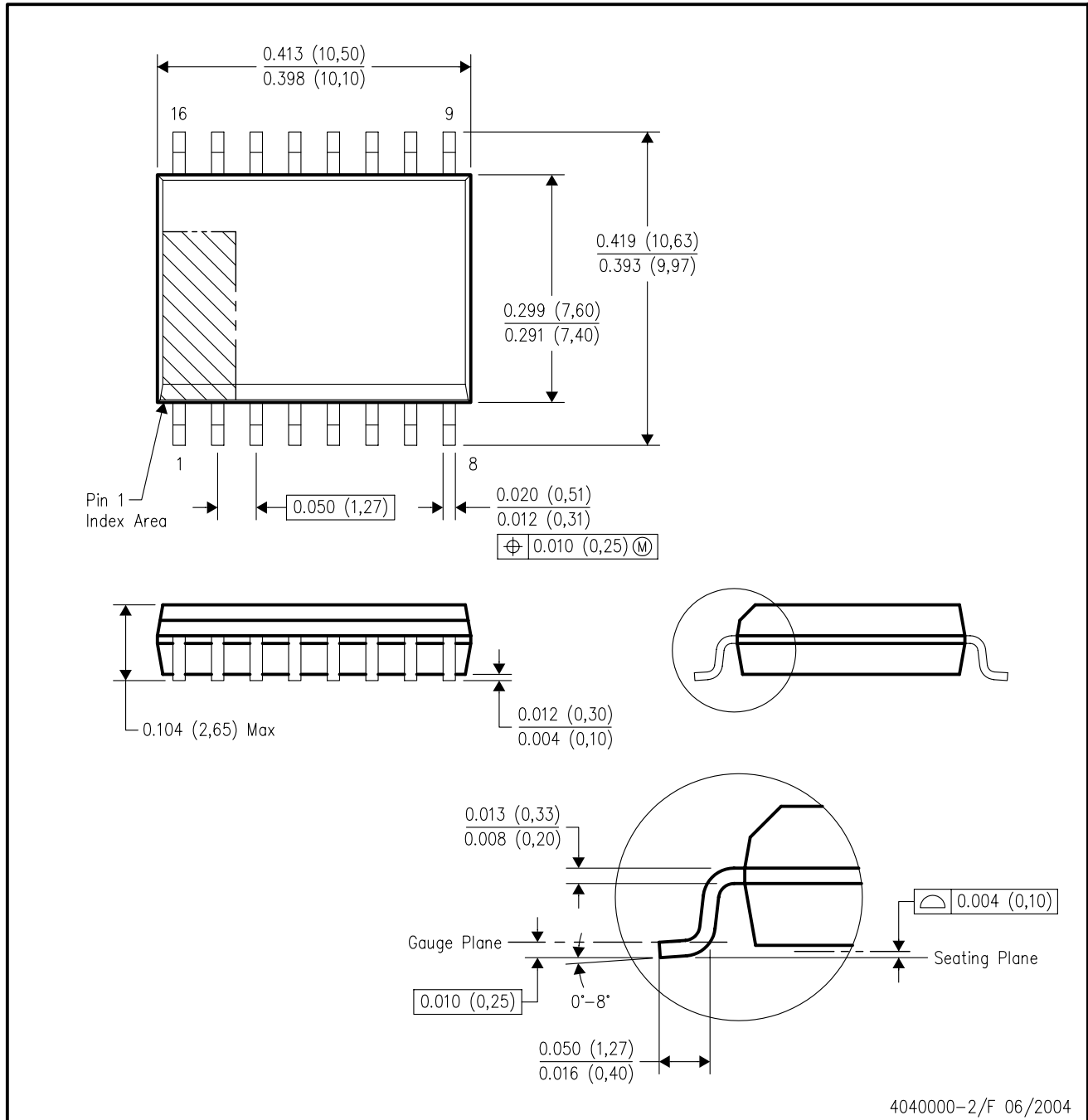


4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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-  Alternative Solution
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