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PCB Layout Recommendations for Leaded Packages

Technical Note

FPGA-TN-02160-1.4

November 2019

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1. Introduction

This document provides general PCB layout guidance for Lattice QFP (Quad Flat Package) and QFN (Quad Flat No Lead) products. Table 1.1 below lists the common nomenclature for different types of packages. As it is anticipated that users may have specific PCB design rules and requirements, the recommendations made herein should be considered as reference guidelines only. When designing a PCB for a QFN or QFP package, the following primary factors can affect the successful package mounting on the board:

- Perimeter Land Pad and Trace Design
- Stencil design
- Type of vias
- Board thickness
- Lead finish on the package
- Surface finish on the board
- Type of solder paste
- Reflow profile

Table 1.1. Leaded Package Types

Package Type	Description
QFN	**Quad Flat No Lead.** Plastic package with flat lead frame base coplanar along its bottom side.
DR-QFN	**Dual Row-Quad Flat No Lead.** QFN package that has two row staggered contacts.
QFP	**Quad Flat Package.** Plastic package with “gull wing” leads extending from four sides of the body.
PQFP	**Plastic Quad Flat Package.** QFP with body thickness from 2.0mm and above.
TQFP	**Thin Quad Flat Package.** QFP with thin body profile typical at 1.40mm and 1.0mm.

2. Perimeter Land Pad and Trace Design

In several published QFN tests, trace cracking was observed during board-level drop and bend tests. The reported trace cracking usually occurred at the edge of the solder mask opening around the metal pad. To avoid this failure mode, widen the trace under the solder mask edge so that it is wider than the remainder of the trace as shown in Figure 2.1. Depending on the reliability requirements, the wider part of the trace might need to be as wide as 50 to 75% of the metal pad width.

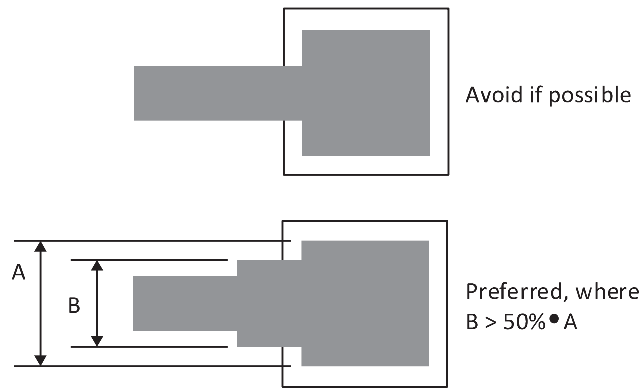

Figure 2.1. Wider Trace Under Solder Mask Edge to Avoid Trace

Non-solder mask defined (NSMD) pads are recommended for dual-row QFN packages, because the copper etching process has tighter control than the solder masking process and improves the reliability of the solder joints.

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3. Stencil Design for Perimeter Land Pads

For reliable solder joints on dual-row QFN packages, pay extra attention because of the small land surface area and the sole reliance on printed solder paste on the PCB surface. Special considerations are needed in stencil design and paste printing for both perimeter lands. Because the surface mount process varies from company to company, careful process development is recommended. The following section provides some guidelines for stencil design based on industry experience.

The optimum and reliable solder joints on the perimeter pads have about 50 to 70 ?m (2 to 3 mils) standoff height. Tightly control the stencil aperture tolerance because these tolerances can effectively reduce the aperture size. Area ratios of 0.66 and aspect ratios of 1.5 were never exceeded. The land pattern on the PCB should be 1:1 to the land pads on QFN package.

Stencil thickness of 0.125 mm is recommended for 0.5 mm dual-row QFN packages. A laser-cut stainless steel stencil with electro-polished trapezoidal walls is recommended to improve the paste release. Lattice recommends that no-clean, Type 3 or Type 4 paste be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

4. Reflow Profile

Reflow profile and peak temperature have a strong influence on void formation. Lattice strongly recommends that users follow the profile recommendation of the paste suppliers, since this is specific to the requirements of the flux formation. However, the following profile, as shown in Figure 4.1., serves as a general reference for Lattice QFN devices.

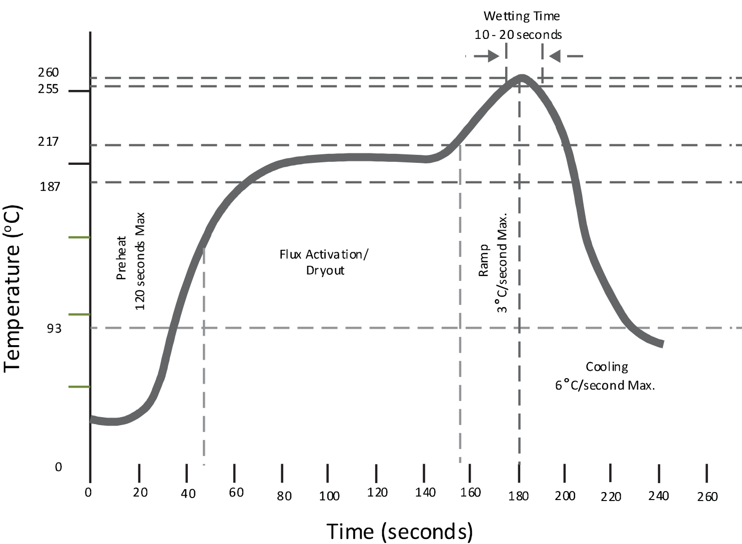

Figure 4.1. Typical Pb-Free Solder Flow

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5. QFP and QFN Board Layout Recommendations

Lattice Semiconductor provides pre-designed layout examples for the various package options as listed in Table 5.1. Some package layout examples provide different options depending on design and cost goals. For instance, layout example includes all the programmable I/O pins but requires more total layers. An alternate layout uses fewer layers but provides few user I/O pins.

Table 5.1. Package Layout Example Summary

Package Code	Pitch (mm)	iCE40 Family Offerings	Max. I/O	SMD/ NSMD	Total Layers	Signal Layers	Pad Size (mm)	Solder Mask (mm)	Via Drill (mil)	Via Size (mil)	Trace Width (mil)	Trace Space (mil)
QN84	0.50	LP	67	NSMD	1	1	0.4 x 0.22	0.502 x 0.322	N/A	N/A	4	3.5
VQ100	0.50	HX	72	NSMD	4	1	0.30	0.452	5	10	5	5
TQ144	0.50	HX	107	NSMD	4	1	0.30 x 1.6	0.452 x 1.75	24	12	8	8

All the examples assume that each I/O bank and the SPI bank each uses a different I/O voltage. In the layout examples for a reduced number of layers, all the mandatory pins connections are routed out, including connections such as the VPP_2V5 and the SPI connections. The PLL pins are also routed out on the packages that support PLLs.

Free Allegro Viewer

If you do not already have a PCB board design software package but would like to view the files, simply download and install the free Allegro viewer software available from Cadence.

Free Cadence Allegro Physical Viewer Downloads

www.cadence.com/products/pcb/Pages/downloads.aspx

6. QN84 Quad-Flat No Lead Package

Leadless Quad Flat Pack (QFN) packages are plastic-encapsulated with a copper lead frame substrate, providing a robust, low-cost solution for small form factor applications such as mobile handsets and other battery operated consumer products. Dual-row QFN packages have interstitial, staggered contacts. The inner row is offset 0.5 mm, resulting in a compact design that does not exceed the surface mount technology (SMT) capability of a typical 0.5 mm pitch surface-mount process.

For applications that require 67 PIO pins or less and a few board layers, the QN84 package uses somewhat aggressive layout rules, as shown in Table 6.2. The single layer is shown in Figure 6.1.

The underside metal die paddle thermal pad is at Ground potential. It is designed to remove heat from the package and enhance electrical performance. Although the low-power iCE40 mobile FPGA family generates little heat, the extra ground connection enhances overall signal integrity.

Instead of one solid solder pad for the die paddle, multiple smaller openings in the solder paste stencil are used, as shown in Table 6.1. This technique helps reduce voids, splattering, and solder balling).

Table 6.1. Solder Stencil Patterns for Thermal Pad

Stencil Pattern		
Dimensions	mm diameter circles at mm pitch	1.35 x 1.35 mm squares at 1.65 mm pitch
Solder Paste Coverage	37%	68%

For additional information on the QN84 package, see the application note Dual-Row QFN Package Assembly and PCB Layout Guidelines (AN016).

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Table 6.2. QN84, Single-Layer Layout Dimensions

Specification	Dimension	
Layers	1	
Pad Size	0.4 x 0.22 mm	15.748 x 8.6614 mils
Pad Solder Mask	0.502 x 0.322 mm	19.7638 x 8.6614 mils
Via Size (Drill)	None required	None required
Via Size (Pad)	None required	None required
Trace Width	0.1016 mm	4 mils
Trace Spacing	0.889 mm	3.5 mils

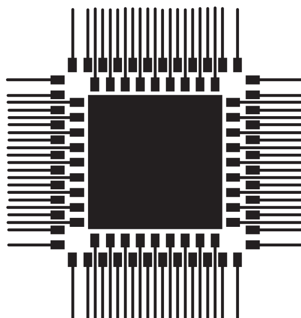

Figure 6.1. QN84 Layout

For multilayer routing, Figure 6.2. shows the suggested board layout for the QN84 package on a top layer of a printed circuit board, assuming NSMD solder mask rules. The labeled dimensions are listed in Table 6.3. Figure 6.3. shows the suggested layout if pads are connected on inner layers.

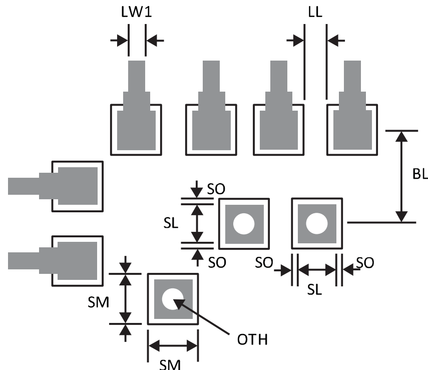

Figure 6.2. Top-Layer Layout

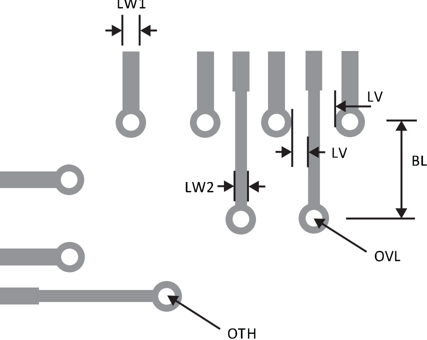

Figure 6.3. Inner-layer Layout

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Table 6.3. QN84, Multi-Layer Layout Dimensions

Specification	Symbol	Dimension
Component Land Pad Diameter	SMD	0.300 mm
Solder Land Diameter	SL	0.300 mm
Solder Mask Opening Diameter	SM	0.425 mm
Solder Land to Solder Land	LL	0.075 mm
Solder Mask Overlap	SO	0.0625 mm
Package Pin Pitch		0.500 mm
Solder Land Pitch	BL	0.650 mm
Line Width between Via Outside and Via Land	LW1	0.127 mm
Line Width between Via and Via Land	LW2	0.100 mm
Line to Via Land	LV	0.050 – 0.100 mm
Via Land Diameter	OVL	0.250 – 0.400 mm
Via Opening Diameter	OTH	0.100 – 0.250 mm

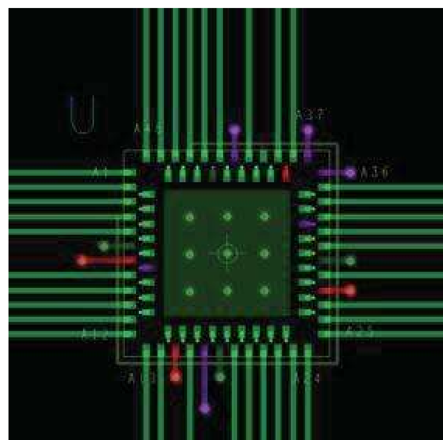

Figure 6.4. Top Layer

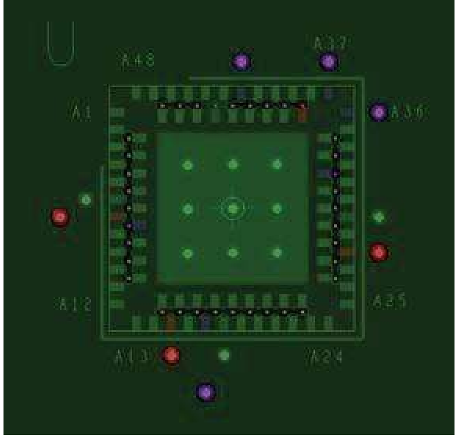

Figure 6.5. Ground Layer

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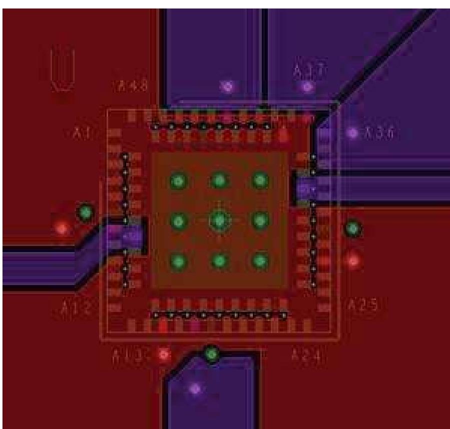

Figure 6.6. Power Layer

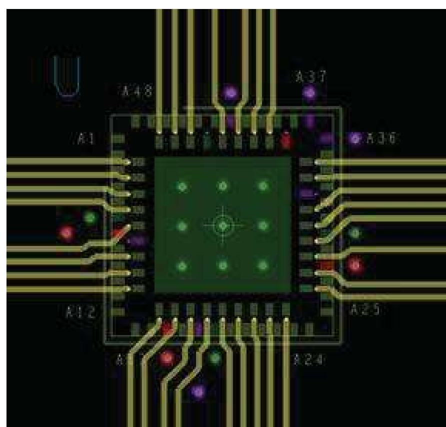

Figure 6.7. Bottom Layer

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7. VQ100 Quad-Flat Package

For applications that require 72 PIO pins or less and where board space is not the primary concern, the VQ100 package is the best option. The VQ100 package has the easiest layout and uses very common, low-cost PCB dimensions, as shown in Table 7.1. All the pins connect on the top layer, shown in Figure 7.1. The power layer, shown in Figure 7.3, supports four different I/O bank voltages plus the core VCC voltage. The SPI_VCC and VPP_2V5 power rails are connected on the top layer.

Table 7.1. VQ100, Four-Layer Layout Dimensions

Specification	Dimension	
Layers	4	
Pad Size	0.30 mm	11.8110 mils
Pad Solder Mask	0.452 mm	17.7953 mils
Via Size (Drill)	0.127 mm	5 mils
Via Size (Pad)	0.254 mm	10 mils
Trace Width	0.127 mm	5 mils
Trace Spacing	0.127 mm	5 mils

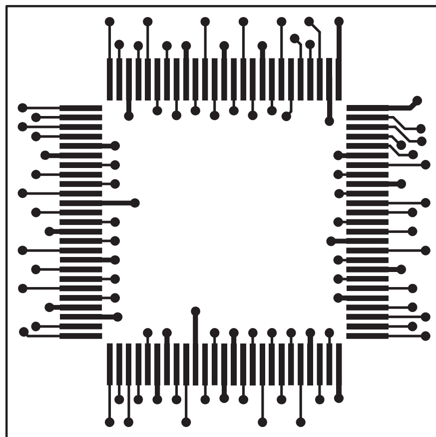

Figure 7.1. Top Layer

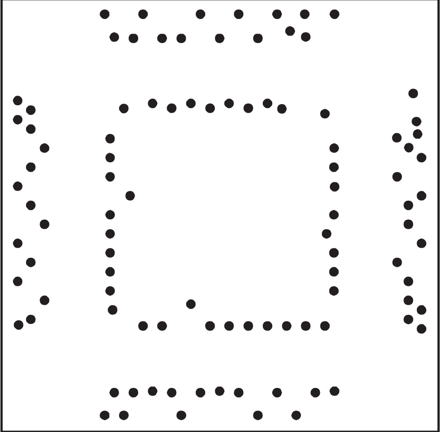

Figure 7.2. Inner Layer

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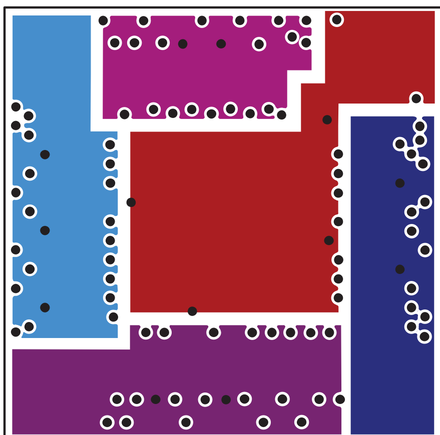

Figure 7.3. Power Layer

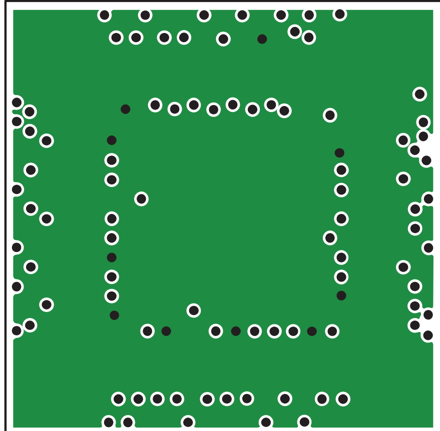

Figure 7.4. Ground Layer

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8. TQ144 Quad-Flat Package

For applications that require 104 PIO pins or less and where board space is not the primary concern, the VQ100 package is the best option. The TQ144 package has the easiest layout and uses very common, low-cost PCB dimensions, as shown in Table 8.1. All the pins connect on the top layer, shown in Figure 8.1. The power layer, shown in Figure 8.3, supports four different I/O bank voltages plus the core VCC voltage. The SPI_VCC and VPP_2V5 power rails are connected on the top layer.

Table 8.1. VQ100, Four-Layer Layout Dimensions

Specification	Dimension	
Layers	4	
Pad Size	0.30 x 1.6 mm	11.8110 x 63.00 mils
Pad Solder Mask	0.45 x 1.75 mm	17.7165 x 68.90 mils
Via Size (Drill)	0.3048 mm	12 mils
Via Size (Pad)	0.6096 mm	24 mils
Trace Width	0.2032 mm	8 mils
Trace Spacing	0.2032 mm	8 mils

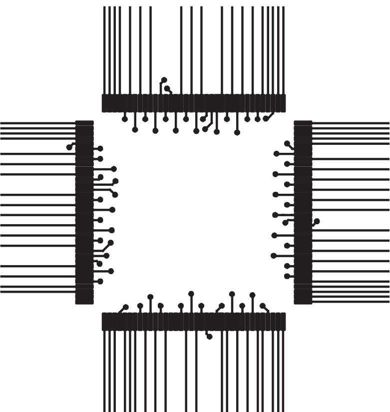

Figure 8.1. Top Layer

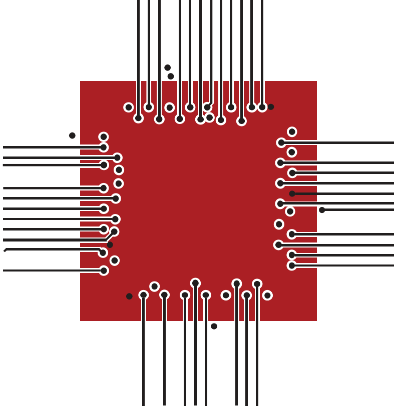

Figure 8.2. Bottom Layer

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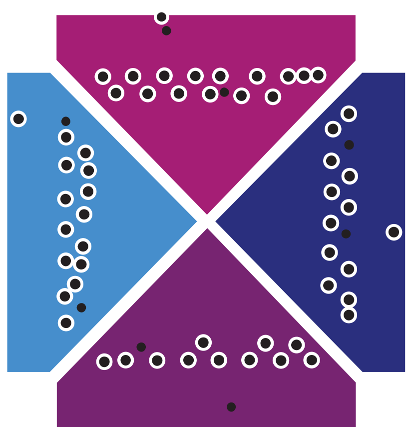

Figure 8.3. Power Layer

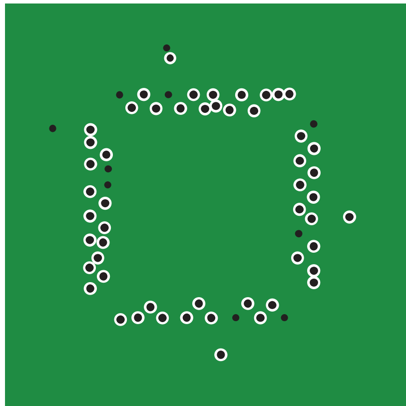

Figure 8.4. Ground Layer

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9. PCB Solder Land Patterns

(Dimensions in Millimeters)

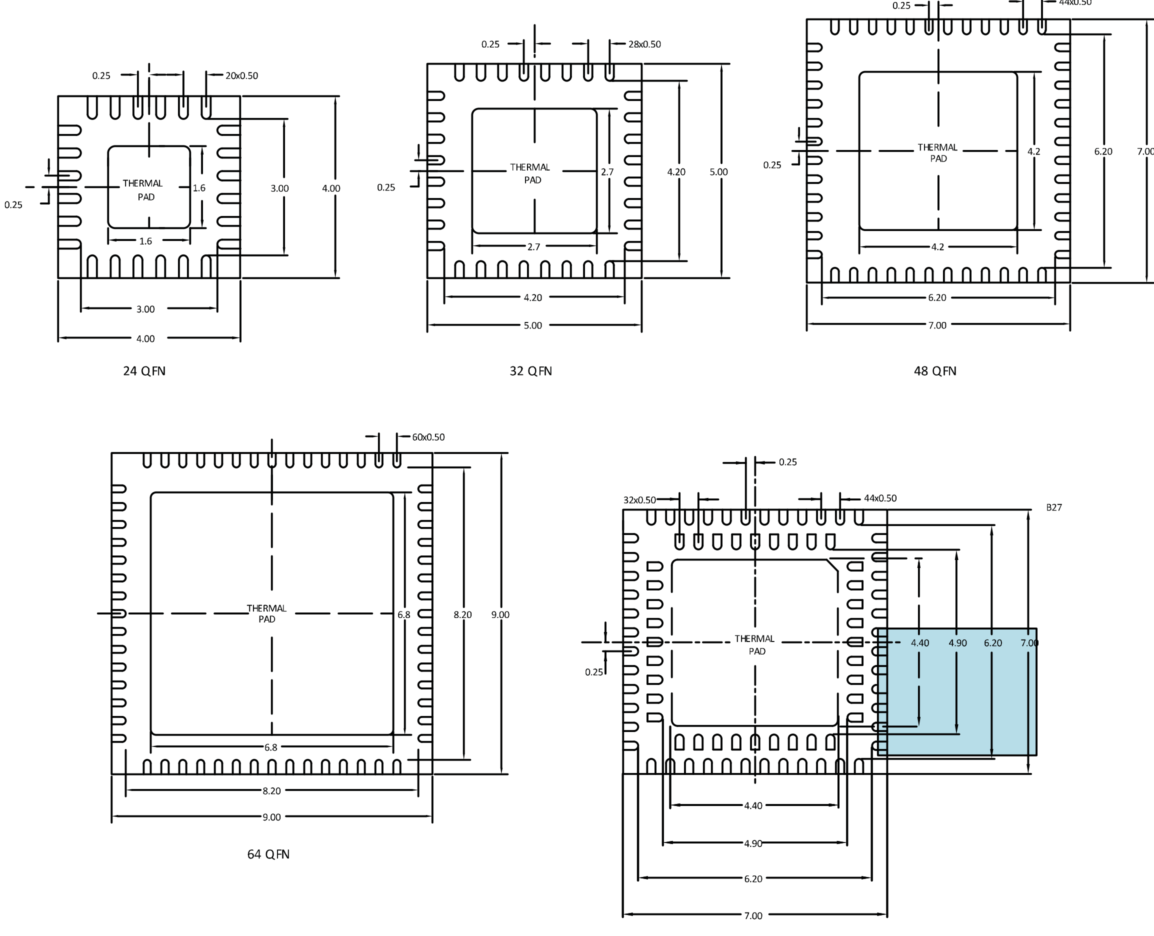

Figure 9.1. QFN Footprints

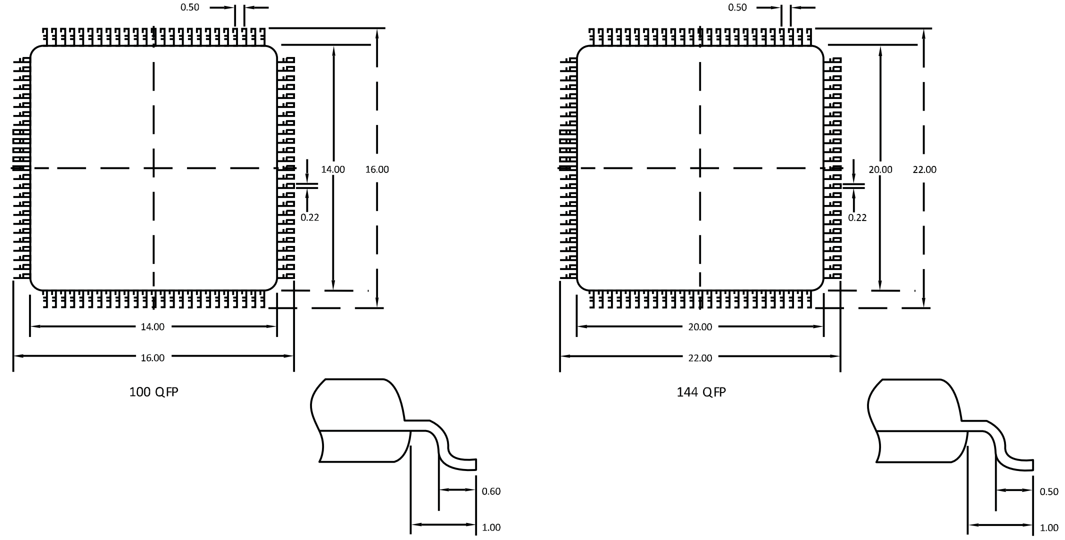

Figure 9.2. QFP Footprints

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10. Thermal Pad

For maximum package thermal dissipation, it is recommended that the QFN Thermal Pad be soldered directly to the user PCB. In order to reduce solder bridging, the stencil pattern for the Thermal Pad should utilize a 'checkerboard' (cross-hatch) pattern which dispenses solder over 75% of the Thermal Pad area as shown in Figure 10.1.

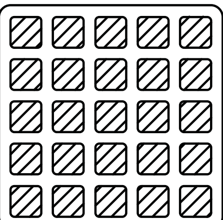

Figure 10.1. Thermal Pad

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11. Lead Finger Details

0.07 Solder Mask Opening
All Around
0.25
R 0.15
0.50

LEAD FINGER DETAIL: 24 QFN

0.07 Solder Mask Opening
All Around
0.24
R 0.15
0.40

LEAD FINGER DETAIL: 32, 48, 64 QFN

0.07 Solder Mask Opening
All Around
0.22
R 0.11
0.40

LEAD FINGER DETAIL: 84 QFN

Figure 11.1. Lead Finger Details

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12. Advantages and Disadvantages of QFP and QFN Packaging

One of the key benefits of QFPs is the exposed lead extending out from the package ends. This enables capability to inspect the solder joints physically, even without the use of x-ray machines. The electrical connections from internal wirebonds are connected to the leads without routing loops. This offers good electrical characteristics of the package. Also, PCB signal routes will not be complex compared with BGAs. Consequently, the package is known for only having peripheral leads which limits the I/O count. In terms of dimensions the gull-wing leads are prone to deformation; also the lead pitch is small so as the gap in between requiring tighter tolerances in assembly to prevent solder bridging.

QFN package offers direct connection from its internal wirebond pads onto the PCB surface without any looping traces which offers reduced lead inductance and good electrical performance. The exposed pad or paddle feature gives better thermal path and reliability compared with other packaging technology. These features make the QFN the best choice for small footprint applications. On the other hand, due to its wide exposed pad area and light weight body however makes it easy to buoy up itself on the molten solder during solder reflow. This makes the unit to drift off and affect the contact alignment to the PCB pads.

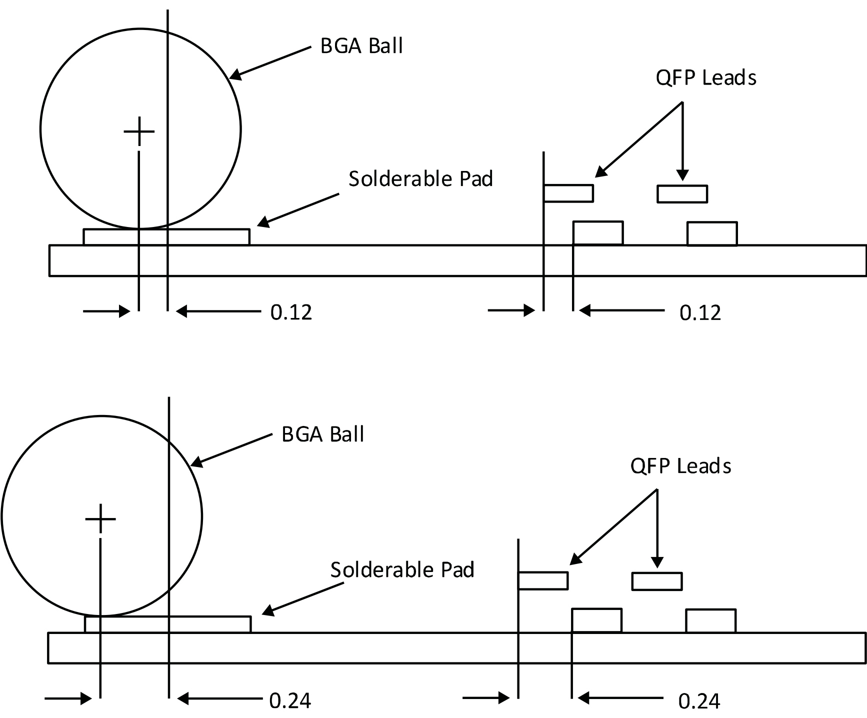

Figure 12.1. Misalignment of BGA Balls vs. QFP Leads

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Reference

- IPC-7351A Generic Requirements for Surface Mount Design and Land Pattern Standard

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Use at Your Own Risk

Successful printed circuit manufacturing requires frequent communication with the printed circuit assembly house during design and layout. The examples shown here may or may not produce a successful or manufacturable design at your assembly house. Please review your iCE40 layout with your printed circuit assembly house before committing to a production run.

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Revision History

Revision 1.4, November 2019

Section	Change Summary
All	• Changed document number from TN1257 to FPGA-TN-02160. • Updated document template.
Disclaimers	Added this section.

Revision 1.3, October 2013

Section	Change Summary
All	• Changed document title from "PCB Layout Recommendations for QFN Packages" to "PCB Layout Recommendations for Leaded Packages". • Included QN84 package details. • Rearranged the order of sections. • Added information to Introduction section.
Perimeter Land Pad and Trace Design, Stencil Design for Perimeter Land Pads	Added these sections.
Reflow Profile	
Advantages and Disadvantages of QFP and QFN Packaging	
References	
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 1.2, February 2013

Section	Change Summary
QFP and QFN Board Layout Recommendations	Included iCE40 VQ100 and TQ144 packages.

Revision 1.1, July 2012

Section	Change Summary
All	Included 84 QFN package.

Revision 1.0, July 2012

Section	Change Summary
All	Initial release.

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