



**THE DATASHEET OF  
PBSS4160PANP,115**





# PBSS4160PANP

60 V, 1 A NPN/PNP low  $V_{CEsat}$  (BISS) transistor

20 December 2017

Product data sheet

## 1. General description

NPN/PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PBSS4160PAN. PNP/PNP complement: PBSS5160PAP.

## 2. Features and benefits

- Very low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain  $h_{FE}$  at high  $I_C$
- Reduced Printed-Circuit Board (PCB) requirements
- High efficiency due to less heat generation
- AEC-Q101 qualified

## 3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

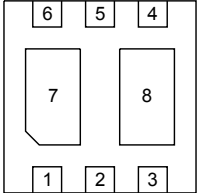
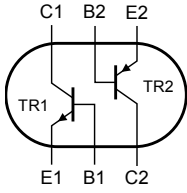
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	60	V
$I_C$	collector current		-	-	1	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1.5	A
<b>TR1 (NPN)</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 0.5$ A; $I_B = 50$ mA; $t_p \leq 300$ $\mu$ s; pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	-	-	240	m $\Omega$
<b>TR2 (PNP)</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -0.5$ A; $I_B = -50$ mA; $t_p \leq 300$ $\mu$ s; pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	-	-	360	m $\Omega$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view <b>DFN2020-6 (SOT1118)</b></p>	 <p><i>sym139</i></p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4160PANP	DFN2020-6	DFN2020-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4160PANP	2M

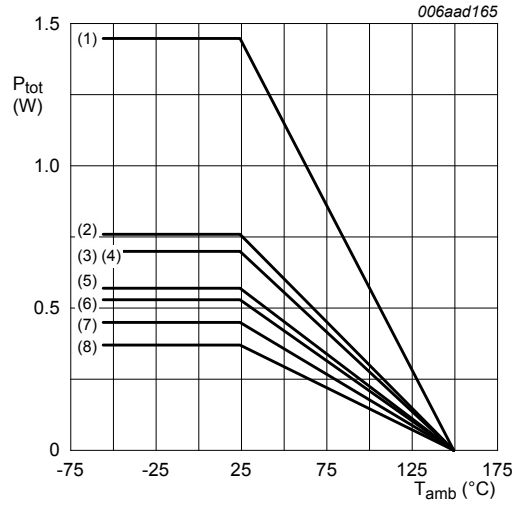
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	60	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	60	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	7	V
I <sub>C</sub>	collector current			-	1	A
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms		-	1.5	A
I <sub>B</sub>	base current			-	0.3	A
I <sub>BM</sub>	peak base current	single pulse; t <sub>p</sub> ≤ 1 ms		-	1	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided 35 μm copper strip line, tin-plated and standard footprint.  
 [2] Device mounted on an FR4 PCB, single-sided 35 μm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.  
 [3] Device mounted on 4-layer PCB 35 μm copper strip line, tin-plated and standard footprint.  
 [4] Device mounted on 4-layer PCB 35 μm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.  
 [5] Device mounted on an FR4 PCB, single-sided 70 μm copper strip line, tin-plated and standard footprint.  
 [6] Device mounted on an FR4 PCB, single-sided 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.  
 [7] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated and standard footprint.  
 [8] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

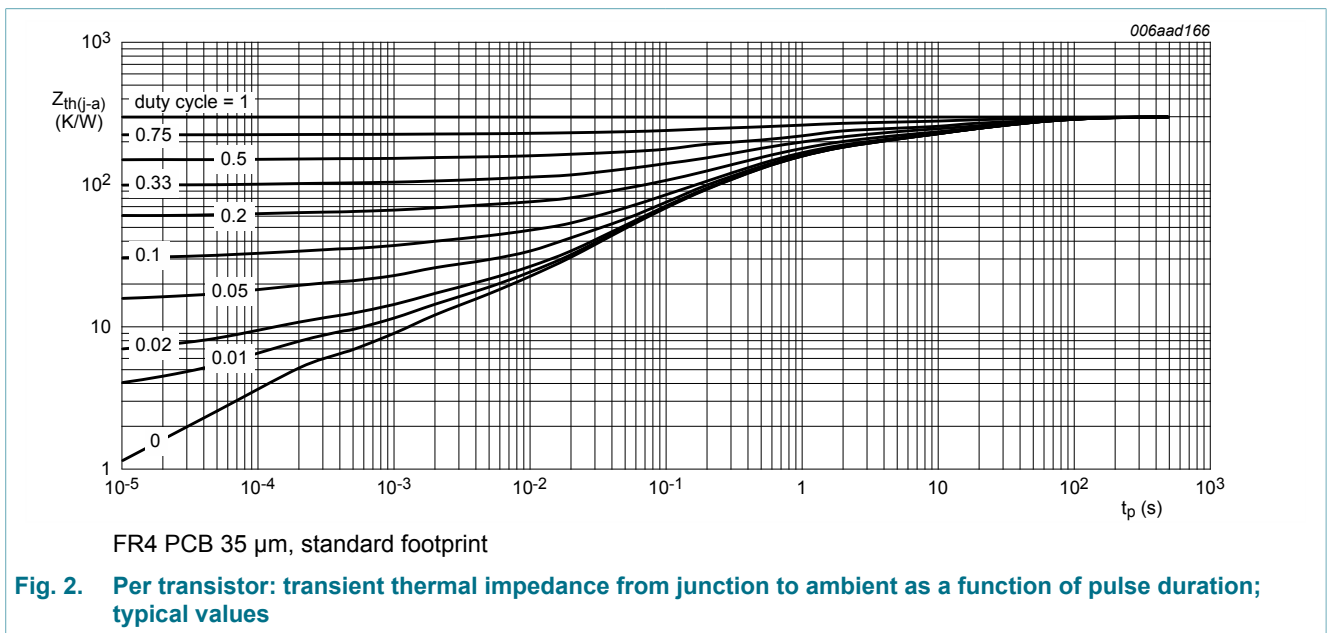
## 9. Thermal characteristics

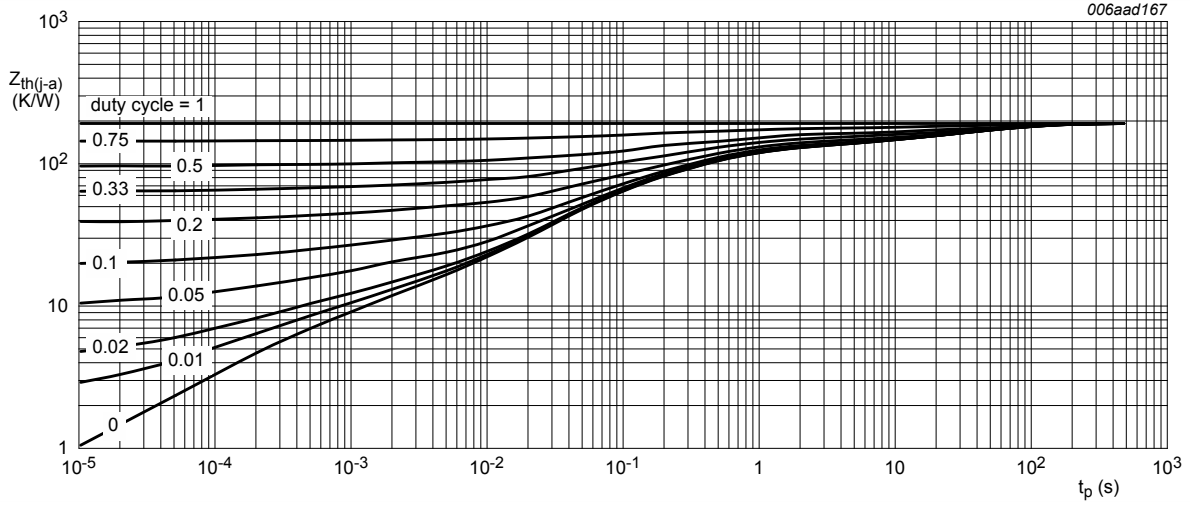
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	30	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

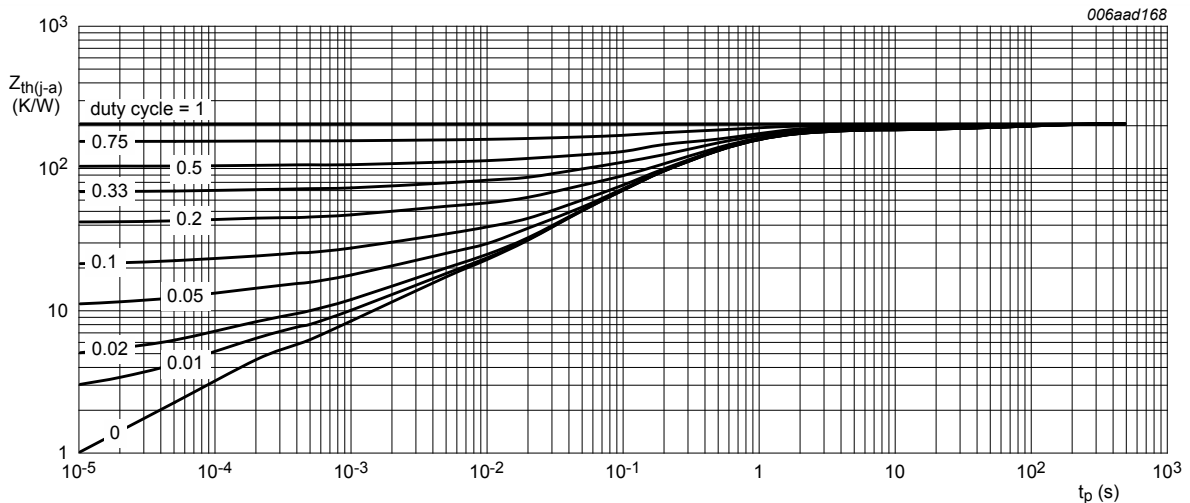
- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.





FR4 PCB 35  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$

**Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



4-layer PCB 35  $\mu\text{m}$ , standard footprint

**Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

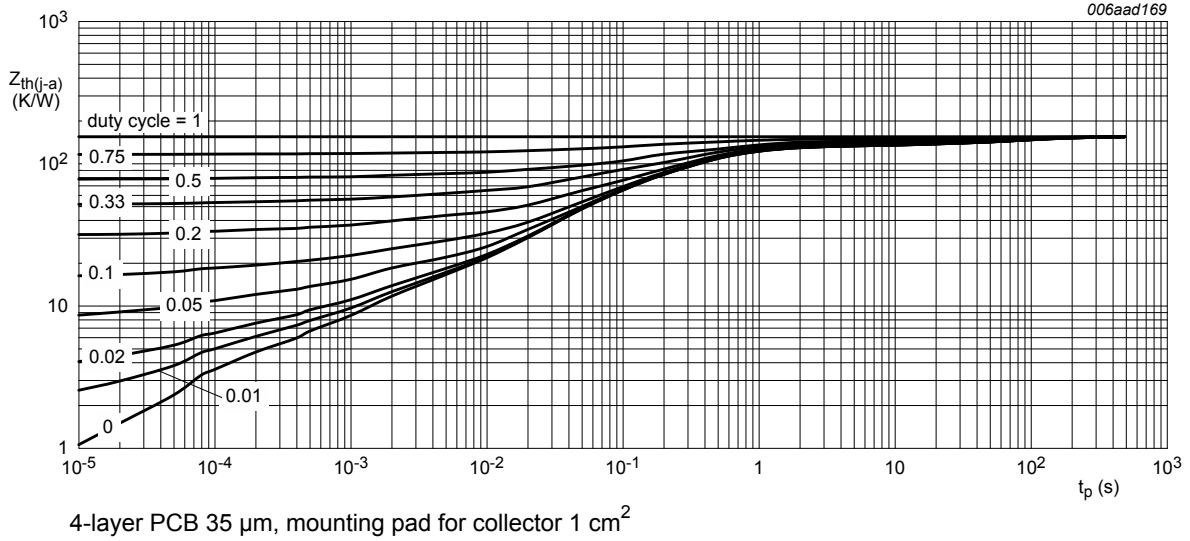


Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

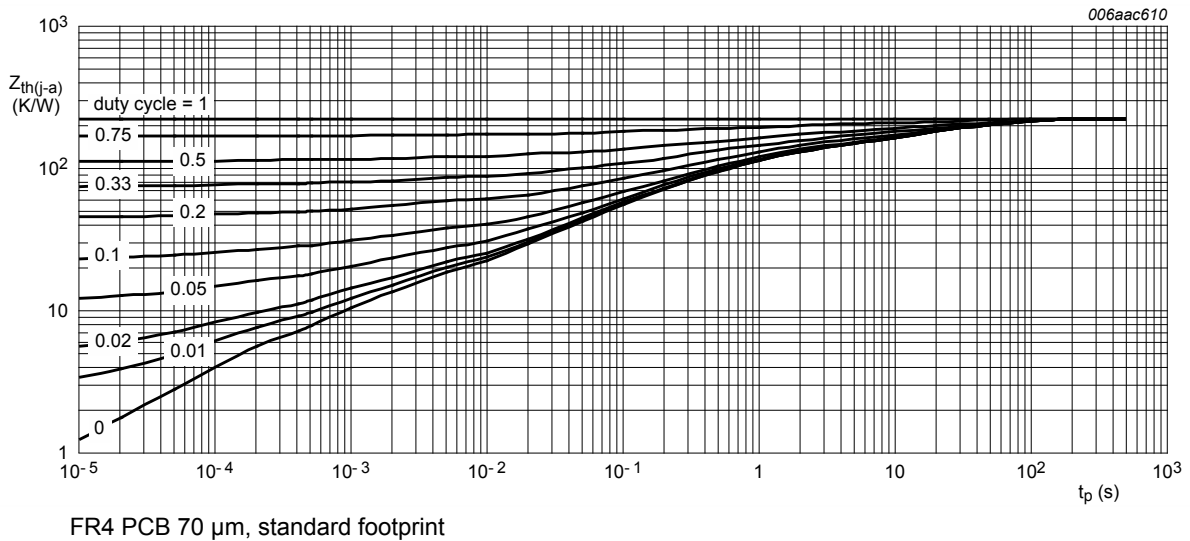
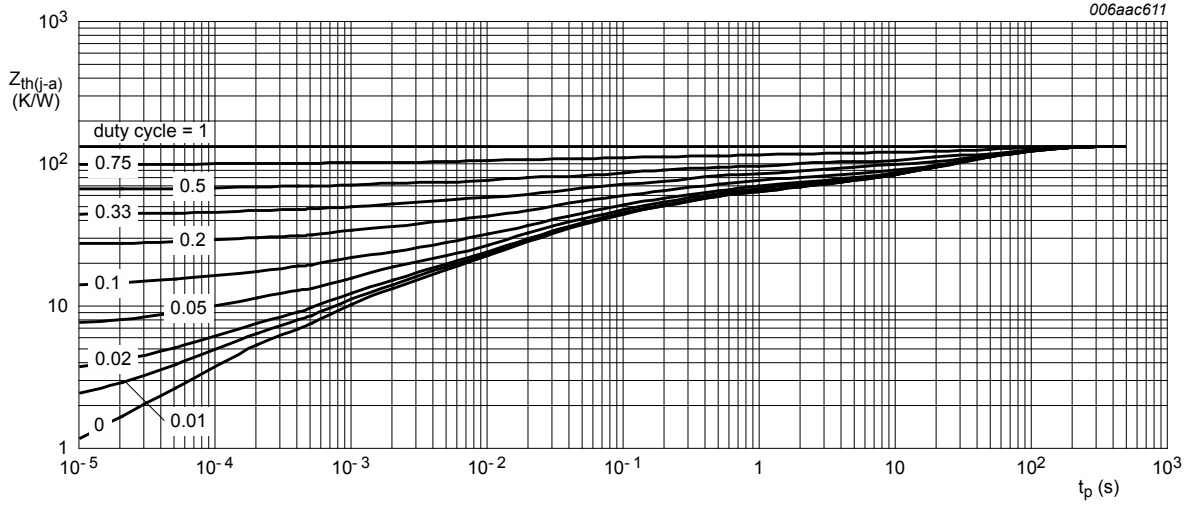
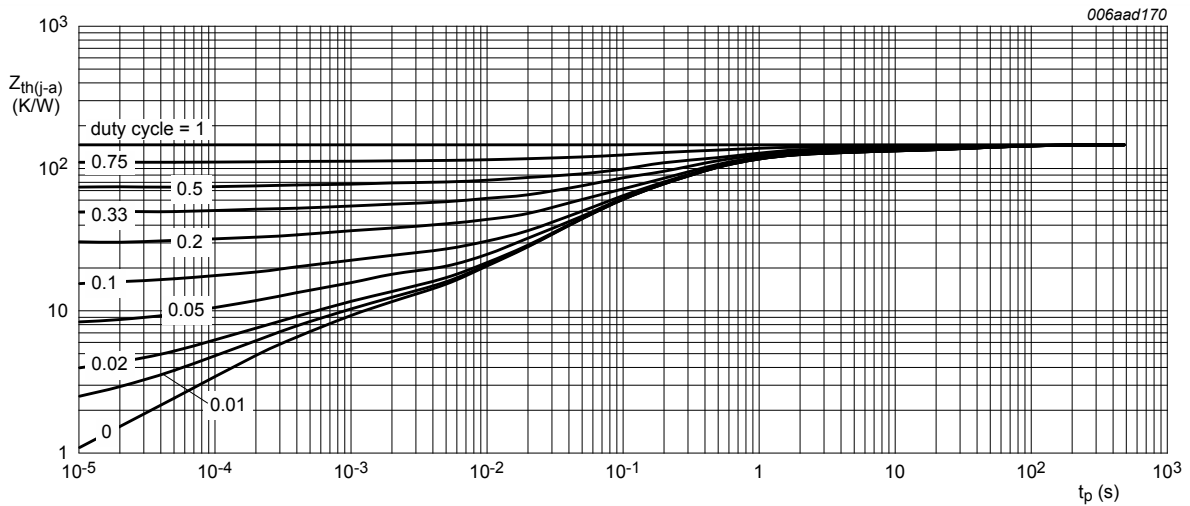


Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



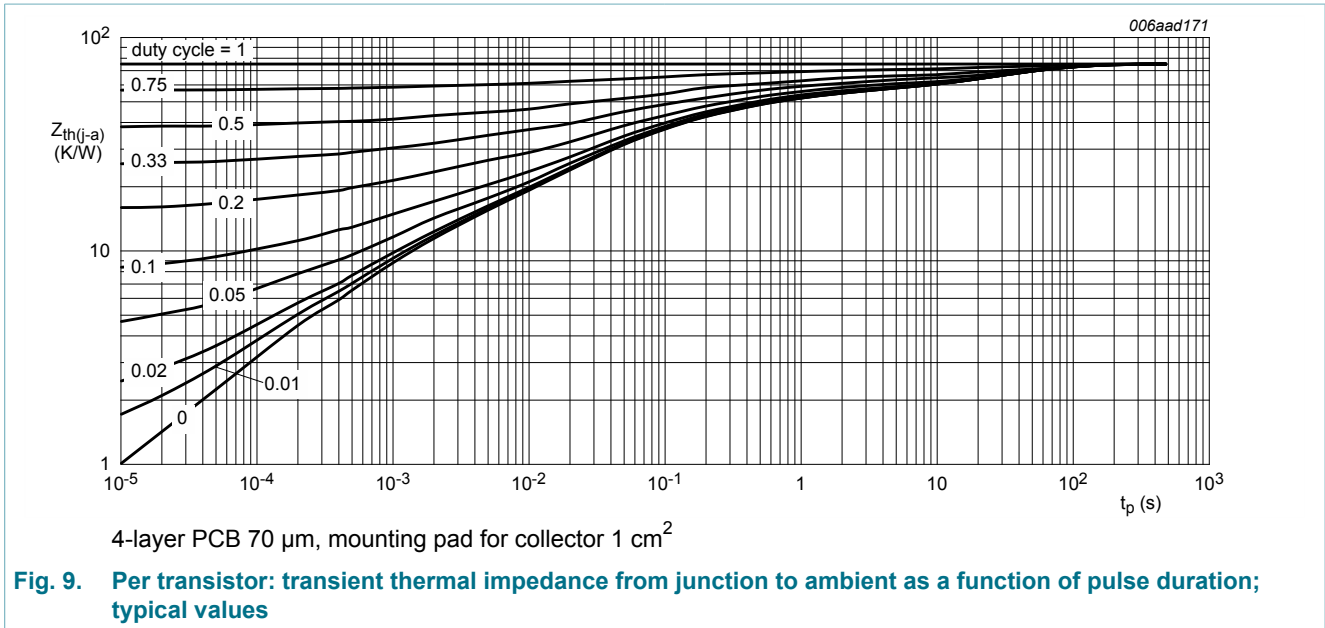
FR4 PCB 70  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$

**Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



4-layer PCB 70  $\mu\text{m}$ , standard footprint

**Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1 (NPN)</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 48 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{CB} = 48 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 2 \text{ V}; I_C = 100 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	290	430	-	
		$V_{CE} = 2 \text{ V}; I_C = 500 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	150	220	-	
		$V_{CE} = 2 \text{ V}; I_C = 1 \text{ A}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	70	110	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	90	120	mV
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	185	240	mV
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	175	220	mV
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 0.5 \text{ A}; I_B = 50 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	240	m $\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1	V
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1.1	V
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 2 \text{ V}; I_C = 0.5 \text{ A}; t_p \leq 300 \text{ } \mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	0.9	V
$t_d$	delay time	$V_{CC} = 10 \text{ V}; I_C = 0.5 \text{ A}; I_{Bon} = 25 \text{ mA};$ $I_{Boff} = -25 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	15	-	ns
$t_r$	rise time		-	90	-	ns
$t_{on}$	turn-on time		-	105	-	ns
$t_s$	storage time		-	410	-	ns
$t_f$	fall time		-	130	-	ns
$t_{off}$	turn-off time		-	540	-	ns
$f_T$	transition frequency		$V_{CE} = 10 \text{ V}; I_C = 50 \text{ mA}; f = 100 \text{ MHz};$ $T_{amb} = 25 \text{ }^\circ\text{C}$	90	175	-
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A};$ $f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	4	6	pF
<b>TR2 (PNP)</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -48 \text{ V}; I_E = 0 \text{ A}$	-	-	-100	nA
		$V_{CB} = -48 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	-50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$	-	-	-100	nA

## 60 V, 1 A NPN/PNP low VCEsat (BISS) transistor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	170	245	-	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	120	170	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	70	100	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-125	-180	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-390	-550	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-240	-340	mV
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	360	m $\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-1	V
		$I_C = -1\text{ A}; I_B = -50\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-1	V
		$I_C = -1\text{ A}; I_B = -100\text{ mA}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -0.5\text{ A}; t_p \leq 300\text{ }\mu\text{s};$ pulsed; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-0.9	V
$t_d$	delay time	$V_{CC} = -10\text{ V}; I_C = -0.5\text{ A}; I_{B(on)} = -25\text{ mA};$ $I_{B(off)} = 25\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	15	-	ns
$t_r$	rise time		-	40	-	ns
$t_{on}$	turn-on time		-	55	-	ns
$t_s$	storage time		-	95	-	ns
$t_f$	fall time		-	40	-	ns
$t_{off}$	turn-off time		-	135	-	ns
$f_T$	transition frequency		$V_{CE} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz};$ $T_{amb} = 25\text{ }^\circ\text{C}$	65	125	-
$C_C$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	9.5	13	pF

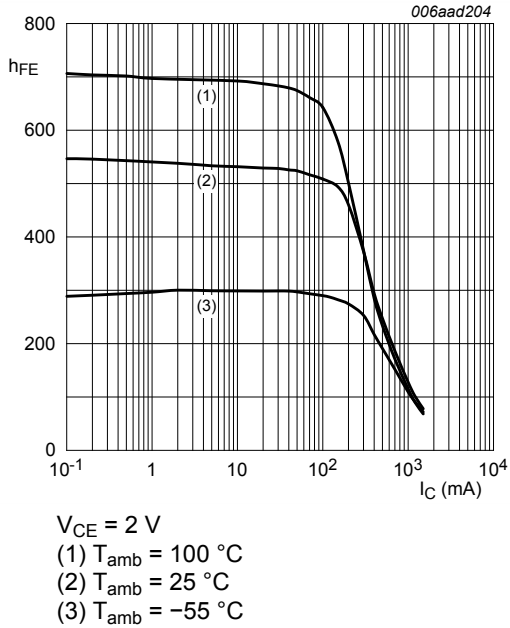


Fig. 10. TR1 (NPN): DC current gain as a function of collector current; typical values

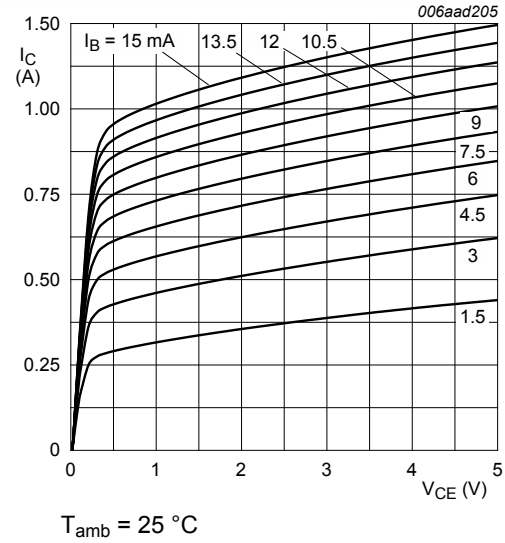


Fig. 11. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

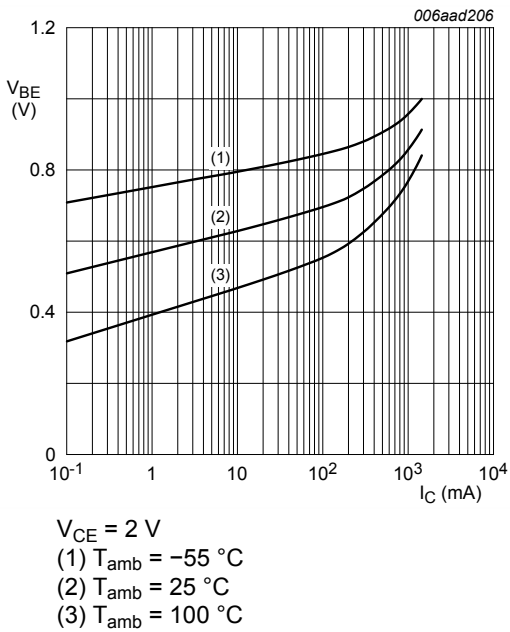


Fig. 12. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values

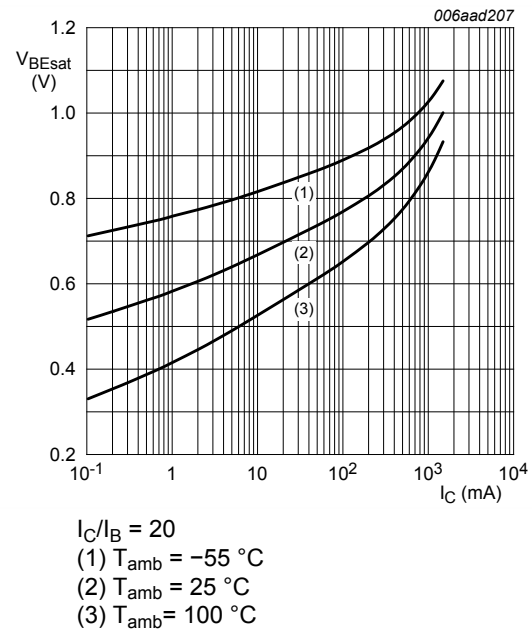


Fig. 13. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values

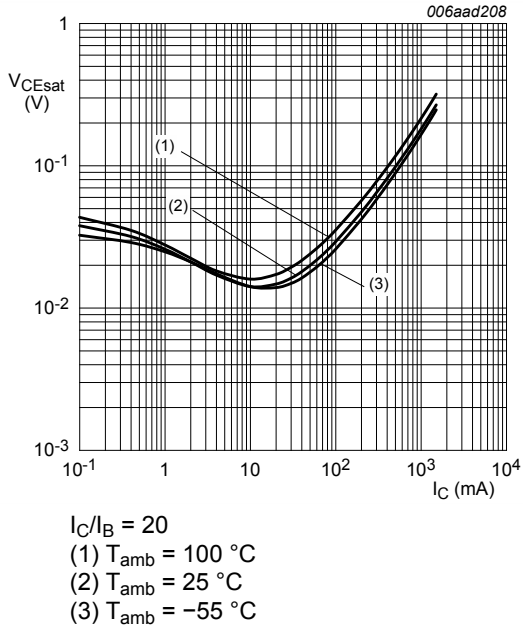


Fig. 14. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

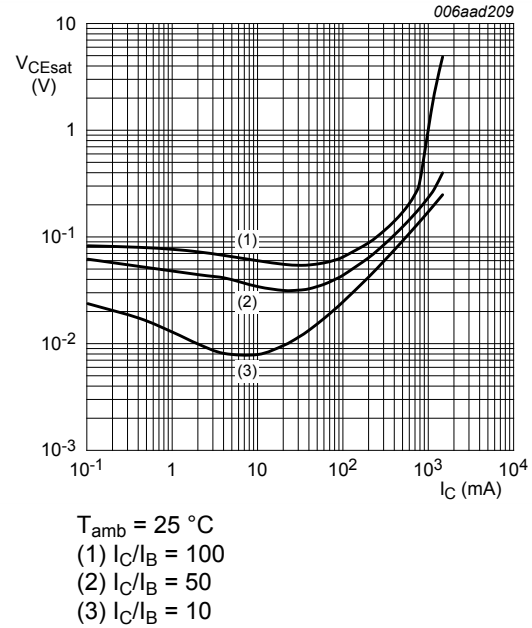


Fig. 15. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

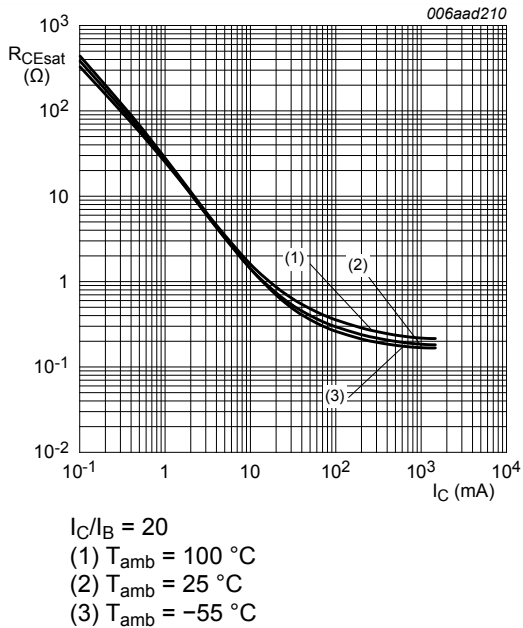


Fig. 16. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

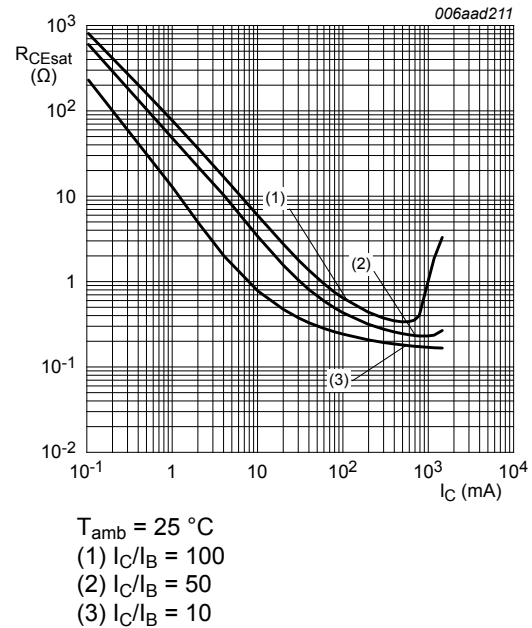


Fig. 17. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

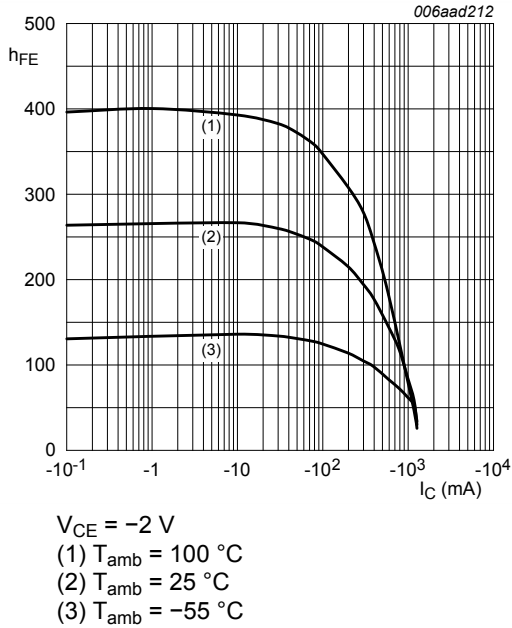


Fig. 18. TR2 (PNP): DC current gain as a function of collector current; typical values

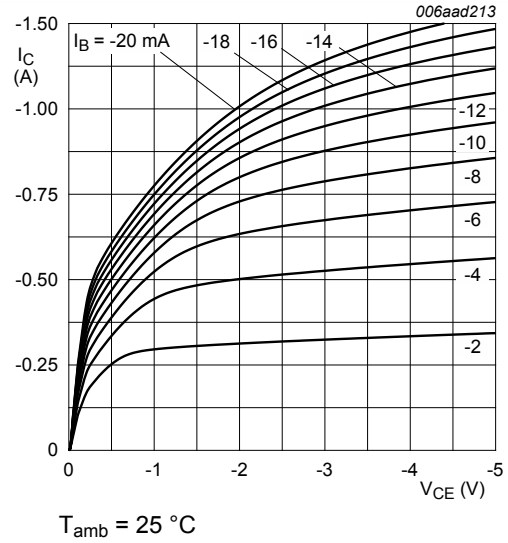


Fig. 19. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

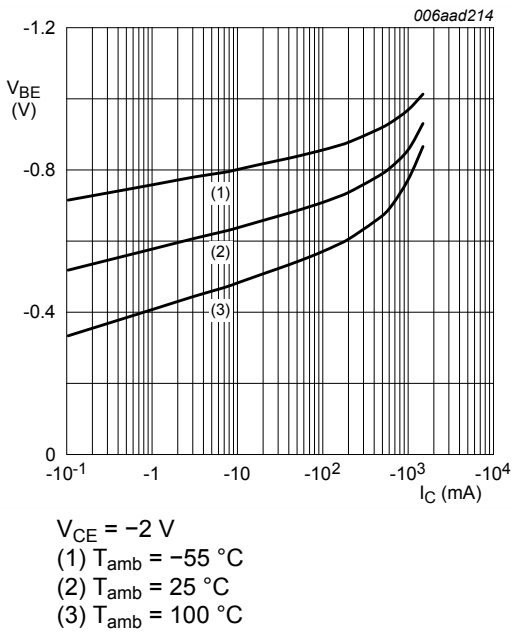


Fig. 20. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values

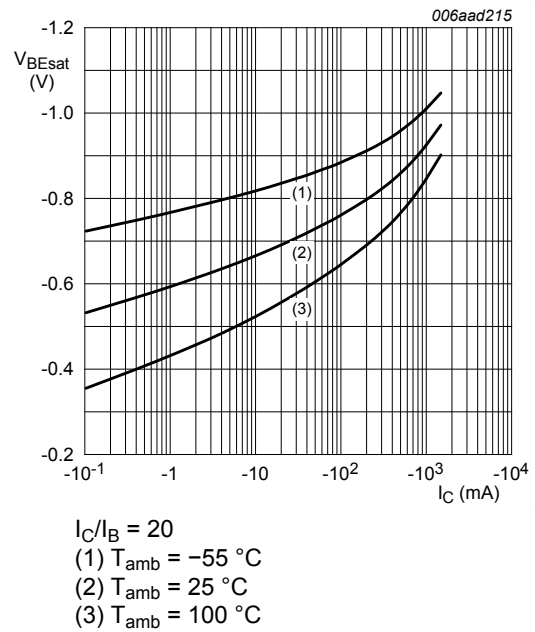
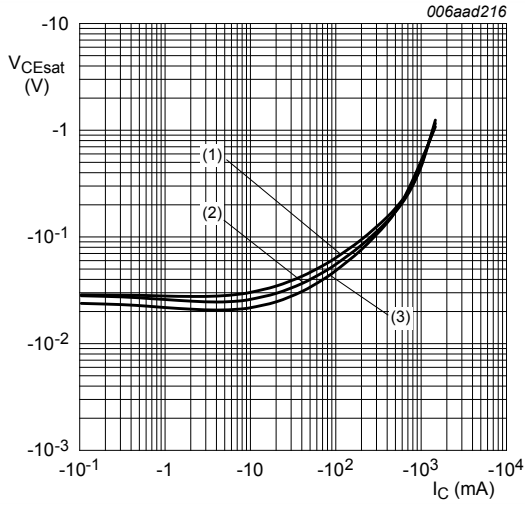
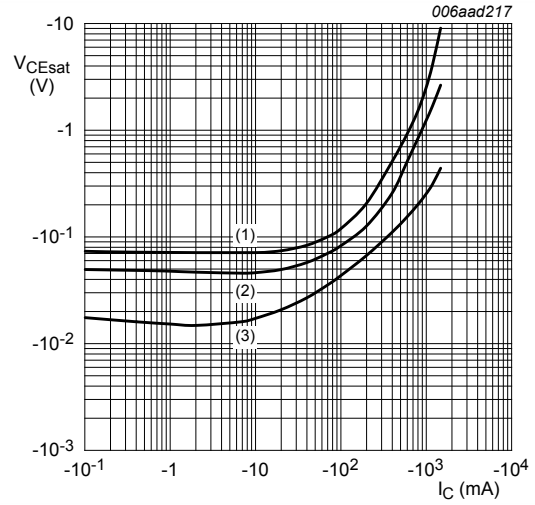


Fig. 21. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



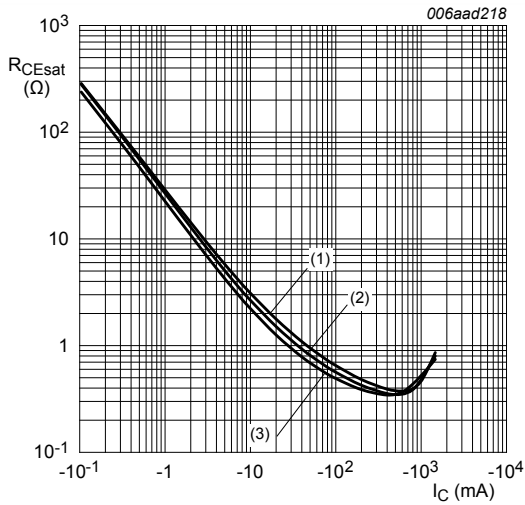
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 22. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



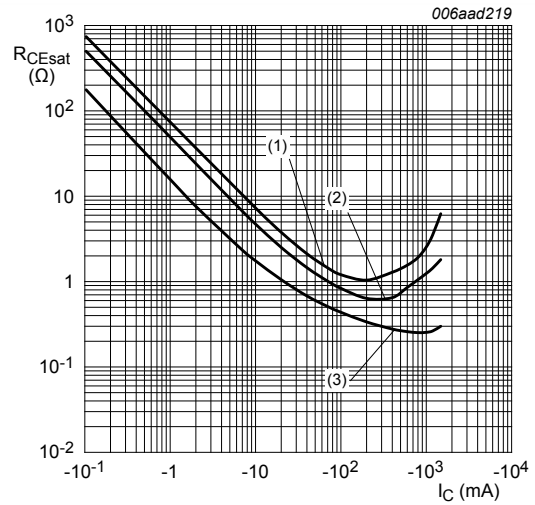
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 23. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 24. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**



$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 25. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**

### 11. Test information

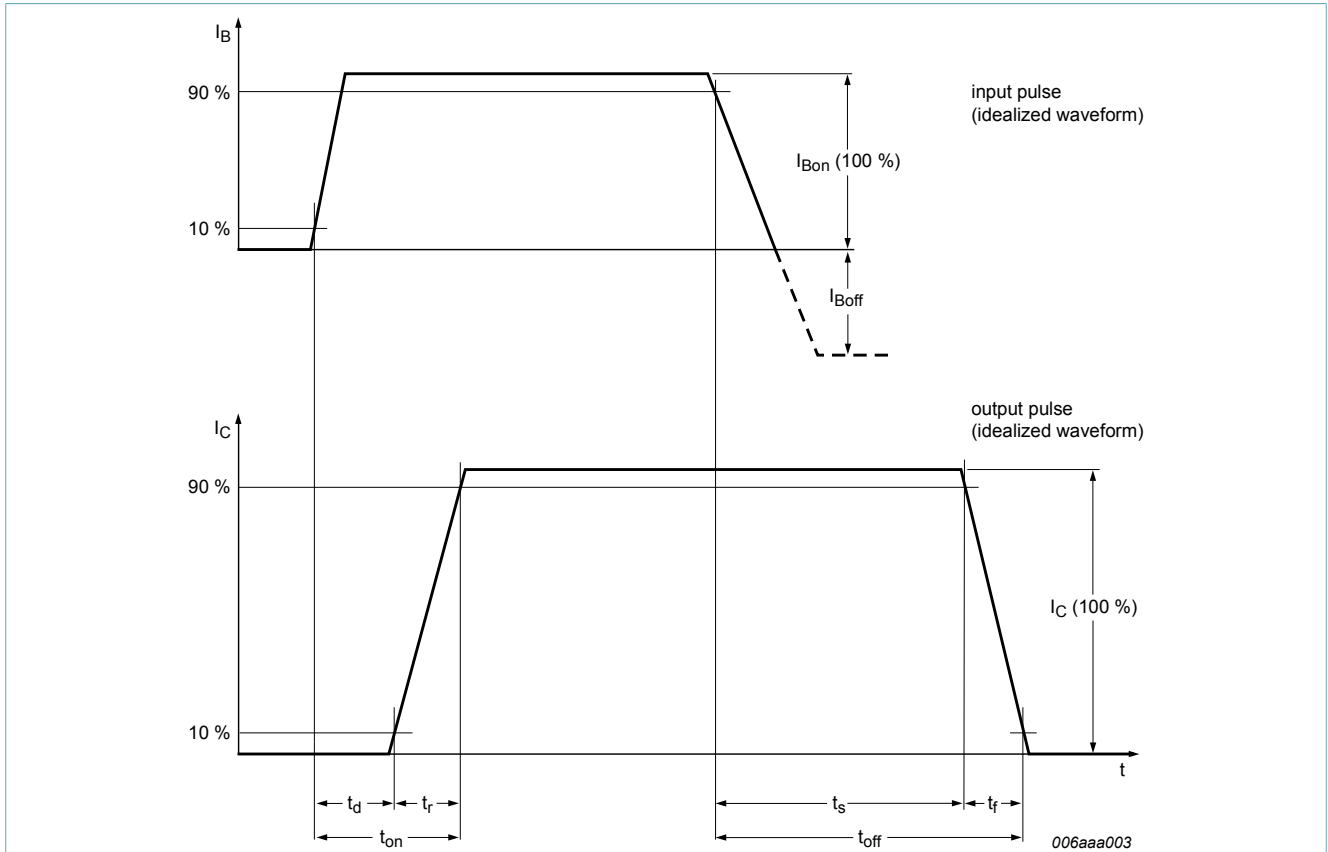


Fig. 26. TR1 (NPN): BISS transistor switching time definition

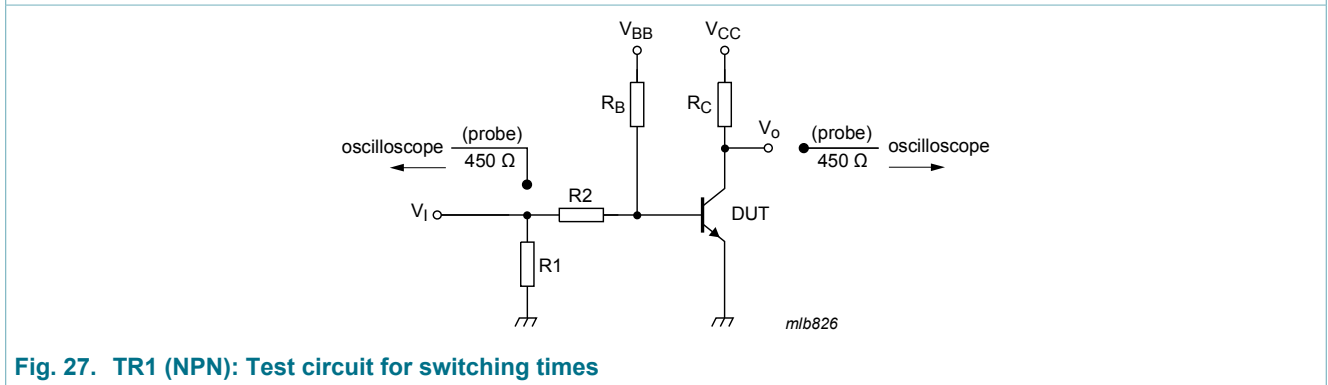


Fig. 27. TR1 (NPN): Test circuit for switching times

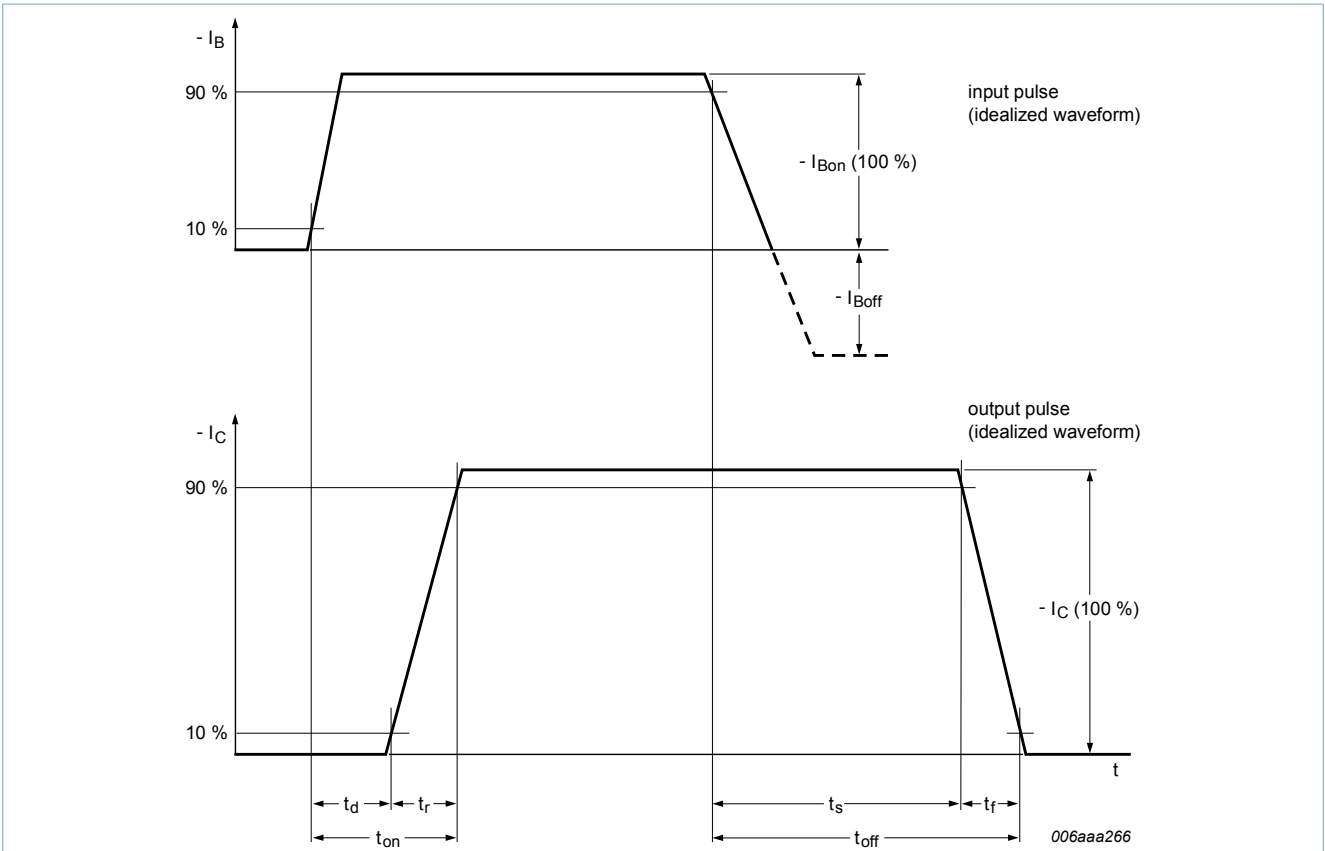


Fig. 28. TR2 (PNP): BISS transistor switching time definition

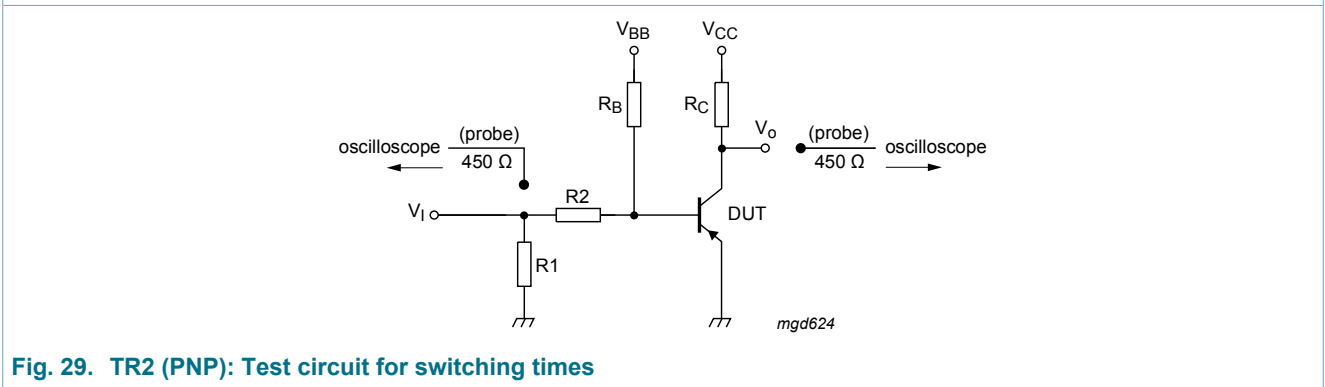


Fig. 29. TR2 (PNP): Test circuit for switching times

**Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### 12. Package outline

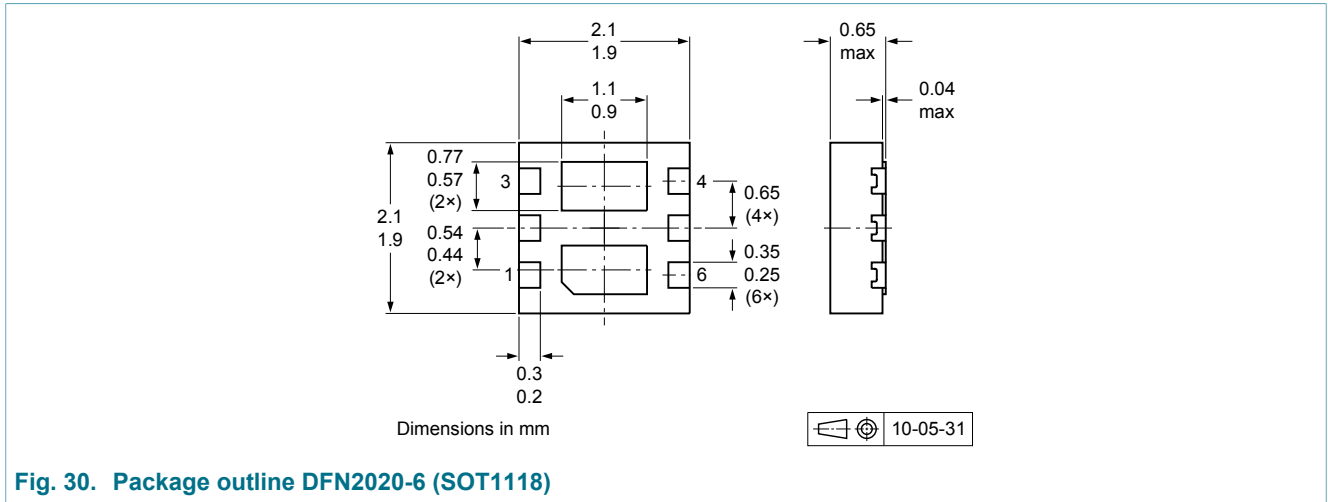


Fig. 30. Package outline DFN2020-6 (SOT1118)

### 13. Soldering

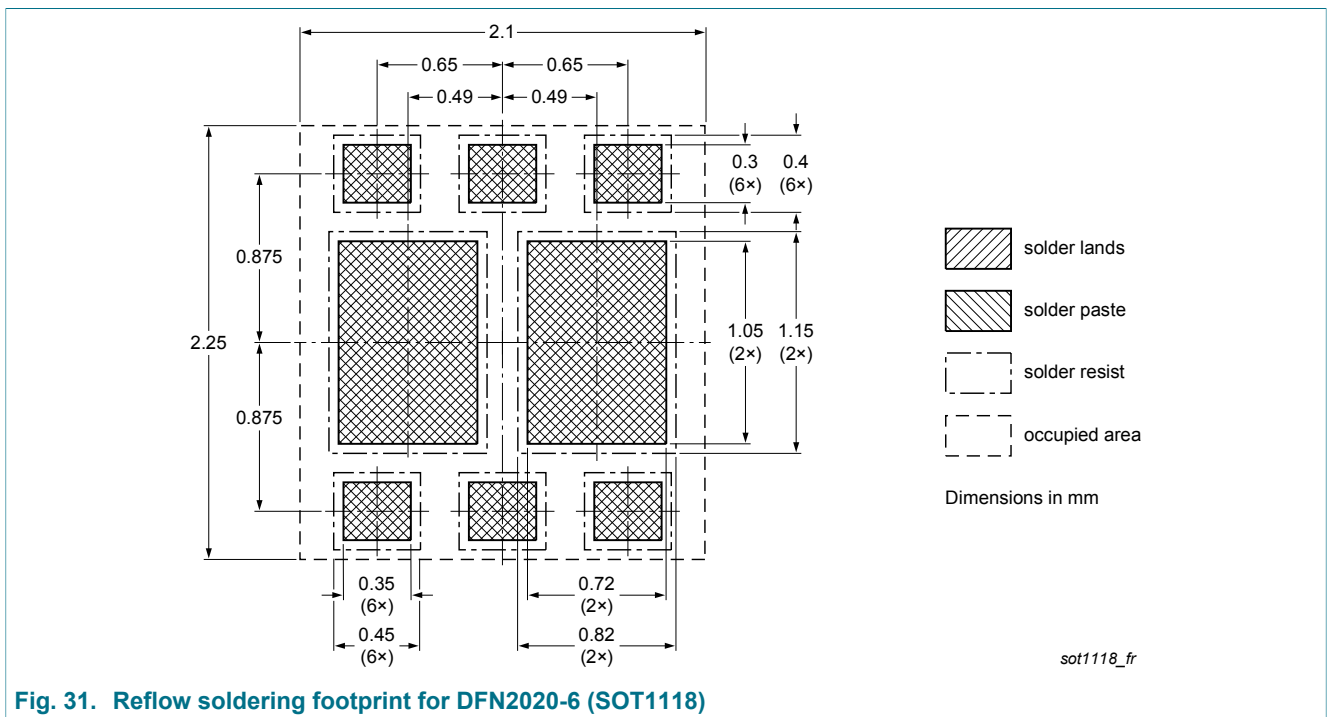


Fig. 31. Reflow soldering footprint for DFN2020-6 (SOT1118)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4160PANP v.2	20171220	Product data sheet	-	PBSS4160PANP v.1
Modifications:	<ul style="list-style-type: none"><li>Characteristics: Fig. 22 corrected</li></ul>			
PBSS4160PANP v.1	20130114	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## 16. Contents

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1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	4
10. Characteristics.....	10
11. Test information.....	16
12. Package outline.....	18
13. Soldering.....	18
14. Revision history.....	19
15. Legal information.....	20

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