



**THE DATASHEET OF
IPP040N06NAKSA1**

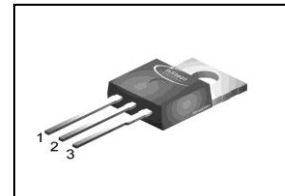


OptiMOS™ Power-Transistor
Features

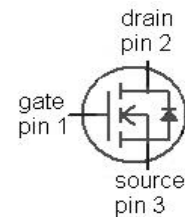
- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

| | | |
|------------------|-----|----|
| V_{DS} | 60 | V |
| $R_{DS(on),max}$ | 4.0 | mΩ |
| I_D | 80 | A |
| Q_{OSS} | 44 | nC |
| $Q_G(0V..10V)$ | 38 | nC |


PG-TO220-3


| Type | Package | Marking |
|------------|------------|---------|
| IPP040N06N | PG-TO220-3 | 040N06N |


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|---------------|---|-------|------|
| Continuous drain current | I_D | $V_{GS}=10\text{ V}, T_C=25\text{ °C}$ | 80 | A |
| | | $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ | 80 | |
| | | $V_{GS}=10\text{ V}, T_C=25\text{ °C}, R_{thJA}=50\text{K/W}$ | 20 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | 320 | |
| Avalanche energy, single pulse ³⁾ | E_{AS} | $I_D=80\text{ A}, R_{GS}=25\text{ Ω}$ | 70 | mJ |
| Gate source voltage | V_{GS} | | ±20 | V |

¹⁾ J-STD20 and JESD22

²⁾ See figure 3 for more detailed information

³⁾ See figure 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|-------------------------------------|-----------------------|---|-------------|------|
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 107 | W |
| | | $T_A=25\text{ °C}$, $R_{\text{thJA}}=50\text{ K/W}$ | 3.0 | |
| Operating and storage temperature | T_j, T_{stg} | | -55 ... 175 | °C |
| IEC climatic category; DIN IEC 68-1 | | | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Thermal characteristics

| | | | | | | |
|-------------------------------------|-------------------|--|---|---|-----|-----|
| Thermal resistance, junction - case | R_{thJC} | | - | - | 1.4 | K/W |
| Device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ⁴⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|-----------------------------|---|-----|-----|------|---------------|
| Drain-source breakdown voltage | $V_{(\text{BR})\text{DSS}}$ | $V_{\text{GS}}=0\text{ V}$, $I_{\text{D}}=1\text{ mA}$ | 60 | - | - | V |
| Gate threshold voltage | $V_{\text{GS(th)}}$ | $V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=50\text{ }\mu\text{A}$ | 2.1 | 2.8 | 3.3 | |
| Zero gate voltage drain current | I_{DSS} | $V_{\text{DS}}=60\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25\text{ °C}$ | - | 0.5 | 1 | μA |
| | | $V_{\text{DS}}=60\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125\text{ °C}$ | - | 10 | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$ | - | 10 | 100 | nA |
| Drain-source on-state resistance | $R_{\text{DS(on)}}$ | $V_{\text{GS}}=10\text{ V}$, $I_{\text{D}}=80\text{ A}$ | - | 3.6 | 4.0 | m Ω |
| | | $V_{\text{GS}}=6\text{ V}$, $I_{\text{D}}=20\text{ A}$ | - | 4.7 | 6.0 | |
| Gate resistance | R_{G} | | - | 1.3 | 1.95 | Ω |
| Transconductance | g_{fs} | $ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$, $I_{\text{D}}=80\text{ A}$ | 60 | 120 | - | S |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics

| | | | | | | |
|------------------------------|--------------|--|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$ | - | 2700 | 3375 | pF |
| Output capacitance | C_{oss} | | - | 670 | 838 | |
| Reverse transfer capacitance | C_{rss} | | - | 28 | 56 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=80\text{ A}, R_{G,ext}=3\ \Omega$ | - | 19 | - | ns |
| Rise time | t_r | | - | 16 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 30 | - | |
| Fall time | t_f | | - | 9 | - | |

Gate Charge Characteristics⁵⁾

| | | | | | | |
|------------------------------|---------------|---|---|-----|----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=30\text{ V}, I_D=80\text{ A}, V_{GS}=0\text{ to }10\text{ V}$ | - | 13 | - | nC |
| Gate charge at threshold | $Q_{g(th)}$ | | - | 8 | - | |
| Gate to drain charge | Q_{gd} | | - | 7 | 9 | |
| Switching charge | Q_{sw} | | - | 13 | - | |
| Gate charge total | Q_g | | - | 38 | 44 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 4.9 | - | V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | $V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$ | - | 33 | - | nC |
| Output charge | Q_{oss} | $V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$ | - | 44 | - | |

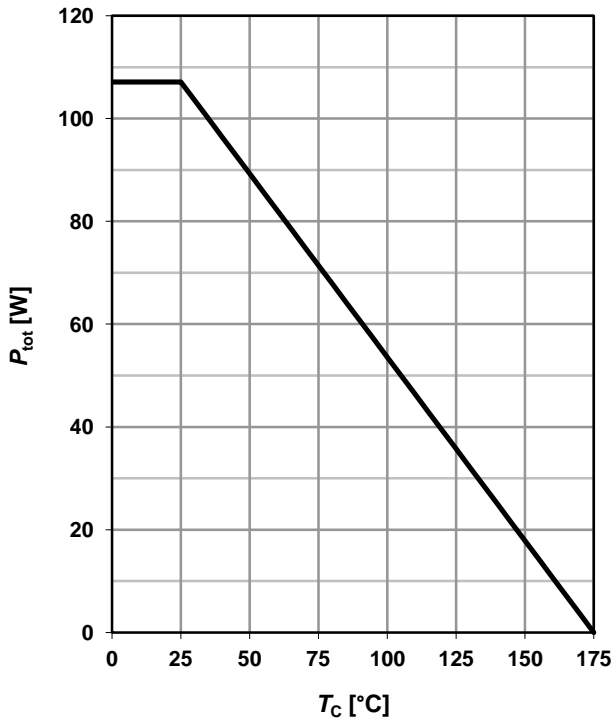
Reverse Diode

| | | | | | | |
|----------------------------------|---------------|--|---|-----|-----|----|
| Diode continuous forward current | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 80 | A |
| Diode pulse current | $I_{S,pulse}$ | | - | - | 320 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=80\text{ A}, T_j=25\text{ }^\circ\text{C}$ | - | 1.0 | 1.2 | V |
| Reverse recovery time | t_{rr} | $V_R=30\text{ V}, I_F=80\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ | - | 34 | 54 | ns |
| Reverse recovery charge | Q_{rr} | | - | 34 | - | nC |

⁵⁾ See figure 16 for gate charge parameter definition

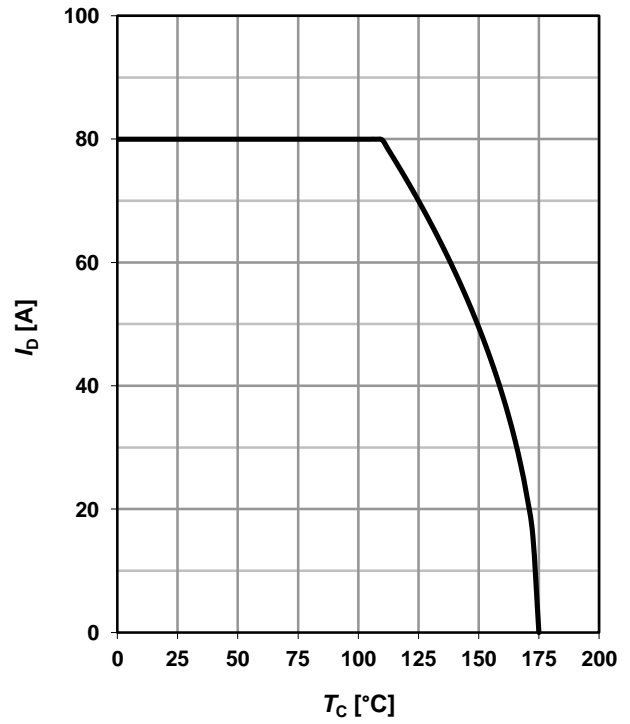
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

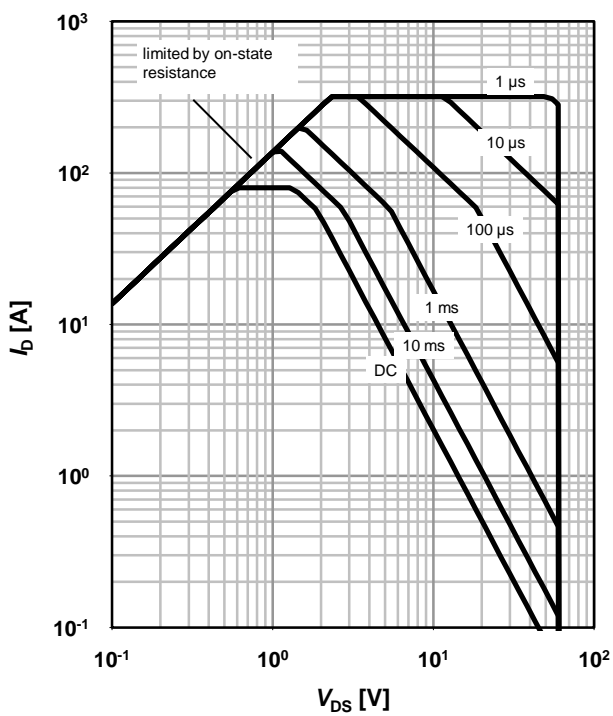
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

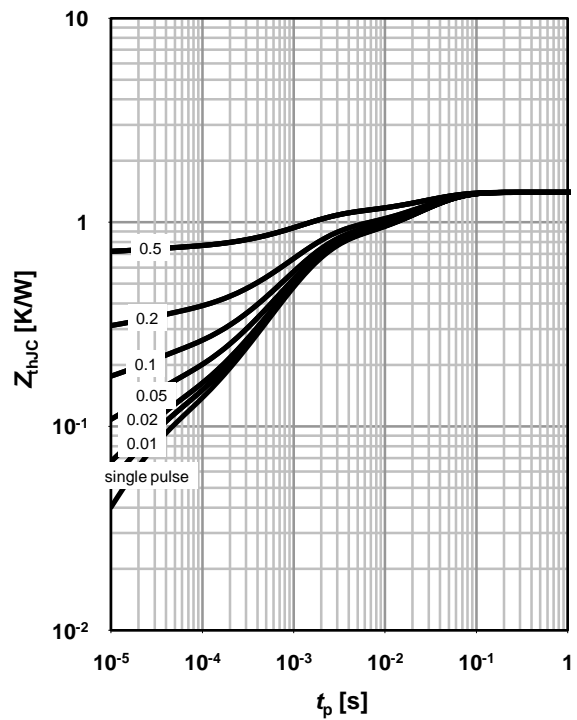
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

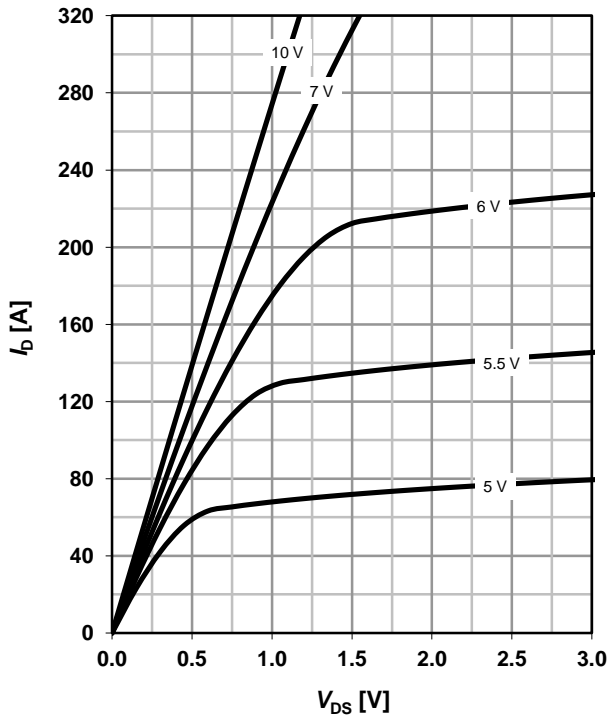
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

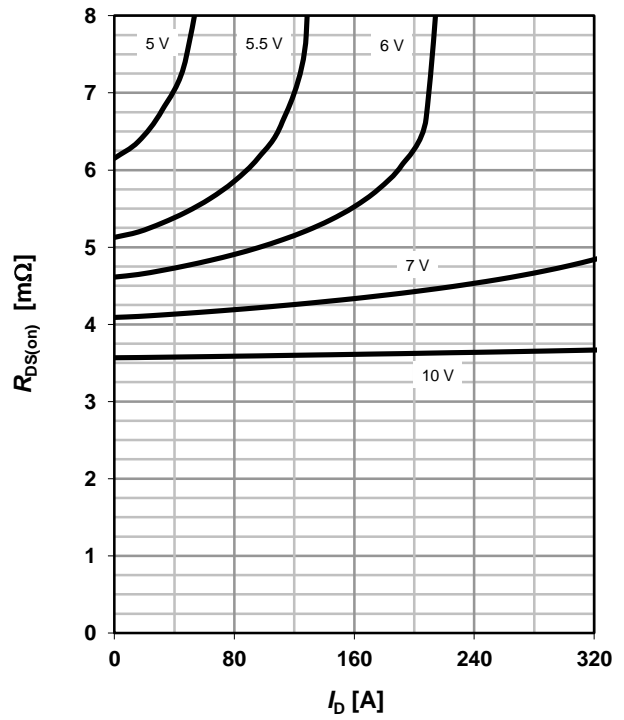
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

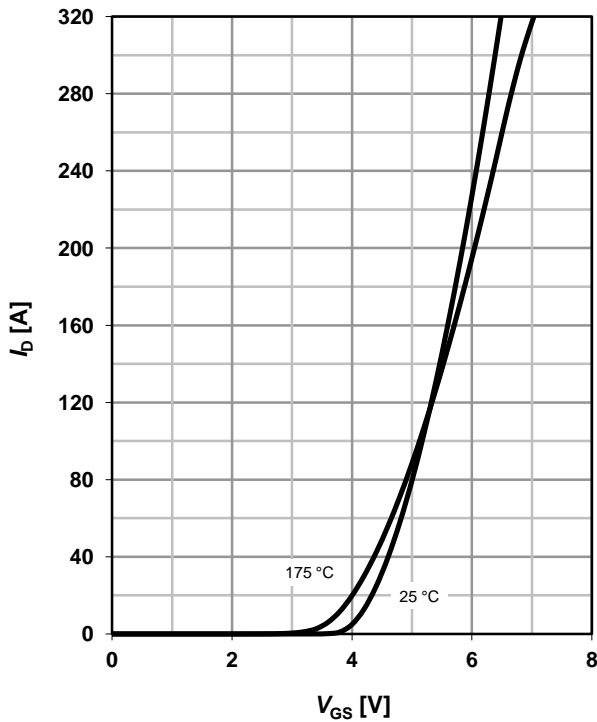
parameter: V_{GS}



7 Typ. transfer characteristics

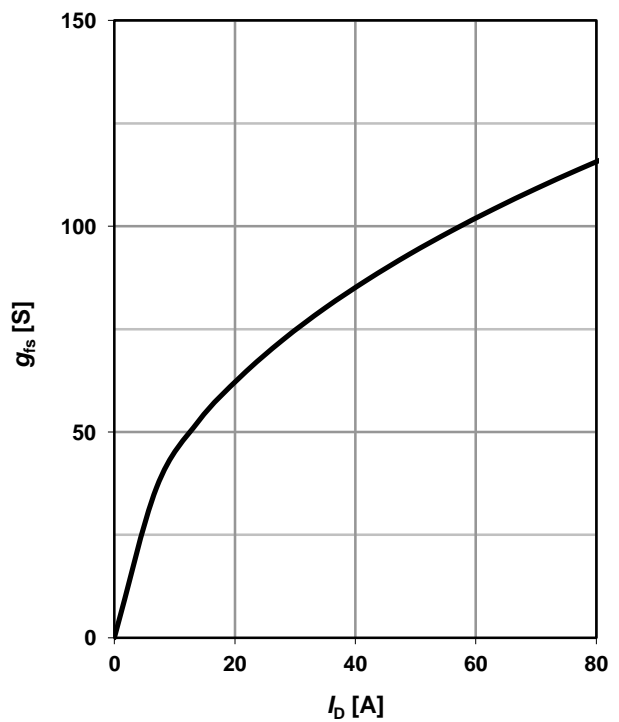
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



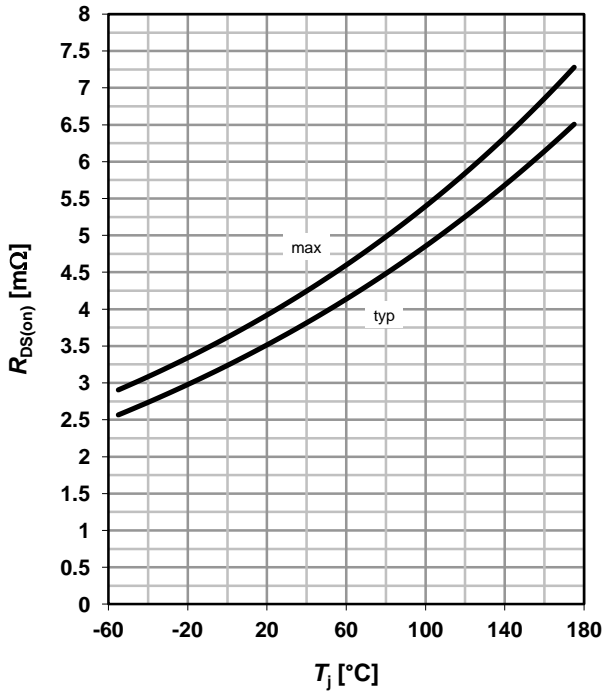
8 Typ. forward transconductance

$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$



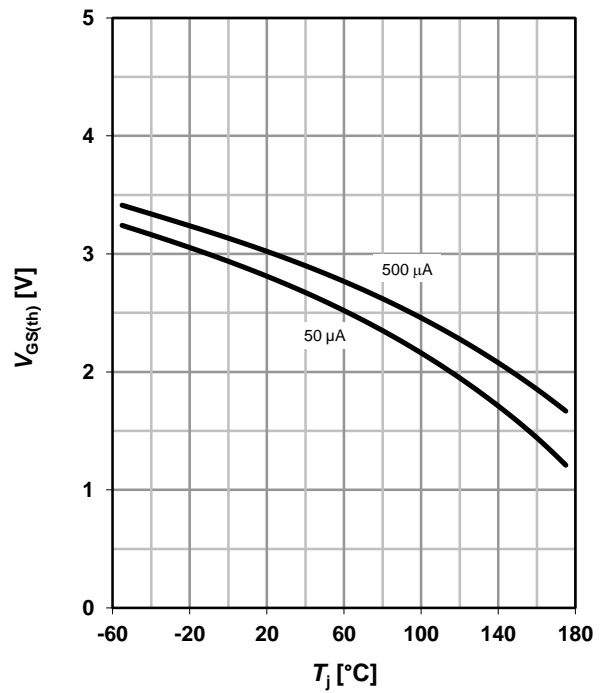
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j); I_D=80\text{ A}; V_{GS}=10\text{ V}$



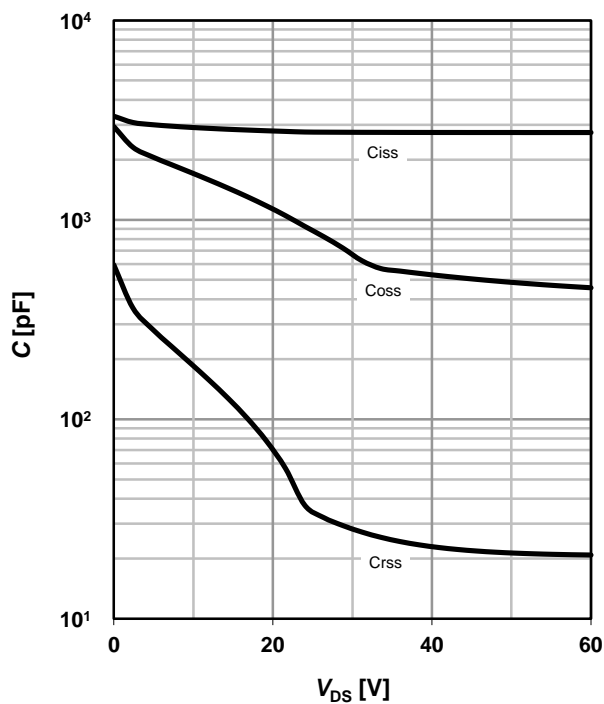
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$



11 Typ. capacitances

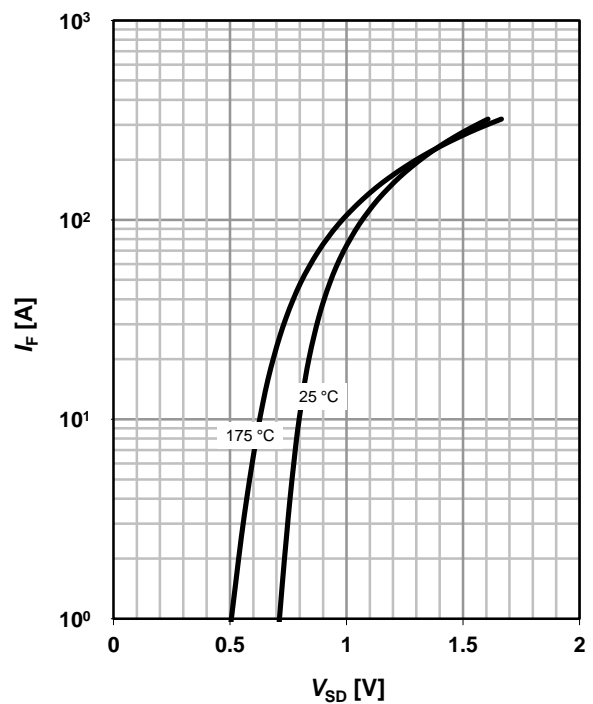
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

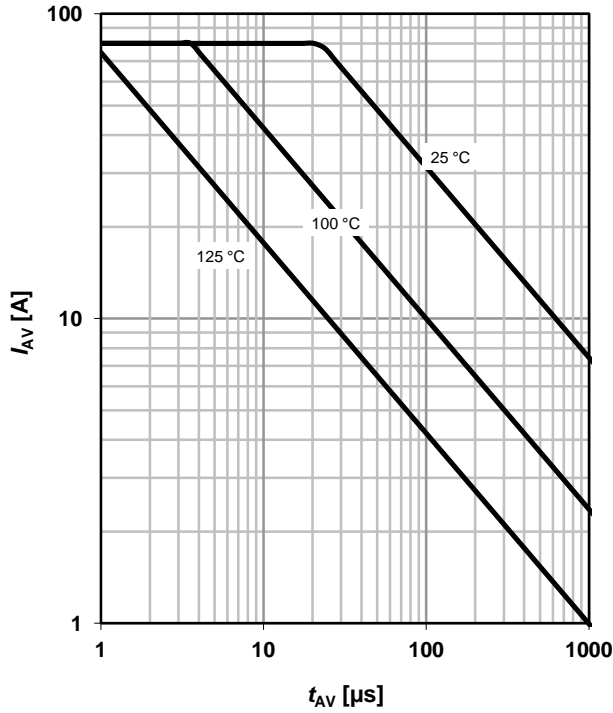
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

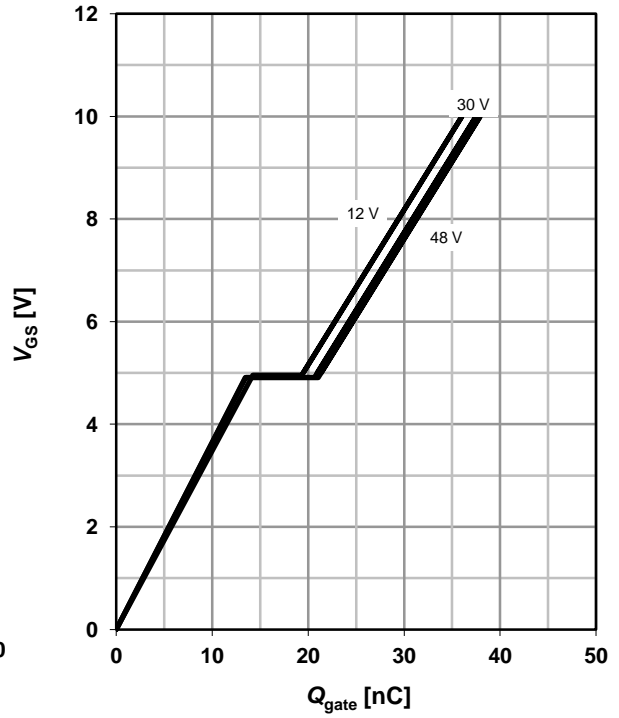
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

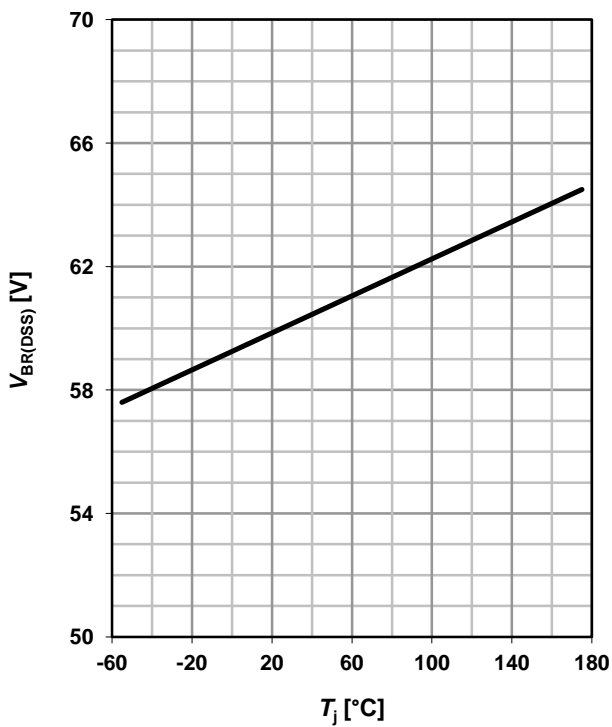
$V_{GS}=f(Q_{\text{gate}}); I_D=80 \text{ A pulsed}$

parameter: V_{DD}

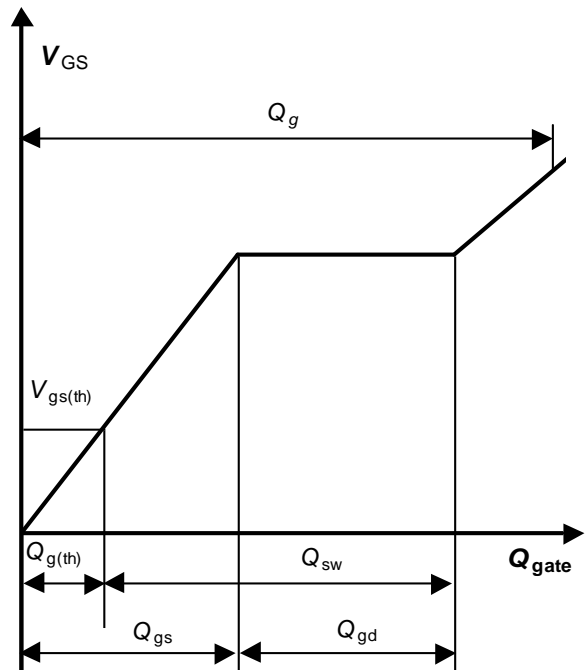


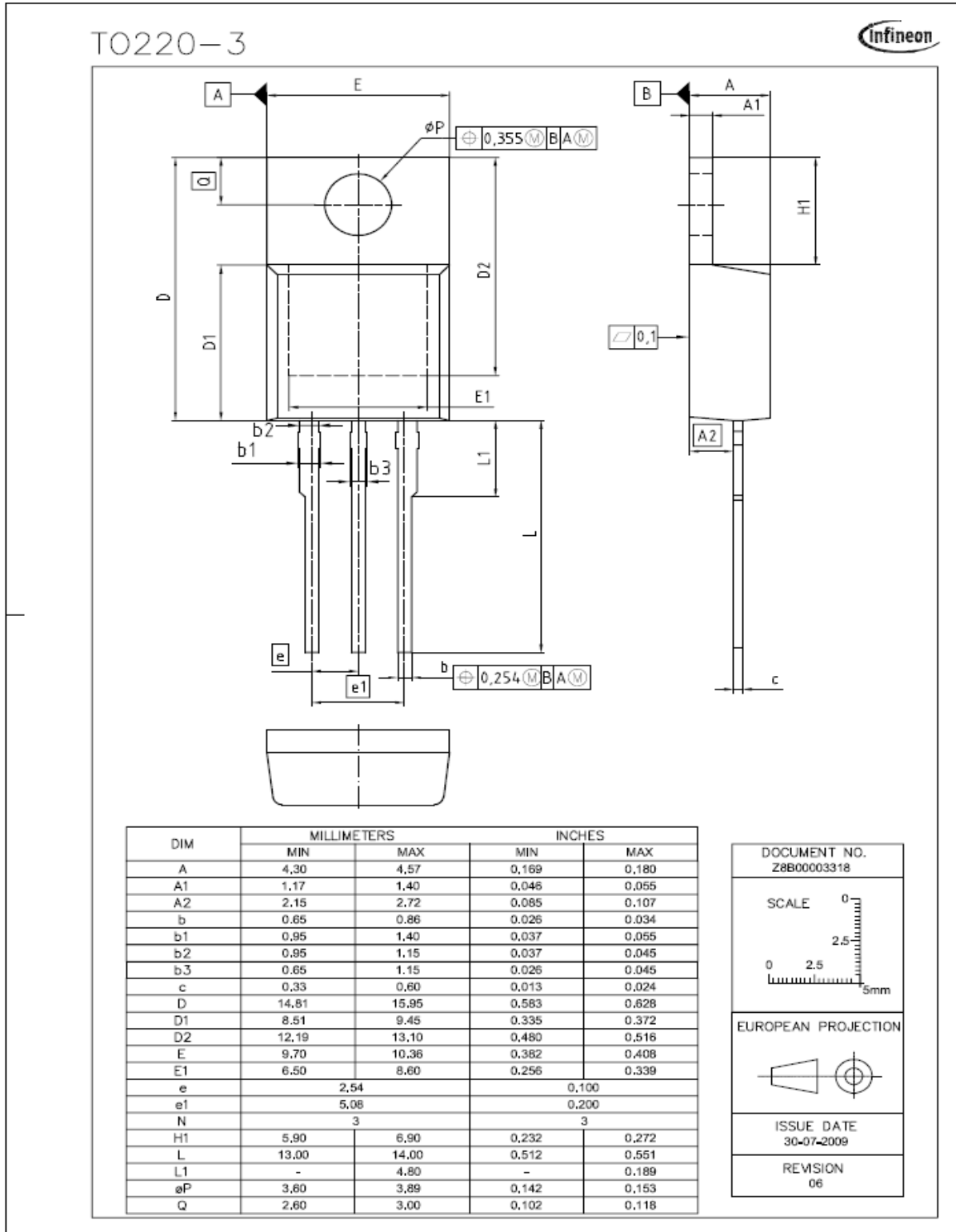
15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms





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