THE DATASHEET OF

LT3435EFE#PBF

High Voltage 3A, 500kHz Step-Down Switching Regulator with 100µA Quiescent Current

FEATURES

- **Wide Input Range: 3.3V to 60V**
- **3A Peak Switch Current**
- **Burst Mode® Operation: 100µA Quiescent Current****
- **Low Shutdown Current: I_Q < 1µA**
- **Power Good Flag with Programmable Threshold**
- **Load Dump Protection to 60V**
- 500kHz Switching Frequency
- Saturating Switch Design: 0.1Ω On-Resistance
- Peak Switch Current Maintained Over Full Duty Cycle Range*
- 1.25V Feedback Reference Voltage
- Easily Synchronizable
- Soft-Start Capability
- Small 16-Pin Thermally Enhanced TSSOP Package

APPLICATIONS

- High Voltage Power Conversion
- 14V and 42V Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems
- USB Powered Systems

DESCRIPTION

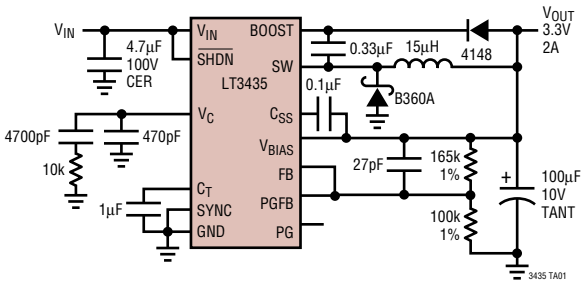
The LT®3435 is a 500kHz monolithic buck switching regulator that accepts input voltages up to 60V. A high efficiency 3A, 0.1Ω switch is included on the die along with all the necessary oscillator, control and logic circuitry. Current mode topology is used for fast transient response and good loop stability.

Innovative design techniques along with a new high voltage process achieve high efficiency over a wide input range. Efficiency is maintained over a wide output current range by employing Burst Mode operation at low currents, utilizing the output to bias the internal circuitry, and by using a supply boost capacitor to fully saturate the power switch. Patented circuitry maintains peak switch current over the full duty cycle range.* Shutdown reduces input supply current to less than 1µA. External synchronization can be implemented by driving the SYNC pin with logic-level inputs. A single capacitor from the C_{SS} pin to the output provides a controlled output voltage ramp (soft-start). The device also has a power good flag with a programmable threshold and time-out and thermal shutdown protection.

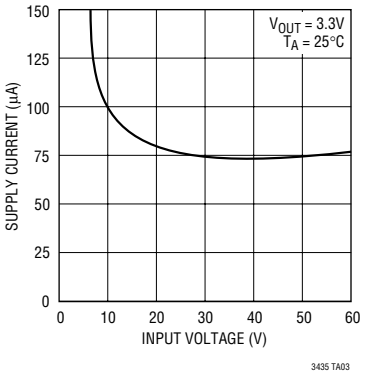
The LT3435 is available in a 16-pin TSSOP package with an exposed pad leadframe for low thermal resistance.

TYPICAL APPLICATION

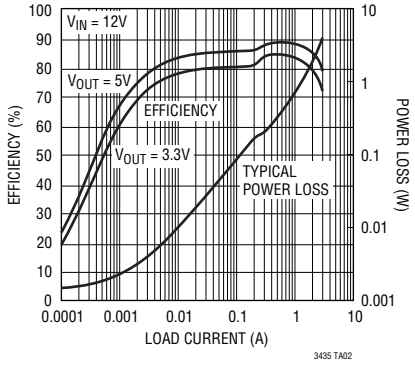
14V to 3.3V Step-Down Converter with 100µA No Load Quiescent Current



Supply Current vs Input Voltage



Efficiency and Power Loss vs Load Current

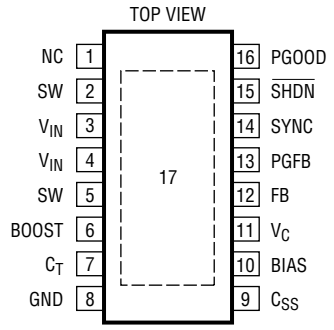


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, $\overline{SHDN}$, BIAS, PGOOD, SW 60V
BOOST Pin Above SW 35V
BOOST Pin Voltage 68V
SYNC, C_{SS}, PGFB, FB 6V
Operating JunctionTemperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W

EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO GND (PIN 8)

ORDER PART NUMBER	FE PART MARKING
LT3435EFE LT3435IFE	3435EFE 3435IFE

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 12V, BIAS = 5V, FB/PGFB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Threshold			1.15	1.3	1.45	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 12V	●		5	20	µA
	Minimum Input Voltage (Note 3)		●		2.4	3	V
I_{VINS}	Supply Shutdown Current	$\overline{SHDN}$ = 0V, BOOST = 0V, FB/PGFB = 0V			0.1	2	µA
	Supply Sleep Current (Note 4)	BIAS = 0V, FB = 1.35V FB = 1.35V	● ●		170 45	250 75	µA µA
I_{VIN}	Supply Quiescent Current	BIAS = 0V, FB = 1.15V BIAS = 5V, FB = 1.15V			3.3 2.6	7 6	mA mA
	Minimum BIAS Voltage (Note 5)		●		2.7	3.1	V
I_{BIASS}	BIAS Sleep Current (Note 4)		●		125	180	µA
I_{BIAS}	BIAS Quiescent Current	SYNC = 3.3V			700	900	µA
	Minimum Boost Voltage (Note 6)	I_{SW} = 1.5A			1.8		V
	Input Boost Current (Note 7)	I_{SW} = 3A			65	85	mA
V_{REF}	Reference Voltage (V_{REF})	3.3V < V_{VIN} < 60V	●	1.225	1.25	1.275	V
I_{FB}	FB Input Bias Current				75	200	nA
	EA Voltage Gain (Note 8)				900		V/V
	EA Voltage g_m	dI(V_C)= ±10µA		400	650	900	µMho

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, SHDN = 12V, BIAS = 5V, FB/PGFB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	EA Source Current	FB = 1.15V		20	40	55	µA
	EA Sink Current	FB = 1.35V		15	30	40	µA
	V_C to SW g_m				6		A/V
	V_C High Clamp	FB = 1.15V		2.1	2.2	2.4	V
I_{PK}	SW Current Limit		●	3	5.2	6.5	A
	Switch On Resistance (Note 9)		●		0.1	0.25	Ω
	Switching Frequency		●	425	500	575	kHz
	Maximum Duty Cycle			86	92		%
	Minimum SYNC Amplitude				1.5	2.0	V
	SYNC Frequency Range			575		700	kHz
	SYNC Input Impedance				45		kΩ
I_{CSS}	C_{SS} Current Threshold (Note 10)	FB = 0V		7	13	20	µA
I_{PGFB}	PGFB Input Current				25	100	nA
V_{PGFB}	PGFB Voltage Threshold (Note 11)		●	88	90	92	%
I_{CT}	C_T Source Current (Note 11)			2	3.6	5.5	µA
	C_T Sink Current (Note 11)			1	2		mA
V_{CT}	C_T Voltage Threshold (Note 11)			1.16	1.2	1.26	V
	PG Leakage (Note 11)				0.1	1	µA
	PG Sink Current (Note 11)	PGFB = 1V, PG = 400mV		100	200		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3435EFE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3435IFE is guaranteed and tested over the full –40°C to 125°C operating junction temperature range.

Note 3: Minimum input voltage is defined as the voltage where switching starts. Actual minimum input voltage to maintain a regulated output will depend upon output voltage and load current. See Applications Information.

Note 4: Supply input current is the quiescent current drawn by the input pin. Its typical value depends on the voltage on the BIAS pin and operating state of the LT3435. With the BIAS pin at 0V, all of the quiescent current required to operate the LT3435 will be provided by the V_{IN} pin. With the BIAS voltage above its minimum input voltage, a portion of the total quiescent current will be supplied by the BIAS pin. Supply sleep current is defined as the quiescent current during the "sleep" portion of Burst Mode operation. See Applications Information for determining application supply currents.

Note 5: Minimum BIAS voltage is the voltage on the BIAS pin when I_{BIAS} is sourced into the pin.

Note 6: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 7: Boost current is the current flowing into the BOOST pin with the pin held 3.3V above input voltage. It flows only during switch on time.

Note 8: Gain is measured with a V_C swing from 1.15V to 750mV.

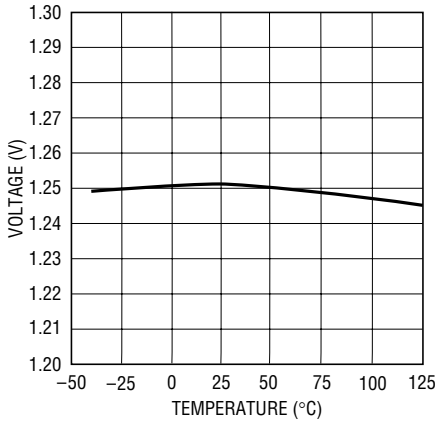
Note 9: Switch on resistance is calculated by dividing V_{IN} to SW voltage by the forced current (3A). See Typical Performance Characteristics for the graph of switch voltage at other currents.

Note 10: The C_{SS} threshold is defined as the value of current sourced into the C_{SS} pin which results in an increase in sink current from the V_C pin. See the Soft-Start section in Applications Information.

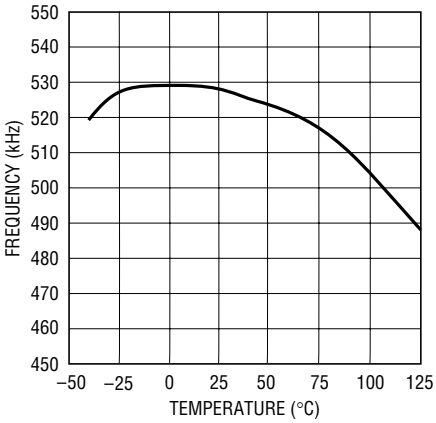
Note 11: The PGFB threshold is defined as the percentage of V_{REF} voltage which causes the current source output of the C_T pin to change from sinking (below threshold) to sourcing current (above threshold). When sourcing current, the voltage on the C_T pin rises until it is clamped internally. When the clamp is activated, the output of the PG pin will be set to a high impedance state. When the C_T clamp is inactive the PG pin will be set active low with a current sink capability of 200µA.

TYPICAL PERFORMANCE CHARACTERISTICS

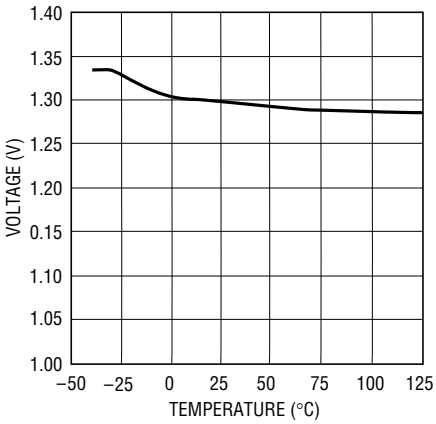
FB Voltage



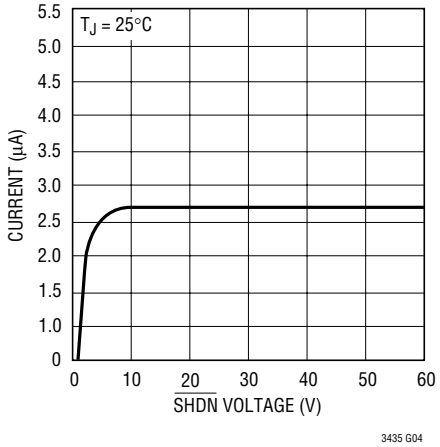
Oscillator Frequency



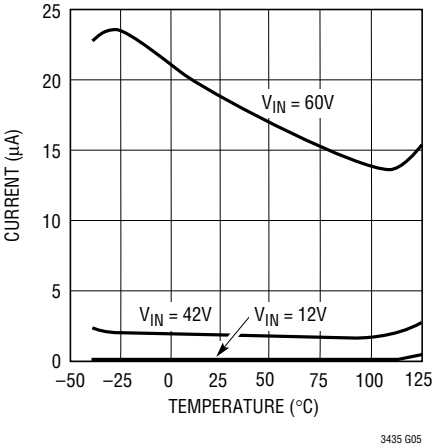
$\overline{SHDN}$ Threshold



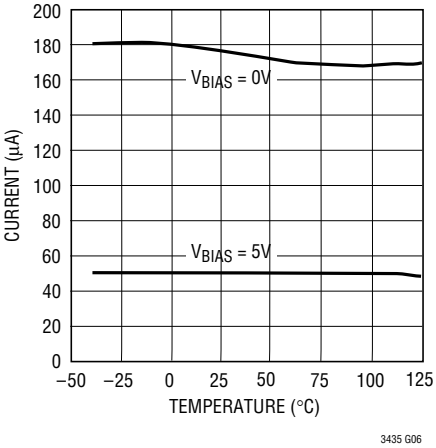
$\overline{SHDN}$ Pin Current



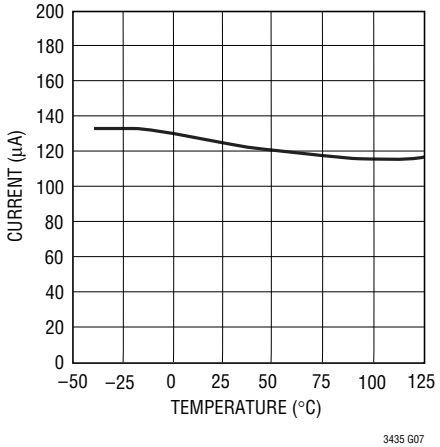
Shutdown Supply Current



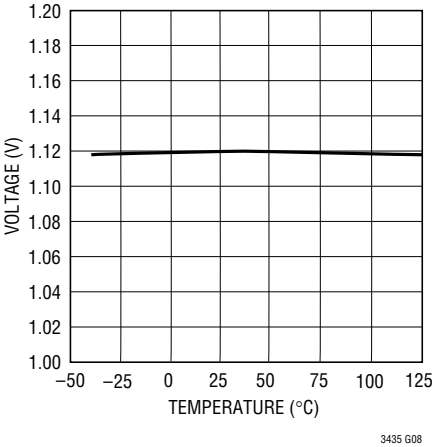
Sleep Mode Supply Current



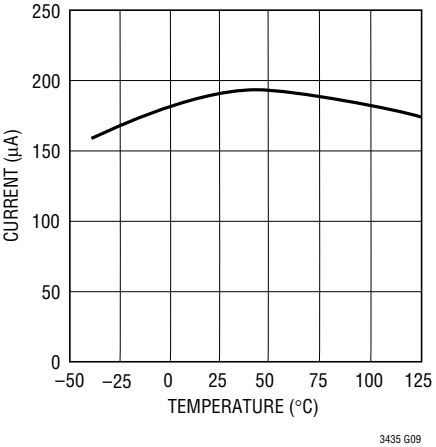
Bias Sleep Current



PGFB Threshold

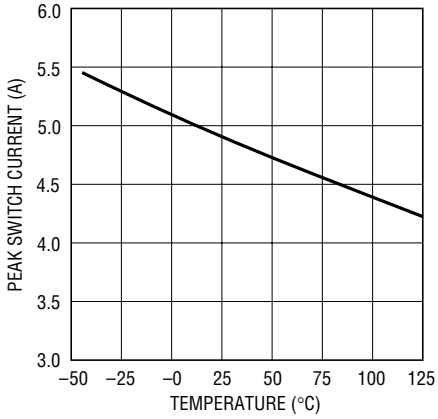


PG Sink Current



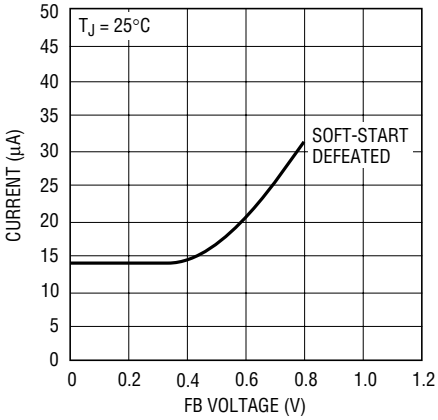
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Peak Current Limit



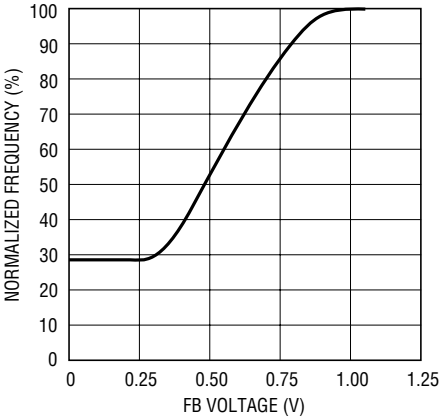
3435 G10

Soft-Start Current Threshold vs FB Voltage



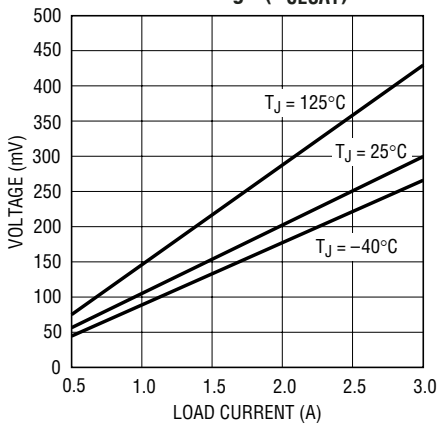
3435 G11

Oscillator Frequency vs FB Voltage



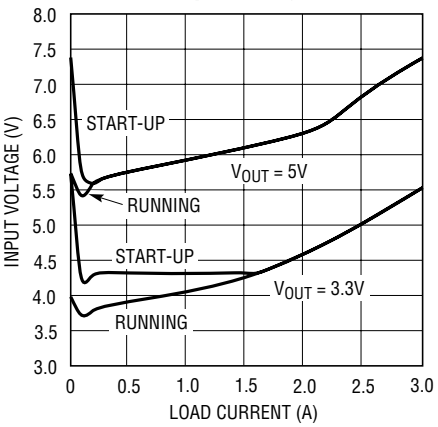
3435 G12

Switch On Voltage (V_{CESAT})



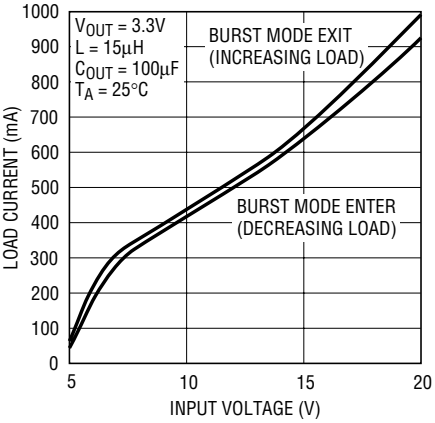
3435 G13

Minimum Input Voltage



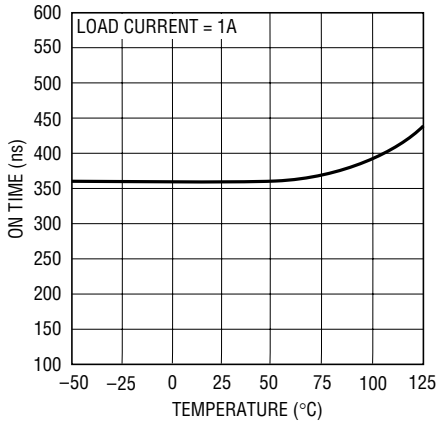
3435 G15

Burst Mode Threshold vs Input Voltage



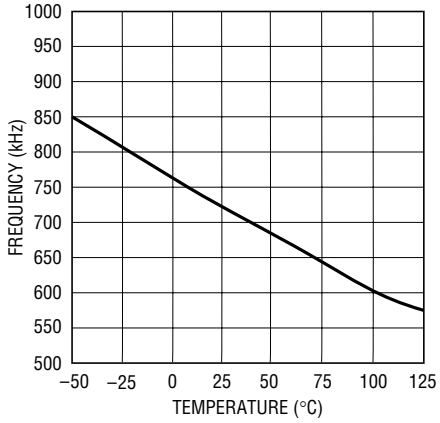
3435 G16

Minimum On-Time for Continuous Mode Operation



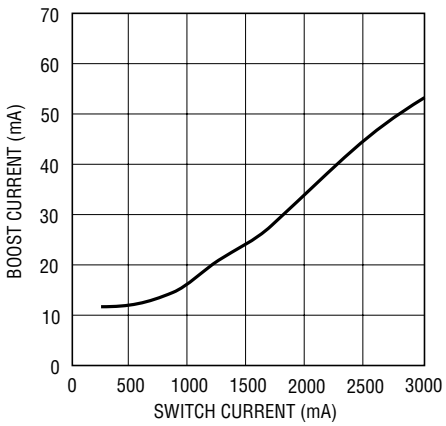
3435 G17

Maximum Synchronization Frequency vs Temperature



3435 G14

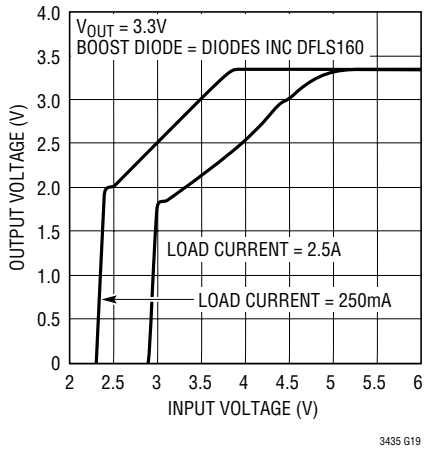
Boost Current vs Switch Current



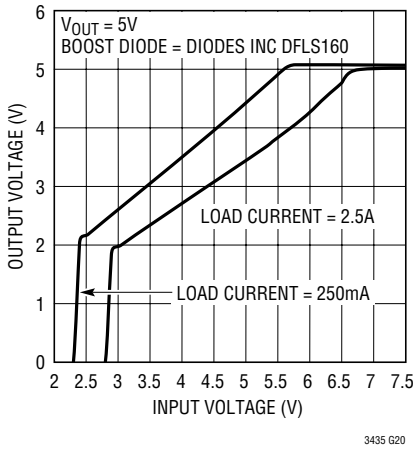
3435 G18

TYPICAL PERFORMANCE CHARACTERISTICS

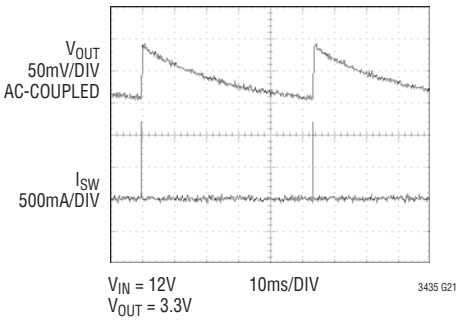
Dropout Operation



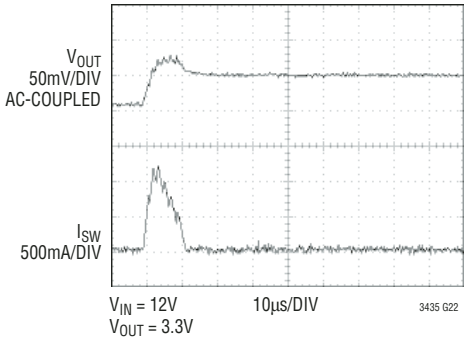
Dropout Operation



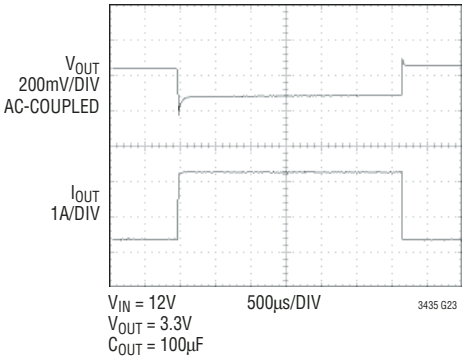
Burst Mode Operation



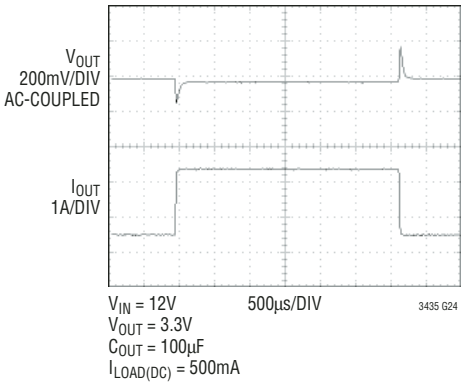
Burst Mode Operation



No Load 2A Step Response



Step Response



PIN FUNCTIONS

NC (Pin 1): No Connection.

SW (Pins 2, 5): The SW pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the SW pin negative during switch off time. Negative voltage is clamped with the external catch diode. Maximum negative switch voltage allowed is –0.8V.

V_{IN} (Pins 3, 4): This is the collector of the on-chip power NPN switch. V_{IN} powers the internal control circuitry when a voltage on the BIAS pin is not present. High di/dt edges occur on this pin during switch turn on and off. Keep the path short from the V_{IN} pin through the input bypass capacitor, through the catch diode back to SW. All trace inductance on this path will create a voltage spike at switch off, adding to the V_{CE} voltage across the internal NPN.

BOOST (Pin 6): The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional BOOST voltage allows the switch to saturate and its voltage loss approximates that of a 0.1Ω FET structure.

C_T (Pin 7): A capacitor on the C_T pin determines the amount of delay time between the PGFB pin exceeding its threshold (V_{PGFB}) and the PG pin set to a high impedance state.

PIN FUNCTIONS

When the PGFB pin rises above V_{PGFB}, current is sourced from the C_T pin into the external capacitor. When the voltage on the external capacitor reaches an internal clamp (V_{CT}), the PG pin becomes a high impedance node. The resultant PG delay time is given by $t = C_{CT} \bullet V_{CT}/I_{CT}$. If the voltage on the PGFB pin drops below V_{PGFB}, C_{CT} will be discharged rapidly to 0V and PG will be active low with a 200µA sink capability. If the C_T pin is clamped (Power Good condition) during normal operation and $\overline{SHDN}$ is taken low, the C_T pin will be discharged and a delay period will occur when $\overline{SHDN}$ is returned high. See the Power Good section in Applications Information for details.

GND (Pins 8, 17): The GND pin connection acts as the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND pin of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pin and the load ground. Keep the path between the GND pin and the load ground short and use a ground plane when possible. The GND pin also acts as a heat sink and should be soldered (along with the exposed leadframe) to the copper ground plane to reduce thermal resistance (see Applications Information).

C_{SS} (Pin 9): A capacitor from the C_{SS} pin to the regulated output voltage determines the output voltage ramp rate during start-up. When the current through the C_{SS} capacitor exceeds the C_{SS} threshold (I_{CSS}), the voltage ramp of the output is limited. The C_{SS} threshold is proportional to the FB voltage (see Typical Performance Characteristics) and is defeated for FB voltage greater than 0.9V (typical). See Soft-Start section in Applications Information for details.

BIAS (Pin 10): The BIAS pin is used to improve efficiency when operating at higher input voltages and light load current. Connecting this pin to the regulated output voltage forces most of the internal circuitry to draw its operating current from the output voltage rather than the input supply. This architecture increases efficiency especially when the input voltage is much higher than the output. Minimum output voltage setting for this mode of operation is 3V.

V_C (Pin 11): The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can also serve as a current clamp or control loop override. V_C sits at about 0.45V for light loads and 2.2V at maximum load. During the sleep portion of Burst Mode operation, the V_C pin is held at a voltage slightly below the burst threshold for better transient response. Driving the V_C pin to ground will disable switching and place the IC into sleep mode.

FB (Pin 12): The feedback pin is used to determine the output voltage using an external voltage divider from the output that generates 1.25V at the FB pin . When the FB pin drops below 0.9V, switching frequency is reduced, the SYNC function is disabled and output ramp rate control is enabled via the C_{SS} pin. See the Feedback section in Applications Information for details.

PGFB (PIN 13): The PGFB pin is the positive input to a comparator whose negative input is set at V_{PGFB}. When PGFB is taken above V_{PGFB}, current (I_{CSS}) is sourced into the C_T pin starting the PG delay period. When the voltage on the PGFB pin drops below V_{PGFB}, the C_T pin is rapidly discharged resetting the PG delay period. The PGFB voltage is typically generated by a resistive divider from the regulated output or input supply. See Power Good section in Applications Information for details.

SYNC (Pin 14): The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 5% and 75% duty cycle. The synchronizing range is equal to maximum initial operating frequency up to 700kHz. When the voltage on the FB pin is below 0.9V the SYNC function is disabled. See the Synchronizing section in Applications Information for details.

$\overline{SHDN}$ (Pin 15): The $\overline{SHDN}$ pin is used to turn off the regulator and to reduce input current to less than 1µA. The $\overline{SHDN}$ pin requires a voltage above 1.3V with a typical source current of 5µA to take the IC out of the shutdown state.

PG (Pin 16): The PG pin is functional only when the $\overline{SHDN}$ pin is above its threshold, and is active low when the internal clamp on the C_T pin is below its clamp level and high impedance when the clamp is active. The PG pin has a typical sink capability of 200µA. See the Power Good section in Applications Information for details.

BLOCK DIAGRAM

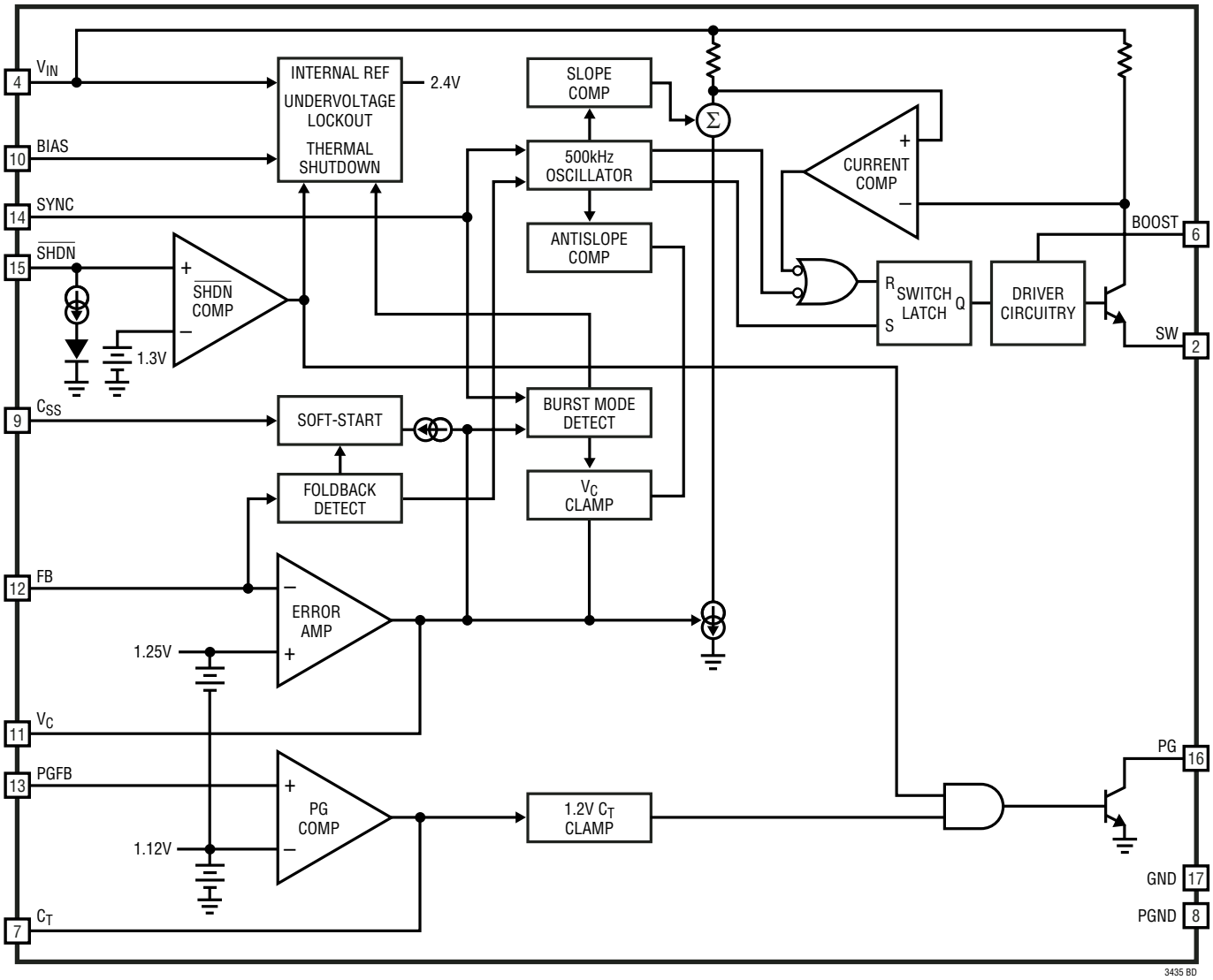


Figure 1. LT3435 Block Diagram

The LT3435 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the RS latch to turn the switch on. When switch current reaches a level set by the current comparator the latch is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

Most of the circuitry of the LT3435 operates from an internal 2.4V bias line. The bias regulator normally draws

BLOCK DIAGRAM

power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3V bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing switch to be saturated. This boosted voltage is generated with an external capacitor and diode.

To further optimize efficiency, the LT3435 automatically switches to Burst Mode operation in light load situations. In Burst Mode operation, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 45μA.

The LT3435 contains a power good flag with a programmable threshold and delay time. A logic-level low on the $\overline{SHDN}$ pin disables the IC and reduces input suppy current to less than 1μA.

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FEEDBACK PIN FUNCTIONS

The feedback (FB) pin on the LT3435 is used to set output voltage and provide several overload protection features. The first part of this section deals with selecting resistors to set output voltage and the remaining part talks about frequency foldback and soft-start features. Please read both parts before committing to a final design.

Referring to Figure 2, the output voltage is determined by a voltage divider from V_{OUT} to ground which generates 1.25V at the FB pin. Since the output divider is a load on the output care must be taken when choosing the resistor divider values. For light load applications the resistor values should be as large as possible to achieve peak efficiency in Burst Mode operation. Extremely large values for resistor R1 will cause an output voltage error due to the 50nA FB pin input current. The suggested value for the output divider resistor (see Figure 2) from FB to ground (R2) is 100k or less. A formula for R1 is shown below. A table of standard 1% values is shown in Table 1 for common output voltages.

$$R1 = R2 \bullet \frac{V_{OUT} - 1.25}{1.25 + R2 \bullet 50nA}$$

More Than Just Voltage Feedback

The FB pin is used for more than just output voltage sensing. It also reduces switching frequency and controls the soft-start voltage ramp rate when output voltage is below the regulated level (see the Frequency Foldback

Table 1

OUTPUT VOLTAGE (V)	R2 (kΩ, 1%)	R1 NEAREST (1%) (kΩ)	OUTPUT ERROR (%)
2.5	100	100	0
3	100	140	0
3.3	100	165	0.38
5	100	301	0.25
6	100	383	0.63
8	100	536	–0.63
10	100	698	–0.25
12	100	866	0.63

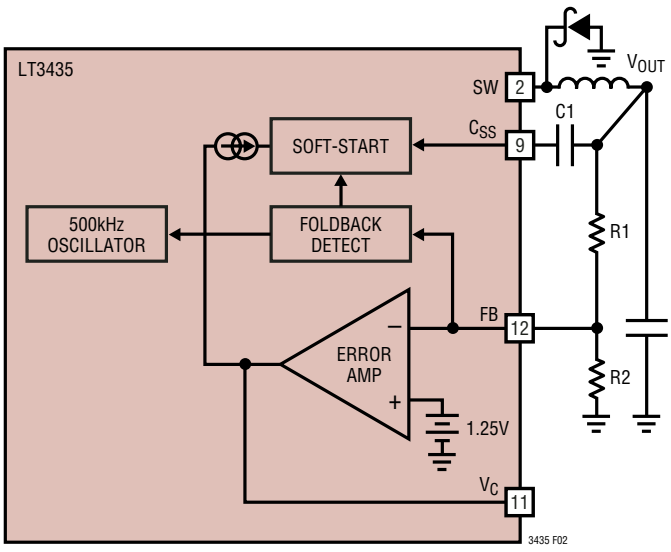

Figure 2. Feedback Network

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and Soft-Start Current graphs in Typical Performance Characteristics).

Frequency foldback is done to control power dissipation in both the IC and in the external diode and inductor during short-circuit conditions. A shorted output requires the switching regulator to operate at very low duty cycles. As a result the average current through the diode and inductor is equal to the short-circuit current limit of the switch (typically 4.7A for the LT3435). Minimum switch on time limitations would prevent the switcher from attaining a sufficiently low duty cycle if switching frequency were maintained at 500kHz, so frequency is reduced by about 4:1 when the FB pin voltage drops below 0.4V (see Frequency Foldback graph). In addition, if the current in the switch exceeds 1.5 times the current limitations specified by the V_C pin, due to minimum switch on time, the LT3435 will skip the next switch cycle. As the feedback voltage rises, the switching frequency increases to 500kHz with 0.95V on the FB pin. During frequency foldback, external syncronization is disabled to prevent interference with foldback operation. Frequency foldback does not affect operation during normal load conditions.

In addition to lowering switching frequency the soft-start ramp rate is also affected by the feedback voltage. Large capacitive loads or high input voltages can cause a high input current surge during start-up. The soft-start function reduces input current surge by regulating switch current via the V_C pin to maintain a constant voltage ramp rate (dV/dt) at the output. A capacitor (C1 in Figure 2) from the C_{SS} pin to the output determines the maximum output dV/dt. When the feedback voltage is below 0.4V, the V_C pin will rise, resulting in an increase in switch current and output voltage. If the dV/dt of the output causes the current through the C_{SS} capacitor to exceed I_{CSS} the V_C voltage is reduced resulting in a constant dV/dt at the output. As the feedback voltage increases I_{CSS} increases, resulting in an increased dV/dt until the soft-start function is defeated with 0.9V present at the FB pin. The soft-start function does not affect operation during normal load conditions. However, if a momentary short (brown out condition) is present at the output which causes the FB voltage to drop below 0.9V, the soft-start circuitry will become active.

INPUT CAPACITOR

Step-down regulators draw current from the input supply in pulses. The rise and fall times of these pulses are very fast. The input capacitor is required to reduce the voltage ripple this causes at the input of LT3435 and force the switching current into a tight local loop, thereby minimizing EMI. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = \frac{I_{OUT}}{V_{IN}} \sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}$$

Ceramic capacitors are ideal for input bypassing. At 500kHz switching frequency input capacitor values in the range of 4.7µF to 20µF are suitable for most applications. If operation is required close to the minimum input required by the LT3435 a larger value may be required. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

Input voltage transients caused by input voltage steps or by hot plugging the LT3435 to a pre-powered source such as a wall adapter can exceed maximum V_{IN} ratings. The sudden application of input voltage will cause a large surge of current in the input leads that will store energy in the parasitic inductance of the leads. This energy will cause the input voltage to swing above the DC level of input power source and it may exceed the maximum voltage rating of the input capacitor and LT3435. All input voltage transient sequences should be observed at the V_{IN} pin of the LT3435 to ensure that absolute maximum voltage ratings are not violated.

The easiest way to suppress input voltage transients is to add a small aluminum electrolytic capacitor in parallel with the low ESR input capacitor. The selected capacitor needs to have the right amount of ESR to critically damp the resonant circuit formed by the input lead inductance and the input capacitor. The typical values of ESR will fall in the range of 0.5Ω to 2Ω and capacitance will fall in the range of 5µF to 50µF.

If tantalum capacitors are used, values in the 22µF to 470µF range are generally needed to minimize ESR and meet ripple current and surge ratings. Care should be

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taken to ensure the ripple and surge ratings are not exceeded. The AVX TPS and Kemet T495 series are surge rated AVX recommends derating capacitor operating voltage by 2:1 for high surge applications.

OUTPUT CAPACITOR

The output capacitor is normally chosen by its effective series resistance (ESR) because this is what determines output ripple voltage. To get low ESR takes volume, so physically smaller capacitors have higher ESR. The ESR range for typical LT3435 applications is 0.05Ω to 0.2Ω. A typical output capacitor is an AVX type TPS, 100µF at 10V, with a guaranteed ESR less than 0.1Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. The value in microfarads is not particularly critical and values from 22µF to greater than 500µF work well, but you cannot cheat Mother Nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR and output ripple voltage could be unacceptable. Table 2 shows some typical solid tantalum surface mount capacitors.

Table 2. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR MAX (Ω)	RIPPLE CURRENT (A)
AVX TPS	0.1 to 0.3	0.7 to 1.1
D CASE SIZE		
AVX TPS	0.1 to 0.3	0.7 to 1.1
C CASE SIZE		
AVX TPS	0.2	0.5

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true and type TPS capacitors are specially tested for surge capability but surge ruggedness is not a critical issue with the output capacitor. Solid tantalum capacitors fail during very high turn-on surges which do not occur at the output of regulators. High discharge surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Unlike the input capacitor RMS, ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular with a typical value of $200mA_{RMS}$. The formula to calculate this is:

Output capacitor ripple current (RMS)

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{OUT})(V_{IN} - V_{OUT})}{(L)(f)(V_{IN})} = \frac{I_{P-P}}{\sqrt{12}}$$

CERAMIC CAPACITORS

Higher value, lower cost ceramic capacitors are now becoming available. They are generally chosen for their good high frequency operation, small size and very low ESR (effective series resistance). Low ESR reduces output ripple voltage but also removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this a resistor R_C can be placed in series with the V_C compensation capacitor C_C (Figure 10). Care must be taken however since this resistor sets the high frequency gain of the error amplifier including the gain at the switching frequency. If the gain of the error amplifier is high enough at the switching frequency output ripple voltage (although smaller for a ceramic output capacitor) may still affect the proper operation of the regulator. A filter capacitor C_F in parallel with the R_C/C_C network, along with a small feedforward capacitor C_{FB}, is suggested to control possible ripple at the V_C pin.

OUTPUT RIPPLE VOLTAGE

Figure 3 shows a typical output ripple voltage waveform for the LT3435. Ripple voltage is determined by the impedance of the output capacitor and ripple current through the inductor. Peak-to-peak ripple current through the inductor into the output capacitor is:

$$I_{P-P} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})(L)(f)}$$

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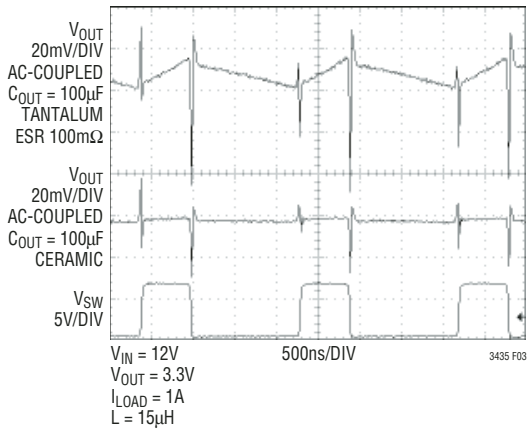

Figure 3. LT3435 Ripple Voltage Waveform

For high frequency switchers the ripple current slew rate is also relevant and can be calculated from:

$$\frac{di}{dt} = \frac{V_{IN}}{L}$$

Peak-to-peak output ripple voltage is the sum of a triwave created by peak-to-peak ripple current times ESR and a square wave created by parasitic inductance (ESL) and ripple current slew rate. Capacitive reactance is assumed to be small compared to ESR or ESL.

$$V_{RIPPLE} = \left(I_{P-P}\right)\left(ESR\right) + \left(ESL\right)\frac{di}{dt}$$

Example: with V_{IN} = 12V, V_{OUT} = 3.3V, L = 15µH, ESR = 0.08Ω, ESL = 10nH:

$$I_{P-P} = \frac{\left(3.3\right)\left(12-3.3\right)}{\left(12\right)\left(15e-6\right)\left(500e3\right)} = 0.319A$$

$$\frac{di}{dt} = \frac{12}{15e-6} = 0.8e6$$

$$V_{RIPPLE} = (0.319A)(0.08) + (10e-9)(0.8e6)$$
$$= 0.026 + 0.008 = 34mV_{P-P}$$

MAXIMUM OUTPUT LOAD CURRENT

Maximum load current for a buck converter is limited by the maximum switch current rating (I_{PK}). The current rating for the LT3435 is 3A. Unlike most current mode converters, the LT3435 maximum switch current limit does not fall off at high duty cycles. Most current mode converters suffer a drop off of peak switch current for duty cycles above 50%. This is due to the effects of slope compensation required to prevent subharmonic oscillations in current mode converters. (For detailed analysis, see Application Note 19.)

The LT3435 is able to maintain peak switch current limit over the full duty cycle range by using patented circuitry to cancel the effects of slope compensation on peak switch current without affecting the frequency compensation it provides.

Maximum load current would be equal to maximum switch current for an infinitely large inductor, but with finite inductor size, maximum load current is reduced by one-half peak-to-peak inductor current. The following formula assumes continuous mode operation, implying that the term on the right ($I_{P-P}/2$) is less than I_{OUT}.

$$I_{OUT(MAX)} = I_{PK} - \frac{\left(V_{OUT}\right)\left(V_{IN}-V_{OUT}\right)}{2\left(L\right)\left(f\right)\left(V_{IN}\right)} = I_{PK} - \frac{I_{P-P}}{2}$$

Discontinuous operation occurs when:

$$I_{OUT(DIS)} \le \frac{V_{OUT}\left(V_{IN}-V_{OUT}\right)}{2(L)(f)(V_{IN})}$$

For V_{OUT} = 5V, V_{IN} = 8V and L = 15µH:

$$I_{OUT(MAX)} = 3 - \frac{\left(5\right)\left(8-5\right)}{2\left(15e-6\right)\left(500e3\right)\left(8\right)}$$
$$= 3 - 0.125 = 2.875A$$

Note that there is less load current available at the higher input voltage because inductor ripple current increases. At V_{IN} = 15V, duty cycle is 33% and for the same set of conditions:

$$I_{OUT(MAX)} = 3 - \frac{\left(5\right)\left(15-5\right)}{2\left(15e-6\right)\left(500e3\right)\left(15\right)}$$
$$= 3 - 0.22 = 2.88A$$

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To calculate actual peak switch current in continuous mode with a given set of conditions, use:

$$I_{SW(PK)} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2\left(L\right)\left(f\right)\left(V_{IN}\right)}$$

If a small inductor is chosen which results in discontinous mode operation over the entire load range, the maximum load current is equal to:

$$I_{OUT(MAX)} = \frac{I_{PK}{}^{2}2\left(f\right)\left(L\right)\left(V_{IN}\right)}{2\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}$$

CHOOSING THE INDUCTOR

For most applications the output inductor will fall in the range of 5µH to 33µH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the LT3435 switch, which has a 3A limit. Higher values also reduce output ripple voltage and reduce core loss.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation and of course cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Choose a value in microhenries such that the maximum load current plus half of the inductor ripple current is less than the minimum peak switch current (I_{PK}). Choosing a small inductor with lighter loads may result in discontinuous mode of operation, but the LT3435 is designed to work well in either mode.

   Assume that the average inductor current is equal to load current and decide whether or not the inductor must withstand continuous fault conditions. If maximum load current is 1A, for instance, a 1A inductor may not survive a continuous 4A overload condition.

Table 3. Inductor Selection Criteria

VENDOR/ PART NO.	VALUE (µH)	$I_{DC(MAX)}$ (Amps)	DCR (Ohms)	HEIGHT (mm)
Sumida				
CDRH104R-4R7	4.7	6	0.013	4
CDRH104R-100	10	4.4	0.035	4
CDRH104R-150	15	3.6	0.050	4
CDRH104R-220	22	2.9	0.073	4
CDRH104R-330	33	2.3	0.093	4
CDRH124-4R7	4.7	5.7	0.015	4.5
CDRH124-100	10	4.5	0.026	4.5
CDRH124-220	22	2.9	0.066	4.5
CDRH124R-330	33	2.7	0.097	4.5
CDRH127-330	33	3.0	0.065	8
CEI122-220	22	2.3	0.085	34
Coiltronics				
UP3B-4R7	4.7	6.5	0.0083	6.8
UP3B-4R7	10	4.3	0.026	6.8
UP3B-330	33	3	0.069	6.8

   For applications with a duty cycle above 50%, the inductor value should be chosen to obtain an inductor ripple current of less than 40% of the peak switch current.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall somewhere in between. The following formula assumes continuous mode of operation, but it errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2\left(f\right)\left(L\right)\left(V_{IN}\right)}$$

   V_{IN} = maximum input voltage

   f = switching frequency, 500kHz

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3. Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.
4. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology's applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Short-Circuit Considerations

The LT3435 is a current mode controller. It uses the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 2.2V, then acts as an output switch peak current limit. This action becomes the switch current limit specification. The maximum available output power is then determined by the switch current limit.

A potential controllability problem could occur under short-circuit conditions. If the power supply output is short circuited, the feedback amplifier responds to the low output voltage by raising the control voltage, V_C, to its peak current limit value. Ideally, the output switch would be turned on, and then turned off as its current exceeded the value indicated by V_C. However, there is finite response time involved in both the current comparator and turn-off of the output switch. These result in a minimum on time $t_{ON(MIN)}$. When combined with the large ratio of V_{IN} to $(V_F + I \bullet R)$, the diode forward voltage plus inductor I • R voltage drop, the potential exists for a loss of control. Expressed mathematically the requirement to maintain control is:

$$f \bullet t_{ON} \leq \frac{V_F + I \bullet R}{V_{IN}}$$

where:

f = switching frequency

t_{ON} = switch on time

V_F = diode forward voltage

V_{IN} = Input voltage

I • R = inductor I • R voltage drop

If this condition is not observed, the current will not be limited at I_{PK} but will cycle-by-cycle ratchet up to some higher value. Using the nominal LT3435 clock frequency of 500kHz, a V_{IN} of 12V and a $(V_F + I \bullet R)$ of say 0.7V, the maximum t_{ON} to maintain control would be approximately 116ns, an unacceptably short time.

The solution to this dilemma is to slow down the oscillator to allow the current in the inductor to drop to a sufficiently low value such that the current doesn't continue to ratchet higher. When the FB pin voltage is abnormally low thereby indicating some sort of short-circuit condition, the oscillator frequency will be reduced. Oscillator frequency is reduced by a factor of 4 when the FB pin voltage is below 0.4V and increases linearly to its typical value of 500kHz at a FB voltage of 0.95V (see Typical Performance Characteristics). In addition, if the current in the switch exceeds 1.5 • I_{PK} current demanded by the V_C pin, the LT3435 will skip the next on cycle effectively reducing the oscillator frequency by a factor of 2. These oscillator frequency reductions during short-circuit conditions allow the LT3435 to maintain current control.

SOFT-START

For applications where $[V_{IN}/(V_{OUT} + V_F)]$ ratios > 10 or large input surge currents can't be tolerated, the LT3435 soft-start feature should be used to control the output capacitor charge rate during start-up, or during recovery from an output short circuit thereby adding additional control over peak inductor current. The soft-start function limits the switch current via the V_C pin to maintain a constant voltage ramp rate (dV/dt) at the output capacitor. A capacitor (C1 in Figure 2) from the C_{SS} pin to the regulated output voltage determines the output voltage

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ramp rate. When the current through the C_{SS} capacitor exceeds the C_{SS} threshold (I_{CSS}), the voltage ramp of the output capacitor is limited by reducing the V_C pin voltage. The C_{SS} threshold is proportional to the FB voltage (see Typical Performance Characteristics) and is defeated for FB voltages greater than 0.9V (typical). The output dV/dt can be approximated by:

$$\frac{dV}{dt} = \frac{I_{CSS}}{C_{SS}}$$

but actual values will vary due to start-up load conditions, compensation values and output capacitor selection.

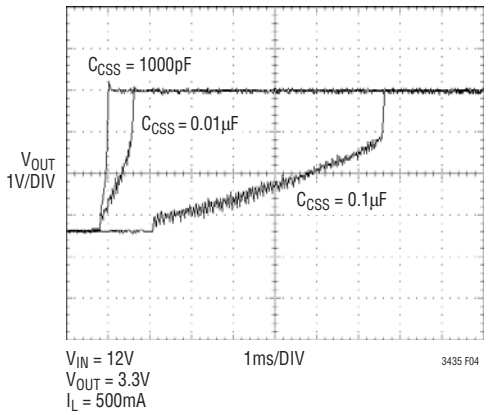

Figure 4. V_{OUT} dV/dt

Burst Mode OPERATION

To enhance efficiency at light loads, the LT3435 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3435 delivers short bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 45µA and 125µA respectively during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LT3435 operates in sleep mode increases and the average input current is greatly reduced resulting in higher efficiency.

The minimum average input current depends on the V_{IN} to V_{OUT} ratio, V_C frequency compensation, feedback divider network and Schottky diode leakage. It can be approximated by the following equation:

$$I_{IN(AVG)} \cong I_{VINS} + I_{SHDN} + \left(\frac{V_{OUT}}{V_{IN}}\right)\frac{\left(I_{BIASS} + I_{FB} + I_S\right)}{\left(\eta\right)}$$

where

I_{VINS} = input pin current in sleep mode

V_{OUT} = output voltage

V_{IN} = input voltage

I_{BIASS} = BIAS pin current in sleep mode

I_{FB} = feedback network current

I_S = catch diode reverse leakage at V_{OUT}

η = low current efficiency (non Burst Mode operation)

Example: For V_{OUT} = 3.3V, V_{IN} = 12V

$$I_{IN(AVG)} = 45\mu A + 5\mu A + \left(\frac{3.3}{12}\right)\frac{(125\mu A + 12.5\mu A + 0.5\mu A)}{(0.8)}$$

$$= 45\mu A + 5\mu A + 44\mu A = 99\mu A$$

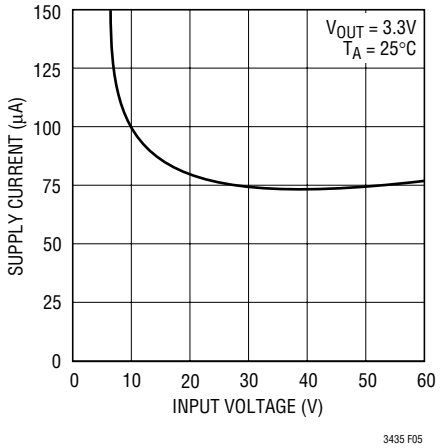

Figure 5. I_Q vs V_{IN}

During the sleep portion of the Burst Mode Cycle, the V_C pin voltage is held just below the level need for normal operation to improve transient response. See the Typical Performance Characteristics section for burst and transient response waveforms.

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If a no load condition can be anticipated, the supply current can be further reduced by cycling the $\overline{SHDN}$ pin at a rate higher than the natural no load burst frequency. Figure 6 shows Burst Mode operation with the $\overline{SHDN}$ pin. V_{OUT} burst ripple is maintained while the average supply current drops to 15µA. The $\overline{PG}$ pin will be active low during the "on" portion of the $\overline{SHDN}$ waveform due to the C_T capacitor discharge when $\overline{SHDN}$ is taken low. See the Power Good section for further information.

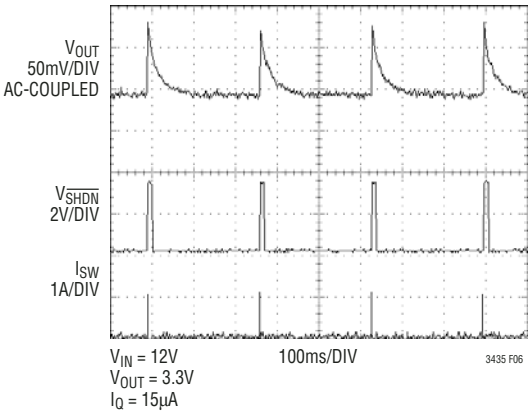

Figure 6. Burst Mode with Shutdown Pin

CATCH DIODE

The catch diode carries load current during the SW off time. The average diode current is therefore dependent on the switch duty cycle. At high input to output voltage ratios the diode conducts most of the time. As the ratio approaches unity the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short circuited. Under this condition the diode must safely handle I_{PEAK} at maximum duty cycle.

To maximize high and low load current efficiency a fast switching diode with low forward drop and low reverse leakage should be used. Low reverse leakage is critical to maximize low current efficiency since its value over temperature can potentially exceed the magnitude of the LT3435 supply current. Low forward drop is critical for high current efficiency since the loss is proportional to forward drop.

These requirements result in the use of a Schottky type diode. DC switching losses are minimized due to its low forward voltage drop and AC behavior is benign due to its lack of a significant reverse recovery time. Schottky diodes are generally available with reverse voltage ratings of 60V and even 100V and are price competitive with other types.

Table 4. Catch Diode Selection Criteria

	LEAKAGE V_{OUT} = 3.3V		V_F AT 1A		I_Q at 125°C V_{IN} =12V V_{OUT} = 3.3	EFFICIENCY V_{IN} =12V V_{OUT} = 3.3V
DIODE	25°C	125°C	25°C	125°C	I_L = 0A	I_L = 1A
IR 10BQ100	0.0µA	59µA	0.72V	0.58V	125µA	74.7%
Diodes Inc. B260SMA	0.1µA	242µA	0.48V	0.41V	215µA	81.7%
Diodes Inc. B360SMB	0.2µA	440µA	0.45V	0.36V	270µA	82.4%
IR MBRS360TR	1µA	1.81mA	0.42V	0.34V	821µA	82.7%
IR 30BQ100	1.7µA	2.64mA	0.40V	0.32V	1088µA	81.1%

The effect of reverse leakage and forward drop on efficiency for various Schottky diodes is shown in Table 4. As can be seen these are conflicting parameters and the user must weigh the importance of each specification in choosing the best diode for the application.

The use of so-called "ultrafast" recovery diodes is generally not recommended. When operating in continuous mode, the reverse recovery time exhibited by "ultrafast" diodes will result in a slingshot type effect. The power internal switch will ramp up V_{IN} current into the diode in an attempt to get it to recover. Then, when the diode has finally turned off, some tens of nanoseconds later, the V_{SW} node voltage ramps up at an extremely high dV/dt, perhaps 5V to even 10V/ns! With real world lead inductances the V_{SW} node can easily overshoot the V_{IN} rail. This can result in poor RFI behavior and, if the overshoot is severe enough, damage the IC itself.

BOOST PIN

For most applications the boost components are a 0.33µF capacitor and a MMSD914 diode. The anode is typically connected to the regulated output voltage to generate a voltage approximately V_{OUT} above V_{IN} to drive the output stage (Figure 7a). However, the output stage discharges the boost capacitor during the on time of the switch. The output driver requires at least 2.5V of headroom throughout this period to keep the switch fully saturated. If the

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output voltage is less than 3.3V it is recommended that an alternate boost supply is used. The boost diode can be connected to the input (Figure 7b) but care must be taken to prevent the boost voltage (V_{BOOST} = V_{IN} • 2) from exceeding the BOOST pin absolute maximum rating. The additional voltage across the switch driver also increases power loss and reduces efficiency. If available, an independent supply can be used to generate the required BOOST voltage (Figure 7c). Tying BOOST to V_{IN} or an independent supply may reduce efficiency but it will reduce the minimum V_{IN} required to start-up with light loads. If the generated BOOST voltage dissipates too much power at maximum load, the BOOST voltage the LT3435 sees can be reduced by placing a Zener diode in series with the BOOST diode (Figure 7a option).

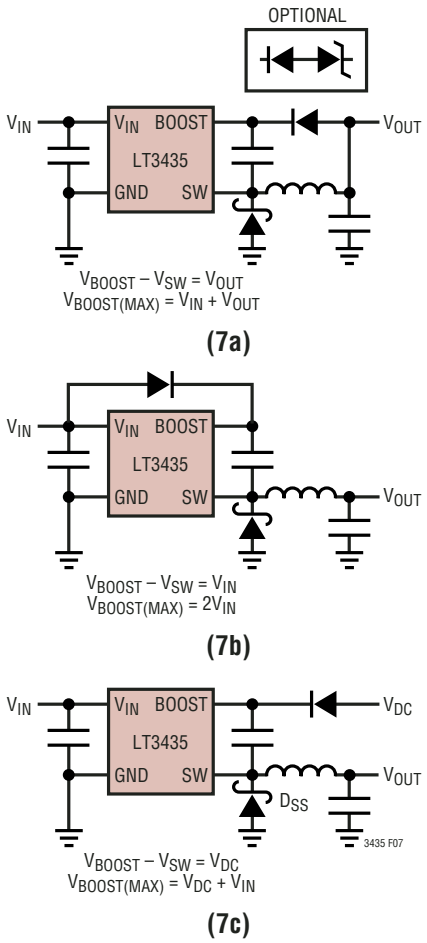

Figure 7. BOOST Pin Configurations

A 0.33µF boost capacitor is recommended for most applications. Almost any type of film or ceramic capacitor is suitable but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The capacitor value is derived from worst-case conditions of 1700ns on time, TBD boost current and 0.7V discharge ripple. The boost capacitor value could be reduced under less demanding conditions but this will not improve circuit operation or efficiency. Under low input voltage and low load conditions a higher value capacitor will reduce discharge ripple and improve start-up operation.

SHUTDOWN FUNCTION AND UNDERVOLTAGE LOCKOUT

The $\overline{SHDN}$ pin on the LT3435 controls the operation of the IC. When the voltage on the $\overline{SHDN}$ pin is below the 1.2V shutdown threshold the LT3435 is placed in a "zero" supply current state. Driving the $\overline{SHDN}$ pin above the shutdown threshold enables normal operation. The $\overline{SHDN}$ pin has an internal sink current of 3µA.

In addition to the shutdown feature, the LT3435 has an undervoltage lockout function. When the input voltage is below 2.4V, switching will be disabled. The undervoltage lockout threshold doesn't have any hysteresis and is mainly used to insure that all internal voltages are at the correct level before switching is enabled. If an undervoltage lockout function with hysteresis is needed to limit input current at low V_{IN} to V_{OUT} ratios refer to Figure 8 and the following:

$$V_{UVLO} = R1\left(\frac{V_{\overline{SHDN}}}{R3} + \frac{V_{\overline{SHDN}}}{R2} + I_{\overline{SHDN}}\right) + V_{\overline{SHDN}}$$

$$V_{HYST} = \frac{V_{OUT}(R1)}{R3}$$

R1 should be chosen to minimize quiescent current during normal operation by the following equation:

$$R1 = \frac{V_{IN} - 2V}{(1.5)(I_{\overline{SHDN}(MAX)})}$$

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Example:

$$R1 = \frac{12 - 2}{1.5(5\mu A)} = 1.3M\Omega$$

$$R3 = \frac{5(1.3M\Omega)}{1} = 6.5M\Omega \text{ (Nearest 1\% } 6.49M\Omega)$$

$$R2 = \frac{1.3}{\frac{7 - 1.3}{1.3M\Omega} - 1\mu A - \frac{1.3}{6.49M\Omega}}$$

$$= 408k \text{ (Nearest 1\% } 412k)$$

See the Typical Performance Characteristics section for graphs of $\overline{SHDN}$ and V_{IN} currents verses input voltage.

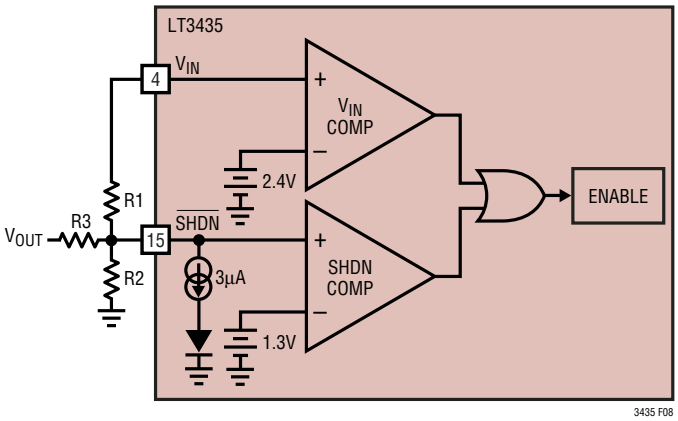

Figure 8. Undervoltage Lockout

SYNCHRONIZING

Oscillator synchronization to an external input is achieved by connecting a TTL logic-compatible square wave with a duty cycle between 5% and 75% to the LT3435 SYNC pin. The synchronizing range is equal to initial operating frequency up to 700kHz. This means that minimum practical sync frequency is equal to the worst-case high self-oscillating frequency (575kHz), not the typical operating frequency of 300kHz. Caution should be used when synchronizing above 575kHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

If the FB pin voltage is below 0.9V (power-up or output short-circuit conditions) the sync function is disabled. This allows the frequency foldback to operate to avoid and hazardous conditions for the SW pin.

If the synchronization signal is present during Burst Mode operation, synchronization will occur during the burst portion of the output waveform. Synchronizing the LT3435 during Burst Mode operation may alter the natural burst frequency which can lead to jitter and increased ripple in the burst waveform.

If no synchronization is required this pin should be connected to ground.

POWER GOOD

The LT3435 contains a power good block which consists of a comparator, delay timer and active low flag that allows the user to generate a delayed signal after the power good threshold is exceeded.

Referring to Figure 2, the PGFB pin is the positive input to a comparator whose negative input is set at V_{PGFB}. When PGFB is taken above V_{PGFB}, current (I_{CSS}) is sourced into the C_T pin starting the delay period. When the voltage on the PGFB pin drops below V_{PGFB} the C_T pin is rapidly discharged resetting the delay period. The PGFB voltage is typically generated by a resistive divider from the regulated output or input supply.

The capacitor on the C_T pin determines the amount of delay time between the PGFB pin exceeding its threshold (V_{PGFB}) and the PG pin set to a high impedance state. When the PGFB pin rises above V_{PGFB} current is sourced (I_{CT}) from the C_T pin into the external capacitor. When the voltage on the external capacitor reaches an internal clamp (V_{CT}), the PG pin becomes a high impedance node. The resultant PG delay time is given by $t = C_{CT} \bullet (V_{CT})/(I_{CT})$. If the voltage on the PGFB pin drops below its V_{PGFB}, C_{CT} will be discharged rapidly and PG will be active low with a 200µA sink capability. If the $\overline{SHDN}$ pin is taken below its

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threshold during normal operation, the C_T pin will be discharged and PG inactive, resulting in a non Power Good cycle when $\overline{SHDN}$ is taken above its threshold. Figure 9 shows the power good operation with PGFB connected to FB and the capacitance on C_T = 0.1µF. The PGOOD pin has a limited amount of drive capability and is susceptible to noise during start-up and Burst Mode operation. If erratic operation occurs during these conditions a small filter capacitor from the PGOOD pin to ground will ensure proper operation. Figure 10 shows several different configurations for the LT3435 Power Good circuitry. Figure 10 shows several different configurations for the LT3435 Power Good circuitry.

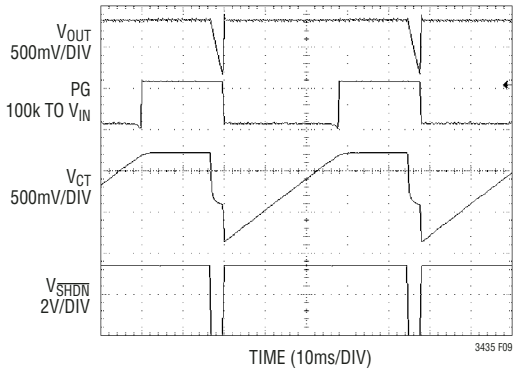
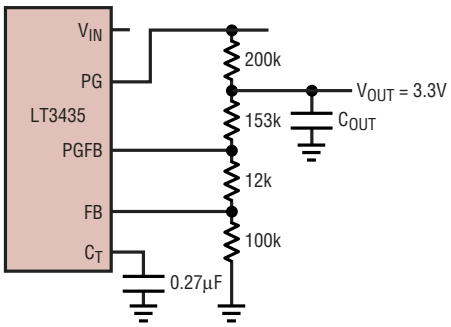


Figure 9. Power Good

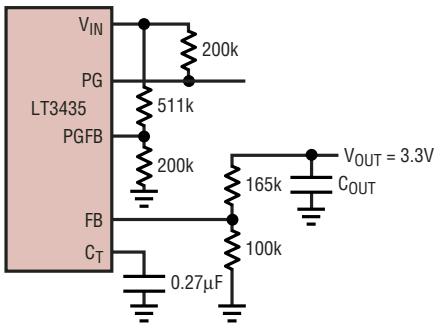
LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For maximum efficiency switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted the high speed switching current path, shown in Figure 11, must be kept as short as possible. This is implemented in the suggested layout of Figure 12. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this

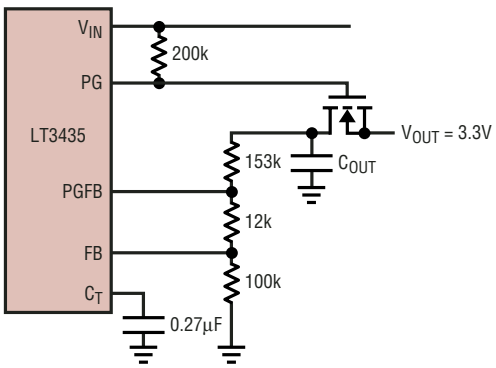
PG at 80% V_{OUT} with 100ms Delay



PG at V_{IN} > 4V with 100ms Delay



V_{OUT} Disconnect at 80% V_{OUT} with 100ms Delay



V_{OUT} Disconnect 3.3V Logic Signal with 100µs Delay

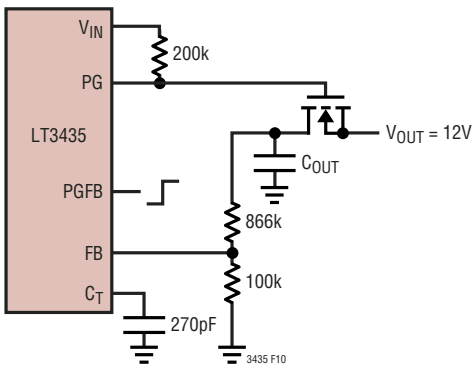


Figure 10. Power Good Circuits

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parasitic inductance produces a flyback spike across the LT3435 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the LT3435 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

The V_C and FB components should be kept as far away as possible from the switch and boost nodes. The LT3435 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. Pin 8 and the exposed die pad, Pin 17, are a continuous copper plate that runs under the LT3435 die. This is the best thermal path for heat out of the package. Reducing the thermal resistance from Pin 8 and exposed pad onto the board will reduce die temperature and increase the power capability of the LT3435. This is achieved by providing as much copper area as possible around the exposed pad. Adding multiple solder filled feedthroughs under and around this pad to an internal ground plane will also help. Similar treatment to the catch diode and coil terminations will reduce any additional heating effects.

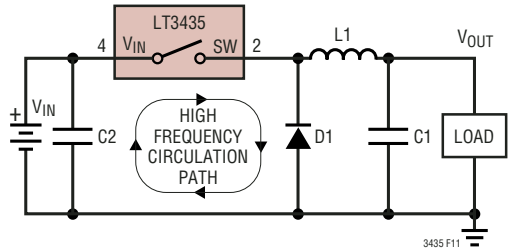

Figure 11. High Speed Switching Path

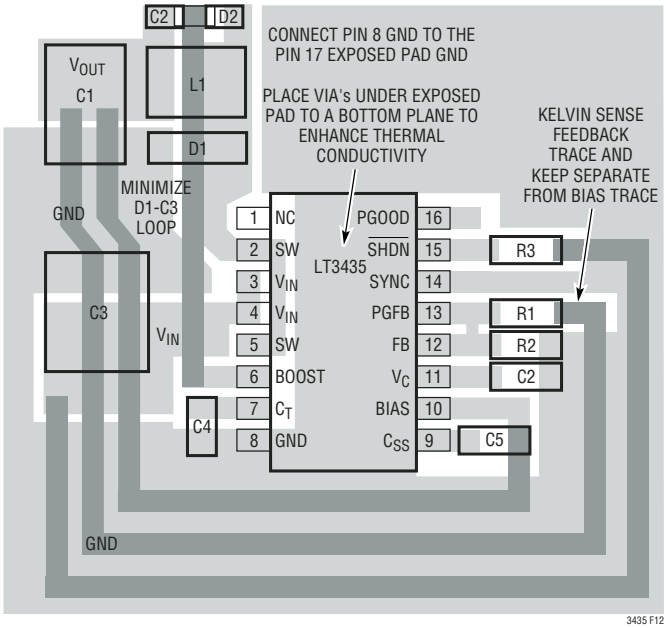

Figure 12. Suggested Layout

THERMAL CALCULATIONS

Power dissipation in the LT3435 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}\left(I_{OUT}\right)^2\left(V_{OUT}\right)}{V_{IN}} + t_{EFF}\left(1/2\right)\left(I_{OUT}\right)\left(V_{IN}\right)\left(f\right)$$

Boost current loss:

$$P_{BOOST} = \frac{\left(V_{OUT}\right)^2\left(I_{OUT}/46\right)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}\,(0.0026) + V_{OUT}\,(0.001)$$

R_{SW} = switch resistance (≈0.15 when hot)

t_{EFF} = effective switch current/voltage overlap time

$(t_r + t_f + t_{IR} + t_{IF})$

$t_r = (V_{IN}/1.2)$ns

$t_f = (V_{IN}/1.7)$ns

$t_{IR} = t_{IF} = (I_{OUT}/0.2)$ns

f = switch frequency

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Example: with V_{IN} = 25V, V_{OUT} = 5V and I_{OUT} = 2A:

$$P_{SW} = \frac{(0.15)(2)^2(5)}{25} + \left(77e^{-9}\right)(1/2)(2)(25)(500e3)$$

$$0.12 + 0.962 = 1.08$$

$$P_{BOOST} = \frac{(5)^2(2/40)}{40} = 0.03W$$

$$P_Q = 40(0.0026) + 5(0.001) = 0.11W$$

Total power dissipation is:

P_{TOT} = 1.08 + 0.03+ 0.11 = 1.22W

Thermal resistance for the LT3435 package is influenced by the presence of internal or backside planes. With a full plane under the FE16 package, thermal resistance will be about 45°C/W. No plane will increase resistance to about 150°C/W. To calculate die temperature, use the proper thermal resistance number for the desired package and add in worst-case ambient temperature:

$T_J = T_A + Q_{JA} (P_{TOT})$

With the FE16 package (Q_{JA} = 45°C/W) at an ambient temperature of 70°C:

T_J = 70 + 45(1.22) = 125°C

Input Voltage vs Operating Frequency Considerations

The absolute maximum input supply voltage for the LT3435 is specified at 60V. This is based solely on internal semiconductor junction breakdown effects. Due to internal power dissipation the actual maximum V_{IN} achievable in a particular application may be less than this.

A detailed theoretical basis for estimating internal power loss is given in the section Thermal Considerations. Note that AC switching loss is proportional to both operating frequency and output current. The majority of AC switching loss is also proportional to the square of input voltage.

For example, while the combination of V_{IN} = 40V, V_{OUT} = 5V at 2A and f_{OSC} = 500kHz may be easily achievable, simultaneously raising V_{IN} to 60V and f_{OSC} to 700kHz is not possible. Nevertheless, input voltage transients up to 60V can usually be accommodated, assuming the resulting increase in internal dissipation is of insufficient time duration to raise die temperature significantly.

A second consideration is controllability. A potential limitation occurs with a high step-down ratio of V_{IN} to V_{OUT}, as this requires a correspondingly narrow minimum switch on time. An approximate expression for this (assuming continuous mode operation) is given as follows:

$t_{ON(MIN)} = V_{OUT} + V_F/V_{IN}(f_{OSC})$

where:

V_{IN} = input voltage

V_{OUT} = output voltage

V_F = Schottky diode forward drop

f_{OSC} = switching frequency

A potential controllability problem arises if the LT3435 is called upon to produce an on time shorter than it is able to produce. Feedback loop action will lower then reduce the V_C control voltage to the point where some sort of cycle-skipping or Burst Mode behavior is exhibited.

In summary:

1. Be aware that the simultaneous requirements of high V_{IN}, high I_{OUT} and high f_{OSC} may not be achievable in practice due to internal dissipation. The Thermal Considerations section offers a basis to estimate internal power. In questionable cases a prototype supply should be built and exercised to verify acceptable operation.
2. The simultaneous requirements of high V_{IN}, low V_{OUT} and high f_{OSC} can result in an unacceptably short minimum switch on time. Cycle skipping and/or Burst Mode behavior will result causing an increase in output voltage ripple while maintaining the correct output voltage.

FREQUENCY COMPENSATION

Before starting on the theoretical analysis of frequency response the following should be remembered—the worse the board layout, the more difficult the circuit will be to stabilize. This is true of almost all high frequency analog circuits. Read the Layout Considerations section first. Common layout errors that appear as stability problems are distant placement of input decoupling capacitor and/or

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catch diode and connecting the V_C compensation to a ground track carrying significant switch current. In addition the theoretical analysis considers only first order non-ideal component behavior. For these reasons, it is important that a final stability check is made with production layout and components.

The LT3435 uses current mode control. This alleviates many of the phase shift problems associated with the inductor. The basic regulator loop is shown in Figure 12. The LT3435 can be considered as two g_m blocks, the error amplifier and the power stage.

Figure 13 shows the overall loop response with a 330pF V_C capacitor and a typical 100µF tantalum output capacitor. The response is set by the following terms:

Error amplifier: DC gain is set by g_m and R_O:

EA Gain = 650µ℧ • 1.5M = 975

The pole set by C_F and R_L:

EA Pole = 1/(2π • 1.5M • 470pF) = 220Hz

Unity gain frequency is set by C_F and g_m:

EA Unity Gain Frequency = 650µF/(2π • 470pF)

= 220kHz

Powerstage: DC gain is set by g_m and R_L (assume 10Ω):

PS DC Gain = 6 • 10 = 60

Pole set by C_{OUT} and R_L:

PS Pole = 1/(2π • 100µF • 10) = 159Hz

Unity gain set by C_{OUT} and g_m:

PS Unity Gain Freq = 6/(2π • 100µF) = 94kHz.

Tantalum output capacitor zero is set by C_{OUT} and C_{OUT} ESR

Output Capacitor Zero = 1/(2π • 100µF • 0.1) = 15.9kHz

The zero produced by the ESR of the tantalum output capacitor is very useful in maintaining stability. If better transient response is required, a zero can be added to the loop using a resistor (R_C) in series with the compensation

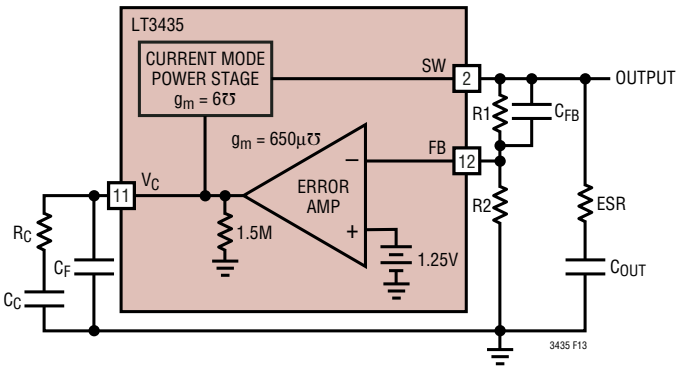


Figure 13. Model for Loop Response

capacitor. As the value of R_C is increased, transient response will generally improve but two effects limit its value. First, the combination of output capacitor ESR and a large R_C may stop loop gain rolling off altogether. Second, if the loop gain is not rolled off sufficiently at the switching frequency output ripple will perturb the V_C pin enough to cause unstable duty cycle switching similar to subharmonic oscillation. This may not be apparent at the output. Small-signal analysis will not show this since a continuous time system is assumed.

When checking loop stability the circuit should be operated over the application's full voltage, current and temperature range. Any transient loads should be applied and the output voltage monitored for a well-damped behavior.

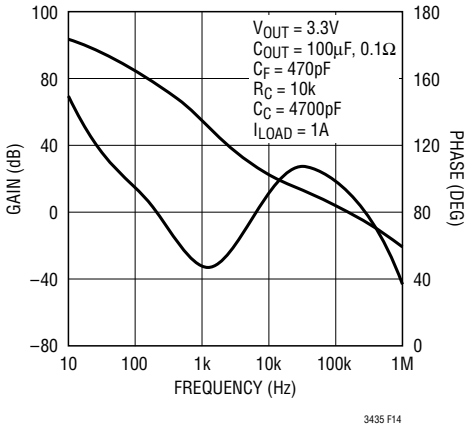
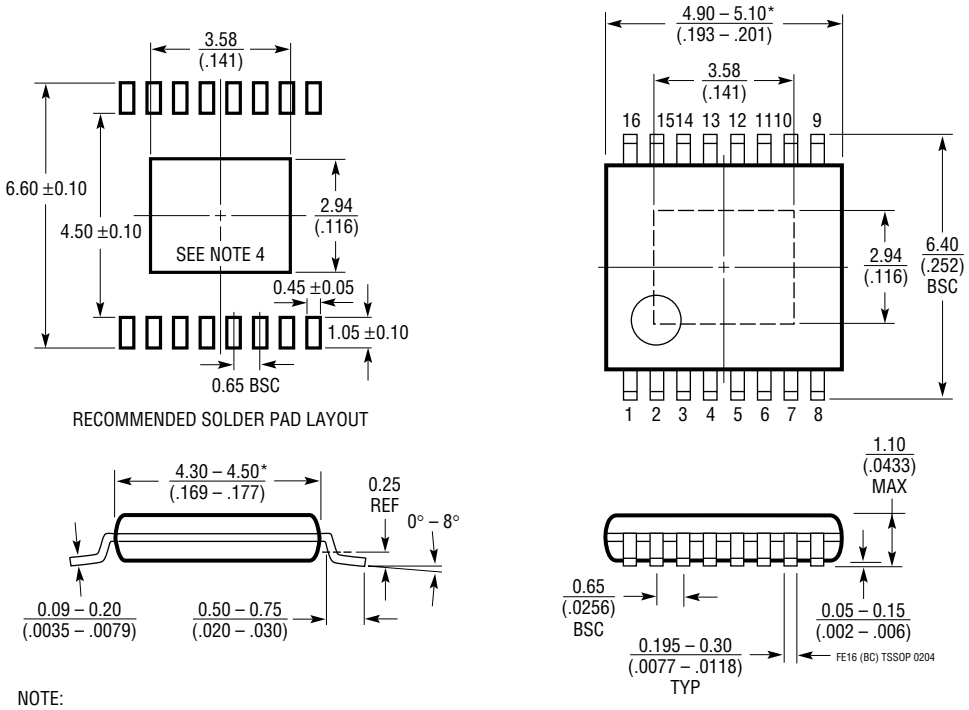


Figure 14. Overall Loop Response

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1074/LT1074HV	4.4A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converters	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$ = 2.21V, I_Q = 8.5mA, I_{SD} < 10µA, DD5/7, TO220-5/7
LT1076/LT1076HV	1.6A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converters	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$ = 2.21V, I_Q = 8.5mA, I_{SD} < 10µA, DD5/7, TO220-5/7
LT1676	60V, 550mA (I_{SW}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 2.5µA, S8
LT1765	25V, 3A (I_{SW}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 15µA, SO-8, TSSOP16E
LT1766	60V, 1.5A (I_{SW}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1767	25V, 1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 6µA, MS8/E
LT1776	40V, 550mA (I_{SW}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 30µA, N8, S8
LTC®1875	1.5A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 15µA, I_{SD} < 1µA, TSSOP16
LT1940	Dual 1.4A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 3.8mA, MS10
LT1956	60V, 1.5A (I_{SW}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1976	60V, 1.5A (I_{SW}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA
LT1977	60V, 1.5A (I_{SW}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA
LT3010	80V, 50mA, Low Noise Linear Regulator	V_{IN}: 1.5V to 80V, $V_{OUT(MIN)}$ = 1.28V, I_Q = 30µA, I_{SD} < 1µA, MS8E
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, MS10
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E
LT3430	60V, 3A (I_{SW}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 30µA, TSSOP16E
LT3431	60V, 3A (I_{SW}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 30µA, TSSOP16E
LT3433	60V, 400mA (I_{OUT}), 200kHz, Buck-Boost DC/DC Converter	V_{IN}: 5V to 60V, V_{OUT}: 3.3V to 20V, I_Q = 100µA, TSSOP-16E
LT3434	60V, 3A (I_{SW}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA
LTC3727/LTC3727-1	36V, 500kHz, High Efficiency Step-Down DC/DC Controllers	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 670µA, I_{SD} < 20µA, QFN-32, SSOP-28

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