WINSOURCE ELECTRONICS

THE DATASHEET OF

UF28150J

UF28150J

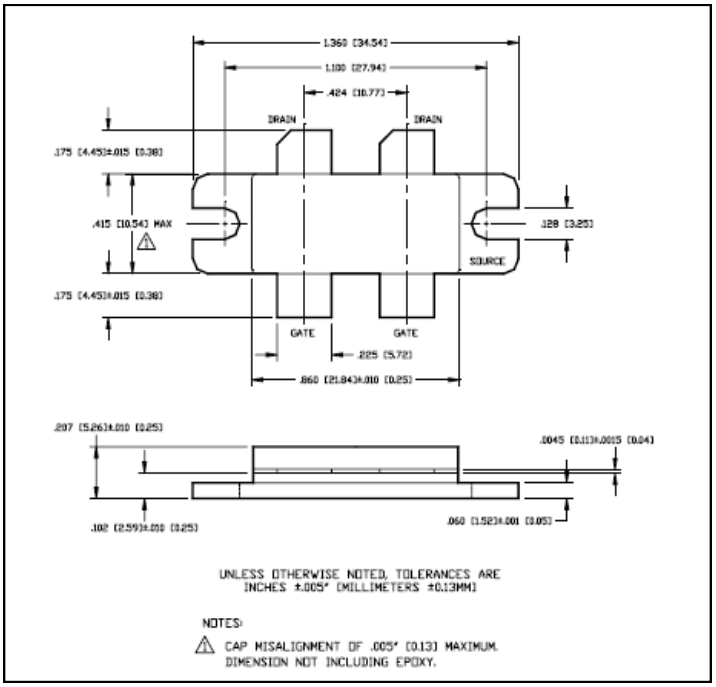
RF Power MOSFET Transistor
150 W, 100 - 500 MHz, 28 V

Rev. V1

Features

- DMOS structure
- Lower capacitance for broadband operation
- Common source configuration

Package Outline



ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	16*	A
Power Dissipation	P_D	389	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance	Θ_{JC}	0.45	°C/W

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these maximum limits.
3. At 25°C Tcase, unless noted.

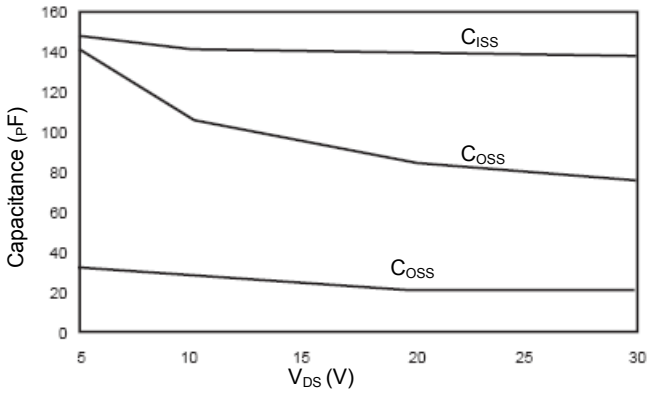
ELECTRICAL SPECIFICATIONS: 25°C

Parameter	Test Conditions	Units	Min.	Max.
Drain-Source Breakdown Voltage	V_{GS} = 0.0 V, I_{DS} = 20.0 mA*	BV_{DSS}	65	—
Drain-Source Leakage Current	V_{DS} = 28.0 V, V_{GS} = 0.0V*	I_{DSS}	—	4.0
Gate-Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0.0 V*	I_{GSS}	—	4.0
Gate Threshold Voltage	V_{DS} = 10.0 V, I_{DS} = 400.0 mA*	$V_{GS(TH)}$	2.0	6.0
Forward Transconductance	V_{DS} = 10.0 V, I_{DS} = 4000.0 mA, ΔV_{GS} = 1.0 V, 80µs pulse*	G_M	2.0	—
Input Capacitance	V_{DS} = 28.0V, F = 1.0 MHz*	C_{ISS}	—	180
Output Capacitance	V_{DS} = 28.0V, F = 1.0 MHz*	C_{OSS}	—	120
Reverse Capacitance	V_{DS} = 28.0V, F = 1.0 MHz*	C_{RSS}	—	32
Power Gain	V_{DD} = 28.0 V, I_{DQ} = 400.0 mA, P_{OUT} = 150.0 W, F = 500 MHz	G_P	8	—
Drain Efficiency	V_{DD} = 28.0 V, I_{DQ} = 400.0 mA, P_{OUT} = 150.0 W, F = 500 MHz	η_D	55	—
Load Mismatch Tolerance	V_{DD} = 28.0 V, I_{DQ} = 400.0 mA, P_{OUT} = 150.0 W, F = 500 MHz	VSWR-T	—	10:1**

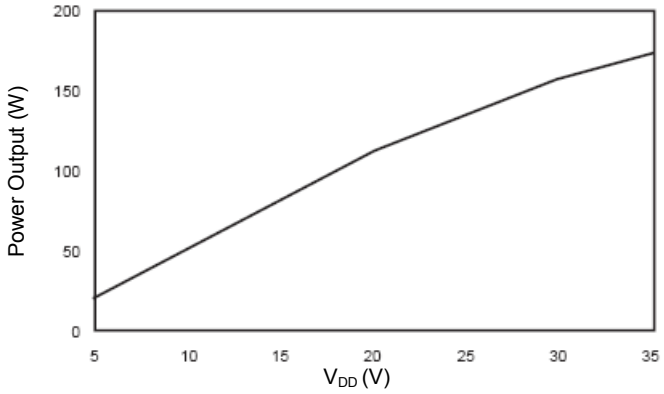
Notes:
* Per side
** At all phase angles

Typical Broadband Performance Curves

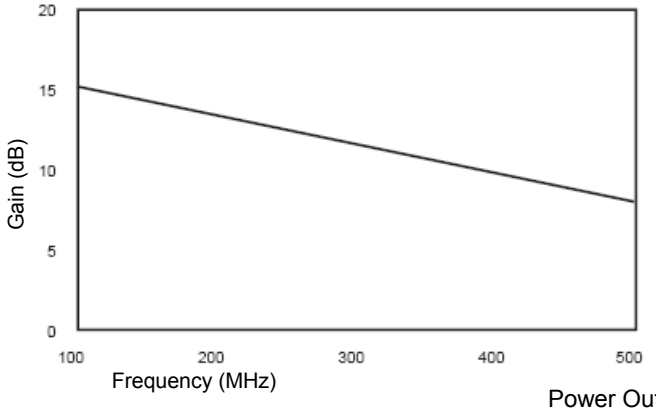
Capacitance vs Voltage
F=1.0 MHz



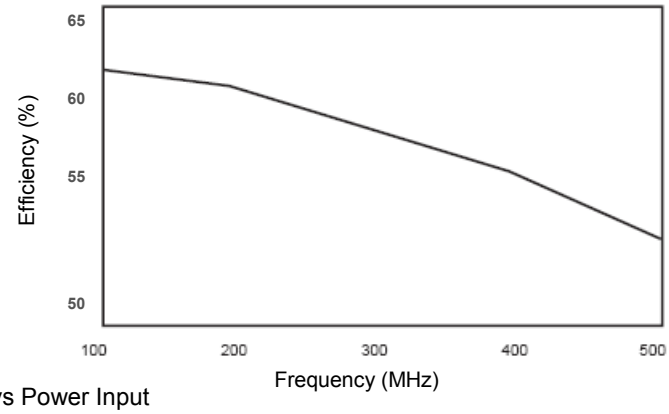
Power Output vs Voltage
P_{IN} =24 W I_{DQ} =400 mA F=500 MHz



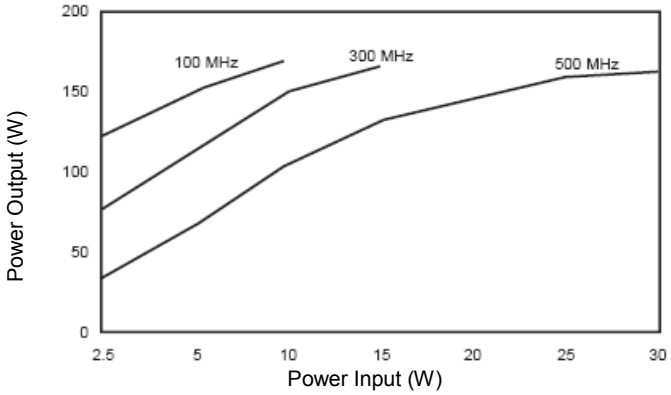
Gain vs Frequency
V_{DD} =28V P_{OUT} =100W I_{DQ} =400mA



Efficiency vs Frequency
V_{DD} =28W I_{DQ} =400mA P_{OUT} =150W



Power Output vs Power Input
V_{DD} =28W I_{DQ} =400mA



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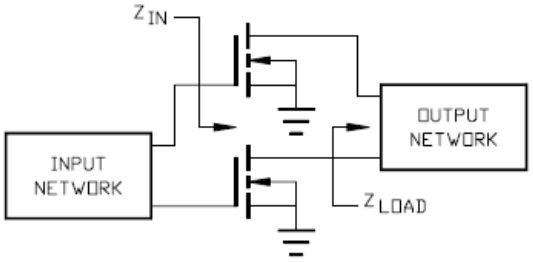
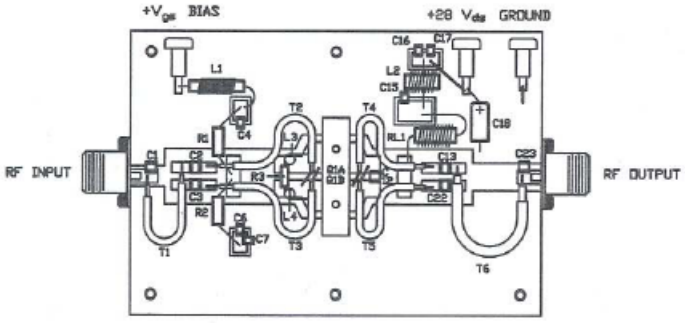
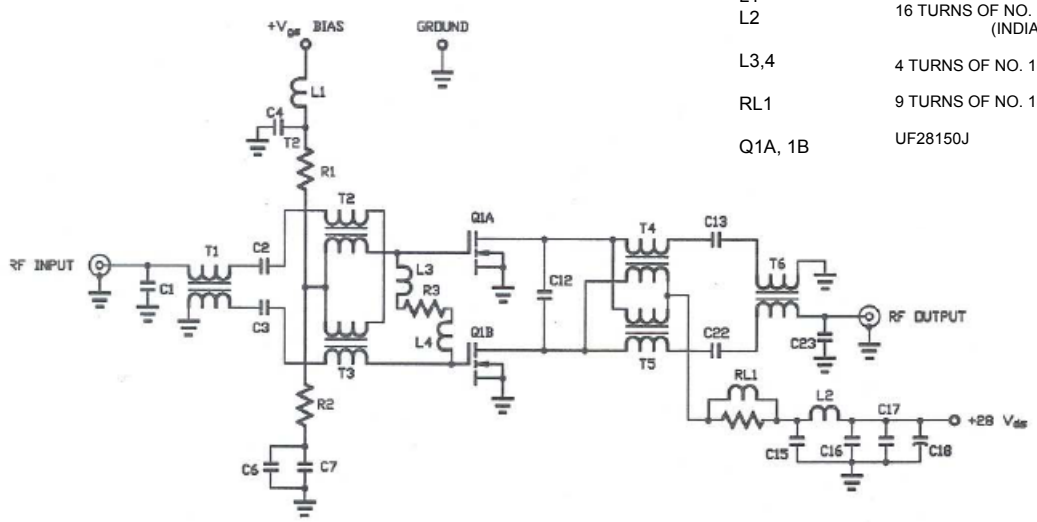
TYPICAL OPTIMUM DEVICE IMPEDANCES

F (MHz)	Z_{IN} (Ω)	Z_{LOAD} (Ω)
100	3.7 - j5.9	3.0 - j0.7
300	2.7 - j5.9	2.6 - j0.55
500	2.5 - j2.9	2.5 - j0.5
V_{DD} = 28V, I_{DQ} = 400mA, P_{OUT} = 150W		







PARTS LIST

C23	1.0pF
C1	9.1pF
C12	11pF
C2, 3, 13, 22	270pF
C7,16	680pF
C4,6,15,17	.015uF
C18	50uF 50V
R1	11K OHM .25 W. 10%
R2	47 OHM .05 W. 10%
R3	12 OHM .25 W. 10%
T1	2.50" OF 50 OHM (.85" OD) SEMI-RIGID CABLE
T2,3,4,5	2.50" OF 10 OHM (.70" OD) SEMI-RIGID CABLE
T6	2.50" OF 50 OHM (.141" OD) SEMI-RIGID CABLE
L1	5uH
L2	16 TURNS OF NO. 18 AWG ON TORID CORE (INDIANA GENERAL F6278-Q1)
L3,4	4 TURNS OF NO. 18 AWG ON .125 DIAMETER
RL1	9 TURNS OF NO. 18 AWG ON 15 OHM 2 W. 10% RESISTOR
Q1A, 1B	UF28150J

HANDLING PROCEDURES: STATIC SENSITIVITY

Please observe the following precautions to avoid damage:
DMOS devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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