



**THE DATASHEET OF
IPB160N04S203ATMA4**

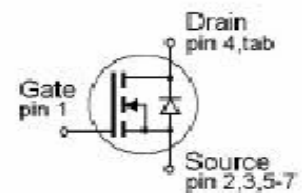


OptiMOS[®] - T Power-Transistor
Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low R_{DS(on)}
- 100% Avalanche tested

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	2.9	mΩ
I_D	160	A

PG-TO263-7-3


Type	Package	Ordering Code	Marking
IPB160N04S2-03	PG-TO263-7-3	SP0002-18151	P2N0403

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	160	A
		$T_C=100\text{ °C}^{2)}$	160	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	640	
Avalanche energy, single pulse	E_{AS}	$I_D=80\text{A}$	810	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	2.1	3.0	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=60\text{ A},$ SMD version	-	2.4	2.9	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	5300	-	pF
Output capacitance	C_{oss}		-	2150	-	
Reverse transfer capacitance	C_{rss}		-	580	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=160\text{ A}, R_G=2.2\ \Omega$	-	27	-	ns
Rise time	t_r		-	45	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	t_f		-	32	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32\text{ V}, I_D=160\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	27	30	nC
Gate to drain charge	Q_{gd}		-	46	75	
Gate charge total	Q_g		-	123	170	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	160	A
Diode pulse current	$I_{S,pulse}$		-	-	640	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.84	1.3	V

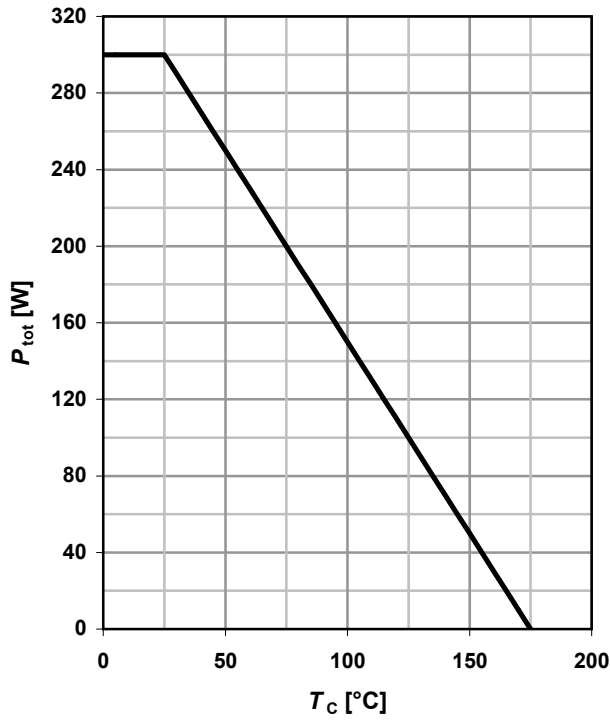
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.5\text{K/W}$ the chip is able to carry 235A at 25°C. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

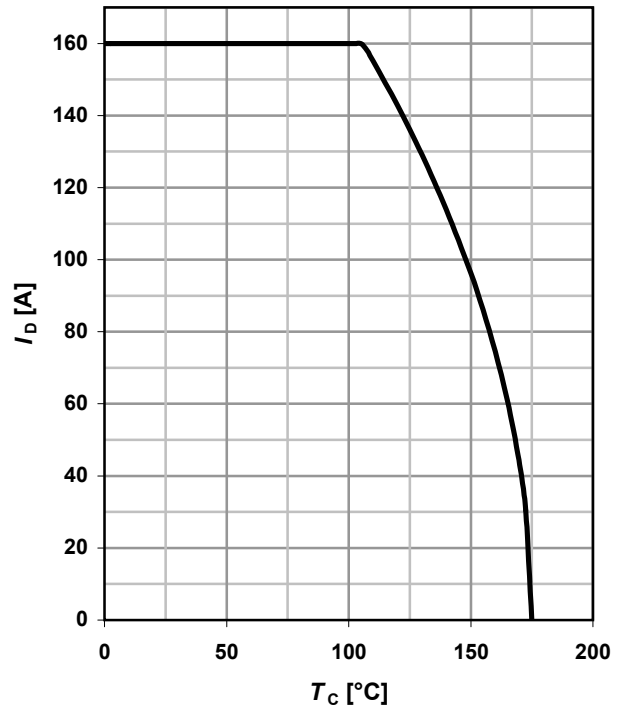
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

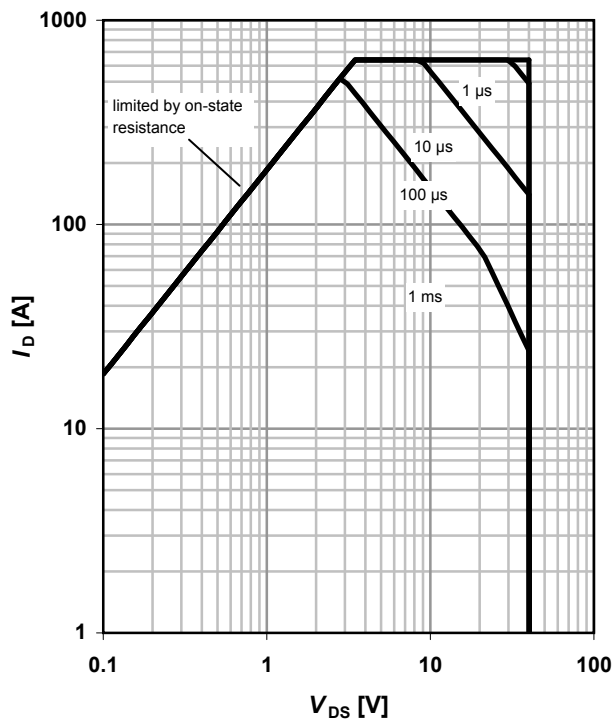
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

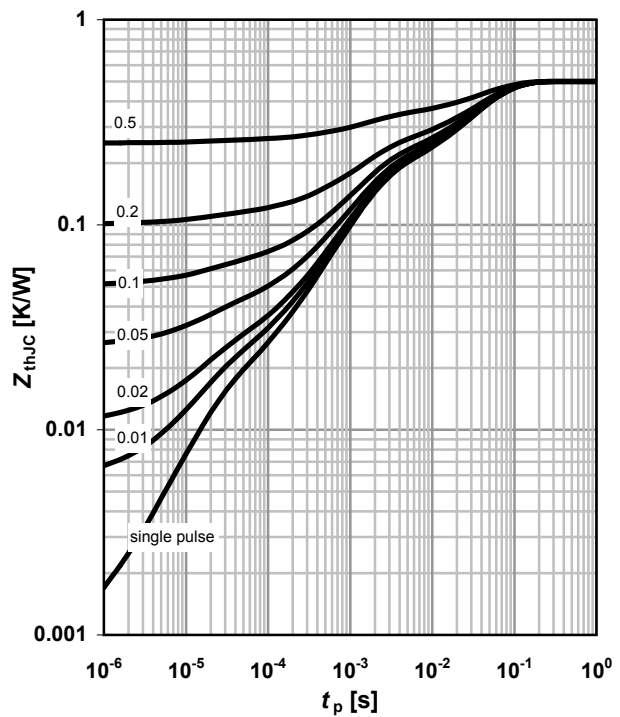
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

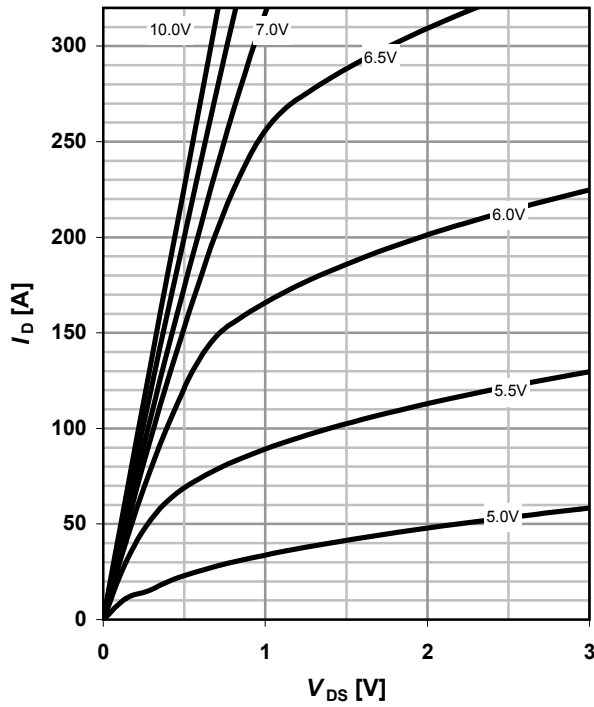
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

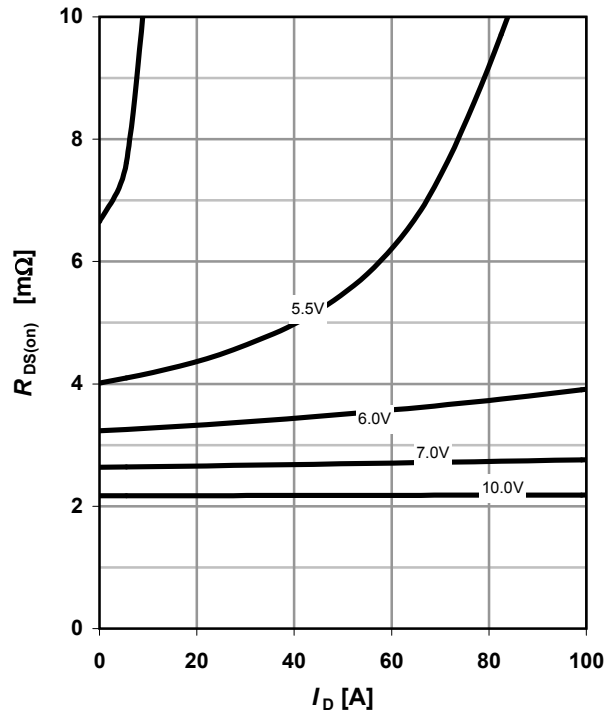
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

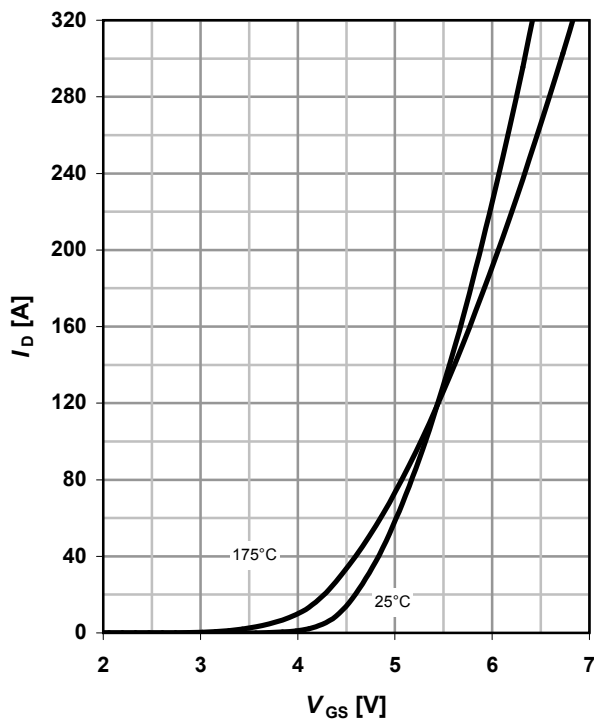
parameter: V_{GS}



7 Typ. transfer characteristics

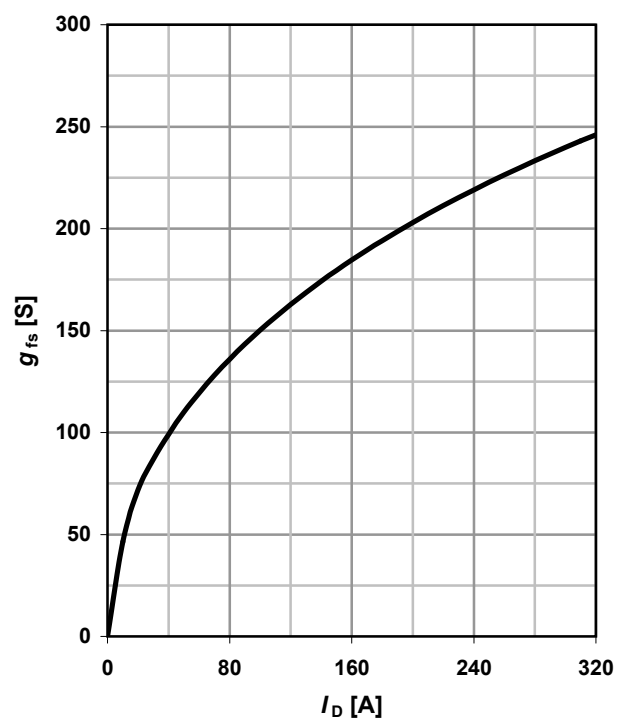
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



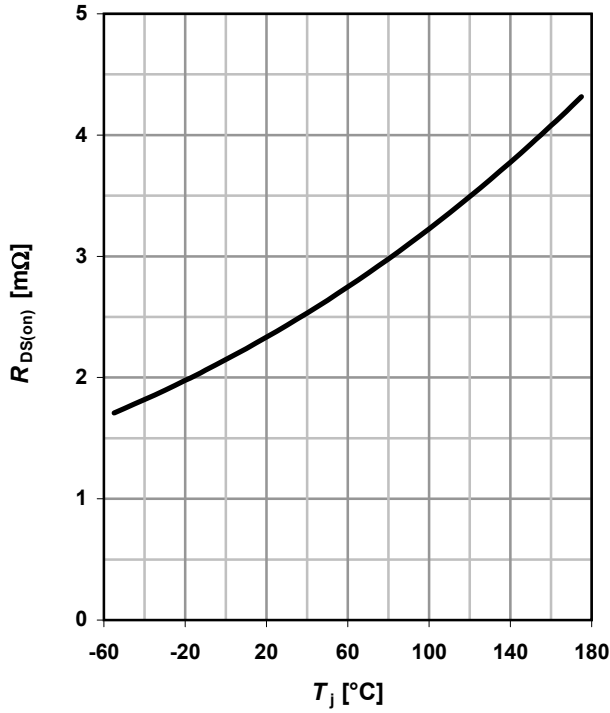
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

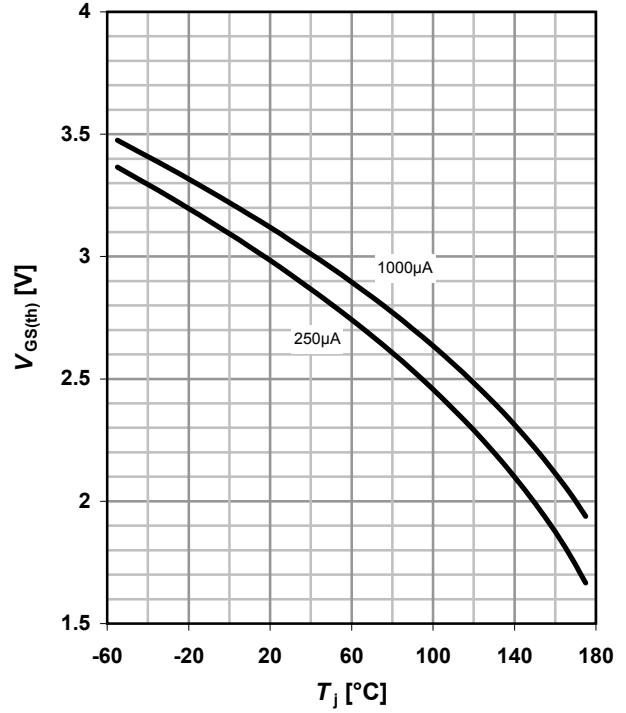
$R_{DS(on)}=f(T_j)$; $I_D=80\text{ A}$; $V_{GS}=10\text{ V}$



10 Typ. gate threshold voltage

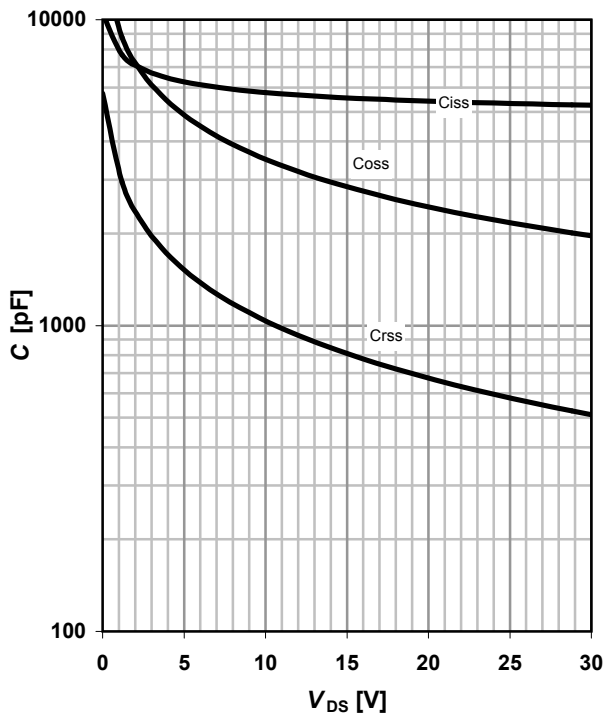
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

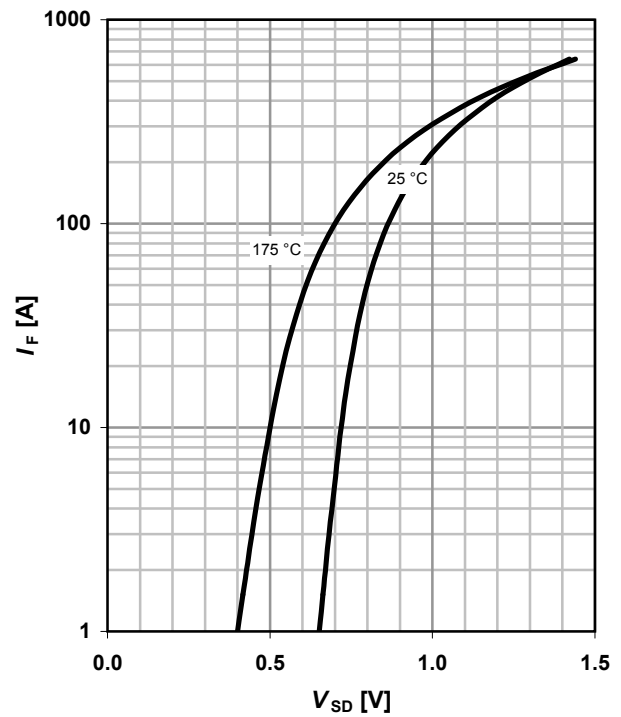
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$



12 Typ. Forward characteristics of reverse diode

$I_F=f(V_{SD})$

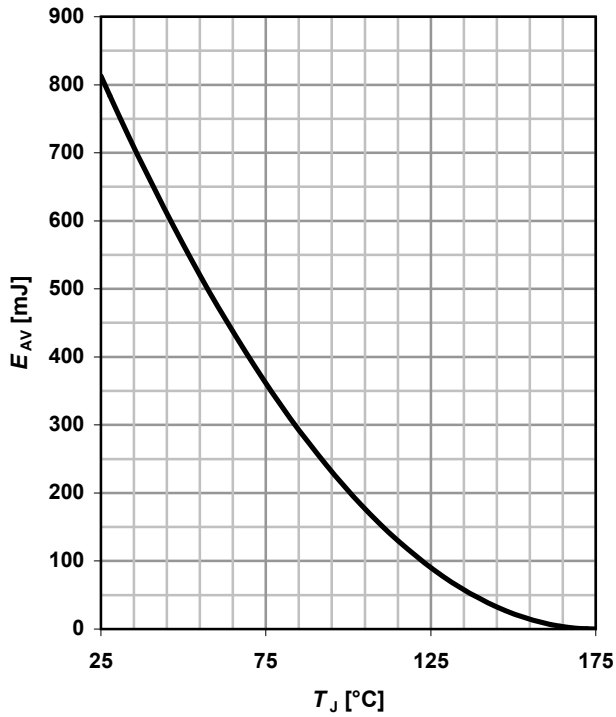
parameter: T_j



13 Typ. avalanche energy

$E_{AS}=f(T_J)$

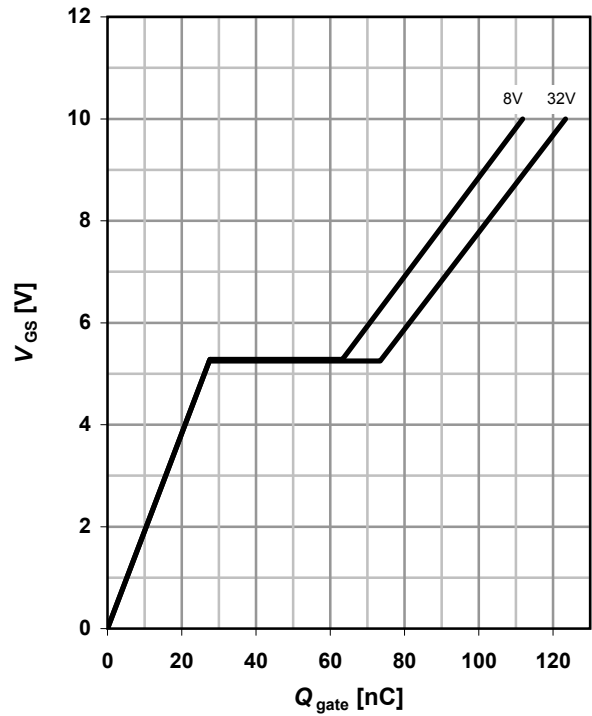
parameter: $I_D=80A, V_{DD}=25V$



14 Typ. gate charge

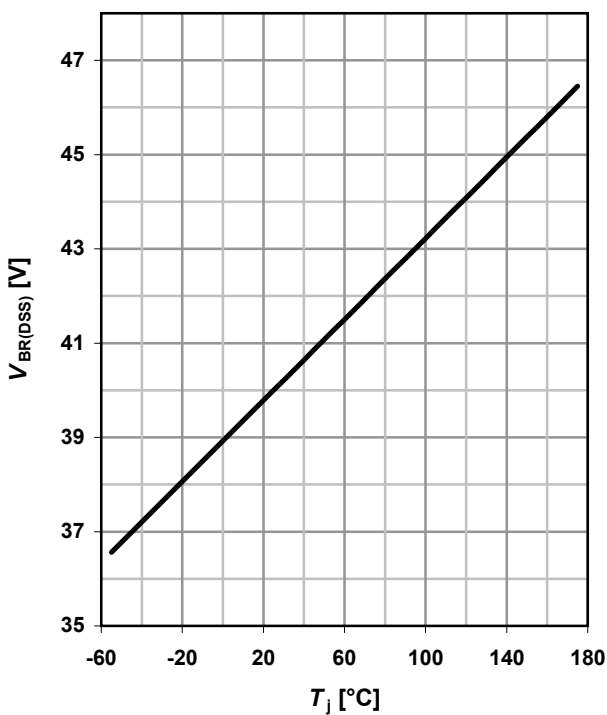
$V_{GS}=f(Q_{gate}); I_D=160A$ pulsed

parameter: V_{DD}

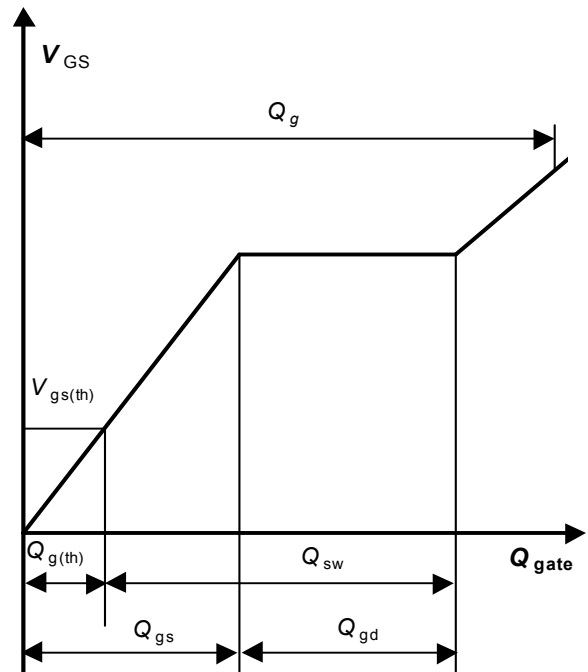


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1$ mA



16 Gate charge waveforms



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