



**THE DATASHEET OF
EVAL-ADUM3221AEBZ**



*i*Coupler ADuM3221EBZ, 4 A Output-Isolated Gate Driver Evaluation Board

FEATURES

Isolated dual-channel gate driver with [ADuM3220/ADuM3221](#)
4 A peak output current
High frequency operation: 1 MHz maximum
CMOS input logic levels
2.5 kV rms isolation
Supports TO-263 or TO-252 IGBT/MOSFETs

SUPPORTED *i*Coupler® MODELS

[ADuM3220](#)
[ADuM3221](#)

GENERAL DESCRIPTION

The EVAL-ADuM3221EBZ supports the [ADuM3220/ADuM3221](#) isolated gate drivers. It is compatible with IGBT/MOSFETs in TO-263 or TO-252 packages. The evaluation board is ideal for evaluating the ADuM322x family with different power devices. It comes with an [ADuM3221A](#) installed.

EVALUATION BOARD

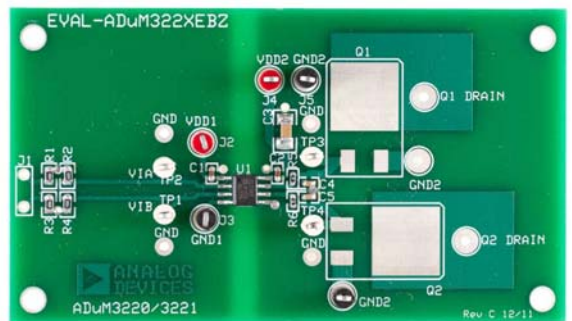


Figure 1. EVAL-ADuM3221EBZ Evaluation Board

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REVISION HISTORY

3/12—Rev. 0 to Rev. A

Changes to User Guide Title, General Description Section, and Figure 1	1
Changes to Pad Layout for the DUT Section, Input Power Connections Section, Output Power Connections Section, I/O Connections Section, and Figure 3	3
Changes to Figure 4 and Figure 5.....	4
Added Ordering Information Section and Bill of Materials Section.....	5

2/11—Revision 0: Initial Version

PAD LAYOUT FOR THE DUT

Figure 4 and Figure 5 show the top and bottom layer artwork of the EVAL-ADuM3221EBZ evaluation board, respectively. Q1 and Q2 can be populated with TO-263 or TO-252 MOSFETs or IGBTs with the footprint shown in Figure 2. C4 and C5 are 2.2 nF and represent a typical gate capacitance. If MOSFETs/IGBTs are soldered to Q1 and Q2, remove these capacitors. R5 and R6 add resistance in series with the gates to control the edges of the gate driver. If the outputs have a lighter load than 2 nF, the resistance of R5 and R6 may need to be increased.

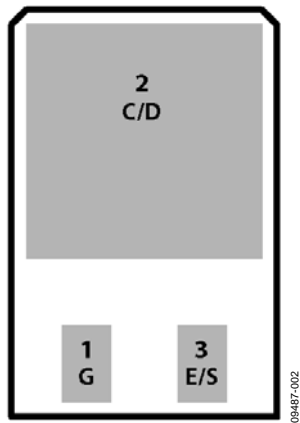


Figure 2. IGBT/MOSFET Footprint

INPUT POWER CONNECTIONS

Connect the input side supply, VDD1 (3 V to 5.5 V) to J2 and its return to J3 (GND1).

OUTPUT POWER CONNECTIONS

Connect the output supply voltage, VDD2 (4.5 V to 18 V) of the [ADuM3220/ADuM3221](#) to J4 and its return to J5 (GND2).

I/O CONNECTIONS

Connect Logic Input A/VIA and Logic Input B/VIB to an external logic signal via J1 or TP1/TP2. The two logic inputs have 50 Ω terminations. The collector/drain outputs of the two IGBTs/MOSFETs, Q1 and Q2, have labeled wire pads.

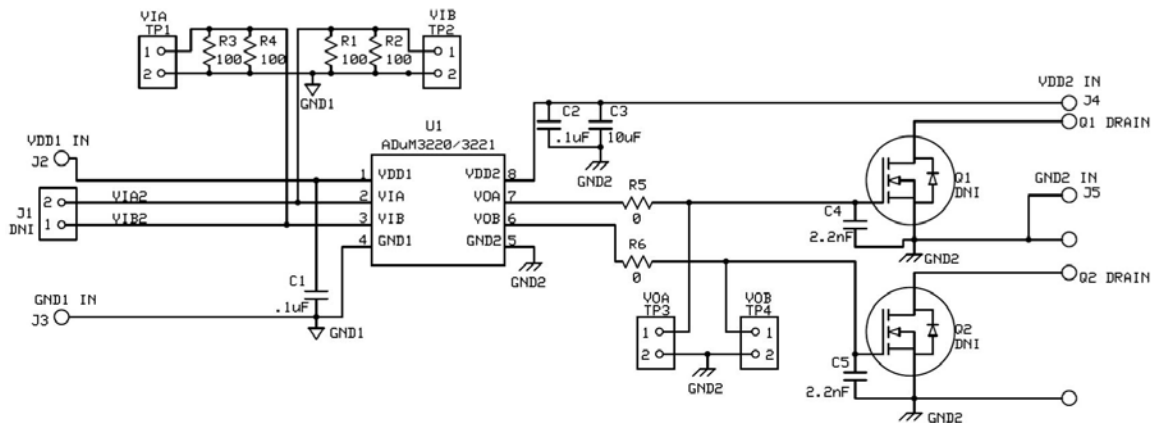


Figure 3. ADuM3220/ADuM3221 Schematic

EVALUATION BOARD LAYOUT

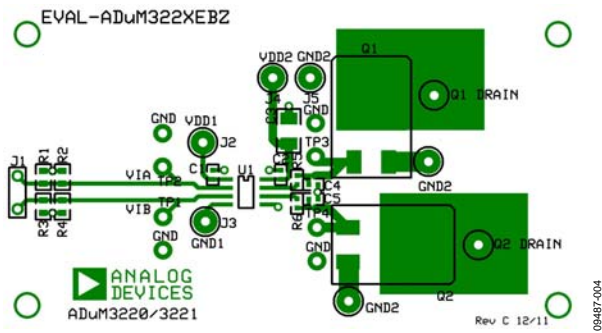


Figure 4. Top Layer of the EVAL-ADuM3221EBZ Evaluation Board

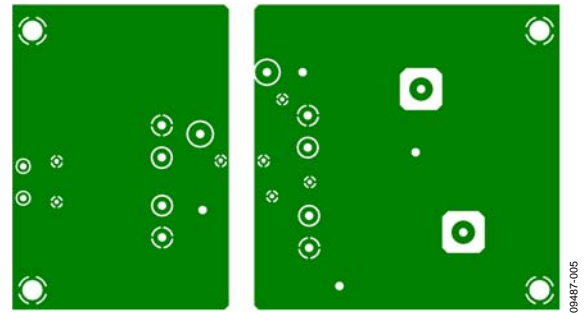


Figure 5. Bottom Layer of the EVAL-ADuM3221EBZ Evaluation Board

ORDERING INFORMATION**BILL OF MATERIALS**

Table 1.

Quantity	Reference Designator	Description
1	U1	ADuM3221A
4	R1 to R4	100 Ω , 1/4 W, 1%, 0805
2	R5, R6	0 Ω , 1/10 W, 0603
2	C1, C2	0.1 μ F, 25 V, 10%, 0603
1	C3	10 μ F, 25 V, 10%, 1206
2	C4, C5	2200 pF, 50 V, 5%, 0603
2	J3, J5	TP-104 series test point, black
2	J2, J4	TP-104 series test point, red
4	TP1 to TP4	TP-104 series test point, white
Not applicable	J1, Q1, Q2	Do not install

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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