



**THE DATASHEET OF
FDWS9508L-F085**



MOSFET – P-Channel, Logic Level, POWERTRENCH®

-40 V, -80 A, 4.9 mΩ

FDWS9508L-F085

Features

- Typ $R_{DS(on)}$ = 3,6 mΩ at $V_{GS} = -10$ V; $I_D = -80$ A
- Typ $Q_{g(tot)}$ = 82 nC at $V_{GS} = -10$ V; $I_D = -80$ A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

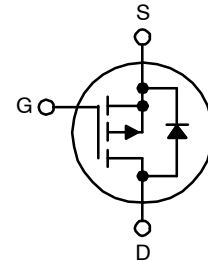
MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	-40	V
V_{GS}	Gate to Source Voltage	± 16	V
I_D	Drain Current ($T_C = 25^\circ\text{C}$) Continuous ($V_{GS} = -10$ V) (Note 1) Pulsed	-80 (see Fig. 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	211	mJ
P_D	Power Dissipation Derate Above 25°C	214 1.43	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance (Junction to case)	0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance (Junction to Ambient) (Note 3)	50	$^\circ\text{C}/\text{W}$

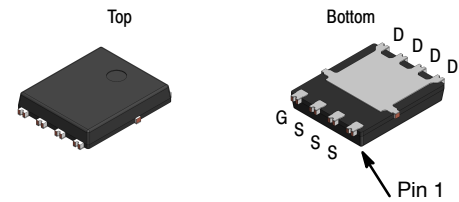
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting $T_j = 25^\circ\text{C}$, $L = 0.1$ mH, $I_{AS} = -65$ A, $V_{DD} = -40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
-40 V	4.9 mΩ @ -10 V	-80 A

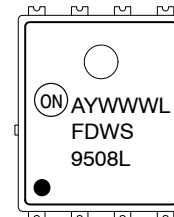


P-Channel MOSFET



DFNW8
CASE 507AU

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- WL = Assembly Lot
- FDWS = Device Code
- 9508L = Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDWS9508L-F085	DFNW8 (Power56) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDWS9508L-F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _{VDS}	Drain-to-Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-40	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = -40 V, V _{GS} = 0 V, T _J = 25°C	-	-	-1	μA
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 175°C (Note 4)	-	-	-1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±16 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1.0	-1.8	-3.0	V
R _{DS(on)}	Drain to Source On-Resistance	I _D = -80 A, V _{GS} = -4.5 V, T _J = 25°C	-	5.6	8.5	mΩ
		I _D = -80 A, V _{GS} = -10 V, T _J = 25°C	-	3.6	4.9	
		I _D = -80 A, V _{GS} = -10 V, T _J = 175°C (Note 4)	-	5.9	8.0	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	-	4840	-	pF	
C _{oss}	Output Capacitance		-	2310	-		
C _{rss}	Reverse Transfer Capacitance		-	49	-		
R _g	Gate Resistance	f = 1 MHz	-	24	-	Ω	
Q _{g(ToT)}	Total Gate Charge at 10 V	V _{GS} = 0 V to -10 V	V _{DD} = -32 V, I _D = -80 A	-	82	107	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 V to -2 V		-	11	-	
Q _{gs}	Gate-to-Source Gate Charge			-	20	-	
Q _{gd}	Gate-to-Drain "Miller" Charge			-	10	-	

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = -20 V, I _D = -80 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	-	-	23	ns
t _{d(on)}	Turn-On Delay Time		-	10	-	
t _r	Rise Time		-	5	-	
t _{d(off)}	Turn-Off Delay Time		-	389	-	
t _f	Fall Time		-	114	-	
t _{off}	Turn-Off Time		-	-	780	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = -80 A, V _{GS} = 0 V	-	-	-1.25	V
		I _{SD} = -40 A, V _{GS} = 0 V	-	-	-1.2	
t _{rr}	Reverse Recovery Time	I _{SD} = -80 A, ΔI _{SD} /Δt = 100 A/μs, V _{DD} = -32 V	-	82	107	ns
Q _{rr}	Reverse Recovery Charge		-	95	124	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE:

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

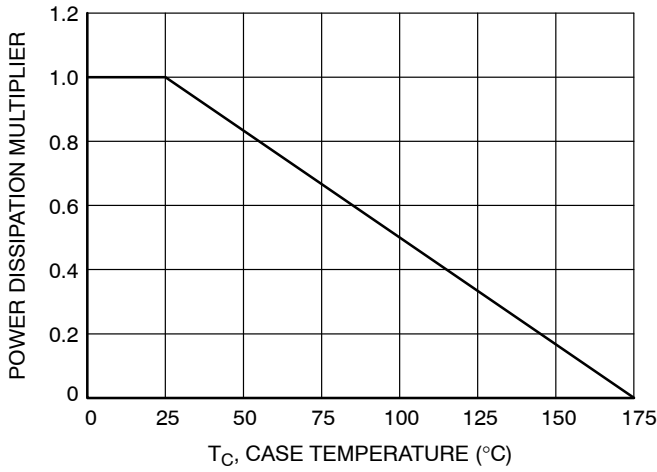


Figure 1. Normalized Power Dissipation vs. Case Temperature

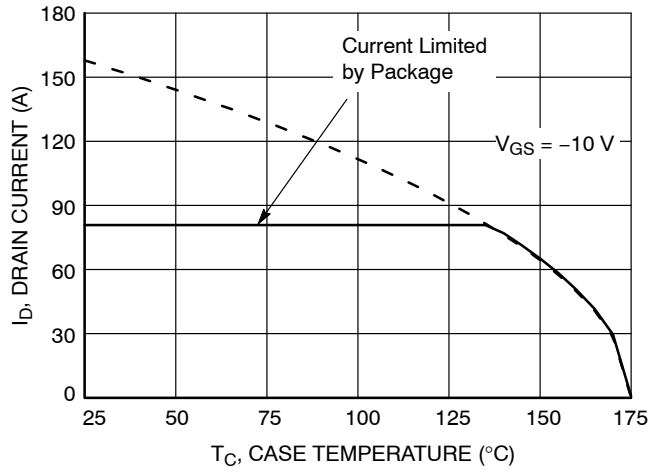


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

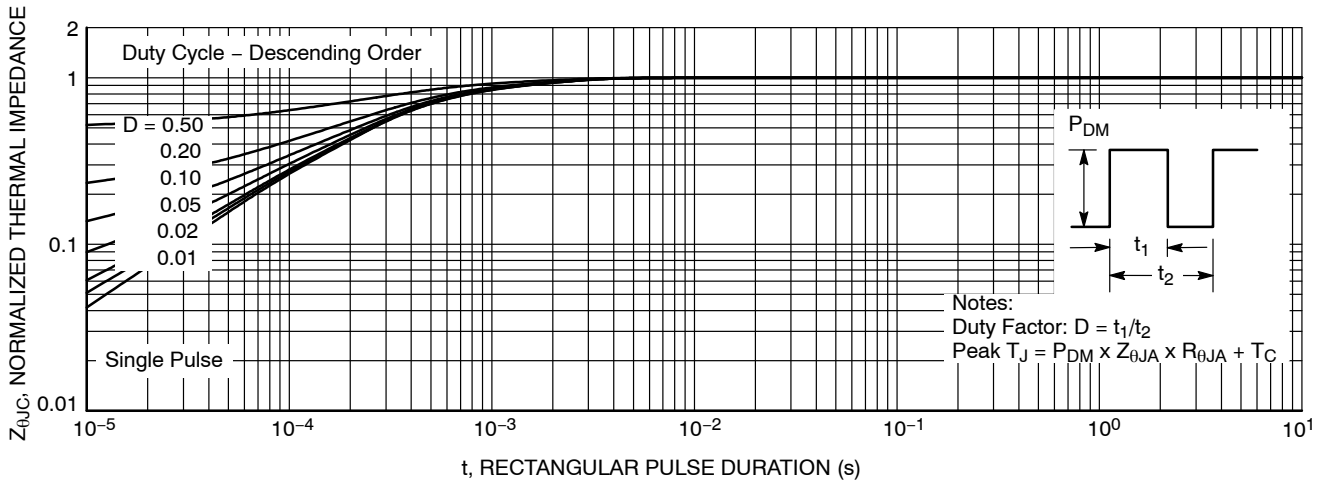


Figure 3. Normalized Maximum Transient Thermal Impedance

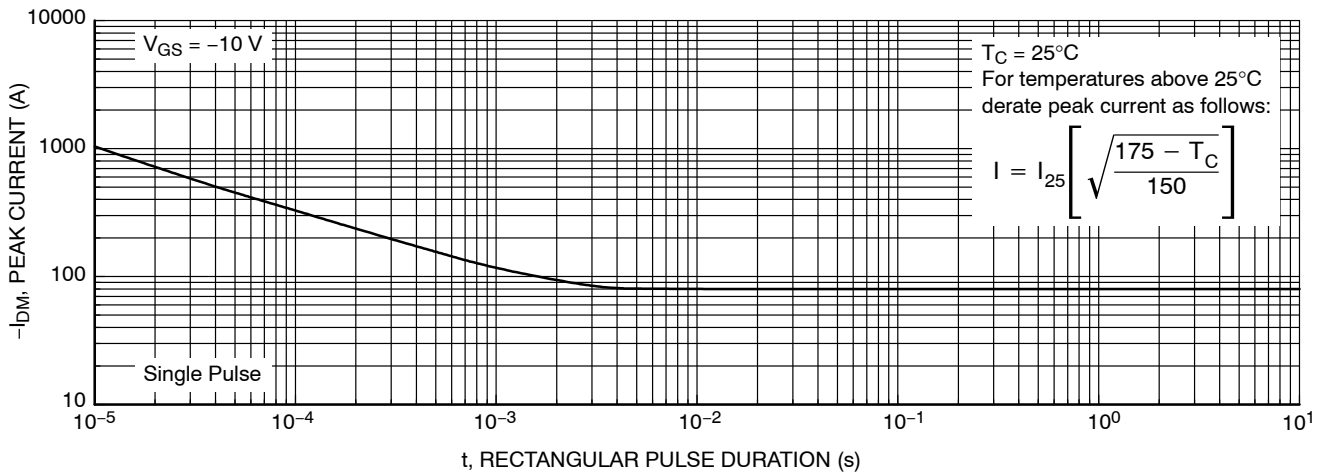


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

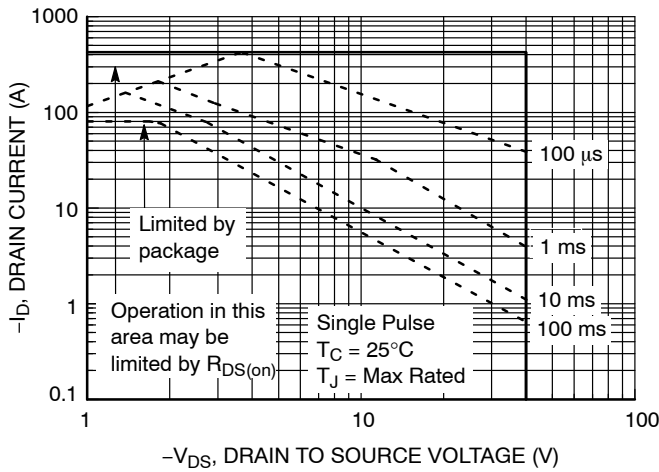


Figure 5. Forward Bias Safe Operating Area

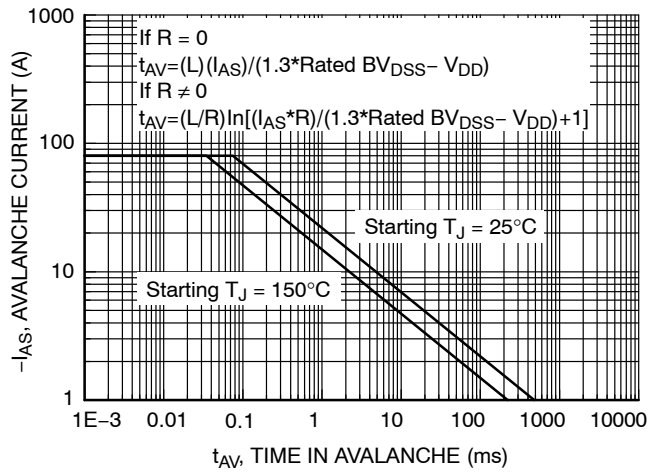


Figure 6. Unclamped Inductive Switching Capability

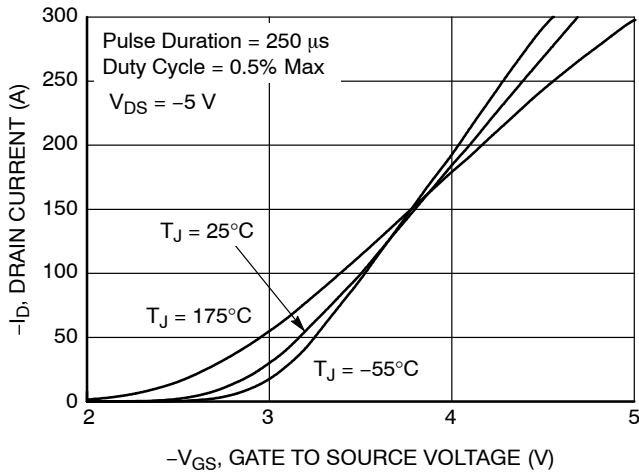


Figure 7. Transfer Characteristics

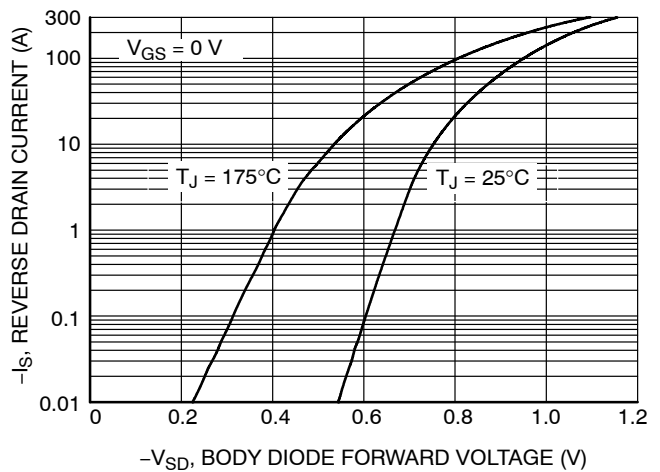


Figure 8. Forward Diode Characteristics

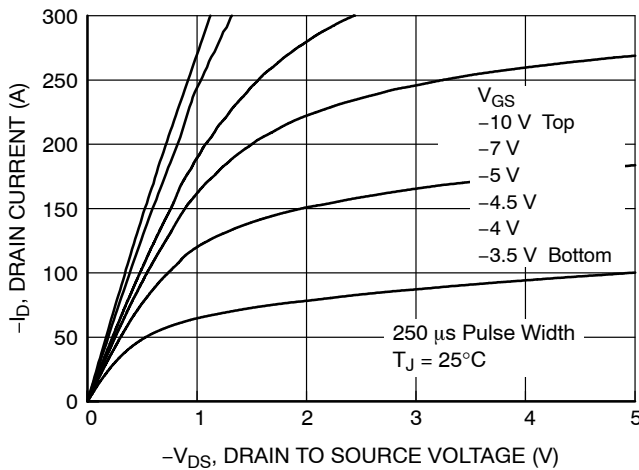


Figure 9. Saturation Characteristics

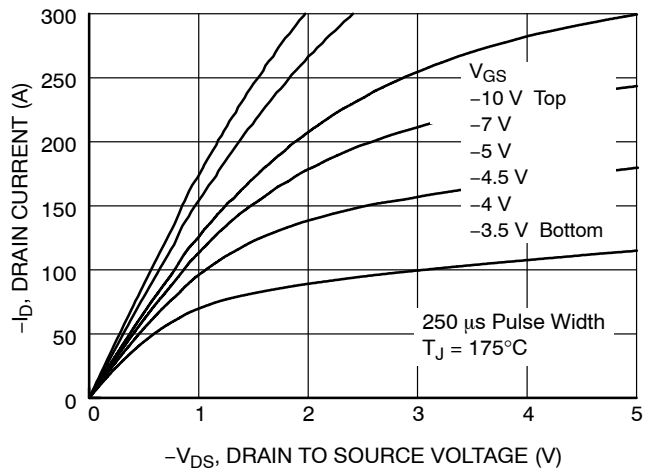


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

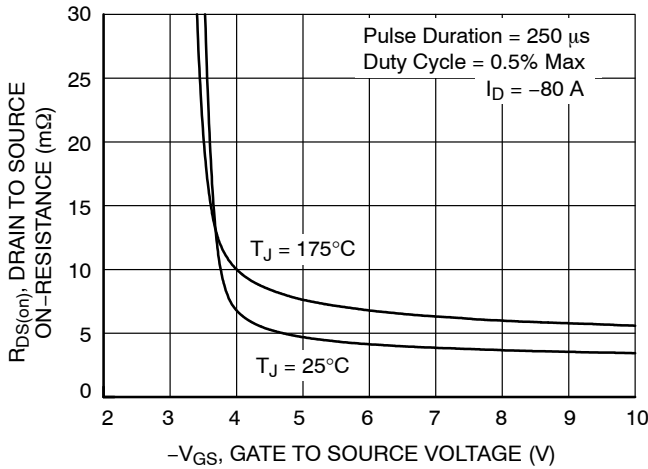


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

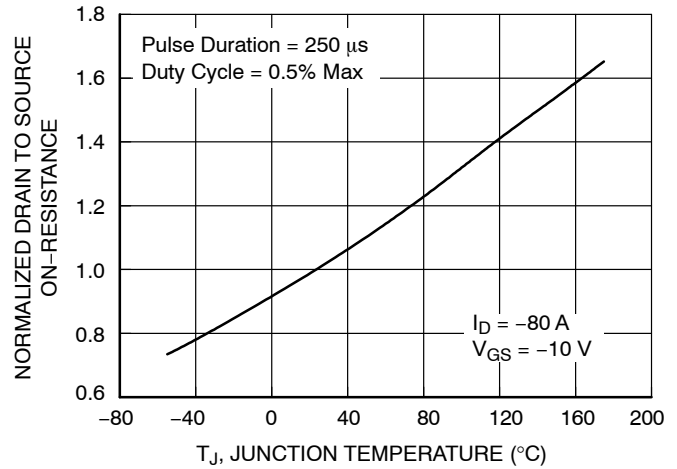


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

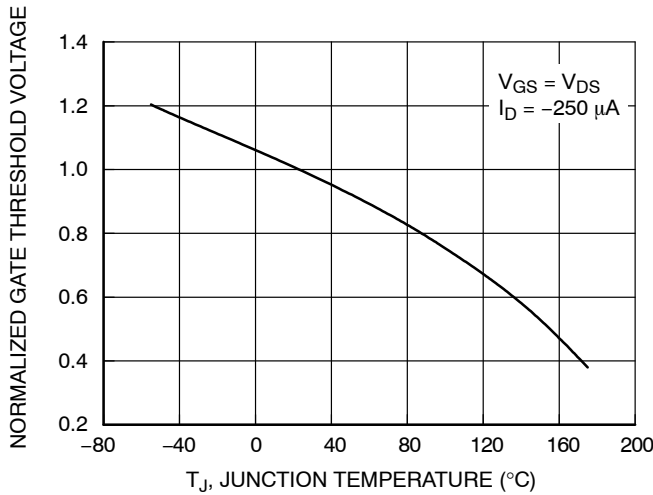


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

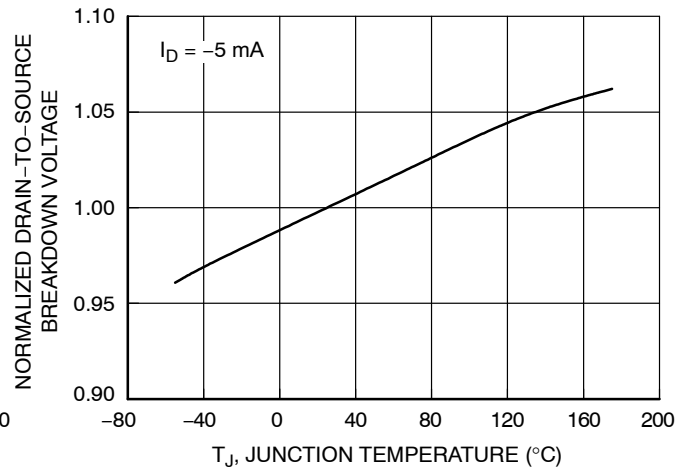


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

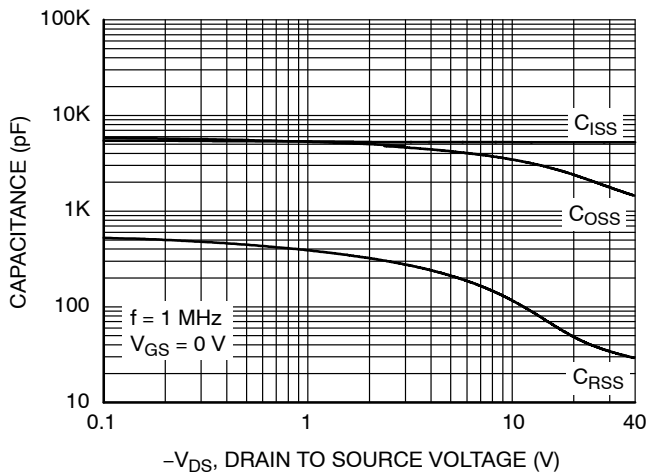


Figure 15. Capacitance vs. Drain to Source Voltage

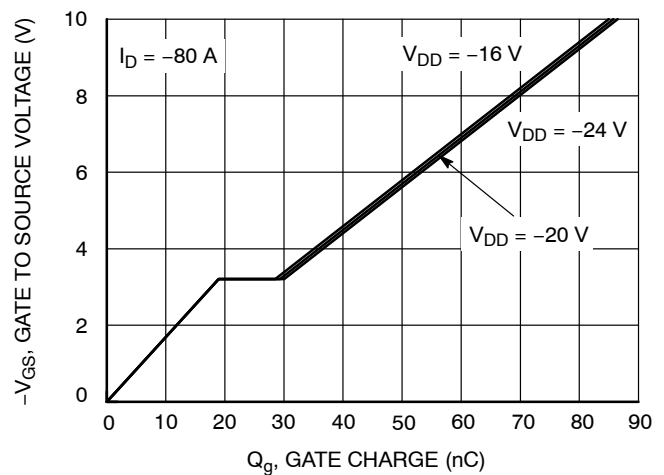
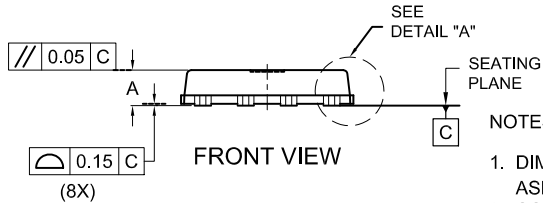
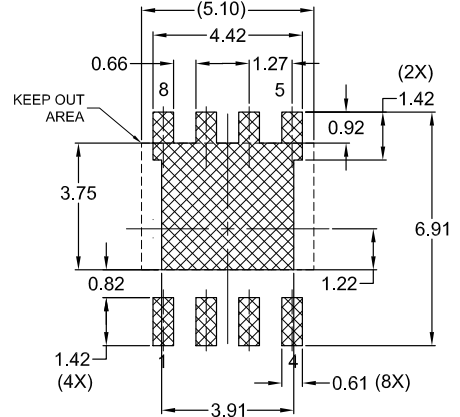
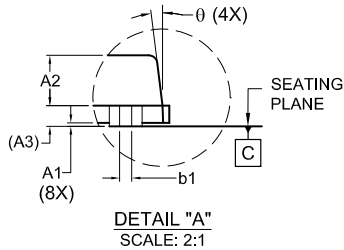
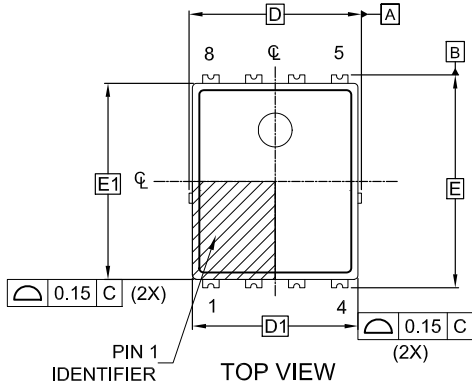


Figure 16. Gate Charge vs. Gate to Source Voltage

FDWS9508L-F085

PACKAGE DIMENSIONS

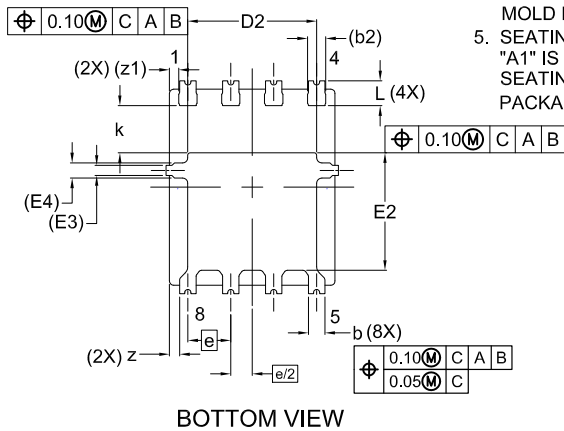
DFNW8 5.2x6.3, 1.27P
CASE 507AU
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	-	-	0.05
A2	0.65	0.75	0.85
A3	0.30 REF		
b	0.47	0.52	0.57
b1	0.13	0.18	0.23
b2	(0.54)		
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30 REF		
E4	0.45 REF		
e	1.27 BSC		
e/2	0.635BSC		
k	1.30	1.40	1.50
L	0.64	0.74	0.84
z	0.24	0.29	0.34
z1	(0.28)		
θ	0°	---	12°

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