



# THE DATASHEET OF IRL60SC216ARMA1



# MOSFET

## StrongIRFET™

### Features

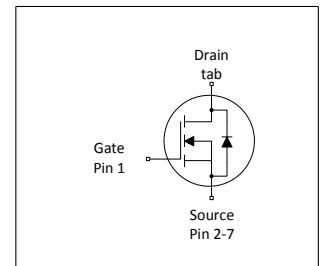
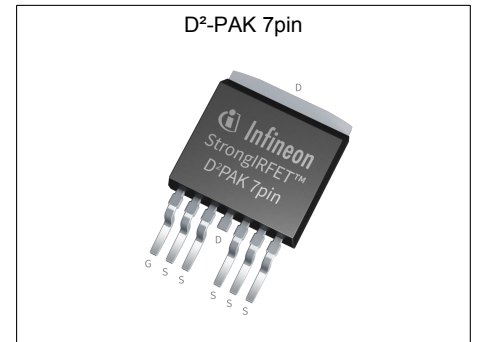
- Very low  $R_{DS(on)}$
- Optimized for logic level drive
- High current carrying capability
- 175°C operating temperature
- Optimized for broadest availability from distribution partners

### Benefits

- Reduced conduction losses
- Increased power density
- Increased reliability versus 150°C rated parts
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),typ}$	1.2	mΩ
$R_{DS(on),max}$	1.5	mΩ
$I_D$ (Silicon Limited)	324	A
$Q_G(0V..10V)$	174	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IRL60SC216	PG-TO263-7	IRL60SC216	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	324 229	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}^{1)}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	1296	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	531	mJ	$I_D=100\text{ A}$ , $R_{GS}=50\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	375 2.4	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{THJA}=62\text{ °C/W}^3)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, $\theta^{4)}$	$R_{thJC}$	-	-	0.4	°C/W	-
Thermal resistance, junction -Ambient, $\theta$	$R_{thJA}$	-	-	62	°C/W	-
Case-to-Sink, Flat Greased Surface	$R_{thCS}$	-	0.5	-	°C/W	-

<sup>1)</sup> See Diagram 3 for more detailed information

<sup>2)</sup> See Diagram 13 for more detailed information

<sup>3)</sup> When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994:

<sup>4)</sup>  $R_{thJC}$  is measured at  $T_j$  approximately 90°C.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=250\text{ }\mu\text{A}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	45	-	mV/°C	$I_D=5\text{ mA}$ , referenced to $25\text{ °C}$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.4	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1 150	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.2 1.4	1.50 1.8	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	2.0	-	$\Omega$	-
Transconductance	$g_{fs}$	-	320	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	16000	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	1100	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	810	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	66	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Rise time	$t_r$	-	149	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	175	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Fall time	$t_f$	-	90	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$

<sup>1)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	43	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	26	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge <sup>2)</sup>	$Q_{gd}$	-	78	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	95	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>2)</sup>	$Q_g$	-	174	218	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.8	-	V	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	96	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	58	-	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

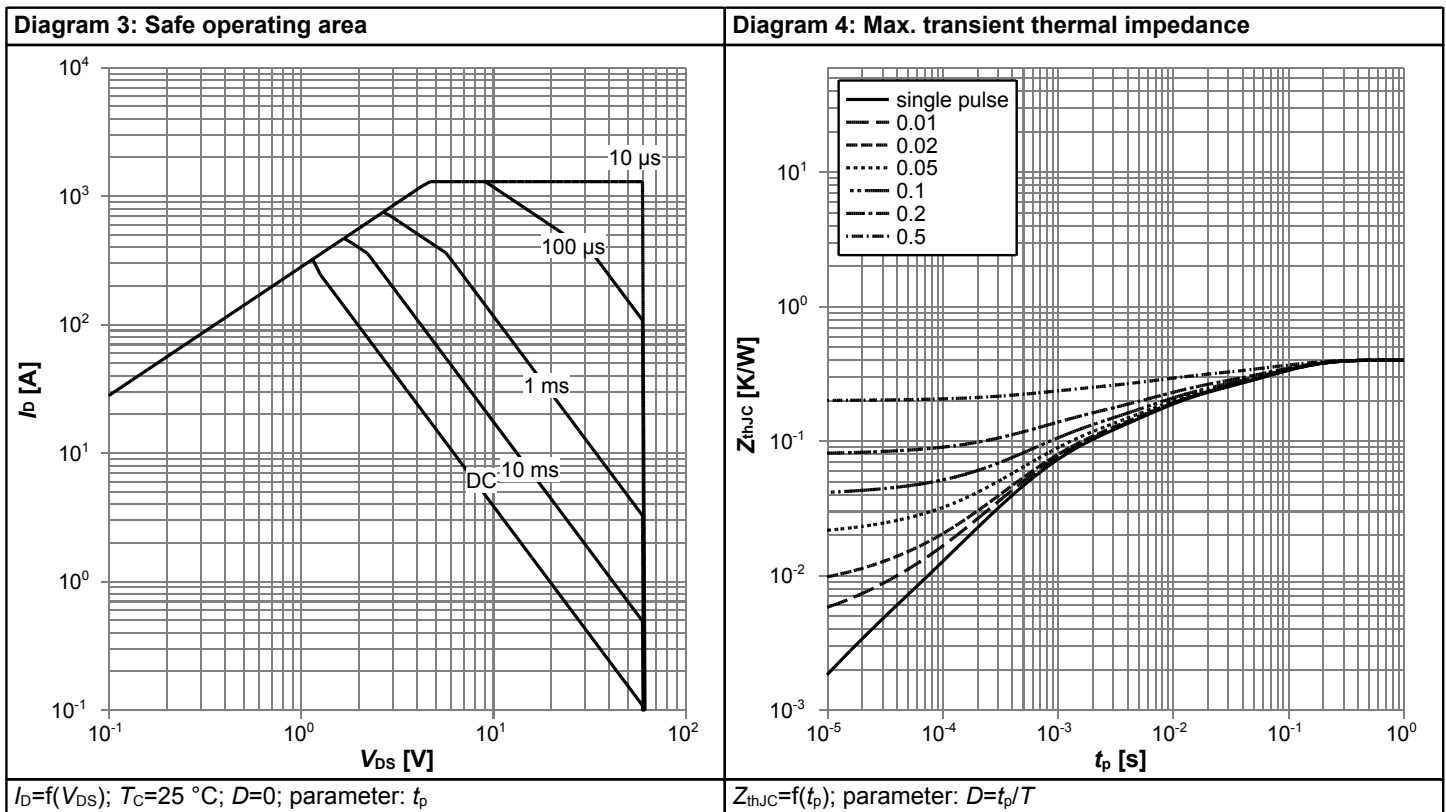
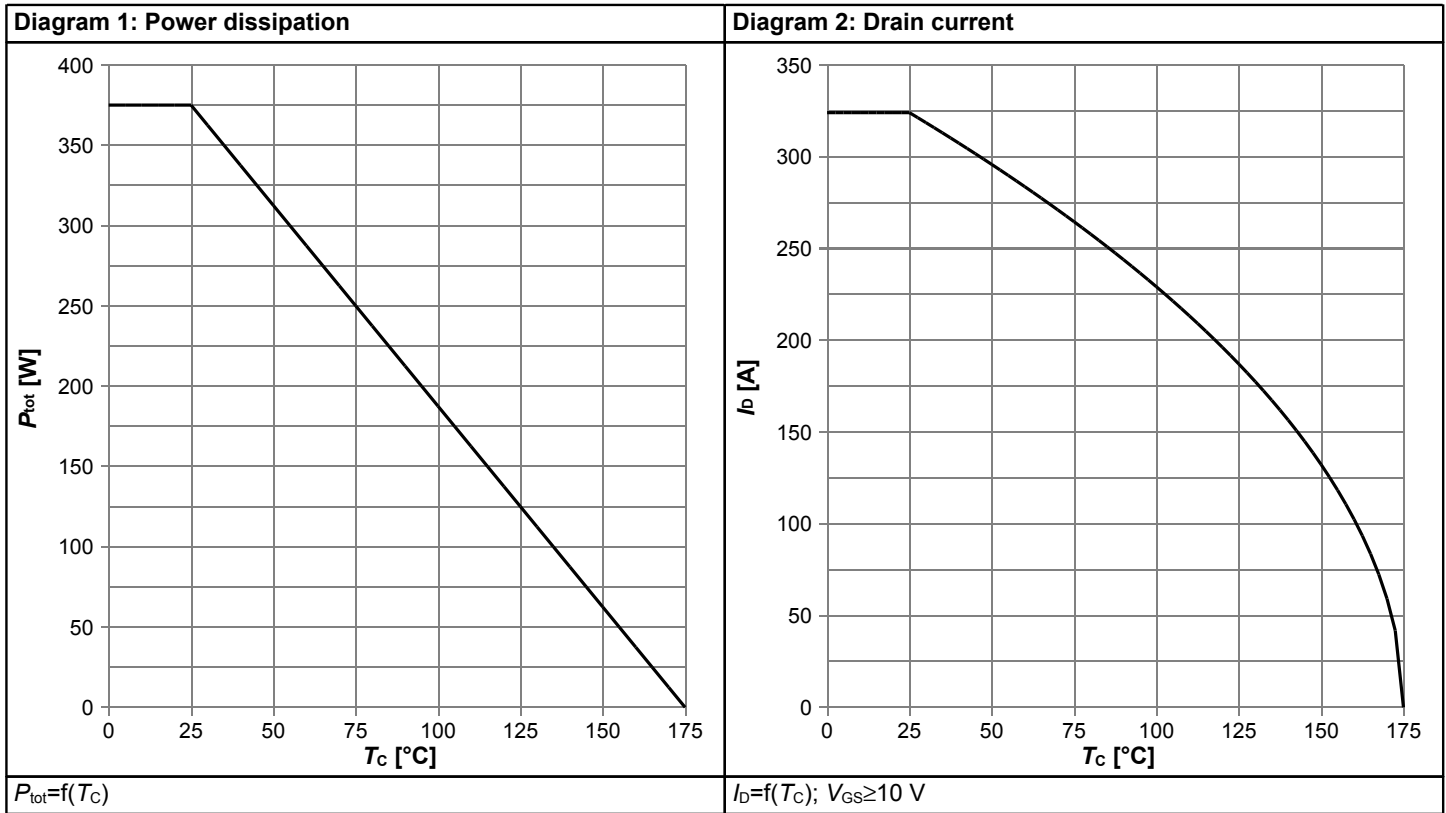
**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	313	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1296	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	-	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=100\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>2)</sup>	$t_{rr}$	-	40	-	ns	$V_R=51\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$	-	52	-	nC	$V_R=51\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

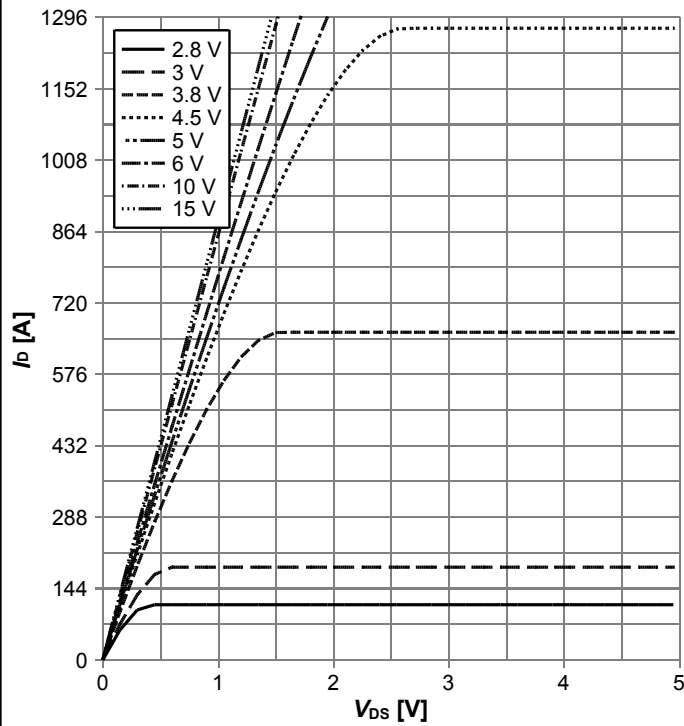
<sup>1)</sup> See "Gate charge waveforms" for parameter definition

<sup>2)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

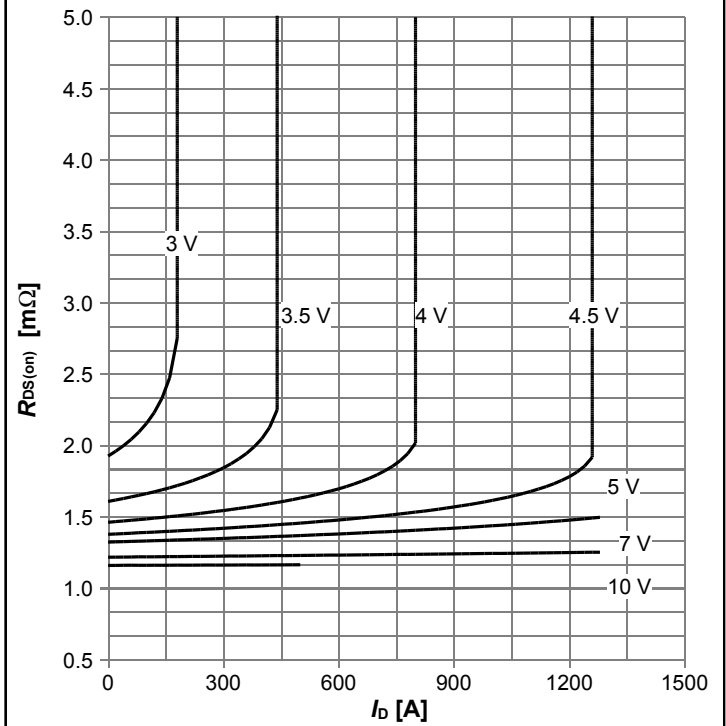


**Diagram 5: Typ. output characteristics**



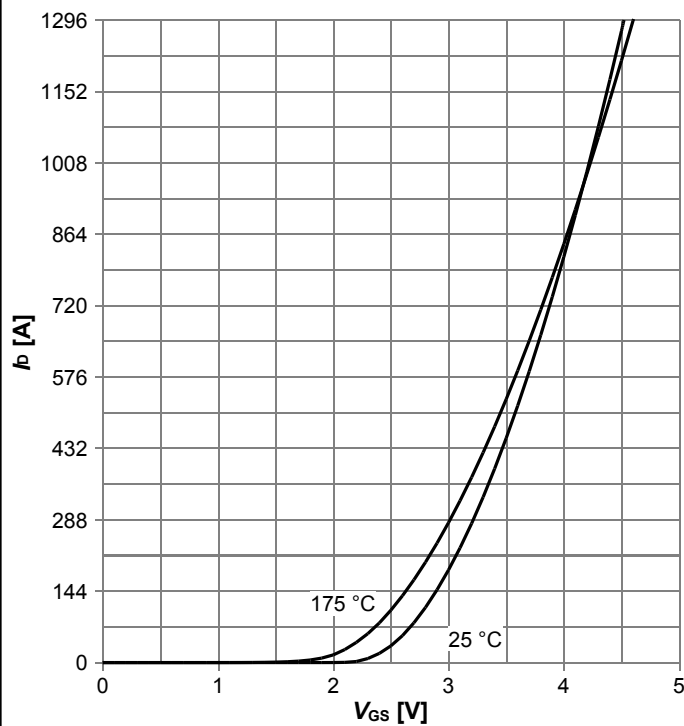
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



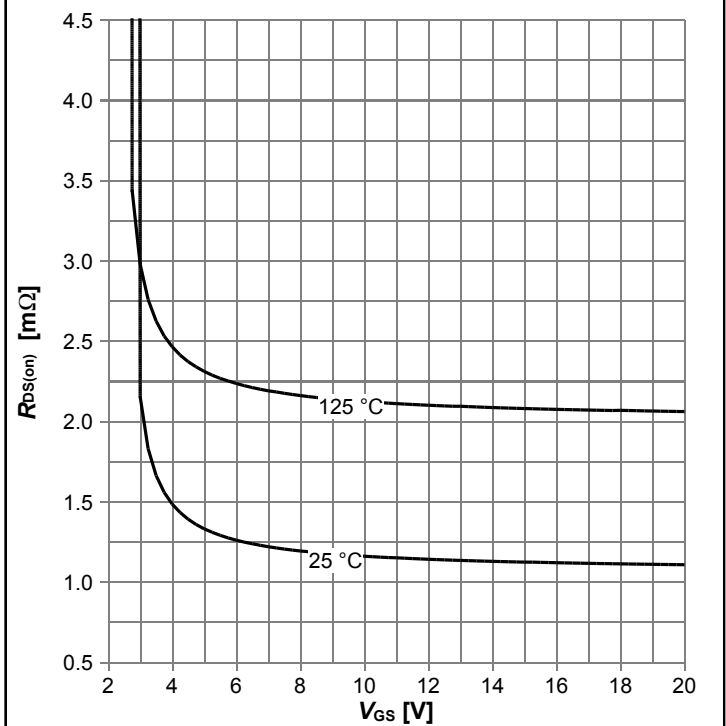
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



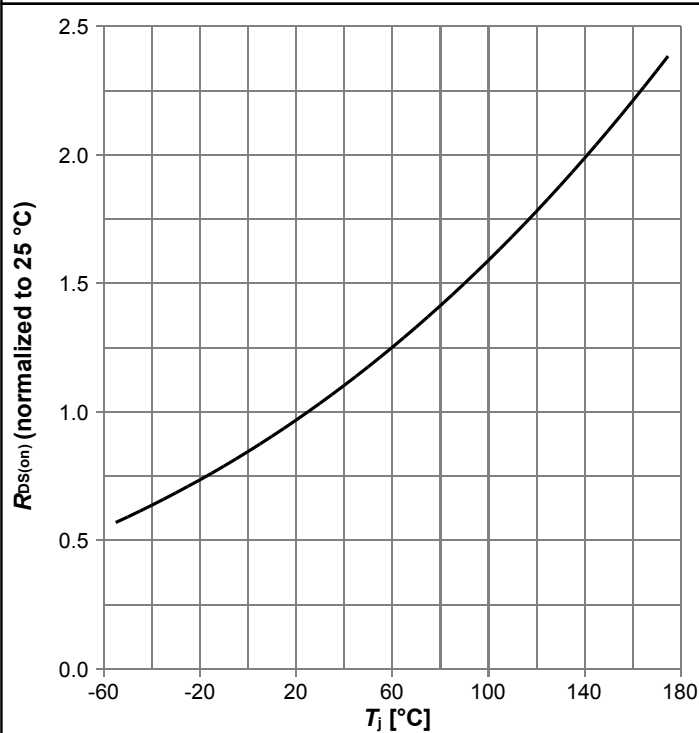
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



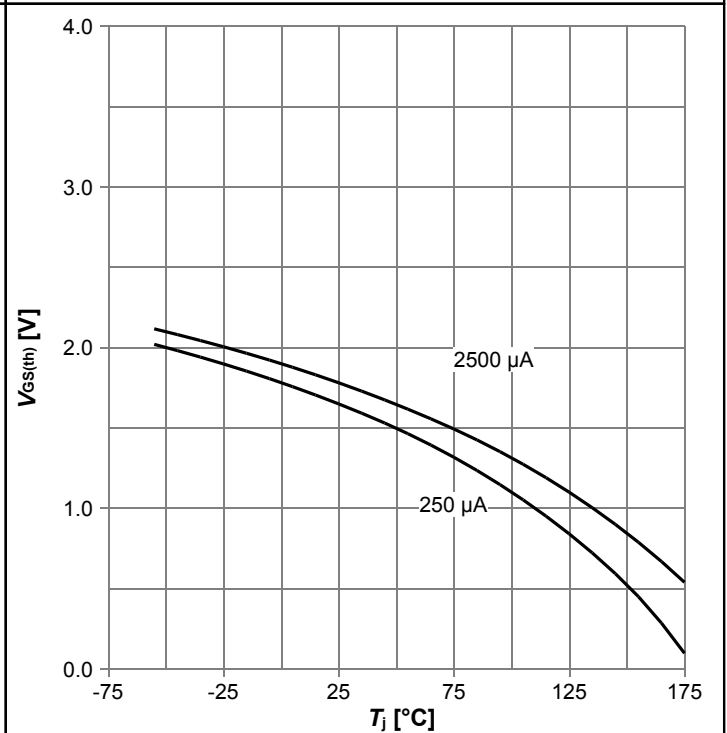
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 100\text{ A}$ ; parameter:  $T_j$

**Diagram 9: Normalized drain-source on resistance**



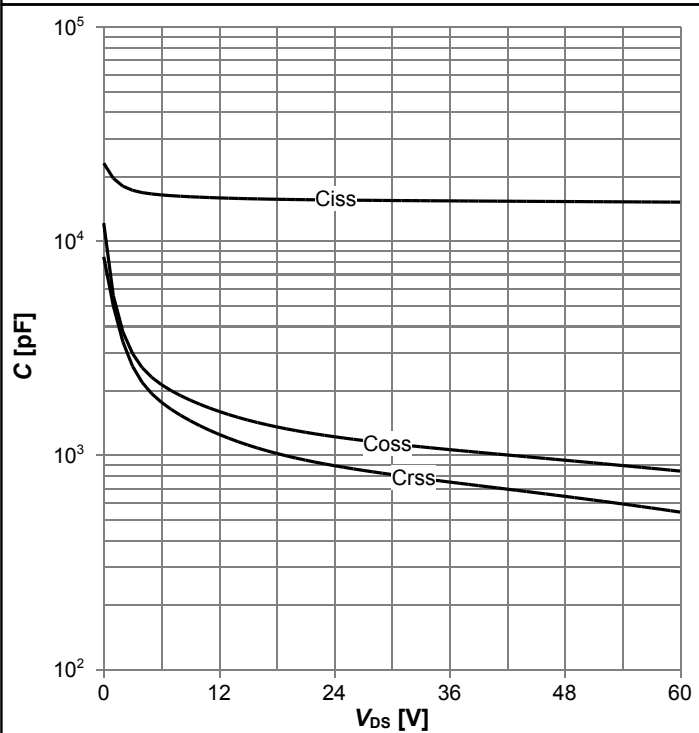
$R_{DS(on)}=f(T_j)$ ,  $I_D=100$  A,  $V_{GS}=10$  V

**Diagram 10: Typ. gate threshold voltage**



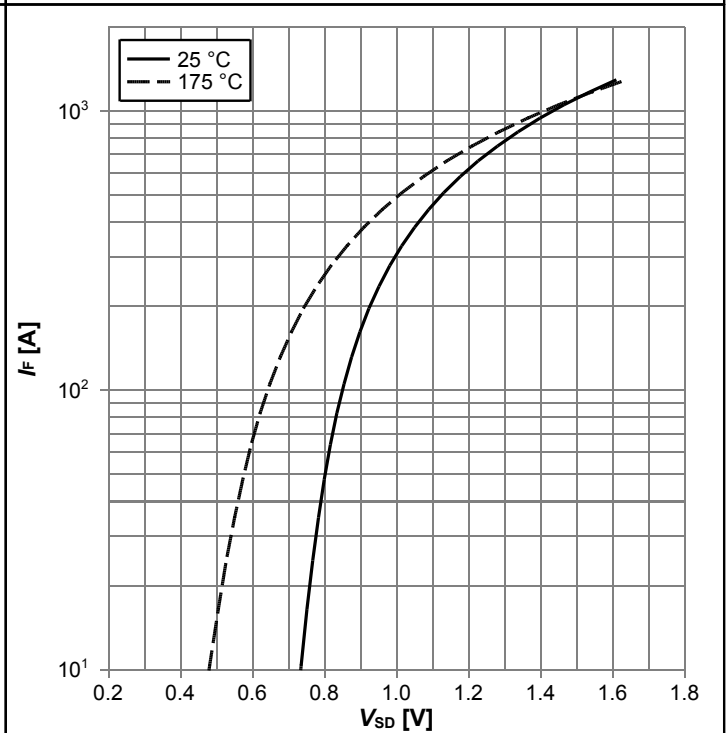
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

**Diagram 11: Typ. capacitances**



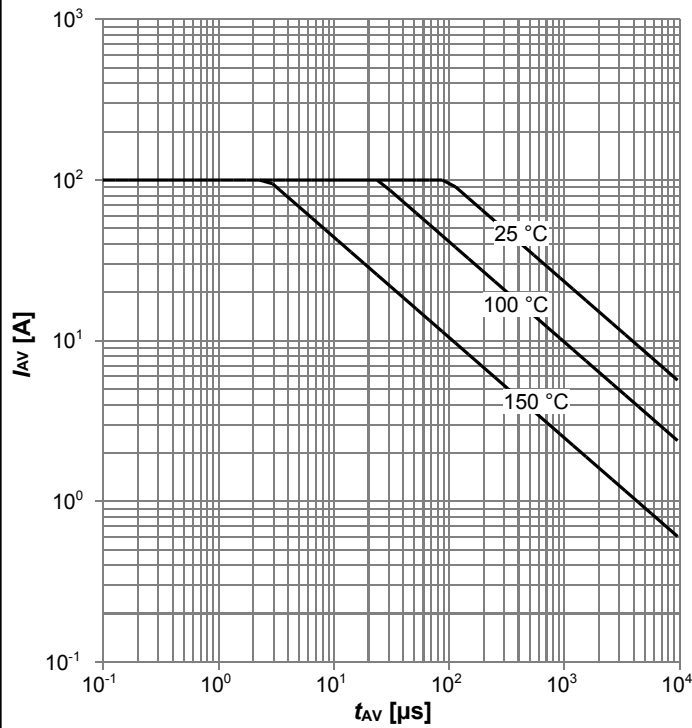
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

**Diagram 12: Forward characteristics of reverse diode**



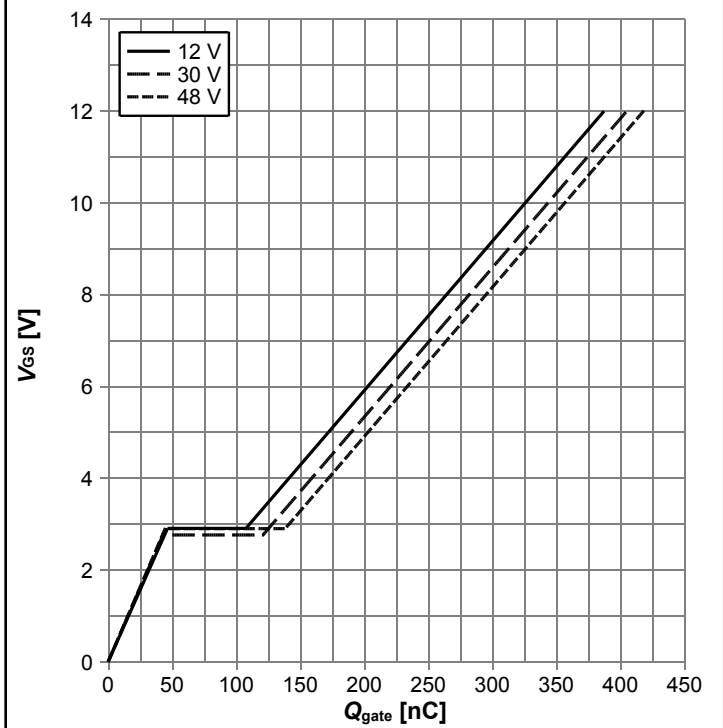
$I_F=f(V_{SD})$ ; parameter:  $T_j$

**Diagram 13: Avalanche characteristics**



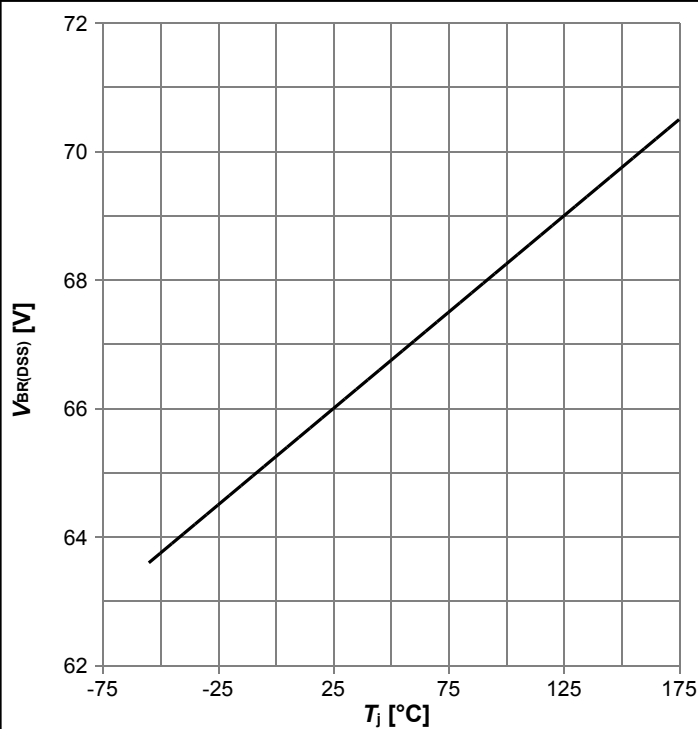
$I_{AS}=f(t_{AV}); R_{GS}=50 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



$V_{GS}=f(Q_{gate}), I_D=100 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

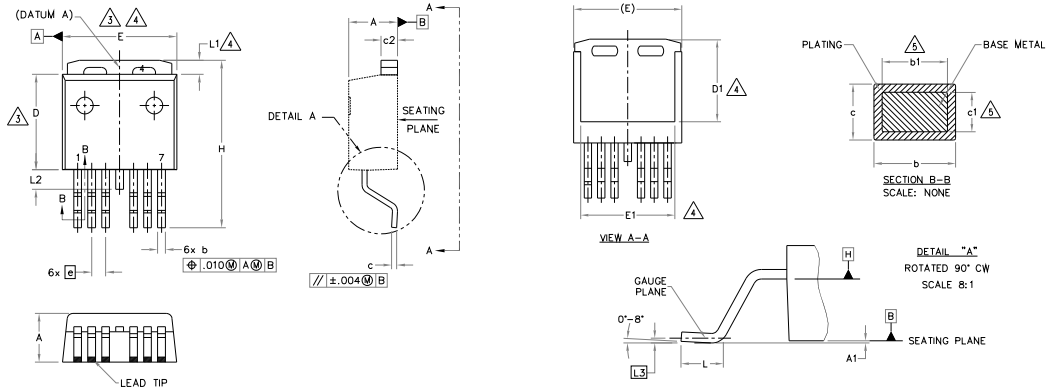


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram Gate charge waveforms**



## 5 Package Outlines

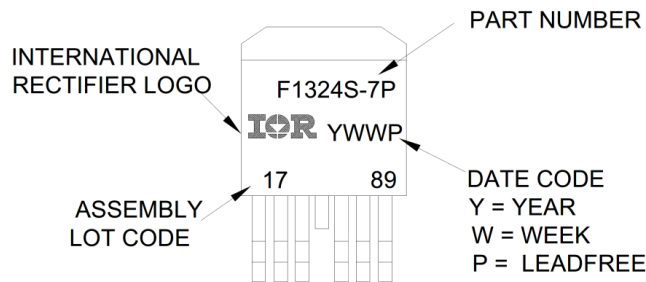


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	—	0.254	—	.010	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	8.00	9.00	.315	.354	
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB EXCEPT FOR DIMS. E, E1 & D1.

### D<sup>2</sup>Pak - 7 Pin Part Marking Information



**Figure 1 Outline PG-TO263-7, dimensions in mm/inches**

## Revision History

IRL60SC216

**Revision: 2020-07-02, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-11-29	Release of preliminary version
2.0	2018-12-04	Release of final version
2.1	2019-05-08	Rev. 1
2.2	2020-07-02	Update from IR MOSFET/StrongIRFET™ to StrongIRFET™

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