THE DATASHEET OF

LTC3876IUHF#PBF

www.win-source.net 0086-755-83957316

Dual DC/DC Controller for DDR Power with Differential VDDQ Sensing and ±50mA VTT Reference

FEATURES

- **Complete DDR Power Solution with VTT Reference**
- **Wide V_{IN} Range: 4.5V to 38V, VDDQ: 1V to 2.5V**
- **±0.67% VDDQ Output Voltage Accuracy**
- **VDDQ and VTT Termination Controllers**
- **±1.2% ±50mA Linear VTTR Reference Output**
- **Controlled On-Time, Valley Current Mode Control**
- **Frequency Programmable from 200kHz to 2MHz Synchronizable to External Clock**
- **$t_{ON(MIN)}$ = 30ns, $t_{OFF(MIN)}$ = 90ns**
- R_{SENSE} or Inductor DCR Current Sensing
- Power Good Output Voltage Monitor
- Overvoltage Protection and Current Limit Foldback
- Thermally Enhanced 38-Pin (5mm × 7mm) QFN and TSSOP Packages

APPLICATIONS

- Motherboard Memory
- Servers

DESCRIPTION

The LTC®3876 is a complete DDR power solution, compatible with DDR1, DDR2, DDR3 and future DDRX lower voltage standards. The LTC3876 includes VDDQ and VTT DC/DC controllers and a precision linear VTT reference. A differential output sense amplifier and precision internal reference combine to offer an accurate VDDQ supply. The VTT controller tracks the precision VTTR linear reference with less than 20mV total DC error. The precision VTTR reference maintains 1.2% regulation accuracy tracking one-half VDDQ over temperature for a ±50mA reference load.

The LTC3876 allows operation from 4.5V to 38V maximum at the input. The VDDQ output can range from 1.0V to 2.5V, with a corresponding VTT and VTTR output range of 0.5V to 1.25V. Voltage tracking soft-start, PGOOD and fault protection features are provided.

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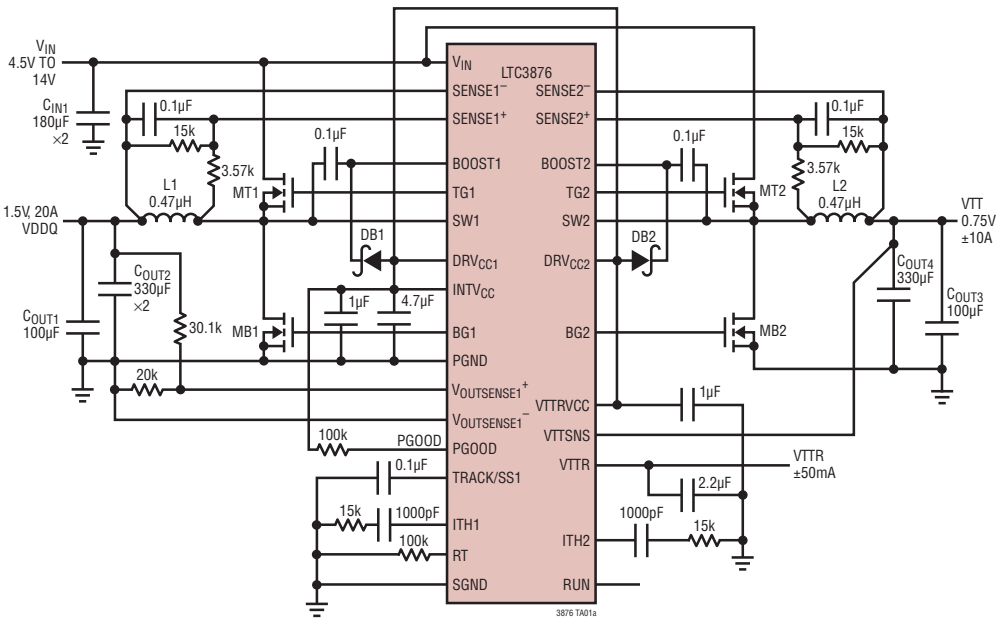
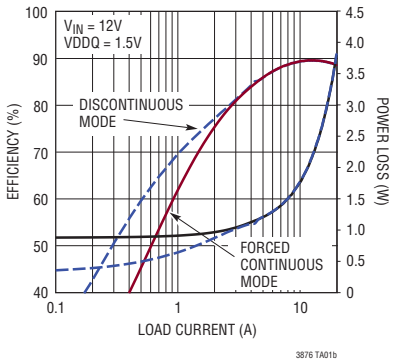
TYPICAL APPLICATION

DDR3 1.5V VDDQ/20A 0.75VTT/±10A 4.5V to 14V Input



Efficiency/Power Loss VDDR Channel 1

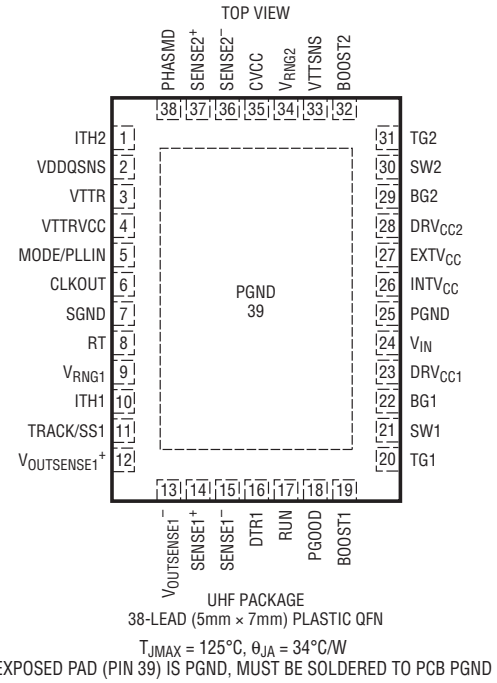


ABSOLUTE MAXIMUM RATINGS

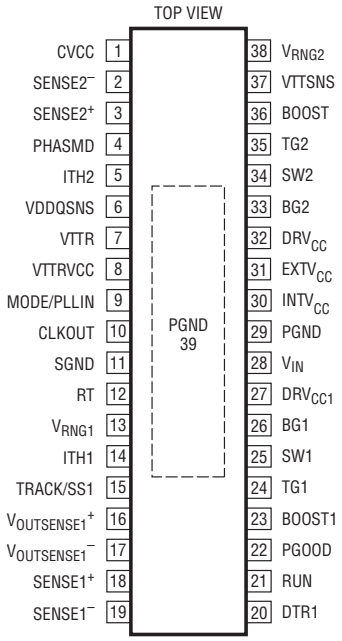
(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
BOOST1, BOOST2 Voltages ..... –0.3V to 46V
SW1, SW2 Voltages ..... –5V to 40V
$INTV_{CC}$, DRV_{CC1}, DRV_{CC2}, $EXTV_{CC}$, PGOOD, RUN, (BOOST1-SW1), (BOOST2-SW2), MODE/PLLIN Voltages ..... –0.3V to 6V
$V_{OUTSENSE1}^+$, $V_{OUTSENSE1}^-$, $SENSE1^+$, $SENSE1^-$, $SENSE2^+$, $SENSE2^-$ Voltages ..... –0.6V to 6V
TRACK/SS1 Voltage ..... –0.3V to 5V
DTR1, CVCC, PHASMD, RT, V_{RNG1}, V_{RNG2}, VTTSNS, VDDQSNS, VTTR, ITH1, ITH2 Voltages ..... –0.3V to ($INTV_{CC}$ + 0.3V)
Operating Junction Temperature Range (Notes 2, 3, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package ..... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB PGND



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3876EUHF#PBF	LTC3876EUHF#TRPBF	3876	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3876IUHF#PBF	LTC3876IUHF#TRPBF	3876	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3876EFE#PBF	LTC3876EFE#TRPBF	LTC3876FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3876IFE#PBF	LTC3876IFE#TRPBF	LTC3876FE	38-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{IN}	Input Voltage Operating Range			4.5		38	V
VDDQ(REG) VTTR(REG) VTTSNS(REG)	VDDQ Regulated Operating Range VTTR Regulated Operating Range VTTSNS Regulated Operating Range	VDDQ Regulates Differentially with Respect to $V_{OUTSENSE1}^-$, VTTSNS and VTTR Regulate Differentially to One-Half VDDQ with Respect to $V_{OUSTSENSE1}^-$		1.0 0.5 0.5		2.5 1.25 1.25	V V V
I_Q	Input DC Supply Current Both Channels Enabled Shutdown Supply Current	 MODE/PLLIN = 0V, No Load RUN1 = RUN2 = 0V			 5000 20		 µA µA
$V_{DFB1(REG)}$	Regulated Differential Feedback Voltage on Channel 1, VDDQ ($V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$)	ITH1 = 1.2V (Note 5) T_A = 25°C T_A = 0°C to 85°C T_A = –40°C to 125°C	 ● ●	 0.5985 0.596 0.594	 0.6 0.6	 0.6015 0.604 0.606	 V V V
	Regulated Differential Feedback Voltage on Channel 1, VDDQ Over Line, Load and Common Mode	V_{IN} = 4.5V to 38V, ITH1 = 0.5V to 1.9V, $V_{OUTSENSE1}^-$ = ±500mV (Notes 5, 7) T_A = 0°C to 85°C T_A = –40°C to 125°C	 ● ●	 0.594 0.591	 0.6 0.6	 0.606 0.609	 V V
VTTSNS(REG)	Regulated Voltage Error on Channel 2, VTTSNS (Referenced to VTTR)	ITH2 = 1.4V (Note 5) T_A = 0°C to 85°C T_A = –40°C to 125°C	 ● ●	 –10 –15	 	 10 15	 mV mV
	Regulated Voltage Error on Channel 2, VTTSNS Over Line, Load and Common Mode. (Referenced to VTTR)	V_{IN} = 4.5V to 38V, ITH1 = 0.5V to 1.9V, (Notes 5, 7) T_A = 0°C to 85°C T_A = –40°C to 125°C	 ● ●	 –15 –20	 	 15 20	 mV mV
$I_{VOUTSENSE1}^+$	$V_{OUTSENSE1}^+$ Input Bias Current	V_{DFB1} [$V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$] = 0.6V			±5	±25	nA
$I_{VOUTSENSE1}^-$	$V_{OUTSENSE1}^-$ Input Bias Current	V_{DFB1} [$V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$] = 0.6V			–25	–50	µA
I_{VTTSNS}	I_{VTTSNS} Input Bias Current	I_{VTTSNS} = 750mV			±5	±50	nA
$g_{m(EA)1,2}$	Error Amplifier Transconductance	ITH = 1.2V (Note 3)			1.7		mS
$t_{ON(MIN)1,2}$	Minimum On-Time	V_{IN} = 38V, R_T = 20k, VDDSNS = 1.2V, V_{SENSE}^- = 0.6V			30		ns
$t_{OFF(MIN)1,2}$	Minimum Off-Time				90		ns
Current Sensing							
$V_{SENSE1(MAX)}$	Maximum Valley Current Sense Threshold ($V_{SENSE1}^+ - V_{SENSE1}^-$)	V_{RNG} = 2V, V_{DFB1} = 0.57V, V_{SENSE1}^- = 1.5V V_{RNG} = 0V, V_{DFB1} = 0.57V, V_{SENSE1}^- = 1.5V V_{RNG} = $INTV_{CC}$, V_{DFB1} = 0.57V, V_{SENSE1}^- = 1.5V	● ● ●	80 21 39	100 30 50	120 40 61	mV mV mV
$V_{SENSE1(MIN)}$	Minimum Valley Current Sense Threshold ($V_{SENSE1}^+ - V_{SENSE1}^-$) (Forced Continuous Mode)	V_{RNG} = 2V, V_{DFB1} = 0.63V, V_{SENSE1}^- = 1.5V V_{RNG} = 0V, V_{DFB1} = 0.63V, V_{SENSE1}^- = 1.5V V_{RNG} = $INTV_{CC}$, V_{DFB1} = 0.63V, V_{SENSE1}^- = 1.5V			–50 –15 –25		mV mV mV
$V_{SENSE2(MAX)}$	Maximum Valley Current Sense Threshold ($V_{SENSE2}^+ - V_{SENSE2}^-$)	V_{RNG} = 2V, VTTSNS = 0.72V, V_{SENSE2}^- = 0.75V V_{RNG} = 0V, VTTSNS = 0.72V, V_{SENSE2}^- = 0.75V V_{RNG} = $INTV_{CC}$, VTTSNS = 0.72V, V_{SENSE2}^- = 0.75V	● ● ●	80 21 39	100 30 50	120 40 61	mV mV mV
$V_{SENSE2(MIN)}$	Minimum Valley Current Sense Threshold ($V_{SENSE1}^+ - V_{SENSE1}^-$) (Forced Continuous Mode)	V_{RNG} = 2V, VTTSNS = 0.78V, V_{SENSE2}^- = 0.75V V_{RNG} = 0V, VTTSNS = 0.78V, V_{SENSE2}^- = 0.75V V_{RNG} = $INTV_{CC}$, VTTSNS = 0.78V, V_{SENSE2}^- = 0.75V			–120 –36 –60		mV mV mV
$I_{SENSE1,2}^+$	SENSE1,2+ Pins Input Bias Current	V_{SENSE}^+ = 0.6V V_{SENSE}^+ = 2.5V			±5 1	±50 ±2	nA µA
$I_{SENSE1,2}^-$	SENSE2– Pins Input Bias Current (Internal 500k Resistor to SGND)	V_{SENSE1}^- = 0.6V V_{SENSE1}^- = 2.5V			1.2 5		µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Start-Up and Shutdown							
$V_{RUN(TH)}$	RUN Pin On Threshold	V_{RUN} Rising	●	1.15	1.2	1.25	V
$V_{RUN(HYS)}$	RUN Pin On Hysteresis	V_{RUN} Falling from $V_{RUN(TH)}$			100		mV
$I_{RUN(OFF)}$	RUN Pin Pull-Up Current When Off	RUN = SGND			2.5		µA
$I_{RUN(HYS)}$	RUN Pin Pull-Up Current Hysteresis	$I_{RUN(HYS)} = I_{RUN(ON)} - I_{RUN(OFF)}$			10		µA
$V_{UVLO(INTVCC)}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling $INTV_{CC}$ Rising	● ●	3.3	3.7 4.2	 4.5	V V
$I_{TRACK/SS}$	Soft-Start Pull-Up Current	0V < TRACK/SS < 0.6V			1		µA
Frequency and Clock Synchronization							
f_{CLKOUT}	Clock Output Frequency (Steady-State Switching Frequency)	R_T = 205k R_T = 80.6k R_T = 18.2k		 450	200 500 2000	 550	kHz kHz kHz
ϕ_{VTT}	VTT Channel 2 Phase (Relative to Channel 1)	V_{PHASMD} = SGND V_{PHASMD} = Floating V_{PHASMD} = $INTV_{CC}$			180 180 240		Deg Deg Deg
ϕ_{CLKOUT}	CLKOUT Phase (Relative to Channel 1)	V_{PHASMD} = SGND V_{PHASMD} = Floating V_{PHASMD} = $INTV_{CC}$			60 90 120		Deg Deg Deg
$V_{CLKOUT(H)}$	Clock Output Voltage High	Pulling to $INTV_{CC}$				V_{INTVCC}	V
$V_{CLKOUT(L)}$	Clock Output Voltage Low	Pulling to SGND		0			V
$V_{PLLIN(H)}$	Clock Input Voltage High	$f_{MODE/PLLIN}$ >100kHz		2			V
$V_{PLLIN(L)}$	Clock Input Voltage Low	$f_{MODE/PLLIN}$ >100kHz				–0.5	V
$R_{MODE/PLLIN}$	MODE/PLLIN Input DC Resistance				600		kΩ
Gate Drivers							
$R_{TG(UP)1,2}$	TG Driver Pull-Up On-Resistance	TG High			2.5		Ω
$R_{TG(DOWN)1,2}$	TG Driver Pull-Down On-Resistance	TG Low			1.2		Ω
$R_{BG(UP)1}$	BG Driver 1 Pull-Up On-Resistance	BG1 High			2.5		Ω
$R_{BG(UP)2}$	BG Driver 2 Pull-Up On-Resistance	BG2 High			1.6		Ω
$R_{BG(DOWN)1,2}$	BG Driver Pull-Down On-Resistance	BG Low			0.8		Ω
$T_{D(TG/BG)1,2}$	Top Gate Off to Bottom Gate On Delay Time	(Note 6)			20		ns
$T_{D(BG/TG)1,2}$	Bottom Gate Off to Top Gate On Delay Time	(Note 6)			15		ns
VTT Reference							
$VTTR(I_{VTTR})$	VTTR Load Regulation ($VTTR(I_{VTTR})$ is Measured Through an Internal Kelvin Connection to the VTTR Pin and is Specified as the Ratio ($VTTR(I_{VTTR})$/VDDQ)	–50mA < I_{VTTR} < 50mA; T_A = –40°C to 125°C 1.5 < VDDQ < 2.5 1.0 < VDDQ < 1.5	 ● ●	 0.4940 0.4930		 0.5060 0.5070	 V/V V/V
Internal V_{CC} Regulator							
V_{DRVCC1}	Internal Regulated DRV_{CC1} Voltage	6V < V_{IN} < 38V		5.0	5.3	5.6	V
ΔV_{DRVCC1}	DRV_{CC1} Load Regulation	I_{CC} = 0mA to 100mA			–1.5	–3	%
$V_{EXTVCC(TH)}$	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising		4.4	4.6	4.8	V
$V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				200		mV
ΔV_{DRVCC2}	$EXTV_{CC}$ to DRV_{CC2} Voltage Drop	V_{EXTVCC} = 5V, I_{DRVCC2} = 100mA			200		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGood Output							
PGD_{OV}	PGOOD Overvoltage Threshold	$V_{OUTSENSE}$, VTTSNS Rising, with Respect to Reference Voltage		5	7.5	10	%
PGD_{UV}	PGOOD Undervoltage Threshold	$V_{OUTSENSE}$, VTTSNS Falling, with Respect to Reference Voltage		–5	–7.5	–10	%
PGD_{HYS}	PGOOD Threshold Hysteresis	$V_{OUTSENSE}$, VTTSNS Returning to Reference Voltage			2.0		%
$V_{PGD(LO)}$	PGOOD Low Voltage	I_{PGOOD} = 2mA			0.1	0.3	V
$t_{PGD(FALL)}$ $t_{PGD(RISE)}$	Delay from OV/UV Fault to PGOOD Falling Delay from OV/UV Recovery to PGOOD Rising				50 20		µs µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3876UHF: $T_J = T_A + (P_D \bullet 34°C/W)$
LTC3876FE: $T_J = T_A + (P_D \bullet 28°C/W)$

Note 3: The LTC3876 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3876E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3876I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the package thermal impedance and other environmental factors.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair the device reliability or permanently damage the device.

Note 5: The LTC3876 is tested in a feedback loop that adjusts ($V_{OUTSENSE1}^+$ $V_{OUTSENSE1}^-$) and VTTSNS to achieve specified error amplifier output voltages (ITH1,2).

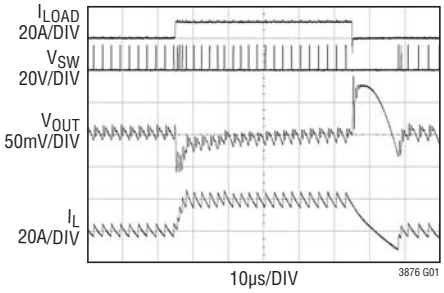
Note 6: Delay times are measured using 50% levels.

Note 7: In order to simplify the total system error computation, the regulated voltage is defined in one combined specification which includes the effects of line, load and common mode variation. The combined regulated voltage specification is tested by independently varying line, load, and common mode, which by design do not significantly affect one another. For any combination of line, load, and common mode variation, the regulated voltage should be within the limits specified that are tested in production to the following conditions:

a. Line: V_{IN} = 4.5V to 38V, ITH = 1V, $V_{OUTSENSE1}^-$ = 0V
b. Load: V_{IN} = 15V, ITH = 0.5V to 1.9V, $V_{OUTSENSE1}^-$ = 0V
c. Common mode: V_{IN} = 15V, ITH = 1V, to $V_{OUTSENSE1}^-$ = ±500mV, (Ch1)

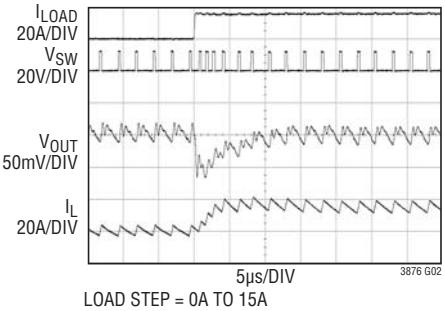
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response VDDQ (Forced Continuous Mode)



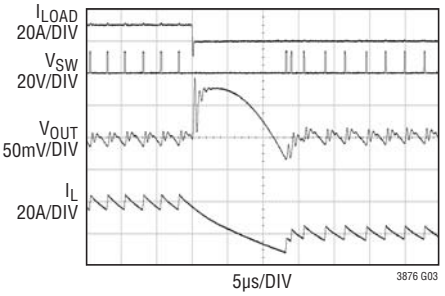
LOAD TRANSIENT = 0A TO 15A
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Load Step VDDQ (Forced Continuous Mode)



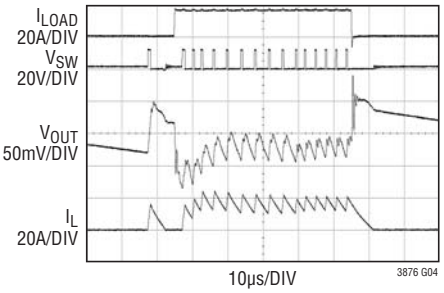
LOAD STEP = 0A TO 15A
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Load Release VDDQ (Forced Continuous Mode)



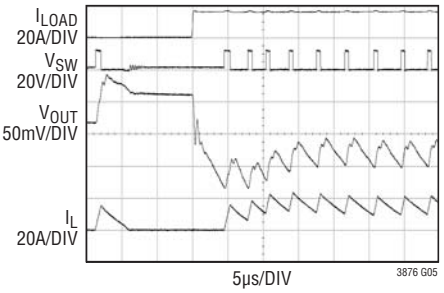
LOAD RELEASE = 15A TO 500mA
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Transient Response VDDQ (Discontinuous Mode)



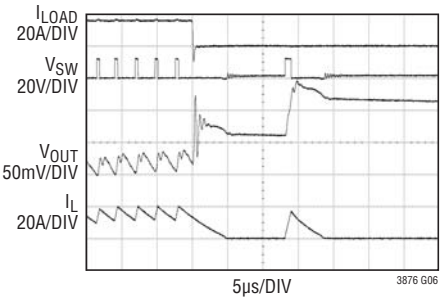
LOAD TRANSIENT = 0A TO 15A
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Load Step VDDQ (Discontinuous Mode)



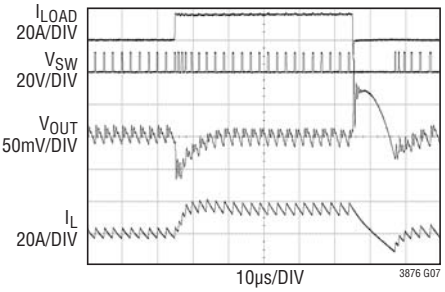
LOAD STEP = 500mA TO 15A
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Load Release VDDQ (Discontinuous Mode)



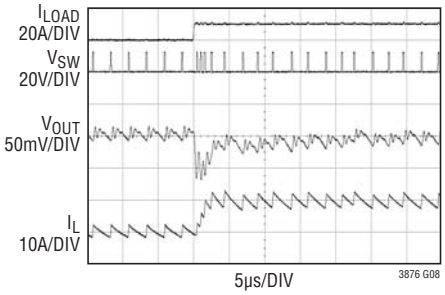
LOAD RELEASE = 15A TO 500mA
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Transient Response VTT (Forced Continuous Mode)



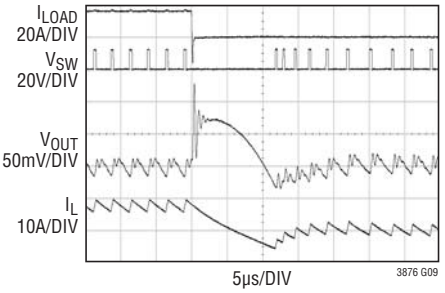
LOAD TRANSIENT = 0A TO 15A
V_{IN} = 12V
V_{OUT} = 1.5V
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

Load Step VTT (Forced Continuous Mode)



LOAD STEP = 0A TO 10A
V_{IN} = 12V
V_{OUT} = 0.75V
FIGURE 10 CIRCUIT, VTT CHANNEL 2

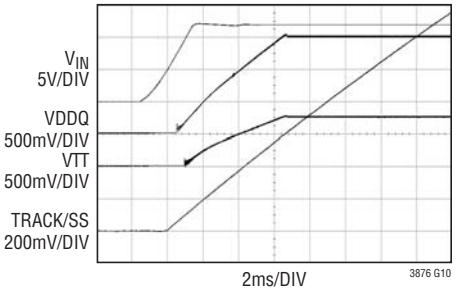
Load Release VTT



LOAD RELEASE = 10A TO 0A
V_{IN} = 12V
V_{OUT} = 0.75V
FIGURE 10 CIRCUIT, VTT CHANNEL 2

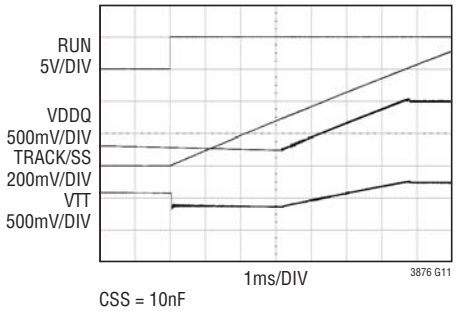
TYPICAL PERFORMANCE CHARACTERISTICS

Regular Soft Start-Up (Forced Continuous Mode)



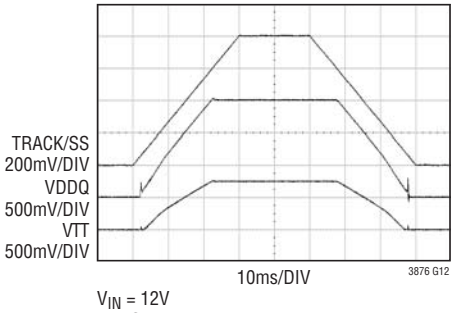
C_{SS} = 10nF
V_{IN} = 12V
VDDQ = 1.5V, VTT = 0.75V
FIGURE 10 CIRCUIT

Soft Start-Up Into Prebiased Output



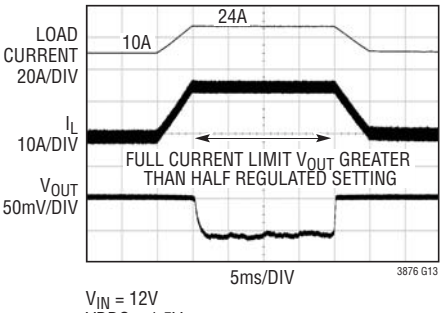
CSS = 10nF
V_{IN} = 12V
VDDQ = 1.5V, VTT = 0.75V
VDDQ PREBIASED TO 0.75V
VTT PREBIASED TO 0.6V
FIGURE 10 CIRCUIT

Output Tracking (Forced Continuous Mode)



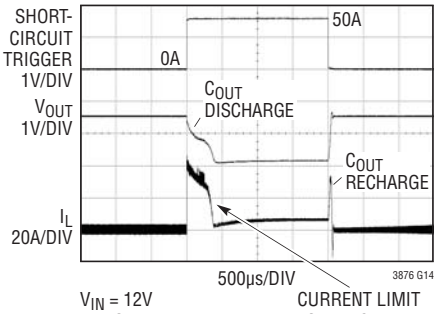
V_{IN} = 12V
VDDQ = 1.5V, VTT - 0.75V
FIGURE 10 CIRCUIT

Overcurrent Protection (Forced Continuous Mode)



V_{IN} = 12V
VDDQ = 1.5V
CURRENT LIMIT = 23A
OVERLOAD = 10A TO 17.5A
FICURE 10 CIRCUIT, VDDQ CHANNEL 1

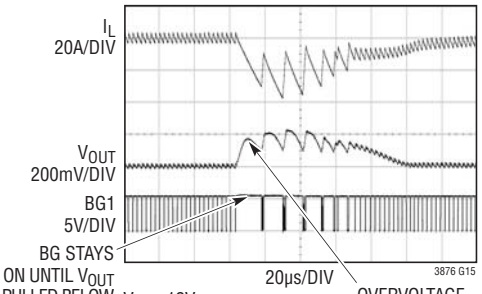
Short-Circuit Protection (Forced Continuous Mode)



V_{IN} = 12V
VDDQ = 1.5V
I_{LOAD} = 0A, SHORT = 50A
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

CURRENT LIMIT FOLDBACK V_{OUT} DROPS BELOW HALF REGULATED SET POINT

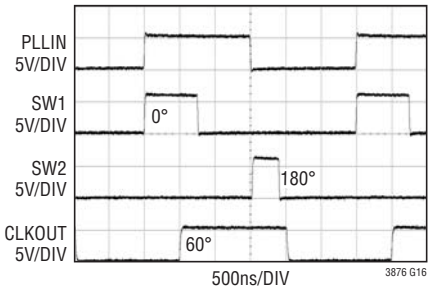
Overvoltage Protection (Forced Continuous Mode)



V_{IN} = 12V
VDDQ = 1.5V
I_{LOAD} = 0A
FIGURE 10 CIRCUIT, VDDQ CHANNEL 1

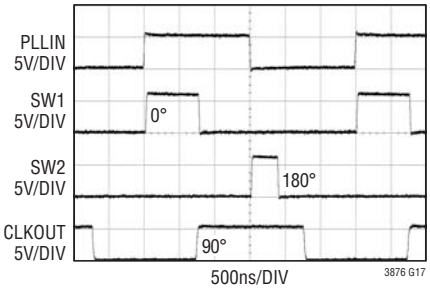
OVERVOLTAGE CREATED BY APPLYING A CHARGED CAPACITOR TO V_{OUT}

Phase Relationship: PHASMD = Ground (Forced Continuous Mode)



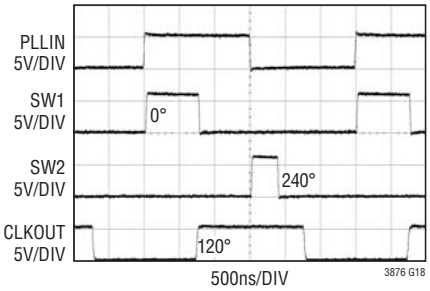
PHASMD = GND
V_{IN} = 6V
VDDQ = 1.5V, VTT = 0.75V
LOAD = 0A
FIGURE 10 CIRCUIT

Phase Relationship: PHASMD = Float (Forced Continuous Mode)



PHASMD = FLOAT
V_{IN} = 6V
VDDQ = 1.5V, VTT = 0.75V
LOAD = 0A
FIGURE 10 CIRCUIT

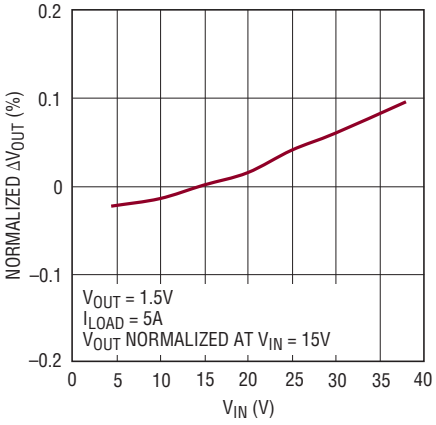
Phase Relationship: PHASMD = $INTV_{CC}$ (Forced Continuous Mode)



PHASMD = $INTV_{CC}$
V_{IN} = 6V
VDDQ = 1.5V, VTT = 0.75V
LOAD = 0A
FIGURE 10 CIRCUIT

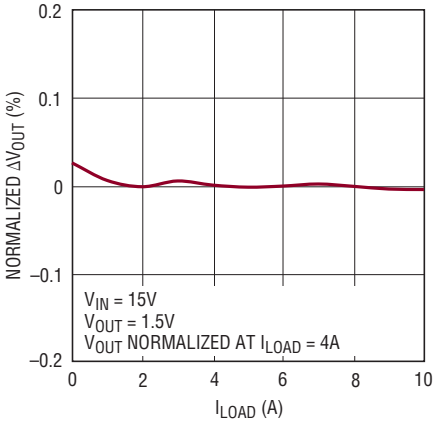
TYPICAL PERFORMANCE CHARACTERISTICS

Output Regulation vs Input Voltage VDDQ Channel 1



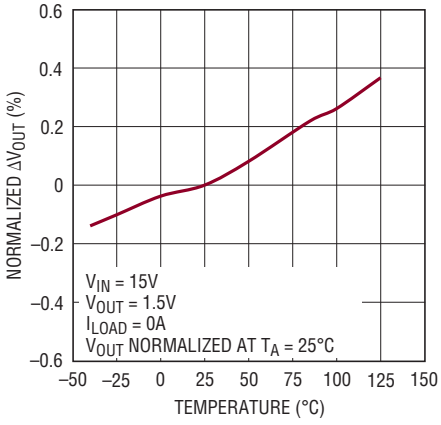
3876 G19

Output Regulation vs Load Current VDDQ Channel 1



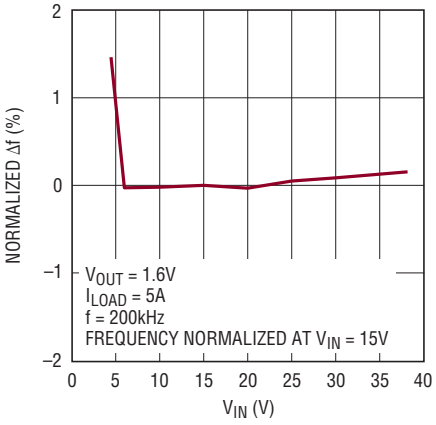
3876 G20

Output Regulation vs Temperature VDDQ Channel 1



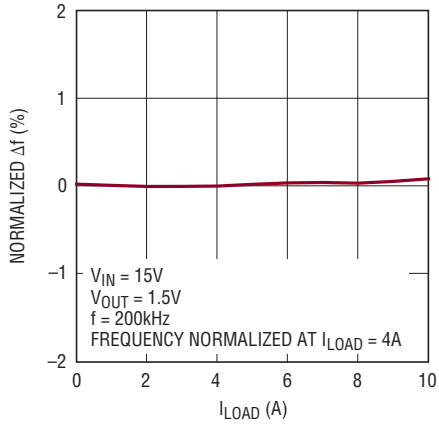
3876 G21

CLKOUT/Switching Frequency vs Input Voltage



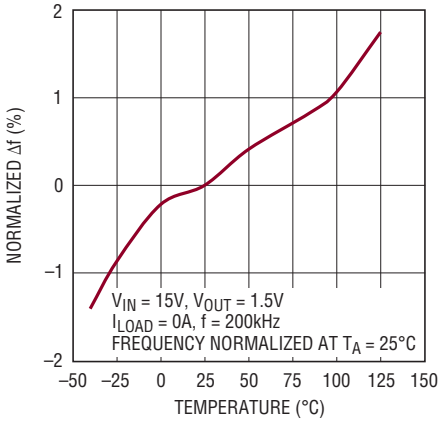
3876 G22

CLKOUT/Switching Frequency vs Load Current



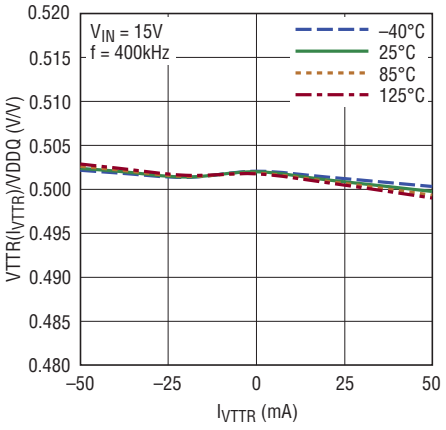
3876 G23

CLKOUT/Switching Frequency vs Temperature



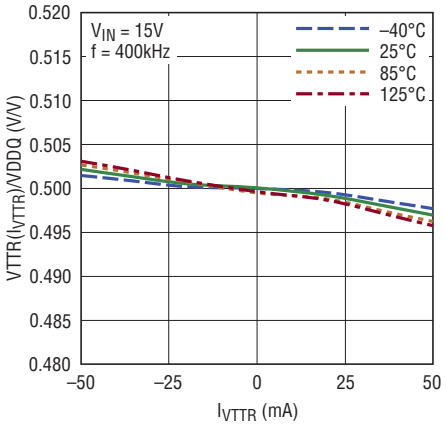
3876 G24

VTTR Load Regulation VDDQ = 2.5V



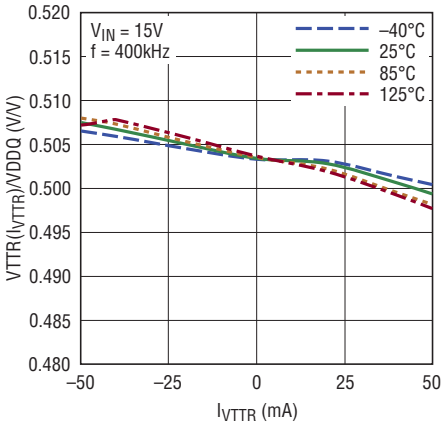
3876 G24

VTTR Load Regulation VDDQ = 1.5V



3876 G26

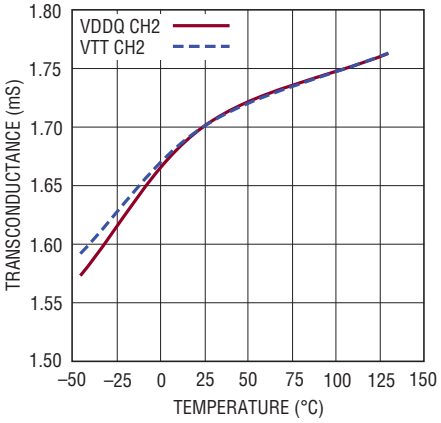
VTTR Load Regulation VDDQ = 1V



3876 G27

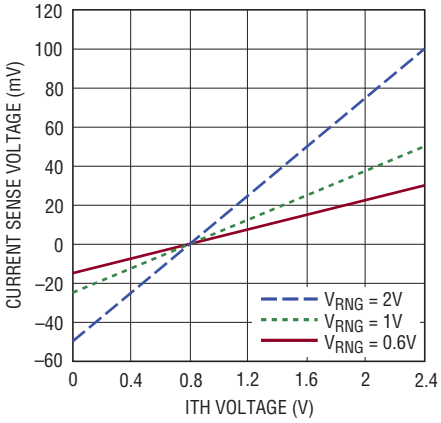
TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Transconductance vs Temperature



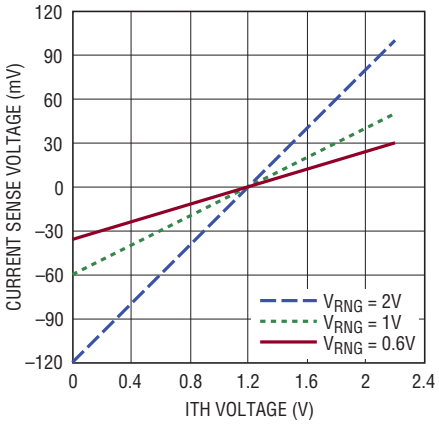
3876 G28

VDDQ Current Sense Voltage vs ITH Voltage



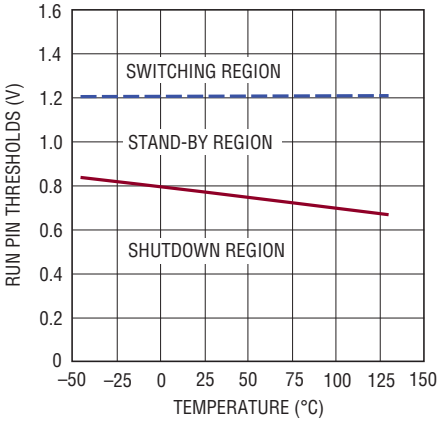
3876 G29

VTT Current Sense Voltage vs ITH Voltage



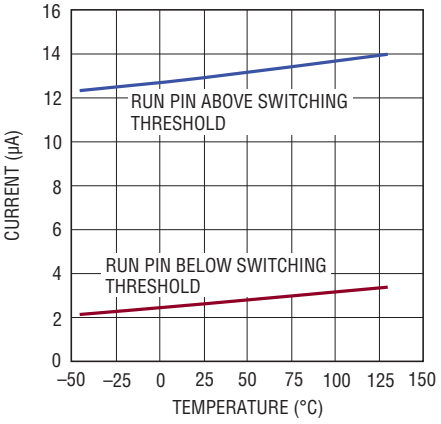
3876 G30

RUN Pin Thresholds vs Temperature



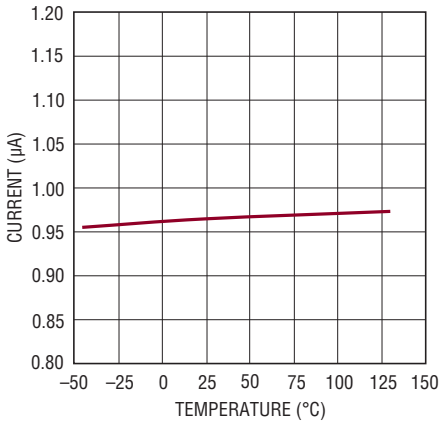
3876 G31

RUN Pull-Up Currents vs Temperature



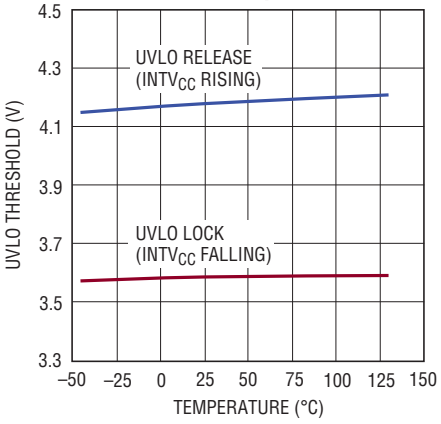
3876 G32

TRACK/SS Pull-Up Current vs Temperature



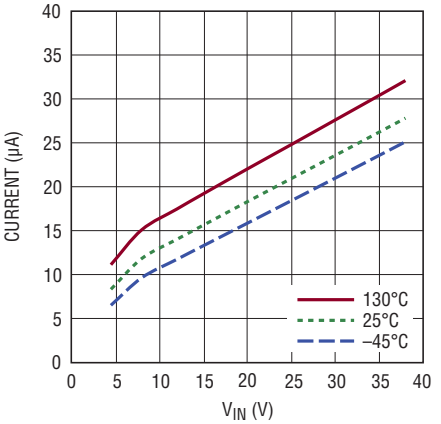
3876 G33

$INTV_{CC}$ Undervoltage Lockout Thresholds vs Temperature



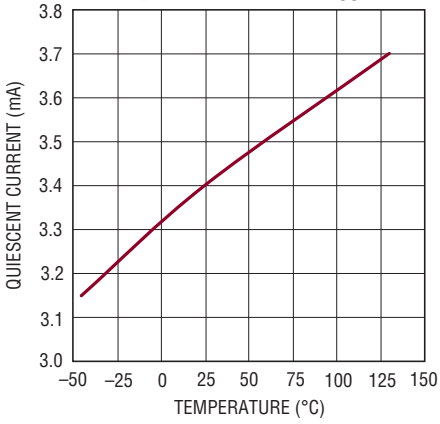
3876 G34

Shutdown Current into V_{IN} Pin vs Voltage on V_{IN} Pin



3876 G35

Quiescent Current Into V_{IN} Pin vs Temperature with $EXTV_{CC}$ = 0V



3876 G36

PIN FUNCTIONS (QFN/TSSOP)

ITH2 (Pin 1/Pin 5): Channel 2 VTT Current Control Threshold. This pin is the output of the error amplifier and the switching regulator's compensation point. The current comparator threshold increases with this control voltage. This voltage ranges from 0V to 2.2V. ITH2 has been optimized to support a symmetric range of positive and negative current by moving the zero sense voltage to 1.2V. (zero inductor valley current).

VDDQSNS (Pin 2/Pin 6): VDDQ Sense. VDDQSNS provides the VDDQ regulation reference point to the VTT differential reference resistor divider. The positive Input to the VTT differential reference resistor divider is VDDQSNS and negative input is $V_{OUTSENSE}^-$. The resistor divider is connected internally between VDDQSNS and $V_{OUTSENSE}^-$ and is composed of two equally sized 105k resistors in series for 210K total resistance.

When VDDQSNS is tied to $INTV_{CC}$, the VTTR linear reference outputs are three-stated and VTTR becomes the VTTSNS reference input. This allows the option to tie the VTTR reference input to the VTTR output of a second LTC3876 in a multiphase application.

VTTR (Pin 3/Pin 7): VTT Reference. VTTR is the buffered output of the VTT differential reference resistor divider. VTTR is specifically designed for large DDR memory systems by providing superior accuracy and load regulation specified for up to ±50mA. Connect VTTR directly to the DDR memory V_{REF} input. VTTR is a high output linear reference which tracks the VTT differential reference resistor divider and is equal to 0.5 • (VDDQSNS – $V_{OUTSENSE}^-$). Power is supplied through VTTRVCC. Internally the VTTR connection is connected to VDDQSNS reference in order to provide Kelvin sensing of VTTR. The output capacitor minimum should be 2.2µF.

VTTRVCC (Pin 4/Pin 8): VTTR Supply Input for VTTR Reference. Connect to DRV_{CC} through an RC decoupling filter of 2.2µF and 1Ω typically.

MODE/PLLIN (Pin 5/Pin 9): Operation Mode Selection or External Clock Synchronization Input. When this pin is tied to $INTV_{CC}$ forced continuous mode operation is selected. Typing this pin to SGND allows discontinuous mode operation on channel 1, VDDQ while channel 2, VTT operates in forced continuous mode. When an external clock is applied at this pin, both channels operate in forced continuous mode and are synchronized to the external clock. Channel 2 VTT operates in forced continuous mode only; permitting it to accurately track VTTR when sourcing and sinking load current.

CLKOUT (Pin 6/Pin 10): Clock Output of Internal Clock Generator. Its output level swings between $INTV_{CC}$ and SGND. If clock input is present at the MODE/PLLIN pin, it will be synchronized to the input clock, with phase set by the PHASMD pin. If no clock is present at the MODE/PLLIN pin, its frequency will be set by the RT pin. To synchronize other controllers, CLKOUT can be connected to their MODE/PLLIN pins.

SGND (Pin 7/Pin 11): Signal Ground. All small-signal analog components should be connected to this ground. Connect SGND to the exposed pad and PGND pin using a single PCB trace.

RT (Pin 8/Pin 12): Clock Generator Frequency Programming Pin. Connect an external resistor from RT to SGND to program the switching frequency between 200kHz and 2MHz. An external clock applied to MODE/PLLIN should be within ±30% of this programmed frequency to ensure frequency lock. When the RT pin is floating, the frequency is internally set to be slightly under 200kHz.

V_{RNG1}, V_{RNG2} (Pin 9, Pin 34/Pin 13, Pin 38): Current Sense Voltage Range Inputs. When programmed between 0.6V and 2V, the voltage applied to $V_{RNG1,2}$ is twenty times (20x) the maximum sense voltage between SENSE1,2$^+$ and SENSE1,2$^-$, i.e., for either channel, ($V_{SENSE}^+ – V_{SENSE}^-$) = 0.5 • V_{RNG}. If a V_{RNG} is tied to SGND the channel operates with a maximum sense voltage of 30mV, equivalent to a V_{RNG} of 0.6V; If tied to $INTV_{CC}$, a maximum sense voltage of 50mV, equivalent to a V_{RNG} of 1V. Do not float these pins.

ITH1 (Pin 10/Pin 14): Channel 1 VDDQ Current Control Threshold. This pin is the output of the error amplifier and the switching regulator's compensation point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V, with 0.8V corresponding to the zero sense voltage (zero inductor valley current).

PIN FUNCTIONS (QFN/TSSOP)

TRACK/SS1 (Pin 11/Pin 15): External Tracking and Soft-Start Input for Channel 1 VDDQ . An internal 1µA temperature-independent pull-up current source is connected to the TRACK/SS1 pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. The LTC3876 regulates V_{DFB1}, the differential feedback voltages ($V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$) to the smaller of 0.6V or the voltage on the TRACK/SS1 pin. Alternatively, another voltage supply connected to this pin allows the output to track the outer supply during start-up.

$V_{OUTSENSE1}^+$ (Pin 12/Pin 16): VDDQ Differential Output Sense Amplifier (+) Input of Channel 1. Connect this pin to a feedback resistor divider between the positive and negative output capacitor terminals of V_{OUT1}. In nominal operation the LTC3876 will attempt to regulate the differential output voltage V_{OUT1} to 0.6V multiplied by the feedback resistor divider ratio.

$V_{OUTSENSE1}^-$ (Pin 13/Pin 17): Differential Output Sense Amplifier (–) Input of Channel 1. Connect this pin to the negative terminal of the output load capacitor. This pin is the remote ground connection for VDDQSNS which provides the input to the VTT reference (VTTR) resistor divider.

SENSE1$^+$, SENSE2$^+$ (Pin 14, Pin 37/Pin 18, Pin 3): Differential Current Comparator (+) Input. The ITH pin voltage and controlled offsets between the SENSE$^+$ and SENSE$^-$ pins set the current trip threshold. The comparator can be used for R_{SENSE} sensing or inductor DCR sensing. For R_{SENSE} sensing Kelvin (4-wire) connect the SENSE$^+$ pin to the (+) terminal of R_{SENSE}. For DCR sensing tie the SENSE$^+$ pin to the connection between the DCR sense capacitor and sense resistor connected across the inductor.

SENSE1$^-$, SENSE2$^-$ (Pin 15, Pin 36/Pin 19, Pin 2): Differential Current Comparator(–) Input. The comparator can be used for R_{SENSE} sensing or inductor DCR sensing. For R_{SENSE} current sensing Kelvin (4-wire) connect the SENSE$^-$ pin to the (–) terminal of R_{SENSE}. For DCR sensing tie the SENSE$^-$ pin to the DCR sense capacitor tied to the inductor V_{OUT} node connection. These pins also function as output voltage sense pins for the top MOSFET on-time adjustment. The impedance looking into these pins is different from the SENSE$^+$ pins because there is an additional 500k internal resistor from each of the SENSE$^-$ pins to SGND.

DTR1 (Pin 16/Pin 20): Detect Load Transient Transient for Overshoot Reduction. When load current suddenly drops, if voltage on this DTR pin drops below half of $INTV_{CC}$, the bottom gate (BG) will turn off and allow the inductor current to drop to zero faster, thus reducing the V_{OUT} overshoot. (Refer to Load-Release Transient Detection in the Applications Information section for more details.) To disable the DTR feature, simply tie the DTR pin to $INTV_{CC}$.

RUN (Pin 17/Pin 21): Run Control Input. An internal proportional-to-absolute temperature (PTAT) pull-up current source (~2.5µA at 25°) is constantly connected to this pin. Taking RUN below a threshold (~0.8V at 25°) shuts down all bias of $INTV_{CC}$ and DRV_{CC} and places the LTC3876 into micropower shutdown mode. Allowing the RUN pin to rise above this threshold turns on the internal bias supply and all circuitry while forcing TG and BG off. When the RUN pin rises above 1.2V the TG and BG drivers are turned on and an additional 10µA temperature-independent pull-up current is connected internally to the RUN pin. The RUN pin can sink up to 50µA or be forced as high as 6V.

PGOOD (Pin 18/Pin 22): Power Good Indicator Output. This open-drain logic output is pulled to ground when VDDQ goes out of a ±7.5% or VTT goes out of a ±10% window around the regulation point, after a 50µs power-bad masking delay. Returning to the regulation point, there is a much shorted delay to power good, and a hysteresis of around 15mV on both sides of the window.

BOOST1, BOOST2 (Pin 19, Pin 32/Pin 23, Pin 36): Boosted Floating Driver Supply for Top MOSFET Drivers. The (+) terminal of the bootstrap capacitor CB connects to this pin. The BOOST pins swings between ($DRV_{CC} - V_{SCHOTTKY}$) and ($V_{IN} + DRV_{CC} - V_{SCHOTTKY}$).

TG1, TG2 (Pin 20, Pin 31/Pin 24, Pin 35): Top Gate Driver Outputs. The TG pins drive the gates of the top N-channel power MOSFET with a voltage swing of DRV_{CC} between SW and BOOST.

SW1, SW2 (Pin 21, Pin 30/Pin 25, Pin 34): Switch Node Connection to Inductors. Voltage swings are from a diode voltage below ground to V_{IN}. The (–) terminal of the bootstrap capacitor, CB connects to this node.

PIN FUNCTIONS (QFN/TSSOP)

BG1, BG2 (Pin 22, Pin 29/Pin 26, Pin 33): Bottom Gate Driver Outputs. The BG pins drive the gates of the bottom N-channel power MOSFET between PGND and DRV_{CC}.

DRV_{CC1}, DRV_{CC2} (Pin 23, Pin 28/Pin 27, Pin 32): Supplies of Bottom Gate Drivers. DRV_{CC1} is also the output of an internal 5.3V regulator, DRV_{CC2} is also the output of the $EXTV_{CC}$ switch. Normally the two DRV_{CC} pins are shorted together on the PCB, and decoupled to PGND with a minimum of 4.7µF ceramic capacitor, C_{DRVCC}.

V_{IN} (Pin 24/Pin 28): Input Voltage Supply. The supply voltage can range from 4.5V to 38V. For increased noise immunity decouple this pin to SGND with an RC filter. Voltage at this pin is also used to adjust top gate on-time, therefore it is recommended to tie this pin to the main power input supply through an RC filter.

PGND (Pin 25, Exposed Pad Pin 39/Pin 29, Exposed Pad Pin 39): Power Ground. Connect this pin as close as practical to the source of the bottom N-channel power MOSFET, the (–) terminal of C_{DRVCC} and the (–) terminal of C_{IN}. Connect the exposed pad and PGND pin to SGND pin using a single PCB trace under the IC. The exposed pad must be soldered to the circuit board for electrical and rated thermal performance.

$INTV_{CC}$ (Pin 26/Pin 30): Supply Input for Internal Circuitry (Not Including Gate Drivers). Normally powered from the DRV_{CC} pins through a decoupling RC filter to SGND (typically 2.2Ω and 1µF)

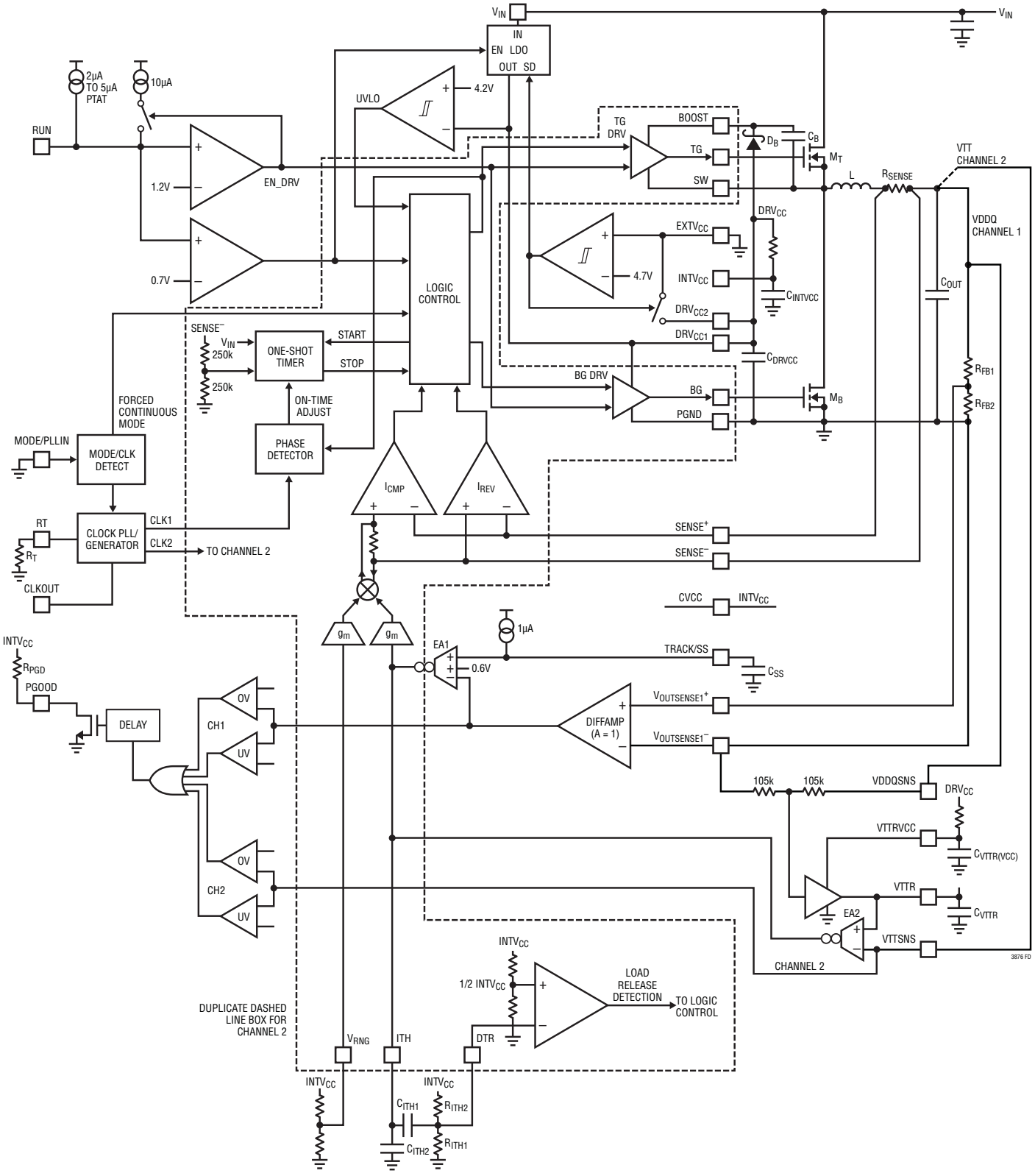
$EXTV_{CC}$ (Pin 27/Pin 31): External Power Input. When $EXTV_{CC}$ exceeds 4.7V, an internal switch connects this pin to DRV_{CC2} and shuts down the internal regulator so that $INTV_{CC}$ and gate-drive power is drawn from $EXTV_{CC}$. The V_{IN} pin still needs to be powered up but draws minimum current.

VTTSNS (Pin 33/Pin 37): VTT Sense, Channel 2 Error Amplifier Feedback Input. Kelvin-connect this pin directly to desired regulation point on the VTT supply, VTTSNS provides the inverting regulation feedback signal for the VTT termination supply. Internally the VTT error amplifier positive input connects to the VTTR output for accurate VTTR reference tracking. VTTSNS will regulate channel 2 VTT termination supply to the differential reference voltage $0.5 \bullet (VDDQSNS - V_{OUTSENSE1}^{-})$.

PHASMD (Pin 38/Pin 4): Phase Selector Input. This pin determines the relative phases of channels and the CLKOUT signal. With zero phase being defined as the rising edge of TG1: Pulling this pin to SGND locks TG2 to 180° and CLKOUT to 60°, Connecting this pin to $INTV_{CC}$ locks TG2 to 240° and CLKOUT to 120° and floating this pin locks TG2 to 180° and CLKOUT to 90°.

CVCC (Pin 35/Pin 1): Connect V_{CC}. This pin should always be connected to $INTV_{CC}$.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

DDR Operation

The LTC3876 is a dual channel, current mode step-down controller designed to provide high efficiency power conversion for high power DDR memory and bus termination supplies. Its unique controlled on-time architecture allows extremely low step-down ratio's while maintaining a fast, constant switching frequency.

The LTC3876 is a complete DDR power solution with one master RUN pin, TRACK/SS input and PGOOD output. The RUN pin enables all supplies. The TRACK/SS pin determines the VDDQ soft-start characteristics and VTT tracks 0.5 • VDDQ. PGOOD monitors both VDDQ and VTT to ensure regulation within a ±7.5% typical window. The current limit settings are set independently on both VDDQ and VTT channels. The VDDQ, VTT and CLKOUT phase relationships are set by the PHASMD pin to permit multiphase operation in high power DDR solutions which require more than one VDDQ or VTT channel.

VDDQ Supply

The LTC3876 is designed to support any DDR application where VDDQ can range from 2.5V down to 1V. The LTC3876 supports high power applications by differentially regulating the VDDQ supply, VTTR reference and VTT supply. The channel 1 feedback resistor divider, VDDQSNS and $V_{OUTSENSE}^-$ should be tied directly to the differential VDDQ regulation points. For best results these connections should be routed separately and Kelvin connected.

VDDQSNS is the VDDQ regulation sense point or positive input and $V_{OUTSENSE}^-$ is the remote ground sense point or negative input to the VTT differential reference resistor divider. The resistor divider is connected internally between VDDQSNS and $V_{OUTSENSE}^-$ and is composed of two equally sized 105k resistors in series for 210K total resistance.

VTT Supply

The VTT supply reference is connected internally to the output of the VTTR VTT reference output. VTTSNS provides the inverting regulation feedback signal for the VTT termination supply. Kelvin-connect the VTTSNS pin directly to desired regulation point on the VTT supply. By sensing VTTSNS the channel 2 VTT supply regulates to VTTR.

The VTT supply operates in forced continuous mode and tracks VDDQ in start-up and in normal operation regardless of the MODE/PLLIN settings. In start-up the VTT supply is enabled coincident with the VDDQ supply. Operating the VTT supply in forced continuous allows accurate tracking in startup and under all operating conditions.

VTT Reference (VTTR)

The linear VTT reference, VTTR, is specifically designed for large DDR memory systems by providing superior accuracy and load regulation for up to ±50mA output load. VTTR is the buffered output of the VTT differential reference resistor divider.

VTTR is a high output linear reference which tracks the VTT differential reference resistor divider and is equal to 0.5 • (VDDQSNS – $V_{OUTSENSE}^-$). Connect VTTR directly to the DDR memory V_{REF} input. Power is supplied through VTTRVCC. Internally the VTTR connection is connected to VDDQSNS reference to provide Kelvin sensing of VTTR.

Both input and output supply decoupling is important to performance and accuracy. A 2.2µF output capacitor is recommended for most typical applications. It is suggested to use no less than 1µF and no more than 47µF on the VTTR output. The typical recommended input VTTRVCC RC decoupling filter is 2.2µF and 1Ω.

When VDDQSNS is tied to $INTV_{CC}$, the VTTR linear reference output is three-stated and VTTR becomes the VTTSNS reference input. This allows the option to tie the VTTR reference input to the VTTR output of a second LTC3876 in a multiphase application.

Main Control Loop

The LTC3876 is a controlled on-time, valley current mode step-down DC/DC dual controller with two channels operating out of phase. Each channel drives both main and synchronous N-channel MOSFETs. The two channels operate independently where channel 1 is VDDQ and channel 2 is the VTT termination supply which tracks 0.5 • VDDQ.

The top MOSFET is turned on for a time interval determined by a one-shot timer. The one-shot timer or the top MOSFET's on-time is controlled to maintain a fixed switch-

OPERATION (Refer to Functional Diagram)

ing frequency. As the top MOSFET is turned off, the bottom MOSFET is turned on after a small delay. The delay, or dead time, is to avoid both top and bottom MOSFETs being on at the same time, causing shoot-through current from V_{IN} directly to power ground. The next switching cycle is initiated when the current comparator, I_{CMP}, senses that inductor current falls below the trip level set by voltages at the ITH and V_{RNG} pins. The bottom MOSFET is turned off immediately and the top MOSFET on again, restarting the one-shot timer and repeating the cycle. Again in order to avoid shoot-through current, there is a small dead-time delay before the top MOSFET turns on. At this moment, the inductor current hits its "valley" and starts to rise again.

Inductor current is determined by sensing the voltage between $SENSE^+$ and $SENSE^-$, either by using an explicit resistor connected in series with the inductor or by implicitly sensing the inductor's DC resistive (DCR) voltage drop through an RC filter connected across the inductor. The trip level of the current comparator, I_{CMP}, is proportional to the voltage at the ITH pin, with a zero-current threshold corresponding to an ITH of 0.8V for channel 1 and 1.2V for channel 2.

The error amplifier (EA) adjusts this ITH voltage by comparing the feedback signal to the internal reference voltage. On channel 1, the difference amplifier (DA) converts the differential feedback signal ($V_{OUTSENSE1}^+ – V_{OUTSENSE1}^-$) to a single-ended input for the EA; channel 2 uses VTTSNS directly. Output voltage is regulated so that the feedback voltage is equal to the internal reference. If the load current increases/decreases, it causes a momentary drop/rise in the differential feedback voltage relative to the reference. The EA then moves ITH voltage, or inductor valley current setpoint, higher/lower until the average inductor current again matches the load current, so that the output voltage comes back to the regulated voltage.

The LTC3876 features a detect transient (DTR) pin on channel 1 to detect "load-release", or a transient where the load current suddenly drops, by monitoring the first derivative of the ITH voltage. When detected, the bottom gate (BG) is turned off and inductor current flows through the body diode in the bottom MOSFET, allowing the SW node voltage to drop below PGND by the body diode's forward-conduction voltage. This creates a more negative differential voltage ($V_{SW} – V_{OUT}$) across the inductor, allowing the inductor current to drop faster to zero, thus creating less overshoot on V_{OUT}. See Load-Release Transient Detection in Applications Information for details.

Differential Output Sensing

This dual controller's first channel, VDDQ features differential output voltage sensing. The output voltage is resistively divided externally to create a feedback voltage for the controller. The internal difference amplifier (DIFFAMP) senses this feedback voltage with respect to the output's remote ground reference to create a differential feedback voltage. This scheme eliminates any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. Channel 1 allows remote output ground deviate as much as ±500mV with respect to local ground (SGND). Channel 2 VTT is referenced to VTTR internally which differentially tracks 0.5 • (VDDQSNS $– V_{OUTSENSE}^-$).

$DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

$DRV_{CC1,2}$ are the power for the bottom MOSFET drivers. Normally the two DRV_{CC} pins are shorted together on the PCB, and decoupled to PGND with a minimum 4.7µF ceramic capacitor, C_{DRVCC}. The top MOSFET drivers are biased from the floating bootstrap capacitors (C_B) which are recharged during each cycle through an external Schottky diode when the top MOSFET turns off and the SW pin swings down.

The DRV_{CC} can be powered on two ways: an internal low-dropout (LDO) linear voltage regulator that is powered from V_{IN} and can output 5.3V to DRV_{CC1}. Alternatively, an internal $EXTV_{CC}$ switch (with on-resistance of around 2Ω) can short the $EXTV_{CC}$ pin to DRV_{CC2}.

If the $EXTV_{CC}$ pin is below the $EXTV_{CC}$ switchover voltage (typically 4.7V with 200mV hysteresis, see the Electrical Characteristics Table), then the internal 5.3V LDO is enabled. If the $EXTV_{CC}$ pin is tied to an external voltage source greater than this $EXTV_{CC}$ switchover voltage, then the LDO is shut down and the internal $EXTV_{CC}$ switch shorts the $EXTV_{CC}$ pin to the DRV_{CC2} pin, thereby powering DRV_{CC}

OPERATION (Refer to Functional Diagram)

and $INTV_{CC}$ with the external voltage source and helping to increase overall efficiency and decrease internal self heating from power dissipated in the LDO. This external power source could be the output of the step-down converter itself, given that the output is programmed to higher than 4.7V. The V_{IN} pin still needs to be powered up but now draws minimum current.

Power for most internal control circuitry other than gate drivers is derived from the $INTV_{CC}$ pin. $INTV_{CC}$ can be powered from the combined DRV_{CC} pins through an external RC filter to SGND to filter out noises due to switching.

Shutdown and Start-Up

The RUN pin has an internal proportional-to-absolute temperature (PTAT) current source (around 2.5µA at 25°C) to pull up the pin. Taking the RUN pin below a certain threshold voltage (around 0.8V at 25°C) shuts down all bias of $INTV_{CC}$ and DRV_{CC} and places the LTC3876 into micropower shutdown mode with a minimum I_Q at the V_{IN} pin. The LTC3876's DRV_{CC} (through the internal 5.3V LDO regulator or $EXTV_{CC}$) and the corresponding channel's internal circuitry off $INTV_{CC}$ will be biased up when either or both RUN pins are pulled up above the 0.8V threshold, either by the internal pull-up current or driven directly by external voltage source such as logic gate output.

No channel of the LTC3876 will start switching until the RUN pin is pulled up to 1.2V. When the RUN pin rises above 1.2V, the TG and BG drivers are enabled, and TRACK/SS released. An additional 10µA temperature-independent pull-up current is connected internally to the RUN pin. To turn off TG, BG and the additional 10µA pull-up current, RUN needs to be pulled down below 1.2V by about 100mV. These built-in current and voltage hystereses prevent false jittery turn-on and turn-off due to noise. Such features on the RUN pin allows input undervoltage lockout (UVLO) to be set up using external voltage dividers from V_{IN}.

At start-up channel 1 is controlled by the voltage on the TRACK/SS pin and channel 2 tracks 0.500 • (VDDQSNS – $V_{OUTSENSE1^-}$). When the voltage on the TRACK/SS pin is less than the 0.6V internal reference, the (differential) feedback voltage is regulated to the TRACK/SS voltage instead of the 0.6V reference. The TRACK/SS pin can be used to program the output voltage soft-start ramp-up time by connecting an external capacitor from a TRACK/SS pin to signal ground. An internal temperature-independent 1µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from ground to 0.6V, the switching starts, VDDQ ramps up smoothly to its final value and the feedback voltage to 0.6V. TRACK/SS will keep rising beyond 0.6V, until being clamped to around 3.7V.

Alternatively, the TRACK/SS pin can be used to track an external supply like in a master slave configuration. Typically, this requires connecting a resistor divider from the master supply to the TRACK/SS pin (see the Applications Information section).

TRACK/SS1 is pulled low internally when the corresponding channel's RUN pin is pulled below the 1.2V threshold (hysteresis applies), or when $INTV_{CC}$ or either of the $DRV_{CC1,2}$ pins drop below their respective undervoltage lockout (UVLO) thresholds.

Channel 1 VDDQ Light Load Operation

If the MODE/PLLIN pin is tied to $INTV_{CC}$ or an external clock is applied to MODE/PLLIN, the LTC3876 will be forced to operate in continuous mode. With load current less than one-half of the full load peak-to-peak ripple, the inductor current valley can drop to zero or become negative. This allows constant-frequency operation but at the cost of low efficiency at light loads.

If the MODE/PLLIN pin is left open or connected to signal ground, channel 1 will transition into discontinuous mode operation, where a current reversal comparator (I_{REV}) shuts off the bottom MOSFET (M_B) as the inductor current approaches zero, thus preventing negative inductor current and improving light-load efficiency. Only VDDQ channel 1 is allowed to operate in discontinuous mode. The VTT channel 2 operates in forced continuous mode at all times independent of the MODE/PLLIN setting. In this mode, both channel 1 switches remain off. As the output capacitor discharges by load current and the output voltage droops lower, channel 1 EA will eventually move the ITH voltage above the zero current level (0.8V) to initiate another switching cycle.

OPERATION (Refer to Functional Diagram)

Power Good and Fault Protection

The PGOOD pin is connected to an internal open-drain N-channel MOSFET. An external resistor or current source can be used to pull this pin up to 6V (e.g., VDDQ/VTT or DRV_{CC}). Overvoltage or undervoltage comparators (OV, UV) turn on the MOSFET and pull the PGOOD pin low when the feedback voltage is outside the ±7.5% window of the 0.6V reference voltage. The PGOOD pin is also pulled low when the channel's RUN pin is below the 1.2V threshold (hysteresis applies), or in undervoltage lockout (UVLO). Note that feedback voltage of channel 1 is sensed differentially through $V_{OUTSENSE1}^+$ with respect to $V_{OUTSENSE1}^-$, while channel 2 is sensed through VTTSNS. PGOOD is only high when both channels are within window.

When the feedback voltage of channel 1 is within the ±7.5% window and channel 2 within the ±10% window, the open-drain NMOS is turned off and the pin is pulled up by the external source. The PGOOD pin will indicate power good immediately after the feedback is within the window. But when a feedback voltage of a channel goes out of the window, there is an internal 50µs delay before its PGOOD is pulled low. In an overvoltage (OV) condition, M_T is turned off and M_B is turned on immediately without delay and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is below one-half of the regulated voltage, such as being shorted to ground. As the feedback drops below one-half of the normal regulation point approaching 0V, the internal ITH clamp voltage gradually drops 2.4V to 1.3V for VDDQ channel 1 and 2.2V to 1.8V for VTT channel 2. This reduces the inductor valley current level to about one-third of its maximum value as the feedback approaches 0V. Foldback current limiting is disabled at start-up.

Frequency Selection and External Clock Synchronization

An internal oscillator (clock generator) provides phase-interleaved internal clock signals for individual channels to lock up to. The switching frequency and phase of each switching channel is independently controlled by adjusting the top MOSFET turn-on time (on-time) through the one-shot timer. This is achieved by sensing the phase relationship between a top MOSFET turn-on signal and its internal reference clock through a phase detector. The time interval of the one-shot timer is adjusted on a cycle-by-cycle basis, so that the rising edge of the top MOSFET turn-on is always trying to synchronize to the internal reference clock signal for the respective channel.

The frequency of the internal oscillator can be programmed from 200kHz to 2MHz by connecting a resistor, R_T, from the RT pin to signal ground (SGND). The RT pin is regulated to 1.2V internally.

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE/PLLIN pin can be used to synchronize the internal clock signals through a clock phase-locked loop (Clock PLL). The LTC3876 operates in forced continuous mode of operation when it is synchronized to the external clock. The external clock frequency has to be within ±30% of the internal oscillator frequency for successful synchronization. The clock input levels should be no less than 2V for "high" and no greater than 0.5V for "low". The MODE/PLLIN pin has an internal 600k pull-down resistor.

Multichip Operations

The PHASMD pin determines the relative phases between the internal reference clock signals for the two channels as well as the CLKOUT signal, as shown in Table 1. The phases tabulated are relative to zero degree (0°) being defined as the rising edge of the internal reference clock signal of channel 1. The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding either a single high current output, or separate outputs.

Table 1

PHASMD	SGND	FLOAT	$INTV_{CC}$
VDDQ Channel 1	0°	0°	0°
VTT Channel 2	180°	180°	240°
CLKOUT	60°	90°	120°

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Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirement, and begins with the selection of inductors and current sense method (either sense resistors R_{SENSE} or inductor DCR sensing). Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

Output Voltage Programming

As shown in Figure 1, external resistor dividers are used from the regulated outputs to their respective ground references to program the output voltages. On channel 1, the resistive divider is tapped by the $V_{OUTSENSE1}^+$ pin, and the ground reference is remotely sensed by the $V_{OUTSENSE1}^-$ pin, this voltage is sensed differentially. Connect the VTTSNS pin directly to the VTT output. By regulating the tapped (differential) feedback voltages to the internal reference 0.6V, the resulting output voltages are:

$$V(VDDQ) - V_{OUTSENSE1}^- = 0.6V \bullet (1 + R_{FB2}/R_{FB1})$$

and

$$V(VTT) = 0.500 \bullet (VDDQ - V_{OUTSENSE1}^-)$$

For example, if V_{OUT1} is programmed to 1.5V and the output ground reference is sitting at –0.5V with respect to SGND, then the absolute value of the output will be 2.0V with respect to SGND. The minimum (differential) output voltages are limited to the internal reference 0.6V, and the maximum are 5.5V.

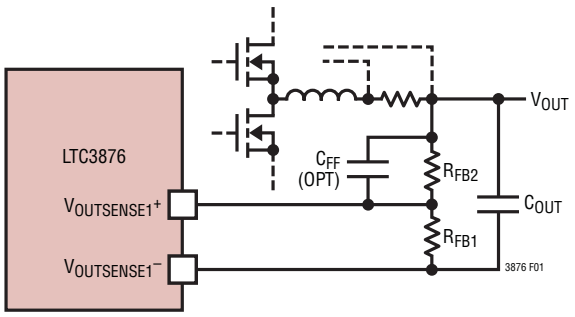

Figure 1. Setting Output Voltage

The $V_{OUTSENSE1}^+$ pin is a high impedance pin with no input bias current other than leakage in the nA range. The $V_{OUTSENSE1}^-$ pin has about 30µA of current flowing out of the pin. The VTTSNS pin is quasi-high impedance pin with minimum bias current out of the pin.

Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 2 illustrates the potential variations in the power and ground lines due to parasitic elements. The variations may be exacerbated in multi-application systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage. The LTC3876 channel 1's differential output sensing can correct for up to ±500mV of variation in the output's power and ground lines.

The LTC3876 channel 1's differential output sensing scheme is distinct from conventional schemes where the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistor divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

The LTC3876's channel 1 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range. The difference amplifier (DIFFAMP) of the LTC3876 has a bandwidth of 8MHz, high enough so that it will not affect main loop compensation and transient behavior.

To avoid noise coupling into the feedback voltage ($V_{OUTSENSE1}^+$), the resistor dividers should be placed close to the $V_{OUTSENSE1}^+$ and $V_{OUTSENSE1}^-$. Remote output and ground traces should be routed together as a differential pair to the remote output. For best accuracy, these traces to the remote output and ground should be connected as close as possible to the desired regulation point.

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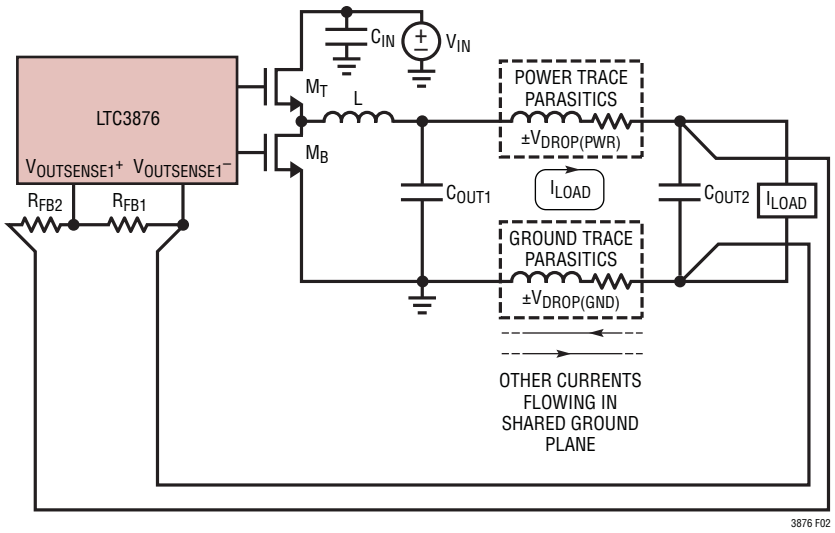

Figure 2. Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane

Switching Frequency Programming

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The switching frequency of the LTC3876 can be programmed from 200kHz to 2MHz by connecting a resistor from the RT pin to signal ground. The value of this resistor can be chosen according to:

$$R_T[k\Omega] = \frac{41550}{f(kHz)} - 2.2$$

The overall controller system, including the clock PLL and switching channels, has a synchronization range of no less than ±30% around this programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency. It is advisable that the RT programmed frequency be equal the external clock for maximum synchronization margin. Refer to the "Phase and Frequency Synchronization" section for more details.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, higher ESR losses in the output capacitor, and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{MAX}$. The maximum ΔI_L occurs at the maximum input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

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Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. The two basic types are iron powder and ferrite. The iron powder types have a soft saturation curve which means they do not saturate hard like ferrites do. However, iron powder type inductors have higher core losses. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation.

Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite core material saturates *hard*, which means that inductance collapses abruptly when the peak design current is exceeded. This results an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse and Würth.

Current Sense Pins

Inductor current is sensed through voltage between $SENSE^+$ and $SENSE^-$ pins, the inputs of the internal current comparators. The input voltage range of the SENSE pins is –0.5V to 5.5V. Care must be taken not to float these pins during normal operation. The $SENSE^+$ pins are quasi-high impedance inputs. There is no bias current into a $SENSE^+$ pin when its corresponding channel's $SENSE^-$ pin ramps up from below 1.1V and stays below 1.4V. But there is a small (~1µA) current flowing into a $SENSE^+$ pin when its corresponding $SENSE^-$ pin ramps down from 1.4V and stays above 1.1V. Such currents also exist on $SENSE^-$ pins. But in addition, each $SENSE^-$ pin has an internal 500k resistor to SGND. The resulted current (V_{OUT}/500k) will dominate the total current flowing into the $SENSE^-$ pins. $SENSE^+$ and $SENSE^-$ pin currents have to be taken into account when designing either R_{SENSE} or DCR inductor current sensing.

Current Limit Programming

The current sense comparators' maximum trip voltage between $SENSE^+$ and $SENSE^-$ (or "sense voltage"), when ITH is clamped at its maximum, is set by the voltage applied to the V_{RNG} pin and is given by:

$$V_{SENSE(MAX)} = 0.05V_{RNG}$$

The valley current mode control loop does not allow the inductor current valley to exceed $0.05V_{RNG}$. In practice, one should allow sufficient margin, to account for tolerance of the parts and external component values. Note that ITH is close to 2.4V for channel 1 and 2.2V for channel 2 when in positive current limit.

An external resistive divider from $INTV_{CC}$ can be used to set the voltage on a V_{RNG} pin between 0.6V and 2V, resulting in a maximum sense voltage between 30mV and 100mV. Such wide voltage range allows for variety of applications. The V_{RNG} pin can also be tied to either SGND or $INTV_{CC}$ to force internal defaults. When V_{RNG} is tied to SGND, the device has an equivalent V_{RNG} of 0.6V. When the V_{RNG} pin is tied to $INTV_{CC}$, the device has an equivalent V_{RNG} of 2V.

R_{SENSE} Inductor Current Sensing

The LTC3876 can be configured to sense the inductor currents through either low value series current sensing resistors (R_{SENSE}) or inductor DC resistance (DCR). The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller.

A typical R_{SENSE} inductor current sensing scheme is shown in Figure 3a. The filter components (R_F, C_F) need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair close together and (4-wire) Kelvin connected underneath the sense resistor, as shown in Figure 3b. Sensing current elsewhere can effectively add parasitic inductance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable.

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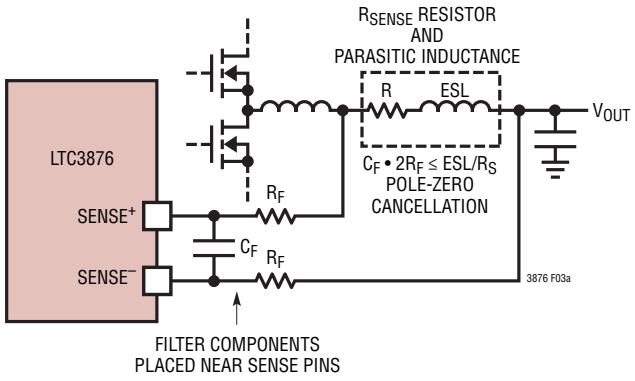

Figure 3a. R_{SENSE} Current Sensing

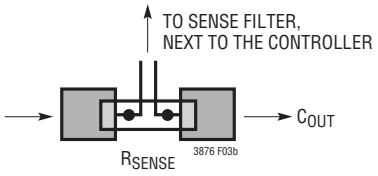

Figure 3b. Sense Lines Placement with Sense Resistor

R_{SENSE} is chosen based on the required maximum output current. Given the maximum current, $I_{OUT(MAX)}$, maximum sense voltage, $V_{SENSE(MAX)}$, set by V_{RNG}, and maximum inductor ripple current $\Delta I_{L(MAX)}$, the value of R_{SENSE} can be chosen as:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{OUT(MAX)} - \frac{\Delta I_{L(MAX)}}{2}}$$

Conversely, given R_{SENSE} and $I_{OUT(MAX)}$, $V_{SENSE(MAX)}$ and thus V_{RNG} voltage can be determined from the above equation. To ensure the maximum output current, sufficient margin should be built in the calculations to account for variations of LTC3876 under different operating conditions and tolerances of external components.

Because of possible PCB noise in the current sensing loop, the current sensing voltage ripple $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, 10mV of ΔV_{SENSE} is recommended as a conservative number to start with, either for R_{SENSE} or inductor DCR sensing applications.

For today's highest current density solutions the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 2MHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance becomes more relevant. A small RC filter placed near the IC has been traditionally used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 4a illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for a 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}}$$

where $V_{ESL(STEP)}$ is the voltage step caused by the ESL and shown in Figure 4a, and t_{ON} and t_{OFF} are top MOSFET on-time and off-time respectively. If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 4b. For applications using low $V_{SENSE(MAX)}$, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{RSENSE}.

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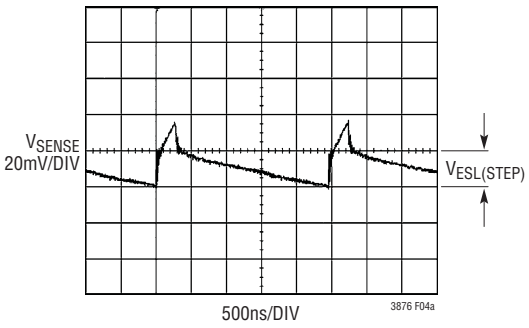

Figure 4a. Voltage Waveform Measured Directly Across the Sense Resistor

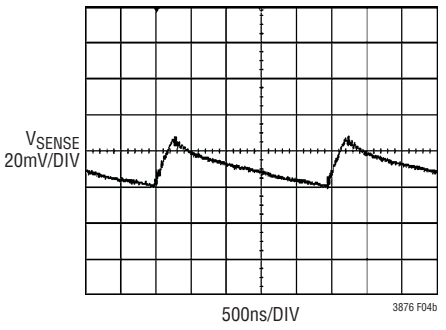

Figure 4b. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω

Note that the SENSE1⁻ and SENSE2⁻ pins are also used for sensing the output voltage for the adjustment of top gate on time, t_{ON}. For this purpose, there is an additional internal 500k resistor from each SENSE⁻ pin to SGND, therefore there is an impedance mismatch with their corresponding SENSE⁺ pins. The voltage drop across the R_F causes an offset in sense voltage. For example, with R_F = 100Ω, at V_{OUT} = V_{SENSE}^- = 5V, the sense-voltage offset $V_{SENSE(OFFSET)}$ = V_{SENSE}^- • R_F/500k = 1mV. Such small offset may seem harmless for current limit, but could be significant for current reversal detection (I_{REV}), causing excess negative inductor current at discontinuous mode. Also, at $V_{SENSE(MAX)}$ = 30mV, a mere 1mV offset will cause a significant shift of zero-current ITH voltage by (2.4V – 0.8V) • 1mV/30mV = 53mV. Too much shift may not allow the output voltage to return to its regulated value after the output is shorted due to ITH foldback. Therefore, when a larger filter resistor R_F value is used, it is recommended to use an *external* 500k resistor from each SENSE⁺ pin to SGND, to balance the *internal* 500k resistor at its corresponding SENSE⁻ pin.

The previous discussion generally applies to high density/high current applications where $I_{OUT(MAX)}$ > 10A and low inductor values are used. For applications where $I_{OUT(MAX)}$ < 10A, set R_F to 10Ω and C_F to 1000pF. This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin (4-wire) connected to the sense resistor.

DCR Inductor Current Sensing

For applications requiring higher efficiency at high load currents, the LTC3876 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 5. The DCR of the inductor represents the small amount of DC winding resistance, which can be less than 1mΩ for today's low value, high current inductors.

In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

The inductor DCR is sensed by connecting an RC filter across the inductor. This filter typically consists of one or two resistors (R1 and R2) and one capacitor (C1) as shown in Figure 5. If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by R2/(R1 + R2). Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than

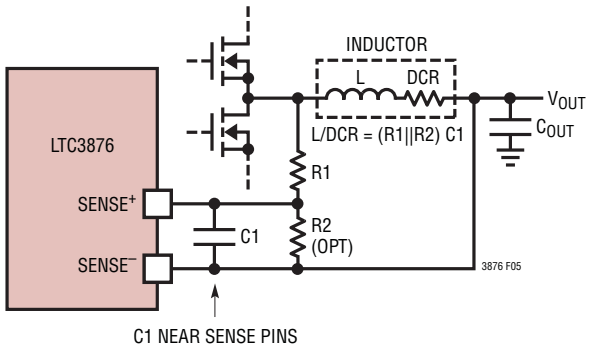

Figure 5. DCR Current Sensing

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the target sense resistance. With the ability to program current limit through the V_{RNG} pin, R2 may be optional. C1 is usually selected in the range of 0.01µF to 0.47µF. This forces R1||R2 to around 2k to 4k, reducing error that might have been caused by the SENSE pins' input bias currents.

Resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. Capacitor C1 should be placed close to the IC pins.

The first step in designing DCR current sensing is to determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 25°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for inductor temperature T_L is 100°C. The DCR of the inductor can also be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

From the DCR value, $V_{SENSE(MAX)}$ is easily calculated as:

$$V_{SENSE(MAX)} = DCR_{MAX(25°C)} \bullet \left[1 + 0.4\% \left(T_{L(MAX)} - 25°C\right)\right] \bullet \left(I_{OUT(MAX)} - \frac{\Delta I_L}{2}\right)$$

If $V_{SENSE(MAX)}$ is within the maximum sense voltage (30mV to 100mV) of the LTC3876 as programmed by the V_{RNG} pin, then the RC filter only needs R1. If $V_{SENSE(MAX)}$ is higher, then R2 may be used to scale down the maximum sense voltage so that it falls within range.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1) = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or R_{SENSE} sensing. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal-to-noise ratio for the current sense signal, start with a ΔV_{SENSE} of 10mV. For a DCR sensing application, the actual ripple voltage will be determined by:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \bullet \frac{V_{OUT}}{V_{IN} \bullet f}$$

Power MOSFET Selection

Two external N-channel power MOSFETs must be selected for each channel of the LTC3876 controller: one for the top (main) switch and one for the bottom (synchronous) switch. The gate drive levels are set by the DRV_{CC} voltage. This voltage is typically 5.3V. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified V_{DS} test voltage.

When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = 1 - \frac{V_{OUT}}{V_{IN}}$$

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The MOSFET power dissipations at maximum output current are given by:

$$P_{TOP} = D_{TOP} \bullet I_{OUT(MAX)}^2 \bullet R_{DS(ON)(MAX)} (1+\delta) + V_{IN}^2 \bullet \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet C_{MILLER} \left[\frac{R_{TG(HI)}}{V_{DRVCC} - V_{MILLER}} + \frac{R_{TG(LO)}}{V_{MILLER}}\right] \bullet f$$

$$P_{BOT} = D_{BOT} \bullet I_{OUT(MAX)}^2 \bullet R_{DS(ON)(MAX)} \bullet (1 + \delta)$$

where δ is the temperature dependency of $R_{DS(ON)}$, $R_{TG(HI)}$ is the TG pull-up resistance, and $R_{TG(LO)}$ is the TG pull-down resistance. V_{MILLER} is the Miller effect V_{GS} voltage and is taken graphically from the MOSFET's data sheet.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve in the power MOSFET data sheet. For low voltage MOSFETs, 0.5% per degree (°C) can be used to estimate δ as an approximation of percentage change of $R_{DS(ON)}$:

$$\delta = 0.005/°C \bullet (T_J - T_A)$$

where T_J is estimated junction temperature of the MOSFET and T_A is ambient temperature.

C_{IN} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The worst-case RMS current occurs by assuming a single-phase application. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3876, additional ceramic capacitors should also be used in parallel for C_{IN} close to the IC and power switches to bypass the high frequency switching noises. Typically multiple X5R or X7R ceramic capacitors are put in parallel with either conductive-polymer or aluminum-electrolytic types of bulk capacitors. Because of its low ESR, the ceramic capacitors will take most of the RMS ripple current. Vendors do not consistently specify the ripple current rating for ceramics, but ceramics *could* also fail due to excessive ripple current. Always consult the manufacturer if there is any question.

Figure 6 represents a simplified circuit model for calculating the ripple currents in each of these capacitors. The input inductance (L_{IN}) between the input source and the input of the converter will affect the ripple current through

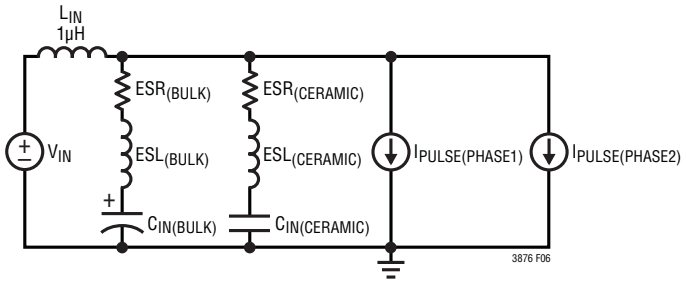

Figure 6. Circuit Model for Input Capacitor Ripple Current Simulation

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the capacitors. A lower input inductance will result in less ripple current through the input capacitors since more ripple current will now be flowing out of the input source.

For simulating positive output current loading using this model, look at the ripple current during steady-state for the case where one phase is fully loaded and the other is not loaded. This will in general be the worst-case for ripple current since the ripple current from one phase will not be cancelled by ripple current from the other phase.

The LTC3876 is more complex than this example because the VTT channel can provide significant negative current. For the LTC3876 steady state worst-case, look at the condition where VDDQ channel is fully loaded and the VTT channel is supplying maximum negative current. This will in *general* be the worst-case for ripple current since the ripple current from VTT will add with ripple current from VDDQ when the VTT channel sinks or provides negative current.

Note that the bulk capacitor also has to be chosen for RMS rating with ample margin beyond its RMS current per simulation with the circuit model provided. For a lower V_{IN} range, a conductive-polymer type (such as Sanyo OS-CON) can be used for its higher ripple current rating and lower ESR. For a wide V_{IN} range that also require higher voltage rating, aluminum-electrolytic capacitors are more attractive since it can provide a larger capacitance for more damping. An aluminum-electrolytic capacitor with a ripple current rating that is high enough to handle all of the ripple current by itself will be very large. But when in parallel with ceramics, an aluminum-electrolytic capacitor will take a much smaller portion of the RMS ripple current due to its high ESR. However, it is crucial that the ripple current through the aluminum-electrolytic capacitor should not exceed its rating since this will produce significant heat, which will cause the electrolyte inside the capacitor to dry over time and its capacitance to go down and ESR to go up.

While it is always safest to choose the input capacitors RMS rating according to the worst-case single-phase application with negative VTT current as discussed above, it is likely not necessary. For DDR memory, the VTT output load current will statistically approach zero and should never operate at sustained negative current for any significant period of time in normal operation. There could be DDR test conditions which do exercise such extremes, but again this should not be continuous. Therefore, determine the worst-case RMS requirement for the input capacitors and reduce as appropriate for sufficient margin.

The V_{IN} sources of the top MOSFETs should be placed close to each other and share common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the IC's V_{IN} pin and ground, placed close to the IC, is suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} and the V_{IN} pin is also recommended as it provides further isolation from switching noise of the two channels.

C_{OUT} Selection

The selection of output capacitance C_{OUT} is primarily determined by the effective series resistance, ESR, to minimize voltage ripple. The output voltage ripple ΔV_{OUT}, in continuous mode is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(R_{ESR} + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is operating frequency, and ΔI_L is ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds that required from ripple current.

In single-output applications, for the same reason that LTC3876 is only truly phase interleaved at steady state, ripple current of individual channels could add up in transient, it is advisable to consider using the worst-case ΔI_L, i.e., the sum of the ΔI_L of all individual channels, in the calculation of ΔV_{OUT}.

The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage.

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Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability.

Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high-Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller.

For high switching frequencies, reducing output ripple and better EMI filtering may require small value capacitors that have low ESL (and correspondingly higher self-resonant frequencies) to be placed in parallel with larger value capacitors that have higher ESL. This will ensure good noise and EMI filtering in the entire frequency spectrum of interest. Even though ceramic capacitors generally have good high frequency performance, small ceramic capacitors may still have to be parallel connected with large ones to optimize performance.

High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance. Remember also to place high frequency decoupling capacitors as close as possible to the power pins of the load.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from DRV_{CC} when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + $INTV_{CC}$. The boost capacitor needs to store approximately 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. It is recommended that the BOOST capacitor be no larger than 10% of the DRV_{CC} capacitor, C_{DRVCC}, to ensure that the C_{DRVCC} can supply the upper MOSFET gate charge and BOOST capacitor under all operating conditions. Variable frequency in response to load steps offers superior transient performance but requires higher instantaneous gate drive. Gate charge demands are greatest in high frequency low duty factor applications under high load steps and at start-up.

DRV_{CC} Regulator and $EXTV_{CC}$ Power

The LTC3876 features a PMOS low dropout (LDO) linear regulator that supplies power to DRV_{CC} from the V_{IN} supply. The LDO regulates its output at the DRV_{CC1} pin to 5.3V. The LDO can supply a maximum current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to minimize interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3876 to be exceeded, especially if the LDO is active and provides DRV_{CC}. Power dissipation for the IC in this case is highest and is approximately equal to $V_{IN} \bullet I_{DRVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equation given in Note 2 of the Electrical Characteristics. For example, when using the LDO, LTC3876's DRV_{CC} current is limited to less than 52mA from a 38V supply at T_A = 70°C in the FE package:

$$T_J = 70°C + (52mA)(38V)(28°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode at maximum V_{IN}.

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When the voltage applied to the $EXTV_{CC}$ pin rises above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ is connected to DRV_{CC2} pin with an internal switch. This switch remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from the LTC3876's switching regulator output V_{OUT} during normal operation and from the LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and DRV_{CC} pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC}$ is less than V_{IN}.

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from the switching converter output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (duty cycle)/(switcher efficiency).

Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (52mA)(5V)(28°C/W) = 77°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive DRV_{CC} power from the converter output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.3V LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to switching converter output V_{OUT} > 4.7V. This provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 4.7V or greater external supply is available, it may be used to power $EXTV_{CC}$ providing that the external supply is sufficient for MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage converters, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power never exceeds 5.3V, tie the DRV_{CC1} and DRV_{CC2} pins to the V_{IN} input through a small resistor, (such as 1Ω to 2Ω) as shown in Figure 7 to minimize the voltage drop caused by the gate charge current. This will override the LDO and will prevent DRV_{CC} from dropping too low due to the dropout voltage. Make sure the DRV_{CC} voltage exceeds the $R_{DS(ON)}$ test voltage for the external MOSFET which is typically at 4.5V for logic-level devices.

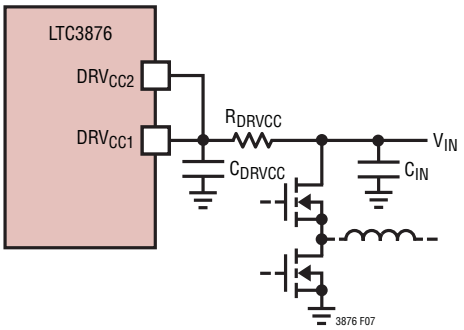

Figure 7. Setup for $V_{IN} \leq 5.3V$

Input Undervoltage Lockout (UVLO)

The LTC3876 has two functions that help protect the controller in case of input undervoltage conditions. An internal UVLO comparator constantly monitors the $INTV_{CC}$ and DRV_{CC} voltages to ensure that adequate voltages are present. The comparator enables internal UVLO signal, which locks out the switching action of both channels, until the $INTV_{CC}$ and $DR_{VCC1,2}$ pins are all above their respective UVLO thresholds. The rising threshold (to release UVLO) of the $INTV_{CC}$ is typically 4.2V, with 0.5V falling hysteresis (to re-enable UVLO). The UVLO thresholds for $DR_{VCC1,2}$ are lower than that of $INTV_{CC}$ but higher than typical threshold voltages of power MOSFETs, to prevent them from turning on without sufficient gate drive voltages.

Generally for V_{IN} > 6V, a UVLO can be set through monitoring the V_{IN} supply by using external voltage dividers at the RUN pins from V_{IN} to SGND. To design the voltage divider, note that both RUN pins have two levels of threshold voltages. The precision gate-drive-enable threshold voltage of 1.2V

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can be used to set a V_{IN} to turn on a channel's switching. If resistor dividers are used on both RUN pins, when V_{IN} is low enough and both RUN pins are pulled below the ~0.8V threshold, the part will shut down all bias of $INTV_{CC}$ and DRV_{CC} and be put in micropower shutdown mode.

The RUN pins' bias currents depend on the RUN voltages. The bias current changes should be taken into account when designing the external voltage divider UVLO circuit. An internal proportional-to-absolute-temperature (PTAT) pull-up current source (~2.5µA at 25°C) is constantly connected to this pin. When a RUN pin rises above 1.2V, the corresponding channel's TG and BG drives are turned on and an *additional* 4µA temperature-independent pull-up current is connected internally to the RUN pin. Pulling the RUN pin to fall below 1.2V by more than an 80mV hysteresis turns off TG and BG of the corresponding channel, and the additional 10µA pull-up current is disconnected.

As voltage on a RUN pin increases, typically beyond 3V, its bias current will start to reverse direction and flow into the RUN pin. Keep in mind that *neither* of the RUN pins can sink more than 50µA; Even if a RUN pin may slightly exceed 6V when sinking 50µA, a RUN pin should *never* be forced to higher than 6V by a low impedance voltage source to prevent faulty conditions.

Soft-Start and Tracking

The LTC3876 has the ability to either soft-start by itself with a capacitor or track the output of another channel or an external supply. Note that the soft-start or tracking features are achieved not by limiting the maximum output current of the controller, but by controlling the output ramp voltage according to the ramp rate on the TRACK/SS pin.

When channel 1 is configured to soft-start by itself, a capacitor should be connected to its TRACK/SS pin. TRACK/SS is pulled low until the RUN pin voltage exceeds 1.2V and UVLO is released, at which point an internal current of 1µA charges the soft-start capacitor, C_{SS}, connected to the TRACK/SS pin. Current-limit foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SS}(SEC) = 0.6(V) \bullet \frac{C_{SS}(\mu F)}{1(\mu A)}$$

When one particular channel is configured to track an external supply, a voltage divider can be used from the external supply to the TRACK/SS pin to scale the ramp rate appropriately. Two common implementations are coincidental tracking and ratiometric tracking. For coincident tracking, make the divider ratio from the external supply the same as the divider ratio for the differential feedback voltage. Ratiometric tracking could be achieved by using a different ratio than the differential feedback.

Note that the 1µA soft-start capacitor charging current is still flowing, producing a small offset error. To minimize this error, select the tracking resistive divider values to be small enough to make this offset error negligible.

The LTC3876 allows the user to program how channel 1 VDDQ tracks an external power supply. Channel 2 VTT will always track VDDQ and be equal to 0.5 • VDDQ.

By selecting different resistors, the LTC3876 can achieve different modes of tracking including the two in Figure 8a. To implement the coincident tracking, connect an additional resistive divider to the external power supply and connect its midpoint to the TRACK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 8b. In this tracking mode, the external power supply must be set higher than VDDQ. To implement the ratiometric tracking, the master channel's feedback divider can be also used to provide TRACK/SS voltage for the slave channel, since the additional divider, if used, should be of the same ratio as the master channel's feedback divider.

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So which mode should be programmed? While either mode satisfies most practical applications, some trade-offs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation.

When the master channel's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

Phase and Frequency Synchronization

For applications that require better control of EMI and switching noise or have special synchronization needs, the LTC3876 can synchronize the turn-on of the top MOSFET to an external clock signal applied to the MODE/PLLIN pin. The applied clock signal needs to be within ±30% of the RT programmed frequency to ensure proper frequency and phase lock. The clock signal levels should generally comply to $V_{PLLIN(H)} > 2V$ and $V_{PLLIN(L)} < 0.5V$. The MODE/PLLIN pin has an internal 600k pull-down resistor to ensure discontinuous current mode operation if the pin is left open.

The LTC3876 uses the voltages on V_{IN} and V_{OUT} pins as well as R_T to adjust the top gate on-time in order to maintain phase and frequency lock for wide ranges of V_{IN}, V_{OUT} and R_T-programmed switching frequency f:

$$t_{ON} \approx \frac{V_{OUT}}{V_{IN} \bullet f}$$

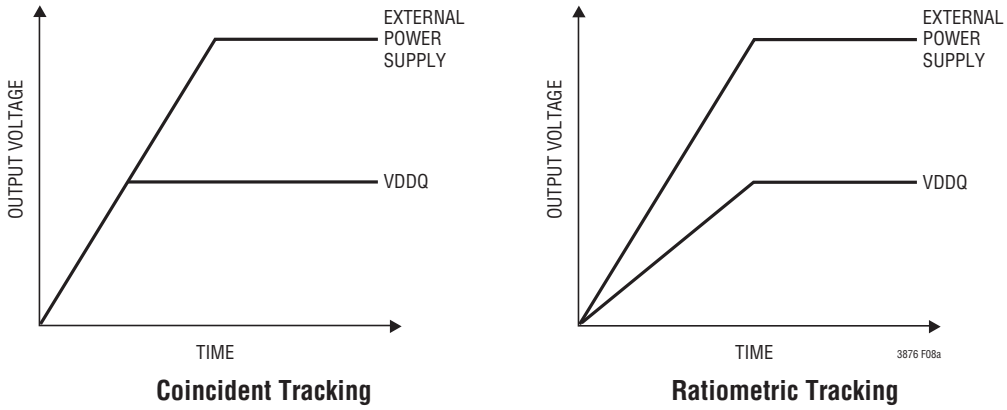

Figure 8a. Two Different Modes of Output Tracking

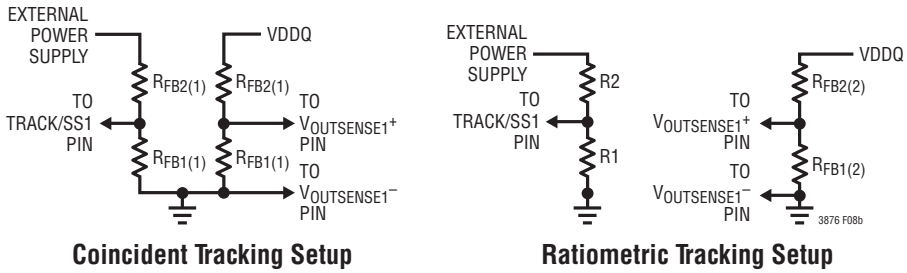

Figure 8b. Setup for Coincident and Ratiometric Tracking

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As the on-time is a function of the switching regulator's output voltage, this output is measured by the V_{OUT} pin to set the required on-time. Simply connecting V_{OUT} to the regulator's local output point is preferable for most applications, as the remotely regulated output point could be significantly different from the local output point due to line losses, and local output versus local ground is typically the V_{OUT} required for the calculation of t_{ON}.

However, there could be circumstances where this V_{OUT} programmed on-time differs significantly different from the on-time required in order to maintain frequency and phase lock. For example, lower efficiencies in the switching regulator can cause the required on-time to be substantially higher than the internally set on-time (see Efficiency Considerations). If a regulated V_{OUT} is relatively low, proportionally there could be significant error caused by the difference between the local ground and remote ground, due to other currents flowing through the shared ground plane.

During dynamic transient conditions either in the line voltage or load current (e.g., load step or release), the top switch will turn on more or less frequently in response to achieve faster transient response. This is the benefit of the LTC3876's controlled on-time, valley current mode architecture. However, this process may understandably lose phase and even frequency lock momentarily. For relatively slow changes, phase and frequency lock can still be maintained. For large load current steps with fast slew rates, phase lock will be lost until the system returns back to a steady-state condition (see Figure 9). It may take up to several hundred microseconds to fully resume the phase lock, but the frequency lock generally recovers quickly, long before phase lock does.

For light load conditions, the phase and frequency synchronization depends on the MODE/PLLIN pin setting. If the external clock is applied, synchronization will be active and switching in continuous mode. If MODE/PLLIN is tied to $INTV_{CC}$, it will operate in forced continuous mode at the R_T-programmed frequency. If the MODE/PLLIN pin is tied to SGND, the LTC3876 will operate in discontinuous mode at light load and switch into continuous conduction at the R_T programmed frequency as load increases. The TG on-time during discontinuous conduction is intentionally slightly extended (approximately 1.2 times the continuous conduction on-time as calculated from V_{IN}, V_{OUT} and f) to create hysteresis at the load-current boundary of continuous/discontinuous conduction.

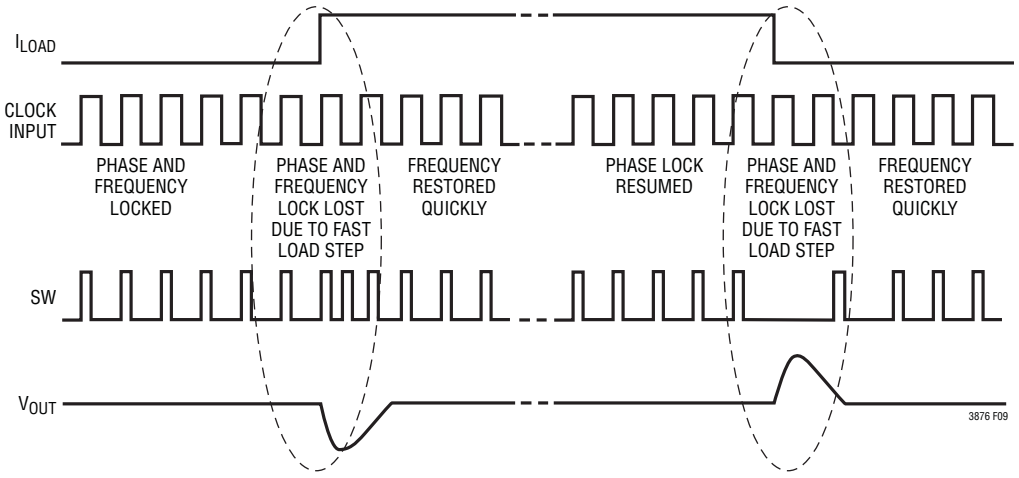

Figure 9. Phase and Frequency Locking Behavior During Transient Conditions

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If an application requires very low (approaching minimum) on-time, the system may not be able to maintain its full frequency synchronization range. Getting closer to minimum on-time, it may even lose phase/frequency lock at no load or light load conditions, under which the SW on-time is effectively longer than TG on-time due to TG/BG dead times. This is discussed further under Minimum On-Time, Minimum Off-Time and Dropout Operation.

Minimum On-Time, Minimum Off-Time and Dropout Operation

The minimum on-time is the smallest duration that LTC3876's TG (top gate) pin can be in high or "on" state. It has dependency on the operating conditions of the switching regulator, and is a function of voltages on the V_{IN} and V_{OUT} pins, as well as the value of external resistor R_T. A minimum on-time of 30ns can be achieved when the V_{OUT} pin is tied to its minimum value of 0.6V while the V_{IN} is tied to its maximum value of 38V. For larger values of V_{OUT} and/or smaller values of V_{IN}, the minimum achievable on-time will be longer. The valley mode control architecture allows low on-time, making the LTC3876 suitable for high step-down ratio applications.

The *effective* on-time, as determined by the SW node pulse width, can be different from this TG on-time, as it also depends on external components, as well as loading conditions of the switching regulator. One of the factors that contributes to this discrepancy is the characteristics of the power MOSFETs. For example, if the top power MOSFET's turn-on delay is much smaller than the turn-off delay, the effective on-time will be longer than the TG on-time, limiting the effective minimum on-time to a larger value.

Light-load operation, in forced continuous mode, will further elongate the effective on-time due to the dead times between the "on" states of TG and BG, as shown in Figure 10. During the dead time from BG turn-off to TG turn-on, the inductor current flows in the reverse direction, charging the SW node high before the TG actually turns on. The reverse current is typically small, causing a slow rising edge. On the falling edge, after the top FET turns off and before the bottom FET turns on, the SW node lingers high for a longer duration due to a smaller peak inductor current available in light load to pull the SW node low. As a result of the sluggish SW node rising and falling edges, the effective on-time is extended and not fully controlled by the TG on-time. Closer to minimum on-time, this may cause some phase jitter to appear at light load. As load current increase, the edges become sharper, and the phase locking behavior improves.

The minimum on-time of the VTT channel is further limited by the fact that it must support negative current operation. Both the TG to BG and BG to TG dead-time delays add

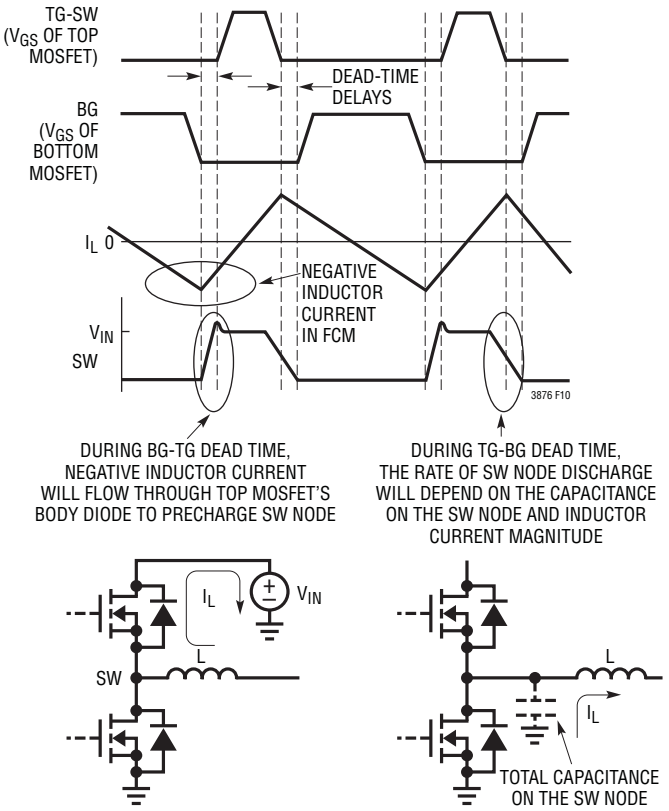

Figure 10. Light Loading On-Time Extension for Forced Continuous Mode Operation

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to the minimum on-time of 30ns as shown in Figure 10. Each of the dead times are in the order of 35ns. Therefore, the VTT channel minimum on time should be no less than 100ns with 150ns preferred.

In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$D_{MIN} = f \bullet t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the effective minimum on-time for the switching regulator. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. If the minimum on-time that LTC3876 can provide is longer than the on-time required by the duty cycle to maintain the switching frequency, the switching frequency will have to decrease to maintain the duty cycle, but the output voltage will still remain in regulation. This is generally more preferable to skipping cycles and causing larger ripple at the output, which is typically seen in fixed frequency switching regulators.

For applications that require relatively low on-time, proper caution has to be taken when choosing the power MOSFET. If the gate of the MOSFET is not able to fully turn on due to insufficient on-time, there could be significant heat dissipation and efficiency loss as a result of larger $R_{DS(ON)}$. This may even cause early failure of the power MOSFET.

The minimum off-time is the smallest duration of time that the TG pin can be turned low and then immediately turned back high. This minimum off-time includes the time to turn on the BG (bottom gate) and turn it back off, plus the dead-time delays from TG off to BG on and from BG off to TG on. The minimum off-time that the LTC3876 can achieve is 90ns.

The *effective* minimum off-time of the switching regulator, or the shortest period of time that the SW node can stay low, can be different from this minimum off-time. The main factor impacting the effective minimum off-time is the top and bottom power MOSFETs' electrical characteristics, such as Qg and turn-on/off delays. These characteristics can either extend or shorten the SW nodes' effective minimum off-time. Large size (high Qg) power MOSFETs generally tend to increase the effective minimum off-time due to longer gate charging and discharging times. On the other hand, imbalances in turn-on and turn-off delays could reduce the effective minimum off-time.

The minimum off-time limit imposes a maximum duty cycle of:

$$D_{MAX} = 1 - f \bullet t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the effective minimum off-time of the switching regulator. Reducing the operating frequency can alleviate the maximum duty cycle constraint.

If the maximum duty cycle is reached, due to a drooping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{D_{MAX}}$$

At the onset of drop-out, there is a region of V_{IN} of about 500mV that generates two discrete off-times, one being the minimum off time and the other being an off-time that is about 40ns to 60ns longer than the minimum off-time. This secondary off-time is due to the extra delay in tripping the internal current comparator. The two off-times average out to the required duty cycle to keep the output in regulation. There may be higher SW node jitter, apparent especially when synchronized to an external clock, but the output voltage ripple remains relatively small.

Fault Conditions: Current Limiting and Overvoltage

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3876, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current mode control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} + \frac{1}{2} \bullet \Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The current limit value should be greater than the inductor current required to produce maximum output power at the worst-case efficiency.

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Worst-case efficiency typically occurs at the highest V_{IN} and highest ambient temperature. It is important to check for consistency between the assumed MOSFET junction temperatures and the resulting value of I_{LIMIT} which heats the MOSFET switches.

To further limit current in the event of a short circuit to ground, the LTC3876 includes foldback current limiting. If the output falls by more than 50%, the maximum sense voltage is progressively lowered, to about one-fourth of its full value as the feedback voltage reaches 0V.

A feedback voltage exceeding 7.5% for VDDQ channel 1 and 10% for VTT channel 2 of the regulated target of 0.6V is considered as overvoltage (OV). In such an OV condition, the top MOSFET is immediately turned off and the bottom MOSFET is turned on indefinitely until the OV condition is removed, i.e., the feedback voltage falling back below the threshold by more than a hysteresis of typical 15mV. Current limiting is not active during an OV. If the OV persists, and the BG turns on for a longer time, the current through the inductor and the bottom MOSFET may exceed their maximum ratings, sacrificing themselves to protect the load.

OPTI-LOOP Compensation

OPTI-LOOP® compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control-loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly 2nd order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The external series R_{ITH}-C_{ITH1} filter at the ITH pin sets the dominant pole-zero loop compensation. The values can be adjusted to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected first because their various types and values determine the loop feedback factor gain and phase.

An additional small capacitor, C_{ITH2}, can be placed from the ITH pin to SGND to attenuate high frequency noise. Note this C_{ITH2} contributes an additional pole in the loop gain therefore can affect system stability if too large. It should be chosen so that the added pole is higher than the loop bandwidth by a significant margin.

The regulator loop response can also be checked by looking at the load transient response. An output current pulse of 20% to 100% of full-load current having a rise time of 1µs to 10µs will produce V_{OUT} and ITH voltage transient-response waveforms that can give a sense of the overall loop stability without breaking the feedback loop. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Connecting a resistive load in series with a power MOSFET, then placing the two directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in load current may not be within the bandwidth of the feedback loop, so it cannot be used to determine phase margin. The output voltage settling behavior is more related to the stability of the closed-loop system. However, it is better to look at the filtered and compensated feedback loop response at the ITH pin.

The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH1}. If R_{ITH} is increased by the same factor that C_{ITH1} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF},

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can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_{FB2} which improves the phase margin.

A more severe transient can be caused by switching in loads with large supply bypass capacitors. The discharged bypass capacitors of the load are effectively put in parallel with the converter's C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver current quick enough to prevent this sudden step change in output voltage, if the switch connecting the C_{OUT} to the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. Hot Swap™ controllers are designed specifically for this purpose and usually incorporate current limiting, short-circuit protection and soft starting.

Load-Release Transient Detection

As the output voltage requirement of step-down switching regulators becomes lower, V_{IN} to V_{OUT} step-down ratio increases, and load transients become faster, a major challenge is to limit the overshoot in V_{OUT} during a fast load current drop, or "load-release" transient.

Inductor current slew rate $di_L/dt = V_L/L$ is proportional to voltage across the inductor $V_L = V_{SW} – V_{OUT}$. When the top MOSFET is turned on, $V_L = V_{IN} – V_{OUT}$, inductor current ramps up. When bottom MOSFET turns on, $V_L = V_{SW} – V_{OUT} = –V_{OUT}$, inductor current ramps down. At very low V_{OUT}, the low differential voltage, V_L, across the inductor during the ramp down makes the slew rate of the inductor current much slower than needed to follow the load current change. The excess inductor current charges up the output capacitor, which causes overshoot at V_{OUT}.

If the bottom MOSFET could be turned off during the load-release transient, the inductor current would flow through the body diode of the bottom MOSFET, and the equation can be modified to include the bottom MOSFET body diode drop to become $V_L = –(V_{OUT} + V_{BD})$. Obviously the benefit increases as the output voltage gets lower, since V_{BD} would increase the sum significantly, compared to a single V_{OUT} only.

The load-release overshoot at V_{OUT} causes the error amplifier output, ITH, to drop quickly. ITH voltage is proportional to the inductor current setpoint. A load transient will result in a quick change of this load current setpoint, i.e., a negative spike of the first derivative of the ITH voltage.

The LTC3876 uses a detect transient (DTR) pin to monitor the first derivative of the ITH voltage, and detect the load-release transient. Referring to the Functional Diagram, the DTR pin is the input of a DTR comparator, and the internal reference voltage for the DTR comparator is half of $INTV_{CC}$. To use this pin for transient detection, ITH compensation needs an additional R_{ITH} resistor tied to $INTV_{CC}$, and connects the junction point of ITH compensation components C_{ITH1}, R_{ITH1} and R_{ITH2} to the DTR pin as shown in the Functional Diagram. The DTR pin is now proportional to the first derivative of the inductor current setpoint, through the highpass filter of C_{ITH1} and (R_{ITH1}//R_{ITH2}).

The two R_{ITH} resistors establish a voltage divider from $INTV_{CC}$ to SGND, and bias the DC voltage on DTR pin (at steady-state load or ITH voltage) slightly above half of $INTV_{CC}$. Compensation performance will be identical by using the same C_{ITH1} and make R_{ITH1}//R_{ITH2} equal the R_{ITH} as used in conventional single resistor OPTI-LOOP compensation. This will also provide the R-C time constant needed for the DTR duration. The DTR sensitivity can be adjusted by the DC bias voltage difference between DTR and half $INTV_{CC}$. This difference could be set as low as 100mV, as long as the ITH ripple voltage with DC load current does not trigger the DTR.

When load current suddenly drops, V_{OUT} overshoots, and ITH drops quickly. The voltage on the DTR pin will also drop quickly, since it is coupled to the ITH pin through a capacitor. If the load transient is fast enough that the DTR voltage drops below half of $INTV_{CC}$, a load release event is detected. The bottom gate (BG) will be turned off, so that the inductor current flows through the body diode in the bottom MOSFET. This allows the SW node to drop below PGND by a voltage of a forward-conducted silicon diode. This creates a more negative differential voltage ($V_{SW} – V_{OUT}$) across the inductor, allowing the inductor current to drop at a faster rate to zero, therefore creating less overshoot on V_{OUT}.

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The DTR comparator output is overridden by reverse inductor current detection (I_{REV}) and overvoltage (OV) condition. This means BG will be turned off when $SENSE^+$ is higher than $SENSE^-$ (i.e., inductor current is positive), as long as the OV condition is not present. When inductor current drops to zero and starts to reverse, BG will turn back on in forced continuous mode (e.g., the MODE/PLLIN pin tied to $INTV_{CC}$, or an input clock is present), even if DTR is still below half $INTV_{CC}$. This is to allow the inductor current to go negative to quickly pull down the V_{OUT} overshoot. Of course, if the MODE/PLLIN pin is set to discontinuous mode (i.e., tied to SGND), BG will stay off as inductor current reverse, as it would with the DTR feature disabled.

Note that it is expected that this DTR feature will cause additional loss on the bottom MOSFET, due to its body diode conduction. The bottom FET temperature may be higher with a load of frequent and large load steps. This is an important design consideration. Experiments on the demo board shows a 20°C increase when a continuous 100% to 50% load step pulse train with 50% duty cycle and 100kHz frequency is applied to the output.

If not needed, this DTR feature can be disabled by tying the DTR pin to $INTV_{CC}$, or simply leave the DTR pin open so that an internal 2.5A current source will pull itself up to $INTV_{CC}$.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percentage efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1\% + L2\% + L3\% + ...)$$

where L1%, L2%, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce power losses, several main sources usually account for most of the losses in LTC3876 circuits:

1. I^2R loss. These arise from the DC resistances of the MOSFETs, inductor, current sense resistor and is the majority of power loss at high output currents. In continuous mode the average output current flows though the inductor L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the inductor's DC resistances (DCR) and the board traces to obtain the I^2R loss. For example, if each $R_{DS(ON)} = 8m\Omega$, $R_L = 5m\Omega$, and $R_{SENSE} = 2m\Omega$ the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A. This results in loss from 0.3% to 3% a 5V output, or 1% to 10% for a 1.5V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of lower output voltages and higher currents load demands greater importance of this loss term in the switching regulator system.
2. Transition loss. This loss mostly arises from the brief amount of time the top MOSFET spends in the saturation (Miller) region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors, and can be significant at higher input voltages or higher switching frequencies.
3. DRV_{CC} current. This is the sum of the MOSFET driver and $INTV_{CC}$ control currents. The MOSFET driver currents result from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from DRV_{CC} to ground. The resulting dQ/dt is a current out of DRV_{CC} that is typically much larger than the controller I_Q current. In continuous mode,

   $$I_{GATECHG} = f \bullet (Qg_{(TOP)} + Qg_{(BOT)}),$$

   where $Qg_{(TOP)}$ and $Qg_{(BOT)}$ are the gate charges of the top and bottom MOSFETs, respectively.

   Supplying DRV_{CC} power through $EXTV_{CC}$ could save several percents of efficiency, especially for high V_{IN} applications. Connecting $EXTV_{CC}$ to an output-derived

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source will scale the V_{IN} current required for the driver and controller circuits by a factor of (duty cycle)/(efficiency). For example, in a 20V to 5V application, 10mA of DRV_{CC} current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

4. C_{IN} loss. The input capacitor filters large square-wave input current drawn by the regulator into an averaged DC current from the supply. The capacitor itself has a zero average DC current, but square-wave-like AC current flows through it. Therefore the input capacitor must have a very low ESR to minimize the RMS current loss on ESR. It must also have sufficient capacitance to filter out the AC component of the input current to prevent additional RMS losses in upstream cabling, fuses or batteries. The LTC3876 2-phase architecture improves the ESR loss.

"Hidden" copper trace, fuse and battery resistance, even at DC current, can cause a significant amount of efficiency degradation, so it is important to consider them during the design phase. Other losses, which include the C_{OUT} ESR loss, bottom MOSFET's body diode reverse-recovery loss, and inductor core loss generally account for less than 2% additional loss.

Power losses in the switching regulator will reflect as a higher than ideal duty cycle, or a longer on-time for a constant frequency. This efficiency accounted on-time can be calculated as:

$$t_{ON} \approx t_{ON(IDEAL)}/\text{Efficiency}$$

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased.

Design Example

The following design example is the DDR3 application circuit as implemented on the standard LTC3876 QFN demo board 1631A. This DC/DC step-down converter design accommodates an input V_{IN} range of 4.5V to 14V, with a VDDQ output of 1.5V and a VTT output of 0.75V. The DDRIII output channels are designed to produce 1.5V VDDQ at 20A, a 0.75V VTT 10A maximum average operating current with a VTT reference output (VTTR) capable of supplying up to ±50mA. (see Figure 11, LTC3876 demo circuit 1631A)

The regulated channel 1 VDDQ output supply voltage is determined by:

$$VDDQ = 0.6V\left(1+\frac{R_{FB2}}{R_{FB1}}\right)$$

Set VDDQ to 1.5V for DDRIII application. Using a 20k resistor for R_{FB1}, the resulting R_{BF2} is 30k.

The regulated channel 2 VTT termination supply is differentially referenced to an internal resistor divider connected between the VDDQSNS and the $V_{OUTSENSE}^-$. The resulting differential VTT reference output (VTTR) is one-half VDDQ which in this design example is 0.75V. The VTT termination supply nominally regulates to 0.75V and will track any dynamic movement of the channel 1 VDDQ supply.

The switching frequency for both channels is programmed by:

$$R_T[k\Omega] = 4 \bullet \frac{41550}{f[kHz]} - 2.2$$

For $f = 400kHz$, $R_T = 102k\Omega$.

The minimum on-time occurs for maximum V_{IN} and should be greater than the typical minimum of 30ns with adequate margin. The minimum on-time margin should allow for device variability and the extension of effective on-time at light load due to the dead times. The reason for the on-time extension at light load is that the negative inductor current causes the switch node to rise which effectively adds to the on time. This is of limited concern to the channel 1 VDDQ but is of greater concern to the channel 2 VTT supply because it supplies significant negative current. For the LTC3876 the minimum on-time without any extension is 30ns, with driver dead times of 30ns. For strong negative currents in VTT the total dead time is the total of the minimum on-time, plus both dead times for 90ns. It is therefore recommended to keep the minimum on-time greater than 100ns for channel 2 VTT to assure PLL lock under all operating conditions.

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The minimum on-time for channel 1 VDDQ is:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{1.5V}{14V \bullet 400kHz} = 268ns$$

The minimum on-time for channel 2 VTT is:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{0.75V}{14V \bullet 400kHz} = 134ns$$

Set the channel 1 VDDQ inductor value L1 to give 35% ripple current at the maximum load to 20A for the maximum V_{IN} of 14V using the adjusted operating frequency.

$$L1 = \frac{V_{OUT}}{(f)(I_{RIPPLE})}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$= \frac{1.5V}{(400kHz)(35\% \bullet 20A)}\left(1 - \frac{1.5}{14}\right) = 0.47\mu H$$

Set the channel 2 VTT inductor value L2 to give 35% ripple current at the maximum load to 10A for the maximum V_{IN} of 14V using the adjusted operating frequency.

$$L1 = \frac{V_{OUT}}{(f)(I_{RIPPLE})}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$= \frac{0.75V}{(400kHz)(37.5\% \bullet 10A)}\left(1 - \frac{0.75}{14}\right) = 0.47\mu H$$

Choose the nearest standard value of 0.47µH for L2, which will result in 37.5% ripple current.

The resulting channel 1 VDDQ maximum ripple current is:

$$\Delta I_{L1} = \frac{1.5V}{(400kHz)(0.47\mu H)}\left(1 - \frac{1.5V}{14V}\right) = 7.12A$$

The resulting channel 2 VTT maximum ripple current is:

$$\Delta I_{L2} = \frac{0.75V}{(400kHz)(0.47\mu H)}\left(1 - \frac{0.75V}{14V}\right) = 3.78A$$

For Figure 11, standard demo board the current limit is set using sense resistors. The V_{RNG} is grounded which results in a maximum V_{SENSE} voltage across the R_{SENSE} resistor of 30mV. If we assume 50% over the nominal output of 20A this gives a starting point of 1mΩ for channel 1 VDDQ and 2mΩ for channel 2 VTT.

Channel 1 VDDQ current limit for 1mΩ R_{SENSE}.

$$ILIMIT_{VDDQ} = \frac{V_{SENSE}}{R_{SENSE}} + \frac{\Delta I_L}{2} = \frac{30mV}{1m\Omega} + \frac{7.12A}{2} = 33.5A$$

Channel 2 VTT current limit for 2mΩ R_{SENSE}.

$$ILIMIT_{VTT} = \frac{V_{SENSE}}{R_{SENSE}} + \frac{\Delta I_L}{2} = \frac{30mV}{2m\Omega} + \frac{3.78A}{2} = 16.9A$$

In high power applications, DCR current sensing is often preferred to R_{SENSE} in order to maximize efficiency. The inductor model is selected based on its inductor and DCR value. The Würth WE7443330047 with a rated current of 20A, a saturation current of 47A and DCR of 0.8mΩ is chosen for channel 1 VDDQ. The Würth WE7443340047 with a rated current of 19A, a saturation current of 32A and DCR of 1.72mΩ is chosen for channel 2 VTT. The DCR demo board design is Figure 13.

In this design example V_{RNG} was grounded to produce an internal default value of 30mV on V_{SENSE}.

Channel 1 VDDQ DCR Current limit:

$$ILIMIT_{VDDQ} = \frac{V_{SENSE}}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

$$= \frac{30mV}{0.8m\Omega \bullet (1 + (100°C - 25°C) \bullet 0.4\%/°C)} + \frac{7.12A}{2}$$

$$= 32.4A$$

Channel 2 VTT DCR Current Limit:

$$ILIMIT_{VTT} = \frac{V_{SENSE}}{R_{SENSE}} + \frac{\Delta IL}{2}$$

$$= \frac{30mV}{1.72m\Omega \bullet (1 + (100°C - 25°C) \bullet 0.4\%/°C)} + \frac{3.78A}{2}$$

$$= 15.3A$$

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The DCR sense filter is designed using a simple RC filter across the inductor. If the inductor value and DCR is known, choose a sense filter C and calculate filter resistance.

Channel 1 DCR filter resistor R_{DCR1}:

$$R_{DCR1} = \frac{L1}{DCR \bullet C_{DCR}} = \frac{0.47\mu H}{0.8m\Omega \bullet 0.1\mu F} = 5.9k$$

Channel 2 DCR filter resistor R_{DCR2}:

$$R_{DCR1} = \frac{L1}{DCR \bullet C_{DCR}} = \frac{0.47\mu H}{1.72m\Omega \bullet 0.1\mu F} = 2.74k$$

The external N-channel MOSFETs are chosen based on current capability and efficiency. The Renesas RJK0305DBP ($R_{DS(ON)}$=13mΩ(maximum), C_{MILLER}=150pF, VGS = 4.5V, V_{MILLER} = 3V, θ_{JA} = 40°C/W, $T_{J(MAX)}$ = 150°C) is chosen for the top MOSFET (main switch). The Renesas RJK0330DBP ($R_{DS(ON)}$ = 3.9mΩ(maximum), V_{GS} = 4.5V, θ_{JA} = 40°C/W, $T_{J(MAX)}$ =150°C) is chosen for the bottom MOSFET (synchronous switch).The power dissipation for each MOSFET can be calculated for V_{IN} = 14V and typical T_J =125°C.

The power dissipation for V_{IN} = 14V and T_J =125°C for the top MOSFET is:

$$P_{TOP} = \frac{1.5V}{14V}(20A)^2\left(1+0.4\%\left(125°C-25°C\right)\right)(0.013\Omega) + (14V)^2\left(\frac{20A}{2}\right)(150pF)\left(\frac{2.5\Omega}{5.3V-3V}+\frac{1.2\Omega}{3V}\right)(400kHz)$$
$$= 0.78W + 0.17W = 0.95W$$

The power dissipation for V_{IN} = 14V and T_J =125°C for 2X bottom MOSFETs is:

$$P_{BOT} = \frac{14V-1.5V}{14V}\left(\frac{20A}{2X}\right)^2 \left(1+0.4\%\left(125°C-25°C\right)\right)(0.0039\Omega) = 0.4875W$$

The resulting junction temperatures for ambient temperature T_A = 75°C are:

$T_{J(TOP)}$ = 75°C + (0.95W)(40°C/W) = 113°C

$T_{J(BOT)}$ = 75°C + (0.975W)(40°C/W) = 94.5°C

These numbers show that careful attention should be paid to proper heat sinking when operating at higher ambient temperatures.

Select C_{IN} capacitors to give ample capacitance and RMS ripple current rating. Consider worst-case duty cycles per Figure 6. If operated at steady-state with SW nodes fully interleaved, the two channels would generate not more than 7.5A RMS at full load. In this design example, 2X 10µF 25V X5R ceramic capacitors are put in parallel to take the RMS ripple current with 330µF aluminum electrolytic bulk capacitors for stability. For 10µF 1210 X5R ceramic capacitors, try to keep the ripple current less than 3A RMS through each device. The bulk capacitor is chosen for RMS rating per simulation with the circuit model provided.

The power supply output capacitor's C_{OUT} are chosen for a low ESR. For channel 1 VDDQ, the output capacitor SANYO 2R5TPE330M9, has an ESR of 9mΩ which results in 4.5mΩ for two in parallel. For channel 2 VTT, the output capacitor SANYO 2R5TPE330M9, has an ESR of 9mΩ.

The output ripple for each channel is given as:

$\Delta VDDQ(RIPPLE) = \Delta I_{L(MAX)}$ (ESR)

= (7.12A) • (4.5mΩ) = 32mV

$\Delta VTT(RIPPLE) = \Delta I_{L(MAX)}$ (ESR)

= (3.78A) • (9mΩ) = 34mV

A 0A to 10A load step in VDDQ will cause an output change of up to:

$\Delta VDDQ(STEP) = \Delta I_{LOAD}$ (ESR) = 10A • 0.0045mΩ = 45mV

A 0A to 5A load step in VTT will cause an output change of up to:

$\Delta VTT(STEP) = \Delta I_{LOAD}$ (ESR) = 5A • 0.009mΩ = 45mV

Optional 100µF ceramic output capacitors are included to minimize the effect of ESL in the output ripple and to improve load step response.

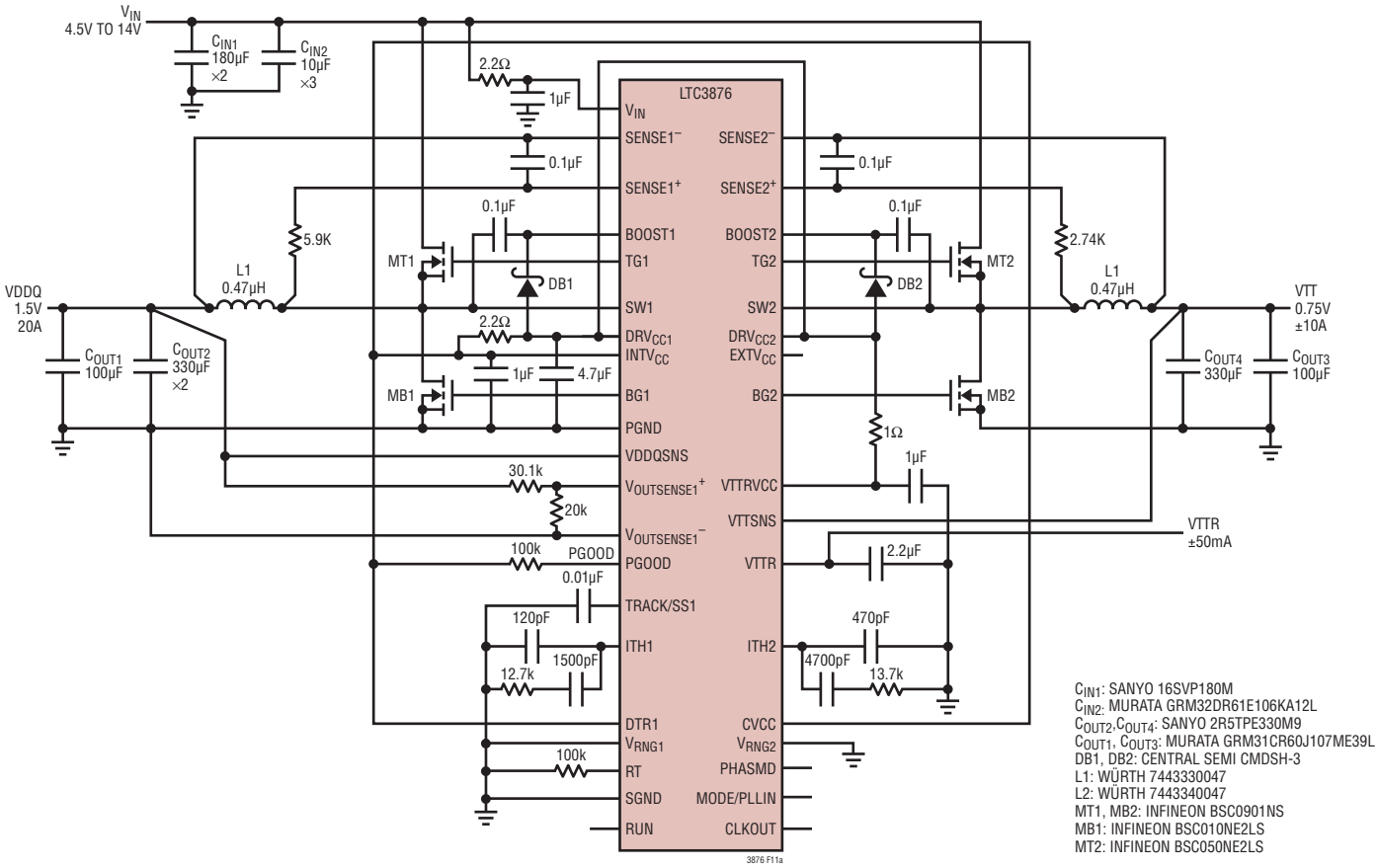
APPLICATIONS INFORMATION

PCB Layout Checklist

The printed circuit board layout is illustrated graphically in Figure 12. Use the following checklist to ensure proper operation of the LTC3876:

- A multilayer printed circuit board with dedicated ground planes is generally preferred to reduce noise coupling and improve heat sinking. The ground plane layer should be immediately next to the routing layer for the power components, e.g., MOSFETs, inductors, sense resistors, input and output capacitors etc.
- Keep SGND and PGND separate. Upon finishing the layout, connect SGND and PGND together with a single PCB trace underneath the IC from the SGND pin through the exposed PGND pad to the PGND pin.
- All power train components should be referenced to PGND; all components connected to noise-sensitive pins, e.g., ITH, RT, TRACK/SS and V_{RNG}, should return to the SGND pin. Keep PGND ample, but SGND area compact. Use a modified "star ground" technique: a low impedance, large copper area central PCB point on the same side of the as the input and output capacitors.
- Place power components, such as C_{IN}, C_{OUT}, MOSFETs, D_B and inductors, in one compact area. Use wide but shortest possible traces for high current paths (e.g., V_{IN}, V_{OUT}, PGND etc.) to this area to minimize copper loss.
- Keep the switch nodes (SW1,2), top gates (TG1,2) and boost nodes (BOOST1,2) away from noise-sensitive small-signal nodes, especially from the opposite channel's voltage and current sensing feedback pins. These nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3876 (power-related pins are toward the right hand side of the IC), and occupy minimum PC trace area. Use compact switch node (SW) planes to improve cooling of the MOSFETs and to keep EMI down. If DCR sensing is used, place the top filter resistor (R1 only in Figure 5) close to the switch node.
- The top N-channel MOSFETs of the two channels have to be located within a short distance from (preferably <1cm) each other with a common drain connection at C_{IN}. Do not attempt to split the input decoupling for the two channels as it can result in a large resonant loop.
- Connect the input capacitor(s), C_{IN}, close to the power MOSFETs. This capacitor provides the MOSFET transient spike current. Connect the drain of the top MOSFET as close as possible to the (+) plate of the ceramic portion of input capacitors C_{IN}. Connect the source of the bottom MOSFET as close as possible to the (–) terminal of the same ceramic C_{IN} capacitor(s). These ceramic capacitor(s) bypass the high di/dt current locally, and both top and bottom MOSFET should have short PCB trace lengths to minimize high frequency EMI and prevent MOSFET voltage stress from inductive ringing.
- The path formed by the top and bottom N-channel MOSFETs, and the C_{IN} capacitors should have short leads and PCB trace. The (–) terminal of output capacitors should be connected close to the (–) terminal of C_{IN}, but away from the loop described above. This is to achieve an effect of Kevin (4-wire) connection to the input ground so that the "chopped" switching current will not flow through the path between the input ground and the output ground, and cause common mode output voltage ripple.
- Several smaller sized ceramic output capacitors, C_{OUT}, can be placed close to the sense resistors and before the rest bulk output capacitors.
- The filter capacitor between the $SENSE^+$ and $SENSE^-$ pins should always be as close as possible to these pins. Ensure accurate current sensing with Kevin (4-wire) connections to the soldering pads from underneath the sense resistors or inductor. A pair of sense traces should be routed together with minimum spacing. R_{SENSE}, if used, should be connected to the inductor on the noiseless output side, and its filter resistors close to the $SENSE^+/SENSE^-$ pins. For DCR sensing, however, filter resistor should be placed close to the inductor, and away from the $SENSE^+/SENSE^-$ pins, as its terminal is the SW node.

APPLICATIONS INFORMATION



CIN1: SANYO 16SVP180M
CIN2: MURATA GRM32DR61E106KA12L
COUT2,COUT4: SANYO 2R5TPE330M9
COUT1, COUT3: MURATA GRM31CR60J107ME39L
DB1, DB2: CENTRAL SEMI CMDSH-3
L1: WÜRTH 7443330047
L2: WÜRTH 7443340047
MT1, MB2: INFINEON BSC0901NS
MB1: INFINEON BSC010NE2LS
MT2: INFINEON BSC050NE2LS

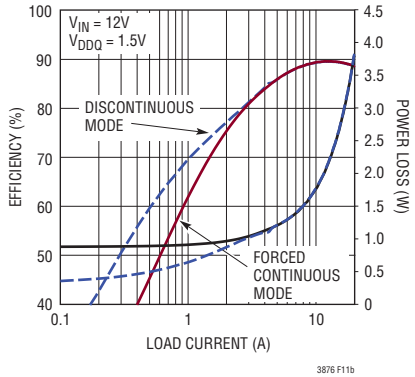


Figure 11. Design Example: 4.5V to 14V Input, VDDQ 1.5V/20A and VTT 0.75V/±10A Output, 400kHz, DCR, Step-Down Converter

- Keep small-signal components connected noise-sensitive pins (give priority to SENSE+/SENSE–, $V_{OUTSENSE1}^+$/$V_{OUTSENSE1}^-$, V_{FB2}, RT, ITH, V_{RNG} pins) on the left hand side of the IC as close to their respective pins as possible. This minimizes the possibility of noise coupling into these pins. If the LTC3876 can be placed on the bottom side of a multilayer board, use ground planes to isolate from the major power components on the top side of the board, and prevent noise coupling to noise sensitive components on the bottom side.

APPLICATIONS INFORMATION

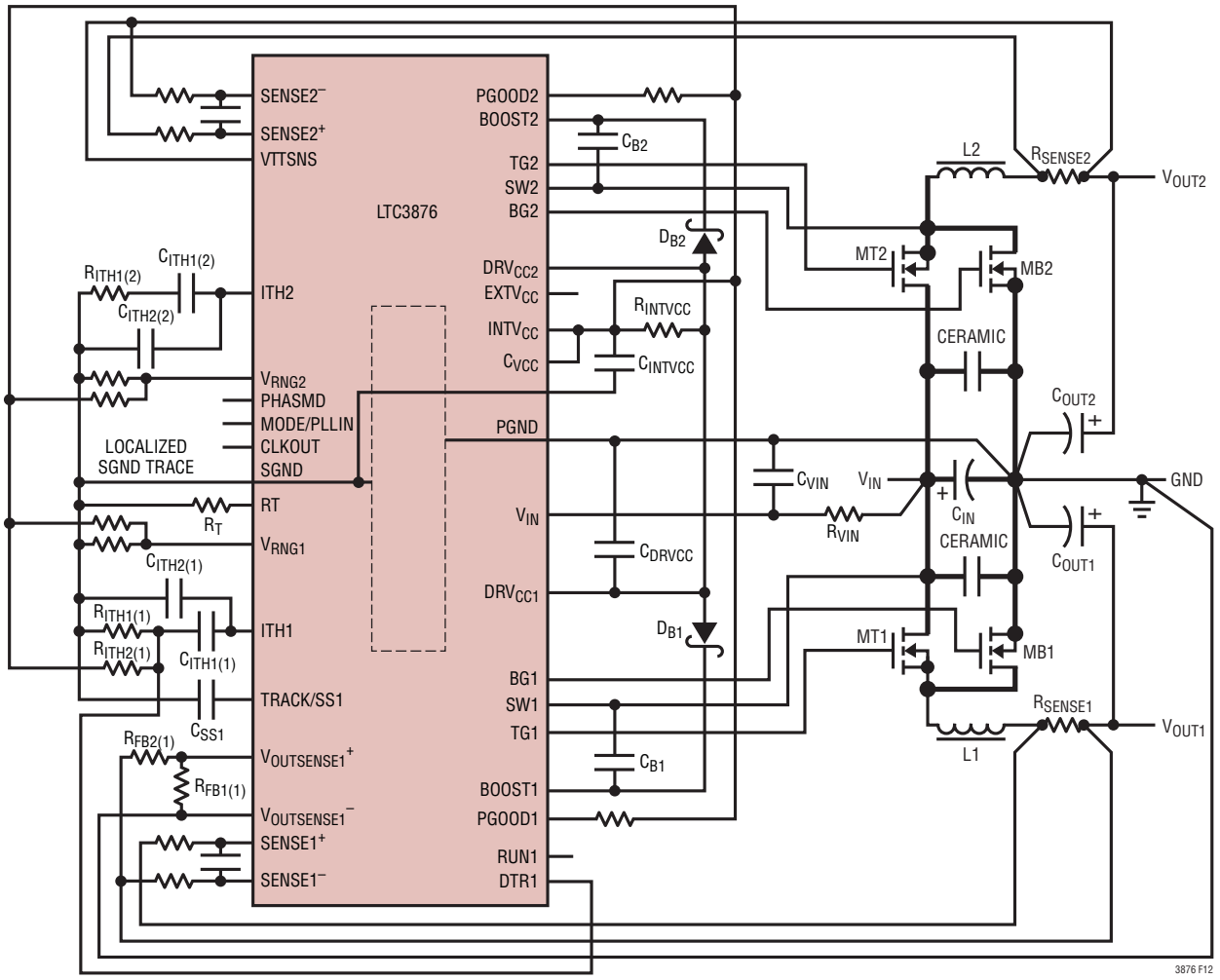


Figure 12. Recommended PCB Layout Diagram

- Place the resistor feedback divider R_{FB1}, R_{FB2} close to $V_{OUTSENSE1}^+$ and $V_{OUTSENSE1}^-$ pins for channel 1, or V_{FB2} pin for channel 2, so that the feedback voltage tapped from the resistor divider will not be disturbed by noise sources. Route remote sense PCB traces (use a pair of wires closely together for differential sensing in channel 1) directly to the terminals of output capacitors for best output regulation.
- Place decoupling capacitors C_{ITH2} next to the ITH and SGND pins with short, direct trace connections.
- Use sufficient isolation when routing a clock signal into the MODE/PLLIN pin or out of the CLKOUT pin, so that the clock does not couple into sensitive pins.
- Place the ceramic decoupling capacitor C_{INTVCC} between the $INTV_{CC}$ pin and SGND and as close as possible to the IC.
- Place the ceramic decoupling capacitor C_{DRVCC} close to the IC, between the combined $DRV_{CC1,2}$ pins and PGND.
- Filter the V_{IN} input to the LTC3876 with an RC filter. Place the filter capacitor close to the V_{IN} pin.
- If vias have to be used, use immediate vias to connect components to the SGND and PGND planes of LTC3876. Use multiple large vias for power components.

APPLICATIONS INFORMATION

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to DC rails only, e.g., PGND.

PCB Layout Debugging

Only after each controller is checked for its individual performance should both controllers be turned on at the same time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator output CLKOUT, or external clock if used. Probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application.

The frequency of operation should be maintained over the input voltage range. The phase should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the phase of SW node pulse can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PCB layout if regulator bandwidth optimization is not required.

A particularly difficult region of operation is when one controller channel is turning on (right after its current comparator trip point) while the other channel is turning off its top MOSFET at the end of its on-time. This may cause minor phase-lock jitter at either channel due to noise coupling.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins.

The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

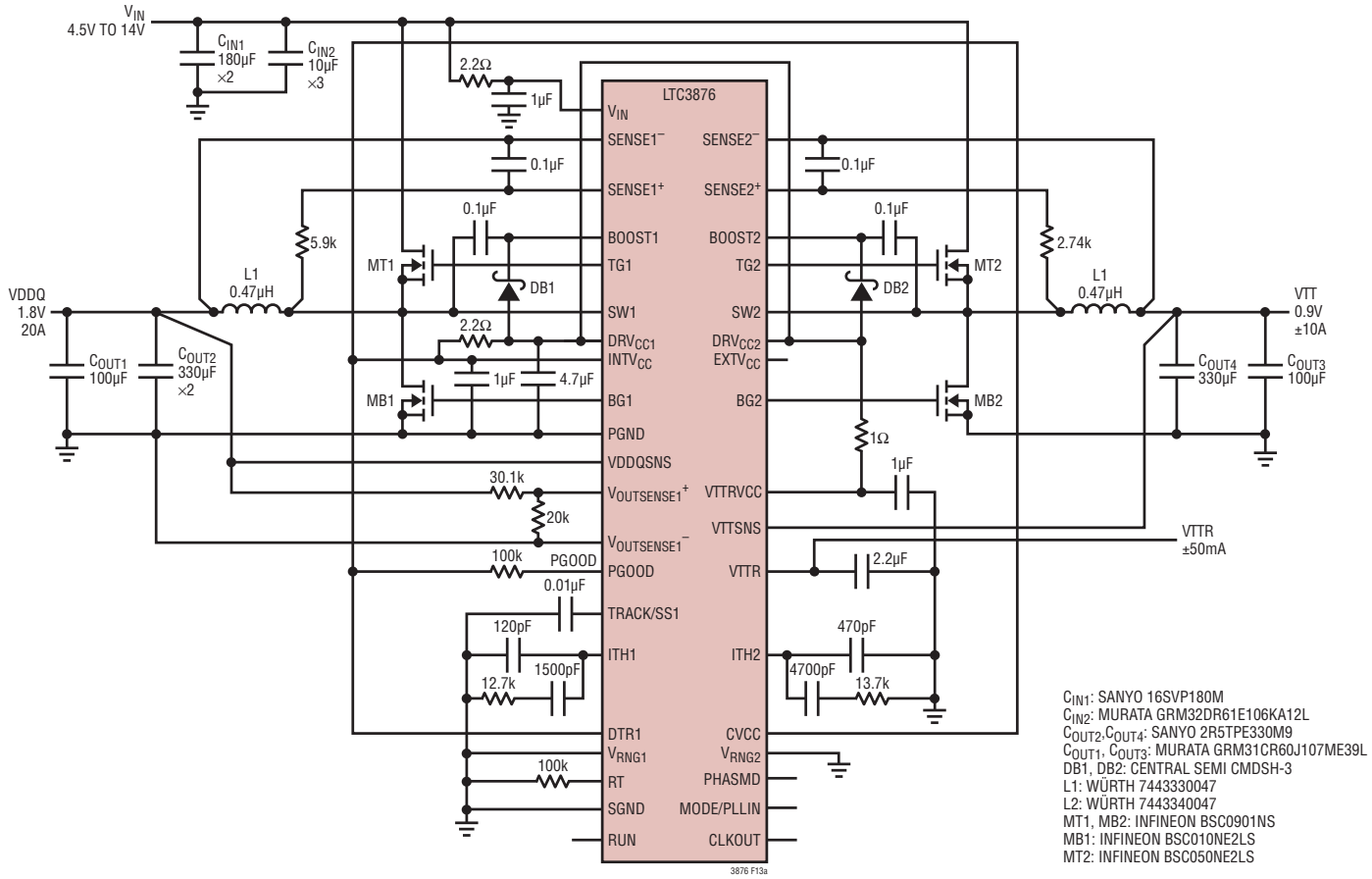
If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, top and bottom MOSFET components to the sensitive current and voltage sensing traces.

In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

High Switching Frequency Operation

At high switching frequencies there may be an increased sensitivity to noise. Special care may need to be taken to prevent cycle-by-cycle instability and/or phase-lock jitter. First, carefully follow the recommended layout techniques to reduce coupling from the high switching voltage/current traces. Additionally, use low ESR and low impedance X5R or X7R ceramic input capacitors: up to 5µF per Amp. of load current may be needed. If necessary, increase ripple sense voltage by increasing sense resistance value and V_{RNG} setting, to improve noise immunity.

APPLICATIONS INFORMATION



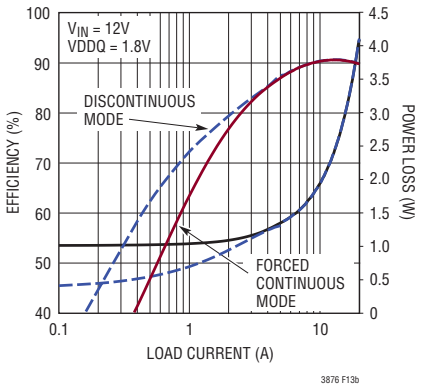
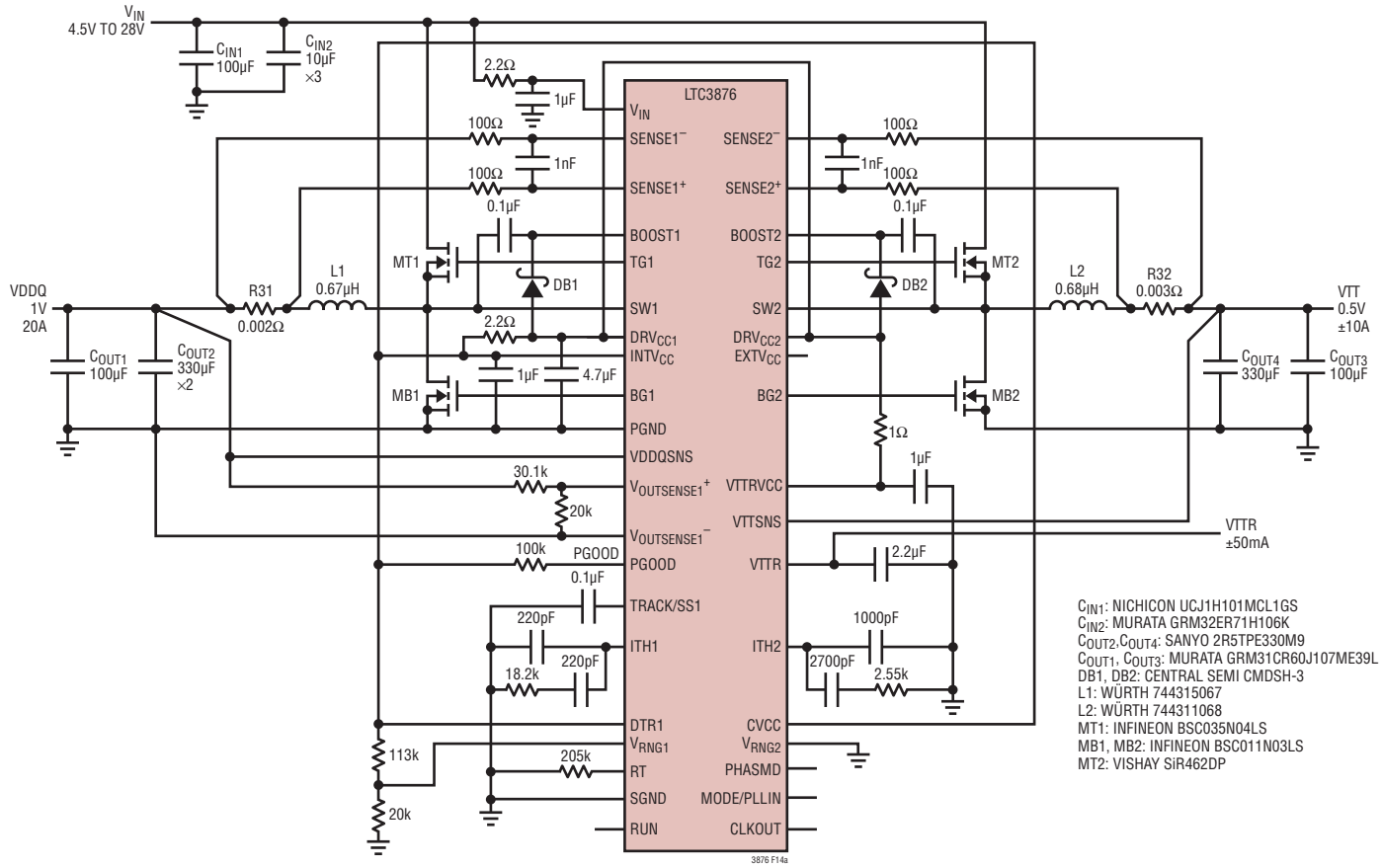


Figure 13. 4.5V to 14V Input, VDDQ 1.8V/20A and VTT 0.9V/±10A Output, 400kHz, DCR, Step-Down Converter

APPLICATIONS INFORMATION



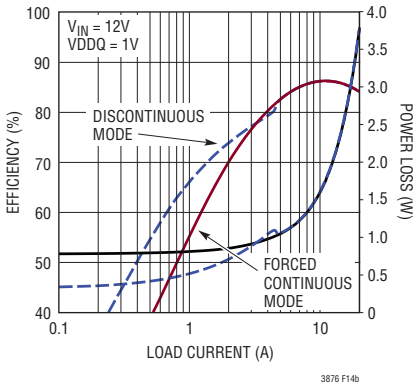
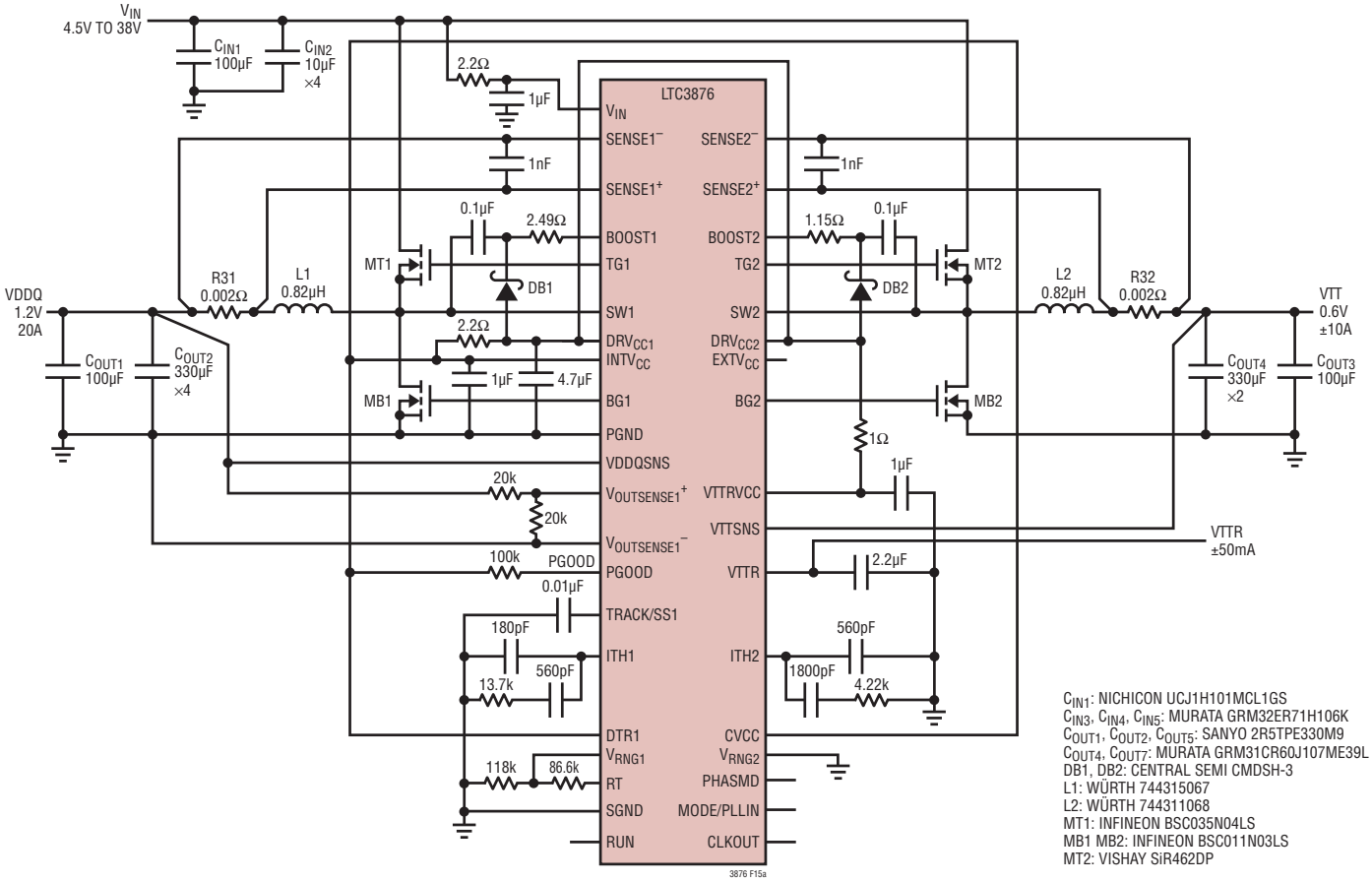


Figure 14. 4.5V to 28V Input, VDDQ 1V/20A and VTT 0.50V/±10A Output, 200kHz, R_{SENSE}, Step-Down Converter

APPLICATIONS INFORMATION



C_{IN1}: NICHICON UCJ1H101MCL1GS
C_{IN3}, C_{IN4}, C_{IN5}: MURATA GRM32ER71H106K
C_{OUT1}, C_{OUT2}, C_{OUT5}: SANYO 2R5TPE330M9
C_{OUT4}, C_{OUT7}: MURATA GRM31CR60J107ME39L
DB1, DB2: CENTRAL SEMI CMDSH-3
L1: WÜRTH 744315067
L2: WÜRTH 744311068
MT1: INFINEON BSC035N04LS
MB1 MB2: INFINEON BSC011N03LS
MT2: VISHAY SiR462DP

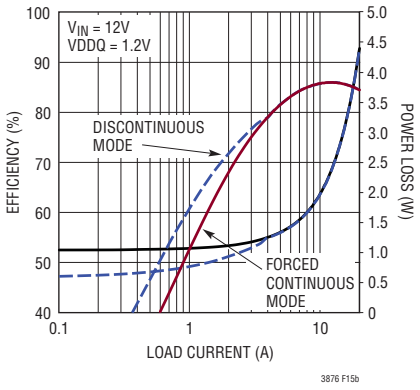
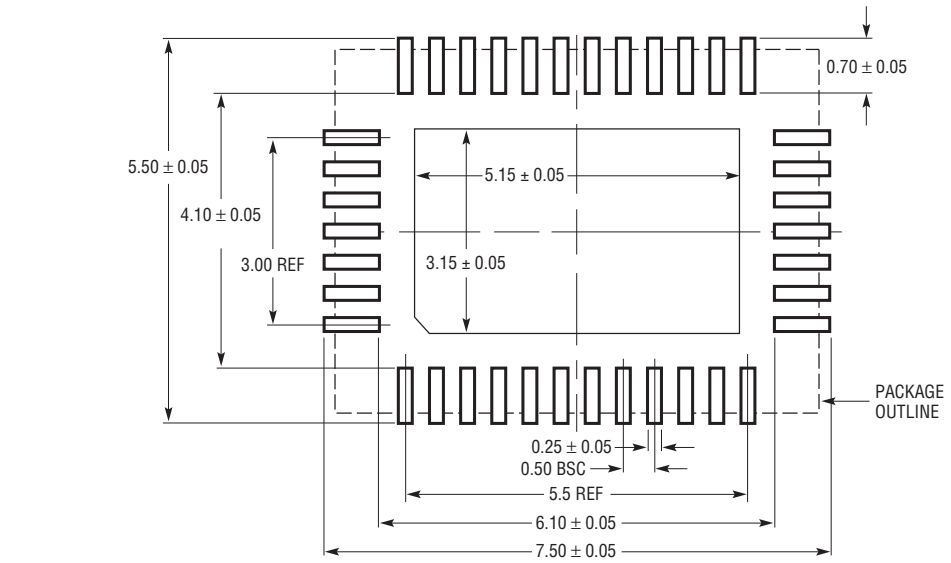


Figure 15. 4.5V to 38V Input, VDDQ 1.2V/20A and VTT 0.60V/±10A Output, 200kHz, R_{SENSE}, Step-Down Converter

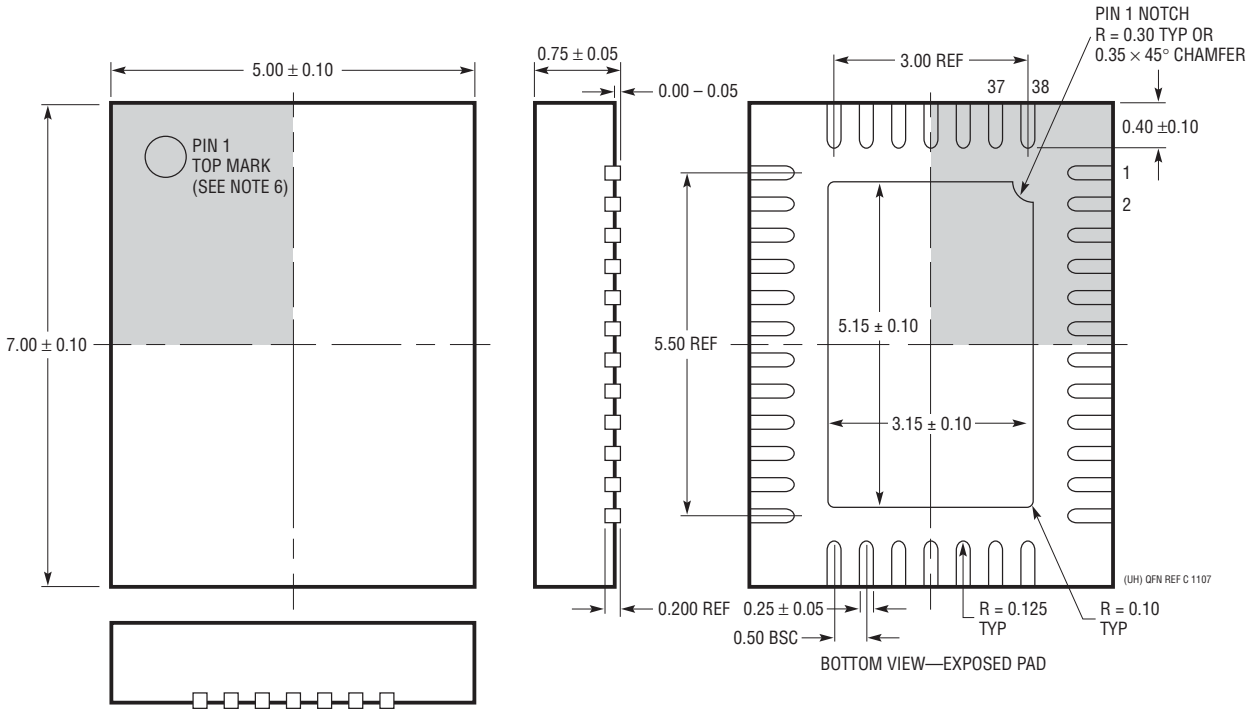
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

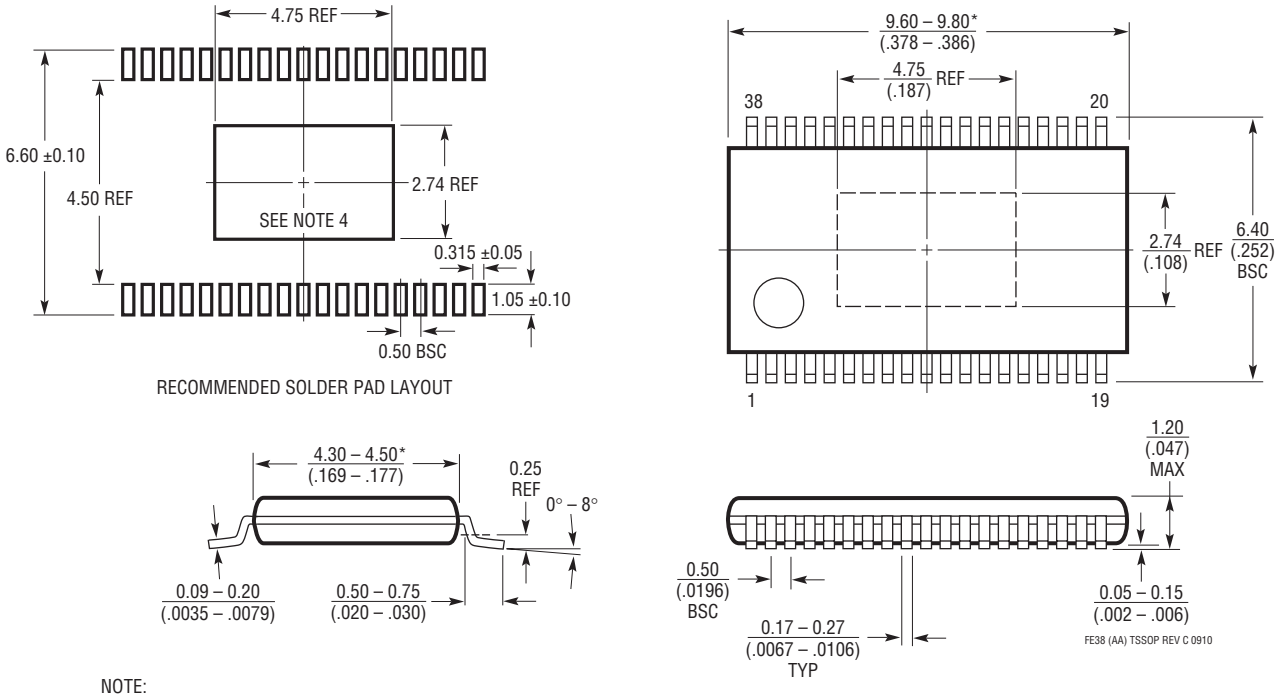


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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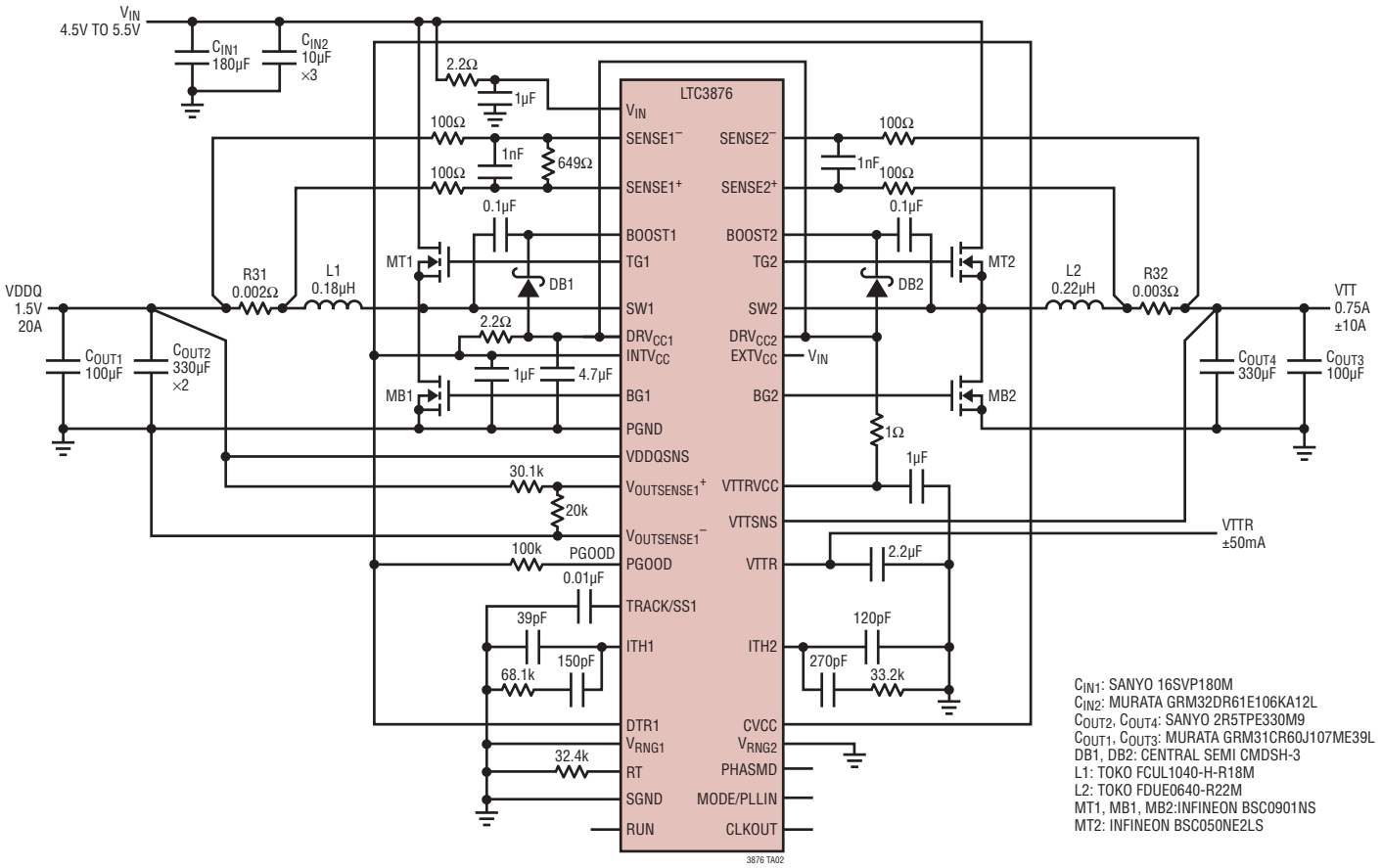
TYPICAL APPLICATION

4.5V to 5.5V Input, VDDQ 1.5V/20A and VTT 0.75V/±10A Output, 1.2MHz, R_{SENSE}, Step-Down Converter



C_{IN1}: SANYO 16SVP180M
C_{IN2}: MURATA GRM32DR61E106KA12L
C_{OUT2}, C_{OUT4}: SANYO 2R5TPE330M9
C_{OUT1}, C_{OUT3}: MURATA GRM31CR60J107ME39L
DB1, DB2: CENTRAL SEMI CMDSH-3
L1: TOKO FCUL1040-H-R18M
L2: TOKO FDUE0640-R22M
MT1, MB1, MB2:INFINEON BSC0901NS
MT2: INFINEON BSC050NE2LS

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3776	Dual, 2-Phase, No R_{SENSE}™, Synchronous Controller for DDR/QDR Memory Termination	2.75V ≤ V_{IN} ≤ 9.8V, V_{OUT} Tracks One-Half V_{REF}, 4mm × 4mm QFN-24, SSOP-24
LTC3717	High Power DDR Memory Termination Regulator	4V ≤ V_{IN} ≤ 36V, V_{OUT} Tracks One-Half V_{IN} or V_{REF}
LTC3718	Bus Termination Supply for Low Voltage V_{IN}	1.5V ≤ V_{IN}, Supplies 5V Gate Drive for N-Channel MOSFETs
LTC3831	High Power DDR Memory Termination Regulator	V_{OUT} Tracks One-Half V_{IN} or V_{REF}, 3V ≤ V_{IN} ≤ 8V
LTC3413	3A Monolithic DDR Memory Termination Regulator	2.25V ≤ V_{IN} ≤ 5.5V, TSSOP-16E
LTC3833	Fast Controller On-Time, High Frequency Synchronous Step-Down Controller with Diff Amp	Up to 2MHz Operating Frequency 4.5V < V_{IN} < 38V, 0.6V < V_{OUT} < 5.5V, 3mm × 4mm QFN-20, TSSOP-20E
LTC3838	Dual, Fast, Accurate Step-Down DC/DC Controller with Differential Output Sensing	Up to 2MHz Operating Frequency 4.5V < V_{IN} < 38V, 0.6V < V_{OUT} < 5.5V, 5mm × 7mm QFN-38, TSSOP-38E
LTC3634	15V Dual 3A Monolithic DDR Memory Termination	3.6V ≤ V_{IN} ≤ 15V, 4mm × 5mm QFN-28, TSSOP-28E
LTC3617	6A Monolithic DDR Memory Termination	2.25V ≤ V_{IN} ≤ 5.5V, 3mm × 5mm QFN-24
LTC3618	Dual 3A Monolithic DDR Memory Termination	2.25V ≤ V_{IN} ≤ 5.5V, 4mm × 4mm QFN-24, TSSOP-24

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- Alternative Solution
- Excess Inventory Management