



# THE DATASHEET OF CD4060BCN



# CD4040BC, 12-Stage Ripple Carry Binary Counters CD4060BC, 14-Stage Ripple Carry Binary Counters

## Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity:  $0.45 V_{DD}$  (Typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation: 8MHz typ. at  $V_{DD} = 10V$
- Schmitt trigger clock input

## General Description

The CD4060BC is a 14-stage ripple carry binary counter, and the CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

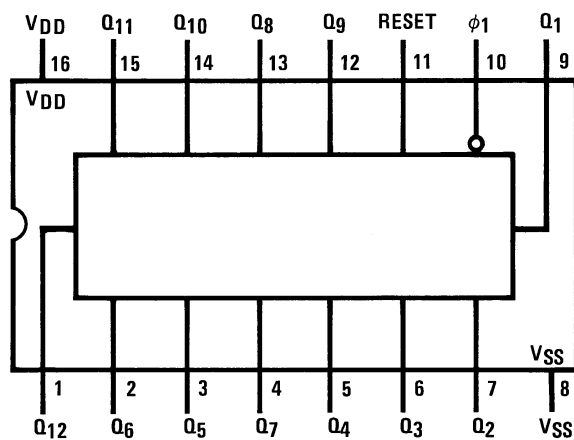
## Ordering Information

Order Number	Package Number	Package Description
CD4040BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4060BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4060BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

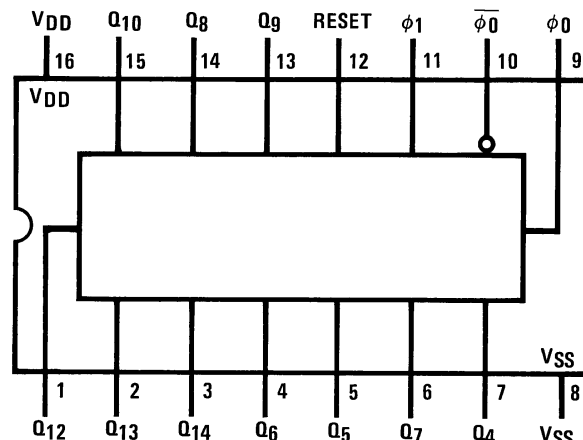
## Connection Diagrams

Pin Assignments for DIP and SOIC  
CD4040BC



Top View

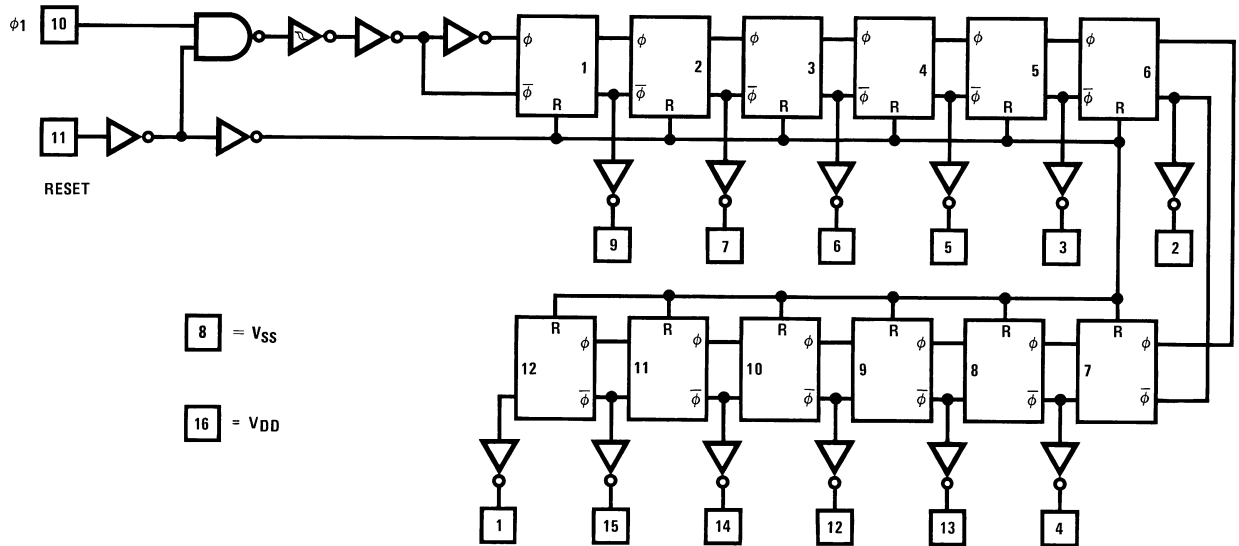
Pin Assignments for DIP and SOIC  
CD4060BC



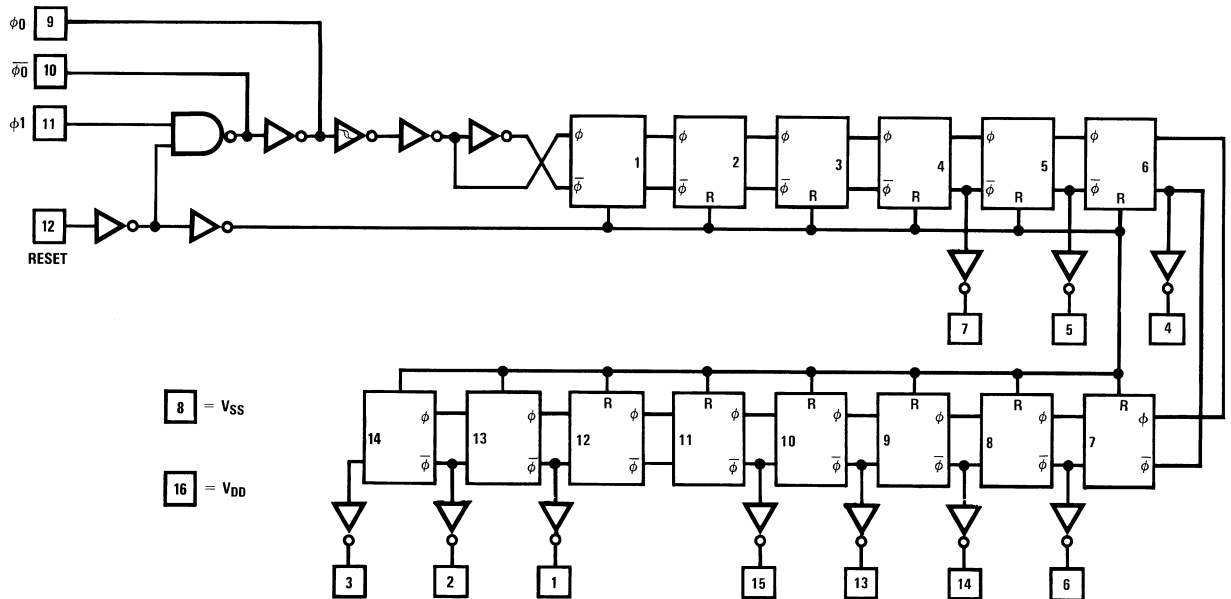
Top View

Schematic Diagrams

CD4040BC

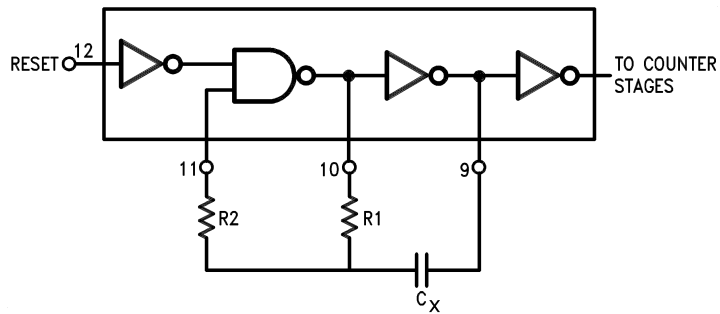


CD4060BC

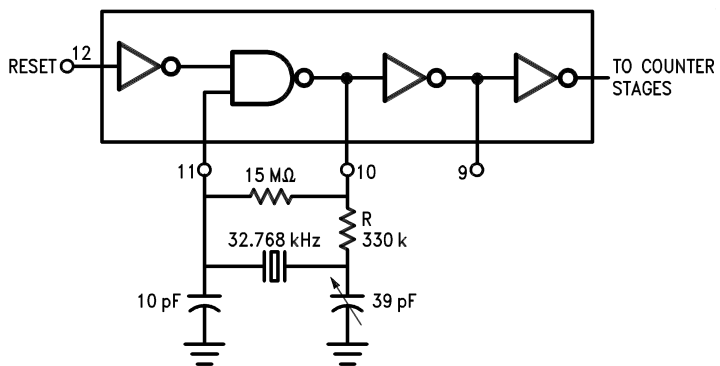


### CD4060B Typical Oscillator Connections

RC Oscillator



Crystal Oscillator



## Absolute Maximum Ratings<sup>(1)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{DD}$	Supply Voltage	-0.5V to +18V
$V_{IN}$	Input Voltage	-0.5V to $V_{DD} + 0.5V$
$T_S$	Storage Temperature Range	-65°C to +150°C
$P_D$	Package Dissipation	
	N Package	700mW
	M Package	500 mW
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

### Note:

- $V_{SS} = 0V$  unless otherwise specified.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{DD}$	Supply Voltage	+3V to +15V
$V_{IN}$	Input Voltage	0V to $V_{DD}$
$T_A$	Operating Temperature Range	-55°C to +125°C

## DC Electrical Characteristics<sup>(2)</sup>

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I <sub>DD</sub>	Quiescent Device Current	V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		5			5		150	μA
		V <sub>DD</sub> = 10V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		10			10		300	
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		20			20		600	
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>DD</sub> = 5V		0.05		0	0.05		0.05	V
		V <sub>DD</sub> = 10V		0.05		0	0.05		0.05	
		V <sub>DD</sub> = 15V		0.05		0	0.05		0.05	
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>DD</sub> = 5V	4.95		4.95	5		4.95		V
		V <sub>DD</sub> = 10V	9.95		9.95	10		9.95		
		V <sub>DD</sub> = 15V	14.95		14.95	15		14.95		
V <sub>IL</sub>	LOW Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V		3.0		4	3.0		3.0	
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V		4.0		6	4.0		4.0	
V <sub>IH</sub>	HIGH Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V	7.0		7.0	6		7.0		
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V	11.0		11.0	9		11.0		
I <sub>OL</sub>	LOW Level Output Current <sup>(3)</sup>	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	0.64		0.51	0.88		0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V	1.6		1.3	2.25		0.9		
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V	4.2		3.4	8.8		2.4		
I <sub>OH</sub>	HIGH Level Output Current <sup>(3)</sup>	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.6V	-0.64		-0.51	-0.88		-0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V	-1.6		-1.3	-2.25		-0.9		
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	-4.2		-3.4	-8.8		-2.4		
I <sub>IN</sub>	Input Current	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V		-0.1		-10 <sup>-5</sup>	-0.1		-1.0	μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = 15V		0.1		10 <sup>-5</sup>	0.1		1.0	

**Note:**

2. V<sub>SS</sub> = 0V unless otherwise specified.

3. Data does not apply to oscillator points  $\phi_0$  and  $\bar{\phi}_0$  of CD4060BC. I<sub>OH</sub> and I<sub>OL</sub> are tested one output at a time.

## AC Electrical Characteristics<sup>(4)</sup>

CD4040BC  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{\text{PHL1}}, t_{\text{PLH1}}$	Propagation Delay Time to $Q_1$	$V_{\text{DD}} = 5\text{V}$		250	550	ns
		$V_{\text{DD}} = 10\text{V}$		100	210	
		$V_{\text{DD}} = 15\text{V}$		75	150	
$t_{\text{PHL}}, t_{\text{PLH}}$	Interstage Propagation Delay Time from $Q_n$ to $Q_{n+1}$	$V_{\text{DD}} = 5\text{V}$		150	330	ns
		$V_{\text{DD}} = 10\text{V}$		60	125	
		$V_{\text{DD}} = 15\text{V}$		45	90	
$t_{\text{THL}}, t_{\text{TLH}}$	Transition Time	$V_{\text{DD}} = 5\text{V}$		100	200	ns
		$V_{\text{DD}} = 10\text{V}$		50	100	
		$V_{\text{DD}} = 15\text{V}$		40	80	
$t_{\text{WL}}, t_{\text{WH}}$	Minimum Clock Pulse Width	$V_{\text{DD}} = 5\text{V}$		125	335	ns
		$V_{\text{DD}} = 10\text{V}$		50	125	
		$V_{\text{DD}} = 15\text{V}$		40	100	
$t_{\text{rCL}}, t_{\text{fCL}}$	Maximum Clock Rise and Fall Time	$V_{\text{DD}} = 5\text{V}$			No Limit	ns
		$V_{\text{DD}} = 10\text{V}$			No Limit	
		$V_{\text{DD}} = 15\text{V}$			No Limit	
$f_{\text{CL}}$	Maximum Clock Frequency	$V_{\text{DD}} = 5\text{V}$	1.5	4		MHz
		$V_{\text{DD}} = 10\text{V}$	4	10		
		$V_{\text{DD}} = 15\text{V}$	5	12		
$t_{\text{PHL(R)}}$	Reset Propagation Delay	$V_{\text{DD}} = 5\text{V}$		200	450	ns
		$V_{\text{DD}} = 10\text{V}$		100	210	
		$V_{\text{DD}} = 15\text{V}$		80	170	
$t_{\text{WH(R)}}$	Minimum Reset Pulse Width	$V_{\text{DD}} = 5\text{V}$		200	450	ns
		$V_{\text{DD}} = 10\text{V}$		100	210	
		$V_{\text{DD}} = 15\text{V}$		80	170	
$C_{\text{IN}}$	Average Input Capacitance	Any Input		5	7.5	pF
$C_{\text{PD}}$	Power Dissipation Capacitance			50		pF

**Note:**

4. AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics<sup>(5)</sup>

CD4060BC  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}$ ,  $t_r = t_f = 20\text{ ns}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{PHL4}, t_{PLH4}$	Propagation Delay Time to $Q_4$	$V_{DD} = 5\text{V}$		550	1300	ns
		$V_{DD} = 10\text{V}$		250	525	
		$V_{DD} = 15\text{V}$		200	400	
$t_{PHL}, t_{PLH}$	Interstage Propagation Delay Time from $Q_n$ to $Q_{n+1}$	$V_{DD} = 5\text{V}$		150	330	ns
		$V_{DD} = 10\text{V}$		60	125	
		$V_{DD} = 15\text{V}$		45	90	
$t_{THL}, t_{TLH}$	Transition Time	$V_{DD} = 5\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		50	100	
		$V_{DD} = 15\text{V}$		40	80	
$t_{WL}, t_{WH}$	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$		170	500	ns
		$V_{DD} = 10\text{V}$		65	170	
		$V_{DD} = 15\text{V}$		50	125	
$t_{rCL}, t_{fCL}$	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$			No Limit	ns
		$V_{DD} = 10\text{V}$			No Limit	
		$V_{DD} = 15\text{V}$			No Limit	
$f_{CL}$	Maximum Clock Frequency	$V_{DD} = 5\text{V}$	1	3		MHz
		$V_{DD} = 10\text{V}$	3	8		
		$V_{DD} = 15\text{V}$	4	10		
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5\text{V}$		200	450	ns
		$V_{DD} = 10\text{V}$		100	210	
		$V_{DD} = 15\text{V}$		80	170	
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5\text{V}$		200	450	ns
		$V_{DD} = 10\text{V}$		100	210	
		$V_{DD} = 15\text{V}$		80	170	
$C_{IN}$	Average Input Capacitance	Any Input		5	7.5	pF
$C_{PD}$	Power Dissipation Capacitance			50		pF

**Note:**

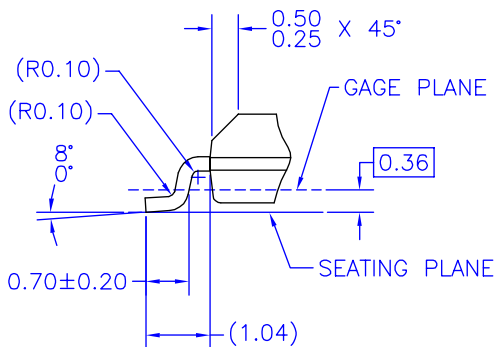
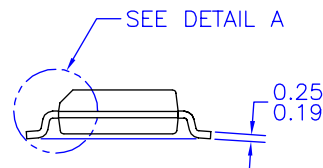
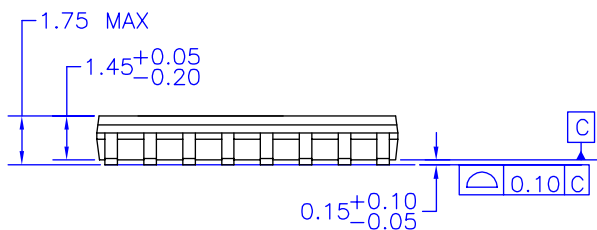
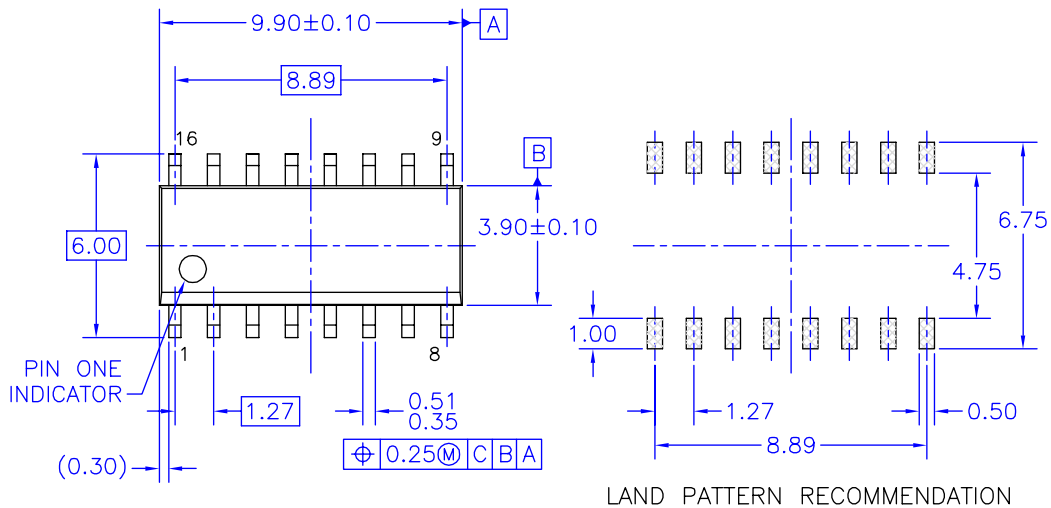
5. AC Parameters are guaranteed by DC correlated testing.

**RC Oscillator Notes:**

- $R_2 = 2 R_1$  to  $10 R_1$
- RC Oscillator applications are not recommended at supply voltages below 7.0V for  $R_1 < 50\text{k}\Omega$
- $f \approx \frac{1}{2.2 R_1 C_X}$  at  $V_{CC} = 10\text{V}$

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICROINCHES / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

**Physical Dimensions** (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

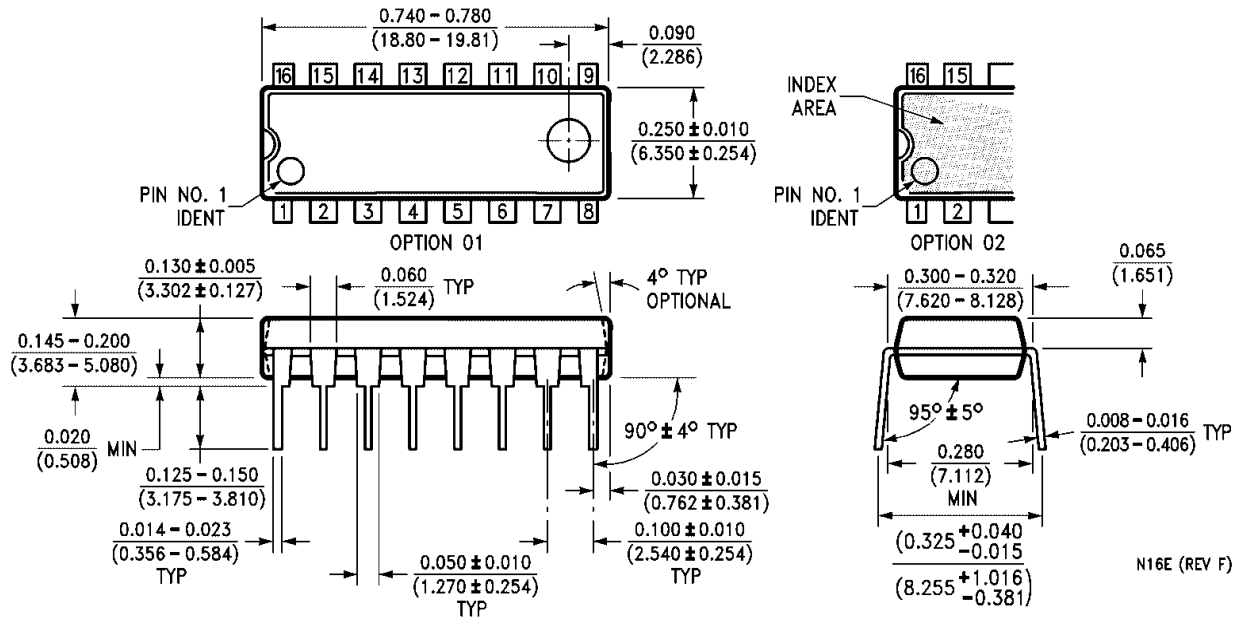



Figure 2. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

N16E (REV F)



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CROSSVOLT™	IntelliMAX™	QFET®	TinyBoost™
CTL™	ISOPLANAR™	QS™	TinyBuck™
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FACT®	Motion-SPM™	SMART START™	TinyPWM™
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FastvCore™	OPTOPLANAR®	STEALTH™	μSerDes™
FPS™	PDP-SPM™	SuperFET™	UHC®
FRFET®	Power220®	SuperSOT™-3	UniFET™
Global Power Resource™	Power247®	SuperSOT™-6	VCX™
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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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