



THE DATASHEET OF CD4511BF



CMOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)

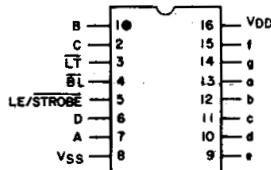


■ CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

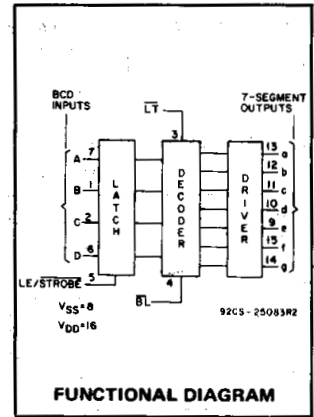
Lamp Test (LT), Blanking (BL), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

These devices are similar to the type MC14511.



TOP VIEW
92CS-25084RI
CD4511B
TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM

Features:

- High-output-sourcing capability up to 25 mA
- Input latches for BCD Code storage
- Lamp Test and Blanking capability
- 7-segment outputs blanked for BCD input codes > 1001
- 100% tested for quiescent current at 20 V
- Max. input current of 1 μ A at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Driving common-cathode LED displays
- Multiplexing with common-cathode LED displays
- Driving incandescent displays
- Driving low-voltage fluorescent displays

MAXIMUM RATINGS, Absolute-Maximum Values:

| | | | |
|---|--|--|--------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | Voltages referenced to V _{SS} Terminal) | | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | | | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | | | ±10mA |
| POWER DISSIPATION, PER PACKAGE (P _D): | | | |
| For T _A = -55°C to +100°C | | | 500mW |
| For T _A = +100°C to +125°C | Derate Linearity at 12mW/°C | | to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | | | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | | | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | | | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | | | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | | | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | | | +265°C |

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

| Characteristic | V _{DD} | Min. | Max. | Units |
|---|-----------------|------|------|-------|
| Supply Voltage Range (T _A): (Full Package-Temperature Range) | — | 3 | 18 | V |
| Set-Up Time (t _S) | 5 | 150 | — | ns |
| | 10 | 70 | — | ns |
| | 15 | 40 | — | ns |
| Hold Time (t _H) | 5 | 0 | — | ns |
| | 10 | 0 | — | ns |
| | 15 | 0 | — | ns |
| Strobe Pulse Width (t _W) | 5 | 400 | — | ns |
| | 10 | 160 | — | ns |
| | 15 | 100 | — | ns |

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4511B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | TEST CONDITIONS | | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | Units | |
|---|-------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|---|
| | I _{OH} (mA) | V _o (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | | |
| | | | | | | | | | Min. | Typ. | Max. | | |
| Quiescent Device Current: I _{DD} Max. | - | - | - | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA | |
| | - | - | - | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | | |
| | - | - | - | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | | |
| | - | - | - | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | | |
| Output Voltage: Low-Level V _{OL} Max. | - | - | 0.5 | 5 | 0.05 | | | | - | 0 | 0.05 | V | |
| | - | - | 0.10 | 10 | 0.05 | | | | - | 0 | 0.05 | | |
| | - | - | 0.15 | 15 | 0.05 | | | | - | 0 | 0.05 | | |
| High-Level V _{OH} Min. | - | - | 0.5 | 5 | 4 | 4 | 4.2 | 4.2 | 4.1 | 4.55 | - | V | |
| | - | - | 0.10 | 10 | 9 | 9 | 9.2 | 9.2 | 9.1 | 9.55 | - | | |
| Input Low Voltage, V _{IL} Max. | - | 0.5, 3.8 | - | 5 | 1.5 | | | | - | - | 1.5 | V | |
| | - | 1.8, 8 | - | 10 | 3 | | | | - | - | 3 | | |
| Input High Voltage, V _{IH} Min. | - | 1.5, 13.8 | - | 15 | 4 | | | | - | - | 4 | V | |
| | - | 0.5, 3.8 | - | 5 | 3.5 | | | | 3.5 | - | - | | |
| | - | 1.8, 8 | - | 10 | 7 | | | | 7 | - | - | V | |
| | - | 1.5, 13.8 | - | 15 | 11 | | | | 11 | - | - | | |
| Output Drive Voltage: High Level V _{OH} Min. | 0 | - | - | 5 | 4.0 | 4.0 | 4.20 | 4.20 | 4.10 | 4.55 | - | V | |
| | 5 | - | - | | - | - | - | - | - | 4.25 | - | | |
| | 10 | - | - | | 3.80 | 3.80 | 3.90 | 3.90 | 3.90 | 3.90 | 4.10 | | - |
| | 15 | - | - | | - | - | 3.50 | 3.50 | - | 3.95 | - | | |
| | 20 | - | - | | 3.55 | 3.55 | 3.30 | - | 3.40 | 3.75 | - | | |
| | 25 | - | - | | 3.40 | 3.40 | - | - | 3.10 | 3.55 | - | | |
| | 0 | - | - | 10 | 9.0 | 9.0 | 9.20 | 9.20 | 9.10 | 9.55 | - | V | |
| | 5 | - | - | | - | - | - | - | 9.25 | - | | | |
| | 10 | - | - | | 8.85 | 8.85 | 9.00 | 9.00 | 9.00 | 9.15 | - | | |
| | 15 | - | - | | - | - | - | - | 9.05 | - | | | |
| | 20 | - | - | | 8.70 | 8.70 | 8.40 | 8.40 | 8.60 | 8.90 | - | | |
| | 25 | - | - | | 8.60 | 8.60 | - | - | 8.30 | 8.75 | - | | |
| 0 | - | - | 15 | 14.0 | 14.0 | 14.20 | 14.20 | 14.10 | 14.55 | - | V | | |
| 5 | - | - | | - | - | - | - | 14.30 | - | | | | |
| 10 | - | - | | 13.90 | 13.90 | 14.0 | 14.0 | 14.0 | 14.20 | - | | | |
| 15 | - | - | | - | - | - | - | 14.10 | - | | | | |
| 20 | - | - | | 13.75 | 13.75 | 13.50 | 13.50 | 13.70 | 13.95 | - | | | |
| 25 | - | - | | 13.65 | 13.65 | - | - | 13.50 | 13.80 | - | | | |
| Output Low (Sink) Current, I _{OL} Min. | - | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA | |
| | - | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | | |
| | - | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | | |
| Input Current, I _{IN} Max. | - | 0.18 | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA | |

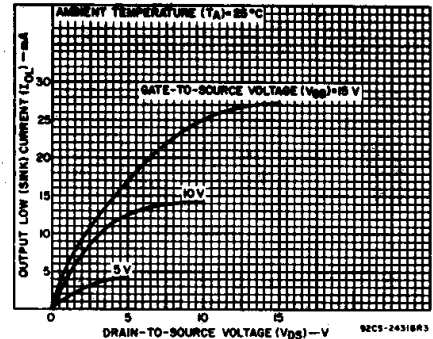


Fig. 1 - Typical output low (sink) current characteristics.

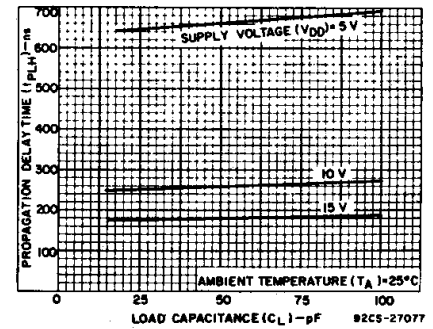


Fig. 2 - Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

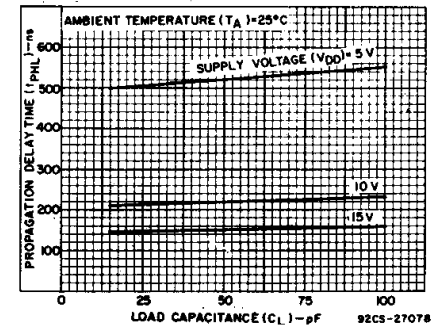


Fig. 3 - Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

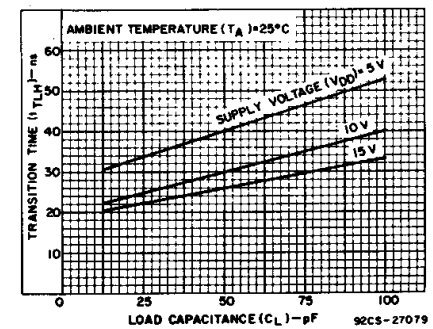


Fig. 4 - Typical low-to-high-level transition time as a function of load capacitance.

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | Test Conditions | LIMITS All Packages | | | UNITS |
|---|-----------------|------------------------|------|------|-------|
| | | V_{DD} Volts | Min. | Typ. | |
| Propagation Delay Time: (Data) High-to-Low Level, t_{PHL} | 5 | — | 520 | 1040 | ns |
| | 10 | — | 210 | 420 | |
| | 15 | — | 150 | 300 | |
| Low-to-High Level, t_{PLH} | 5 | — | 660 | 1320 | ns |
| | 10 | — | 260 | 520 | |
| | 15 | — | 180 | 360 | |
| Propagation Delay Time: (BL) High-to-Low Level, t_{PHL} | 5 | — | 350 | 700 | ns |
| | 10 | — | 175 | 350 | |
| | 15 | — | 125 | 250 | |
| Low-to-High Level, t_{PLH} | 5 | — | 400 | 800 | ns |
| | 10 | — | 175 | 350 | |
| | 15 | — | 150 | 300 | |
| Propagation Delay Time: (LT) High-to-Low Level, t_{PHL} | 5 | — | 250 | 500 | ns |
| | 10 | — | 125 | 250 | |
| | 15 | — | 85 | 170 | |
| Low-to-High Level, t_{PLH} | 5 | — | 150 | 300 | ns |
| | 10 | — | 75 | 150 | |
| | 15 | — | 50 | 100 | |
| Transition Time: Low-to-High Level, t_{TLH} | 5 | — | 40 | 80 | ns |
| | 10 | — | 30 | 60 | |
| | 15 | — | 25 | 50 | |
| High-to-Low Level, t_{THL} | 5 | — | 125 | 310 | ns |
| | 10 | — | 75 | 185 | |
| | 15 | — | 65 | 160 | |
| Minimum Set-Up Time, t_S | 5 | 150 | 75 | — | ns |
| | 10 | 70 | 35 | — | |
| | 15 | 40 | 20 | — | |
| Minimum Hold Time, t_H | 5 | 0 | -75 | — | ns |
| | 10 | 0 | -35 | — | |
| | 15 | 0 | -20 | — | |
| Strobe Pulse Width, t_W | 5 | 400 | 200 | — | ns |
| | 10 | 160 | 80 | — | |
| | 15 | 100 | 50 | — | |
| Input Capacitance, C_{IN} | | — | 5 | 7.5 | pF |

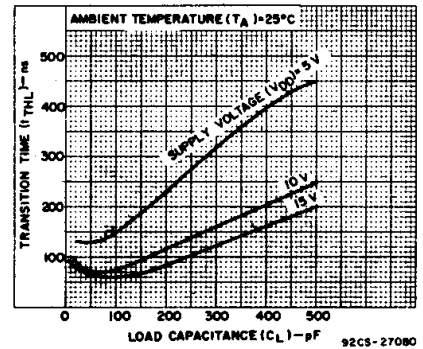


Fig. 5 - Typical high-to-low transition time as a function of load capacitance.

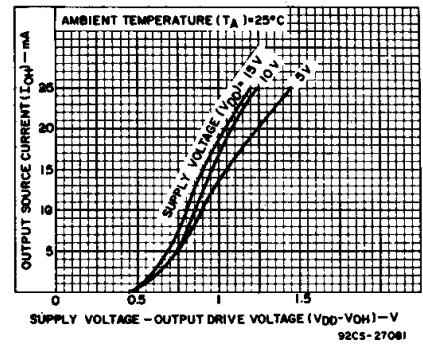


Fig. 6 - Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

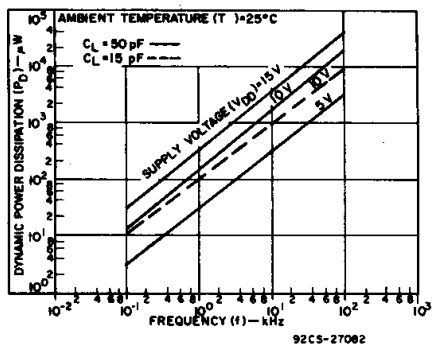


Fig. 7 - Typical dynamic power dissipation characteristics.

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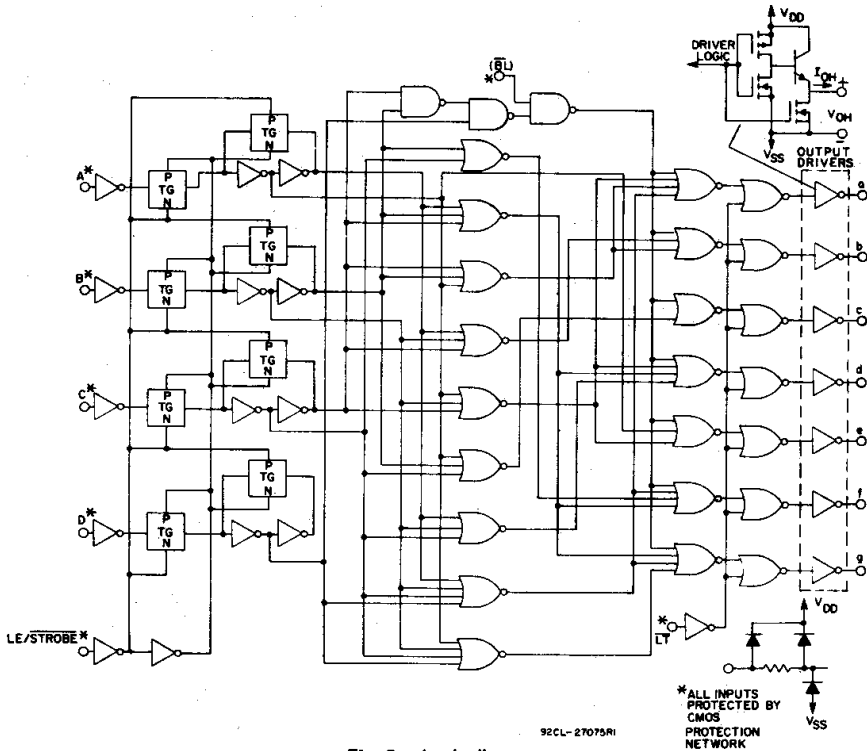


Fig. 8 - Logic diagram.

TRUTH TABLE

| LE | BI | LT | D | C | B | A | a | b | c | d | e | f | g | Display |
|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---------|
| X | X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | X | X | X | X | * | * | * | * | * | * | * | * |

X = Don't Care * Depends on BCD code previously applied when LE = 0
 Note: Display is blank for all illegal input codes (BCD > 1001).

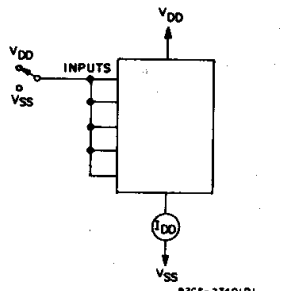


Fig. 9 - Quiescent device current.

TEST CIRCUITS

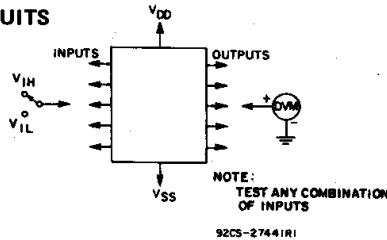


Fig. 10 - Input voltage.

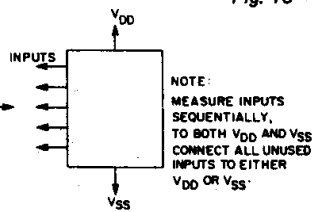


Fig. 11 - Input current.

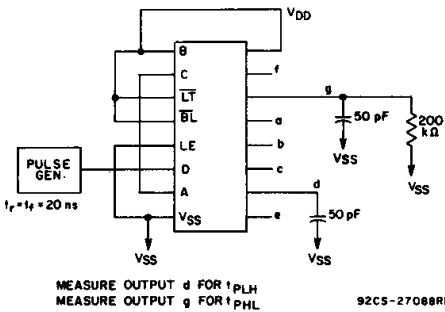


Fig. 12 - Data propagation delay.

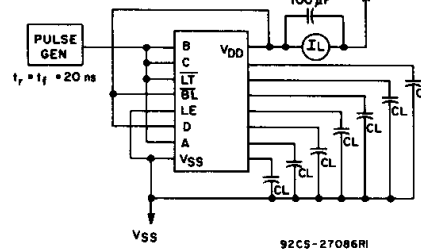
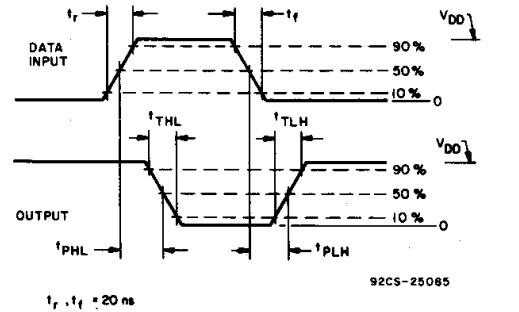
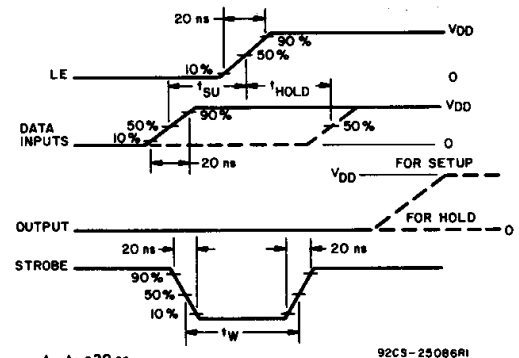


Fig. 13 - Dynamic power dissipation.



t_r, t_f = 20 ns

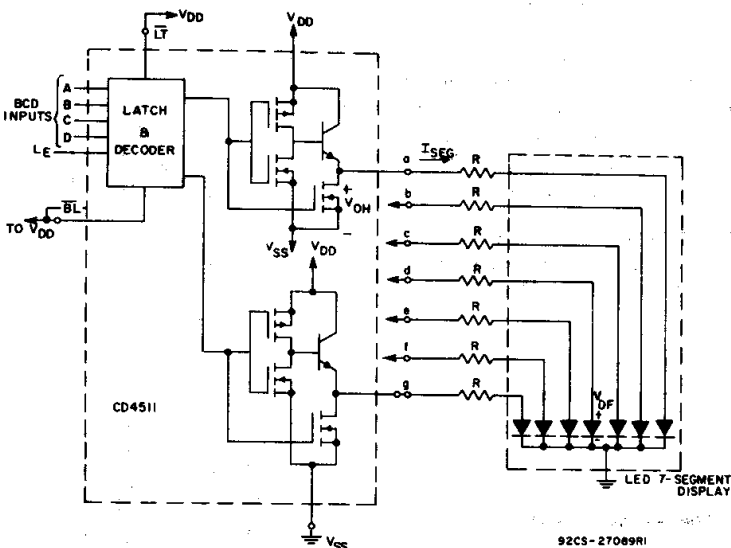


t_r, t_f = 20 ns

Fig. 14 - Dynamic waveforms.

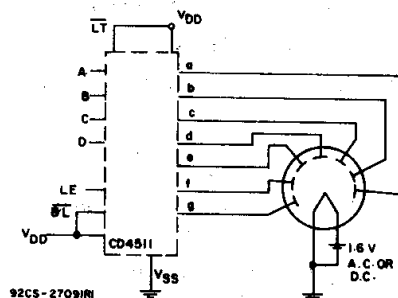
CD4511B Types

APPLICATIONS Interfacing with Various Displays



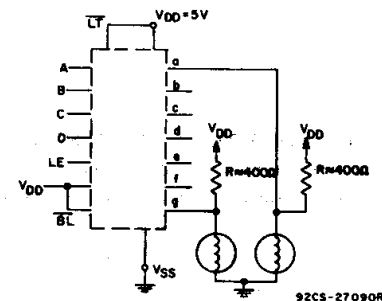
Duty Cycle = 100%
 $I_{SEG} = I_{DIODE\ AVG.} = 20\text{ mA at Luminous Intensity/Segment} = 250\text{ microcandles}$
 $R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$

Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).

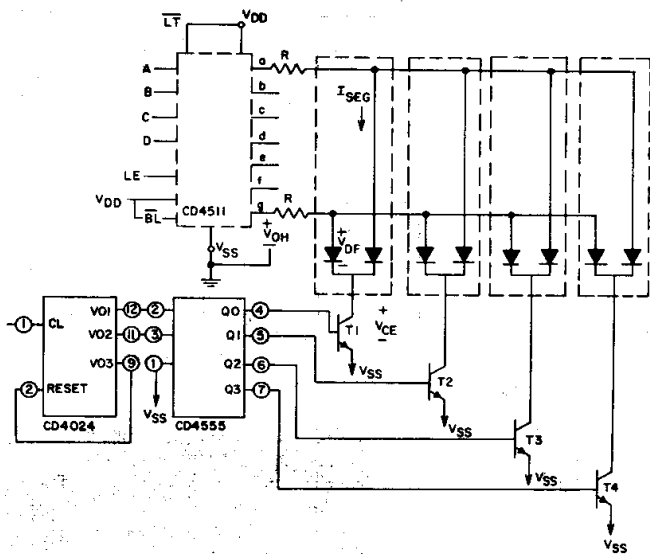


A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.
 Fig. 16 - Driving low-voltage fluorescent displays.



2 of 7 Segments Shown Connected
 Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.
 Fig. 17 - Driving incandescent displays (RCA Numitron DR2000 series displays).

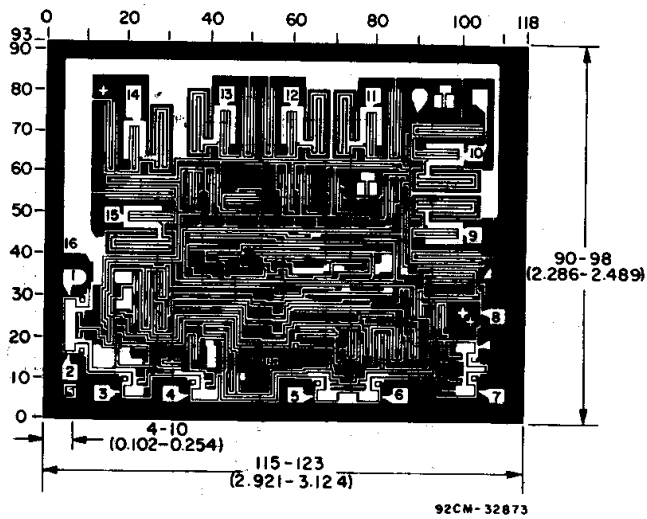


Multiplexing Scheme Showing 2 of 7 Segments Connected
 Transistors T₁-T₄ (RCA-2N3053 or 2N2102) have I_C Max. rating > 7x I_{SEG}

Duty Cycle = 25%
 $I_{SEG} = (I_{DIODE\ AVG.}) \times 4$
 $R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$

All unused inputs on CD4555 are connected to V_{DD} or V_{SS}.

Fig. 18 - Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).



Dimensions and pad layout for CD4511B chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4511BE | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4511BE | Samples |
| CD4511BEE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4511BE | Samples |
| CD4511BF | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD4511BF | Samples |
| CD4511BF3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD4511BF3A | Samples |
| CD4511BNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4511B | Samples |
| CD4511BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4511B | Samples |
| CD4511BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM511B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4511B, CD4511B-MIL :

- Catalog : [CD4511B](#)
- Military : [CD4511B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4511BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4511BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4511BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4511BPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4511BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4511BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4511BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4511BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

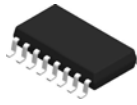
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

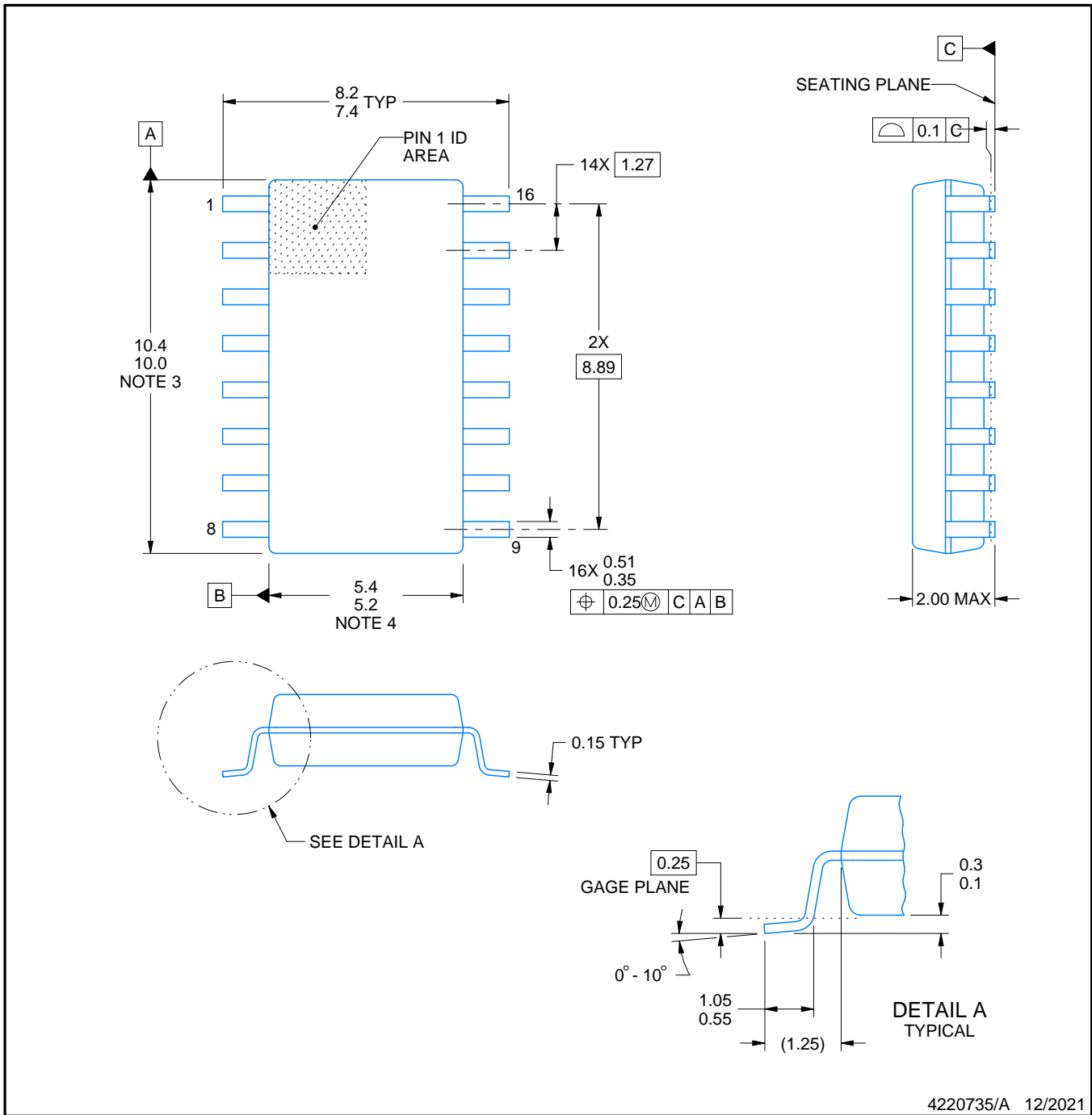


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

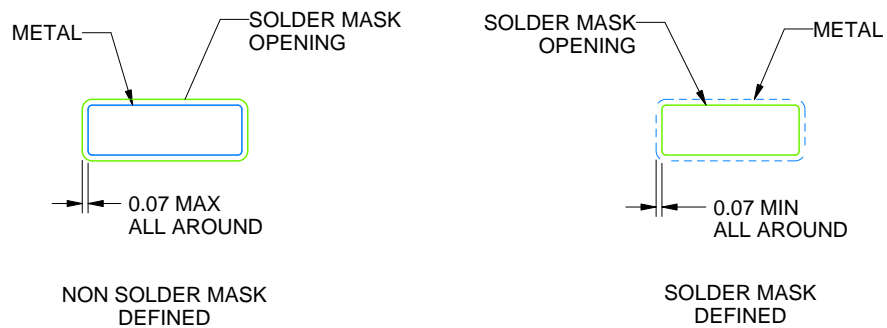
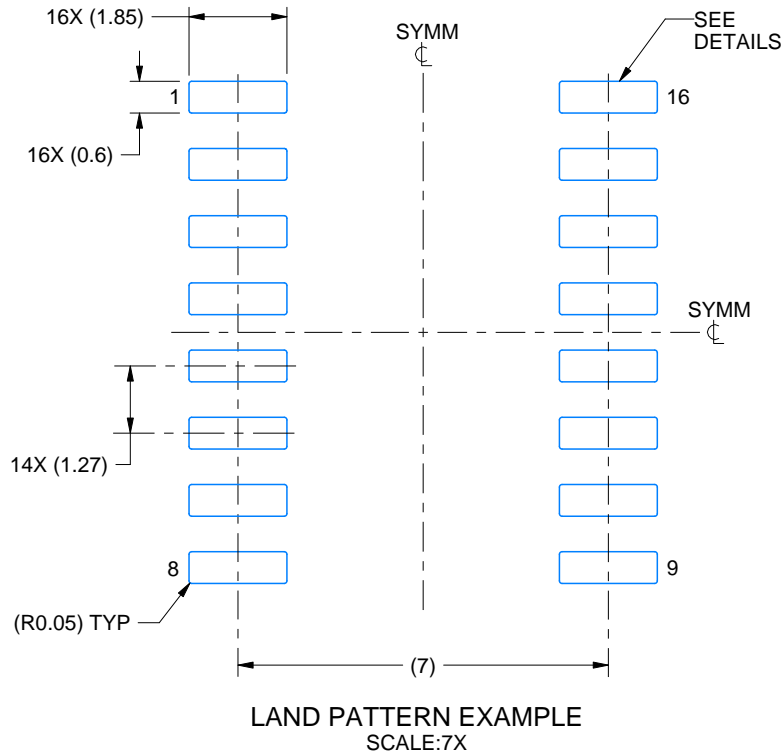
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

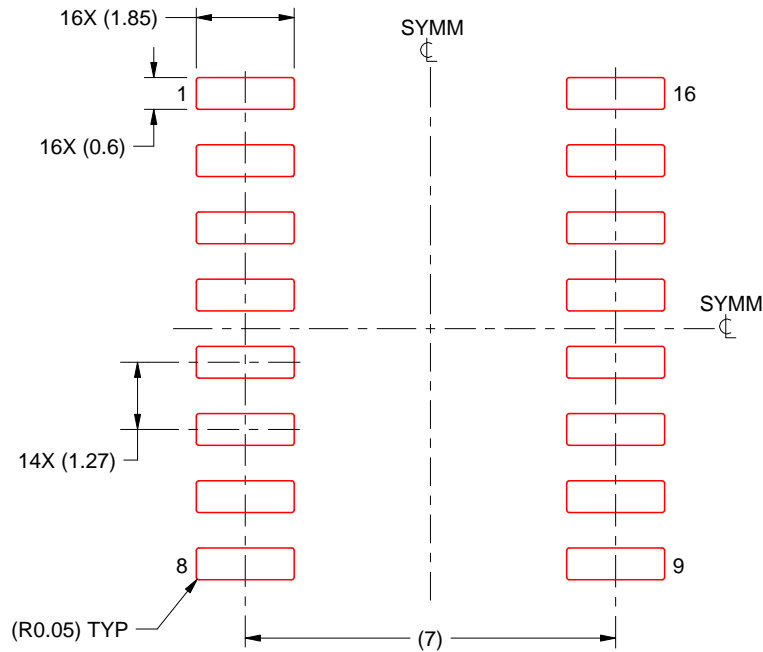
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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