



**THE DATASHEET OF  
CD74HC4002NSR**



## High-Speed CMOS Logic Dual 4-Input NOR Gate

August 1997 - Revised October 2003

### Features

- Typical Propagation Delay = 8ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$

### Description

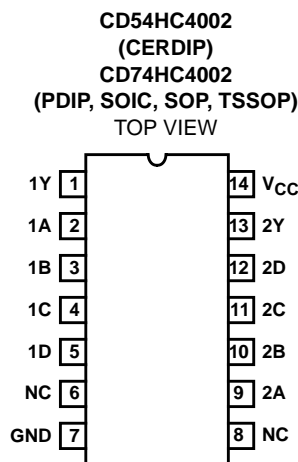
The 'HC4002 logic gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 'HC4002 logic family is functional as well as pin compatible with the standard LS logic family.

### Ordering Information

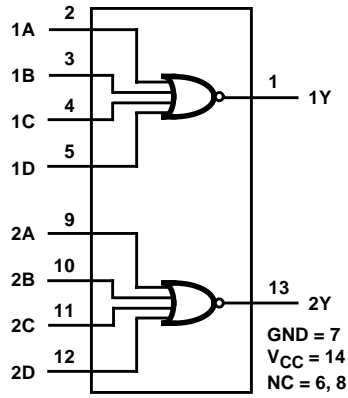
| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC4002F3A | -55 to 125       | 14 Ld CERDIP |
| CD74HC4002E   | -55 to 125       | 14 Ld PDIP   |
| CD74HC4002M   | -55 to 125       | 14 Ld SOIC   |
| CD74HC4002MT  | -55 to 125       | 14 Ld SOIC   |
| CD74HC4002M96 | -55 to 125       | 14 Ld SOIC   |
| CD74HC4002NSR | -55 to 125       | 14 Ld SOP    |
| CD74HC4002PW  | -55 to 125       | 14 Ld TSSOP  |
| CD74HC4002PWR | -55 to 125       | 14 Ld TSSOP  |
| CD74HC4002PWT | -55 to 125       | 14 Ld TSSOP  |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout



**Functional Diagram**

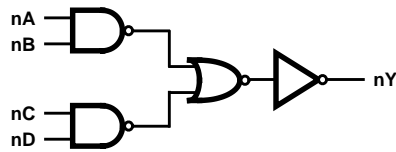


TRUTH TABLE

| INPUTS |    |    |    | OUTPUT |
|--------|----|----|----|--------|
| nA     | nB | nC | nD | nY     |
| L      | L  | L  | L  | H      |
| H      | X  | X  | X  | L      |
| X      | H  | X  | X  | L      |
| X      | X  | H  | X  | L      |
| X      | X  | X  | H  | L      |

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant

**Logic Symbol**



## CD54HC4002, CD74HC4002

### Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                          | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                           |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                          |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$     |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....           | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ ..... | $\pm 50mA$  |

### Thermal Information

|  |                |
|--|----------------|
| Package Thermal Impedance, $\theta_{JA}$ (see Note 1): |                |
| E (PDIP) Package .....                                 | 80°C/W         |
| M (SOIC) Package .....                                 | 86°C/W         |
| NS (SOP) Package .....                                 | 76°C/W         |
| PW (TSSOP) Package .....                               | 113°C/W        |
| Maximum Junction Temperature .....                     | 150°C          |
| Maximum Storage Temperature Range .....                | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) .....         | 300°C          |
| (SOIC - Lead Tips Only)                                |                |

### Operating Conditions

|   |                |
|---|----------------|
| Temperature Range ( $T_A$ ) .....               | -55°C to 125°C |
| Supply Voltage Range, $V_{CC}$                  |                |
| HC Types .....                                  | .2V to 6V      |
| HCT Types .....                                 | 4.5V to 5.5V   |
| DC Input or Output Voltage, $V_I$ , $V_O$ ..... | 0V to $V_{CC}$ |
| Input Rise and Fall Time                        |                |
| 2V .....  | 1000ns (Max)   |
| 4.5V .....                                      | 500ns (Max)    |
| 6V .....  | 400ns (Max)    |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|---|----------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|   |          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| High Level Input Voltage                | $V_{IH}$ | -                    | -          | 2            | 1.5  | -   | -         | 1.5           | -       | 1.5            | -       | V       |
|   |          |                      |            | 4.5          | 3.15 | -   | -         | 3.15          | -       | 3.15           | -       | V       |
|   |          |                      |            | 6            | 4.2  | -   | -         | 4.2           | -       | 4.2            | -       | V       |
| Low Level Input Voltage                 | $V_{IL}$ | -                    | -          | 2            | -    | -   | 0.5       | -             | 0.5     | -              | 0.5     | V       |
|   |          |                      |            | 4.5          | -    | -   | 1.35      | -             | 1.35    | -              | 1.35    | V       |
|   |          |                      |            | 6            | -    | -   | 1.8       | -             | 1.8     | -              | 1.8     | V       |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02      | 2            | 1.9  | -   | -         | 1.9           | -       | 1.9            | -       | V       |
|   |          |                      |            | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
|   |          |                      |            | 6            | 5.9  | -   | -         | 5.9           | -       | 5.9            | -       | V       |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -   | -         | -             | -       | -              | -       | V       |
|   |          |                      |            | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
|   |          |                      |            | 6            | 5.48 | -   | -         | 5.34          | -       | 5.2            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02       | 2            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                      |            | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                      |            | 6            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -   | -         | -             | -       | -              | -       | V       |
|   |          |                      |            | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
|   |          |                      |            | 6            | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or GND      | -          | 6            | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                | $I_{CC}$ | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 2         | -             | 20      | -              | 40      | $\mu A$ |

## CD54HC4002, CD74HC4002

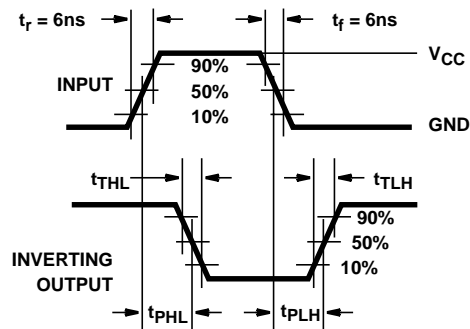
### Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER                                     | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|--------------------|---------------------|--------------|------|-----|---------------|----------------|-------|
|   |                    |                     |              | TYP  | MAX | MAX           | MAX            |       |
| <b>HC TYPES</b>                               |                    |                     |              |      |     |               |                |       |
| Propagation Delay,<br>nA, nB, nC, nD to nY    | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2            | -    | 100 | 125           | 150            | ns    |
|   |                    |                     | 4.5          | -    | 20  | 25            | 30             | ns    |
|   |                    |                     | 6            | -    | 17  | 21            | 26             | ns    |
|   |                    | $C_L = 15\text{pF}$ | 5            | 8    | -   | -             | -              | ns    |
| Output Transition Times<br>(Figure 1)         | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2            | -    | 75  | 95            | 110            | ns    |
|   |                    |                     | 4.5          | -    | 15  | 19            | 22             | ns    |
|   |                    |                     | 6            | -    | 13  | 16            | 19             | ns    |
| Input Capacitance                             | $C_{IN}$           | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Power Dissipation<br>Capacitance (Notes 2, 3) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5            | 22   | -   | -             | -              | pF    |

**NOTES:**

2.  $C_{PD}$  is used to determine the dynamic power consumption, per gate.
3.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuit and Waveform



**FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)    | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|----------------------------|-------------------------|
| CD54HC4002F3A    | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 8404401CA<br>CD54HC4002F3A | <a href="#">Samples</a> |
| CD74HC4002E      | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HC4002E                | <a href="#">Samples</a> |
| CD74HC4002M      | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC4002M                    | <a href="#">Samples</a> |
| CD74HC4002M96    | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC4002M                    | <a href="#">Samples</a> |
| CD74HC4002MT     | ACTIVE        | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC4002M                    | <a href="#">Samples</a> |
| CD74HC4002PW     | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HJ4002                     | <a href="#">Samples</a> |
| CD74HC4002PWR    | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HJ4002                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC4002, CD74HC4002 :**

- Catalog: [CD74HC4002](#)
- Military: [CD54HC4002](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC4002M96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4002MT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4002PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC4002M96 | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| CD74HC4002MT  | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| CD74HC4002PWR | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



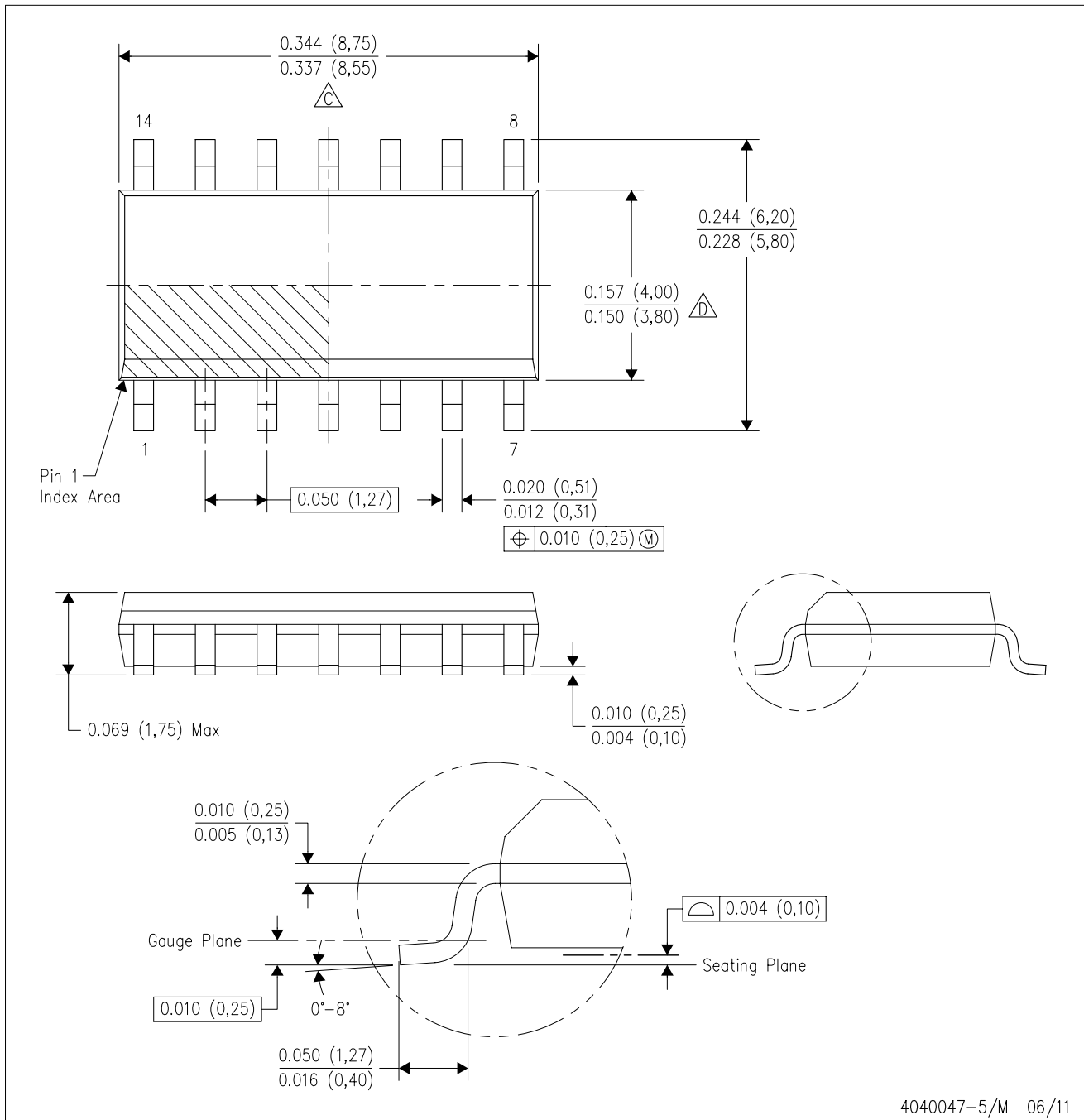
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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