WINSOURCE
ELECTRONICS

THE DATASHEET OF

NTD30N02G

NTD30N02

Power MOSFET
30 Amps, 24 Volts

N−Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb−Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	Vdc
Drain Current − Continuous @ T_A = 25°C − Single Pulse ($t_p \leq 10\ \mu s$)	 I_D I_{DM}	 30 100	Adc Apk
Total Power Dissipation @ T_A = 25°C	P_D	75	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 24 Vdc, V_{GS} = 10 Vdc, L = 1.0 mH, I_L(pk) = 10 A, R_G = 25 Ω)	E_{AS}	50	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

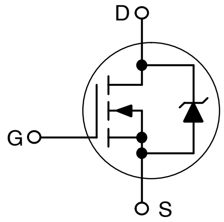
1. When surface mounted to an FR4 board using 1 in. pad size, (Cu Area 1.127 sq in).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 sq in).

ON Semiconductor®

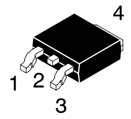
http://onsemi.com

30 AMPERES
24 VOLTS
$R_{DS(on)}$ = 11.2 mΩ (Typ.)

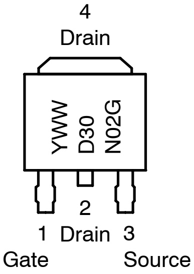
N−Channel



MARKING DIAGRAM



DPAK
CASE 369C
STYLE 2



D30N02 = Device Code
Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NTD30N02	DPAK	75 Units/Rail
NTD30N02G	DPAK (Pb−Free)	75 Units/Rail
NTD30N02T4	DPAK	2500 Tape & Reel
NTD30N02T4G	DPAK (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

February, 2006 − Rev. 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	24	26.5	–	Vdc
Temperature Coefficient (Positive)			–	25.5	–	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)			–	–	0.8	
(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc)			–	–	1.0	
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			–	–	10	
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	2.1	3.0	Vdc
Threshold Temperature Coefficient (Negative)			–	−4.1	–	mV/°C
Static Drain−to−Source On−Resistance (Note 3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 30 Adc)			–	–	14.5	
(V_{GS} = 10 Vdc, I_D = 20 Adc)			–	11.2	14.5	
(V_{GS} = 4.5 Vdc, I_D = 15 Adc)			–	20	24	
Forward Transconductance (Note 3) (V_{DS} = 10 Vdc, I_D = 15 Adc)		g_{FS}	–	20	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	1000	–	pF
Output Capacitance		C_{oss}	–	425	–	
Transfer Capacitance		C_{rss}	–	175	–	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 20 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	–	7.0	15	ns
Rise Time		t_r	–	28	55	
Turn−Off Delay Time		$t_{d(off)}$	–	22	35	
Fall Time		t_f	–	12	20	
Turn−On Delay Time	(V_{DD} = 20 Vdc, I_D = 15 Adc, V_{GS} = 4.5 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	–	12.5	–	ns
Rise Time		t_r	–	115	–	
Turn−Off Delay Time		$t_{d(off)}$	–	15	–	
Fall Time		t_f	–	17	–	
Gate Charge	(V_{DS} = 20 Vdc, I_D = 30 Adc, V_{GS} = 4.5 Vdc) (Note 3)	Q_T	–	14.4	20	nC
		Q_1	–	4.0	–	
		Q_2	–	8.5	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 15 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	0.95	1.2	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc) (Note 3)		–	1.10	–	
	(I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		–	0.80	–	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	–	30	–	ns
		t_a	–	14.5	–	
		t_b	–	15.5	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.013	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

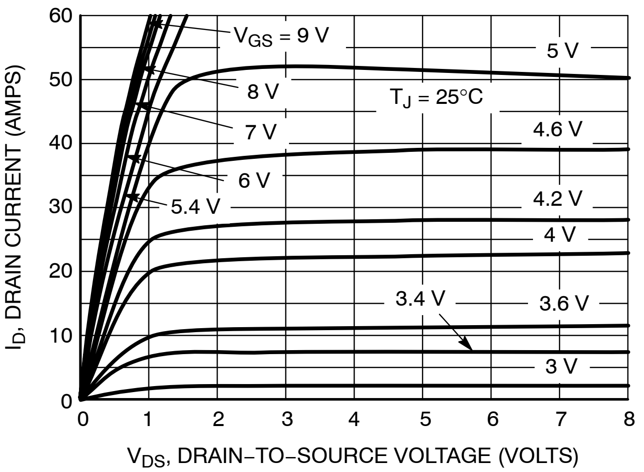


Figure 1. On−Region Characteristics

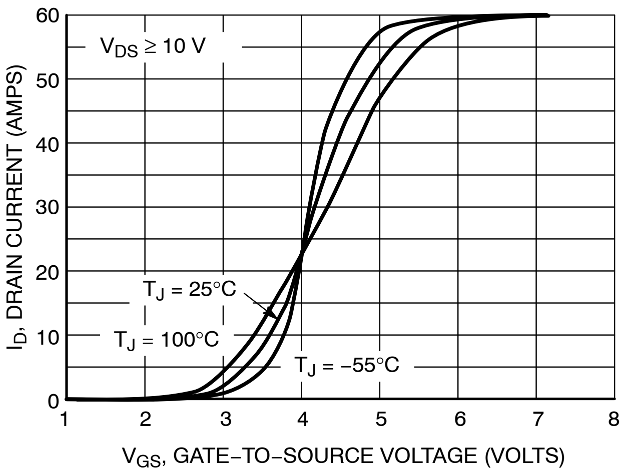


Figure 2. Transfer Characteristics

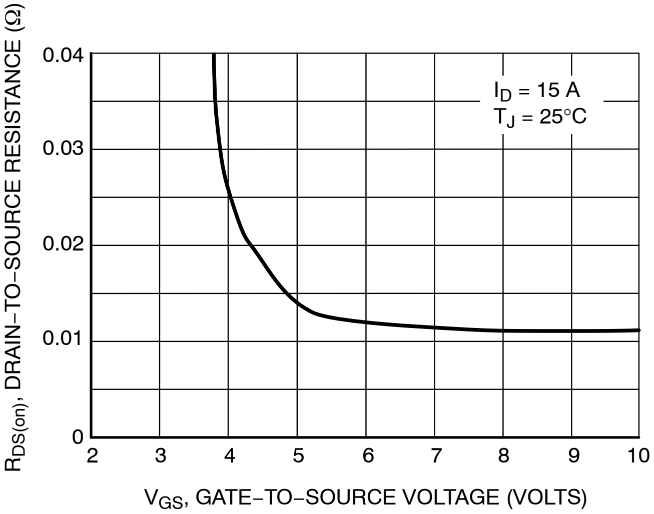


Figure 3. On−Resistance versus Gate−to−Source Voltage

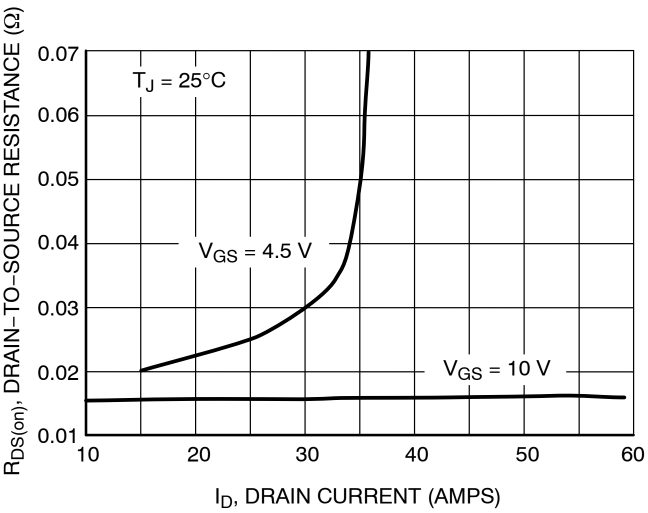


Figure 4. On−Resistance versus Drain Current and Gate Voltage

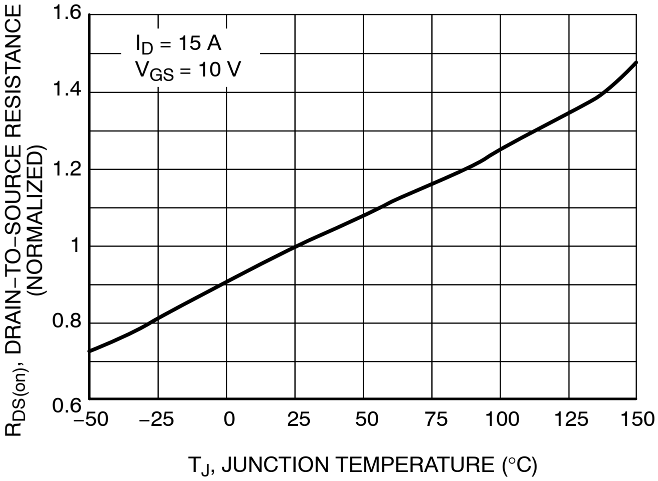


Figure 5. On−Resistance Variation with Temperature

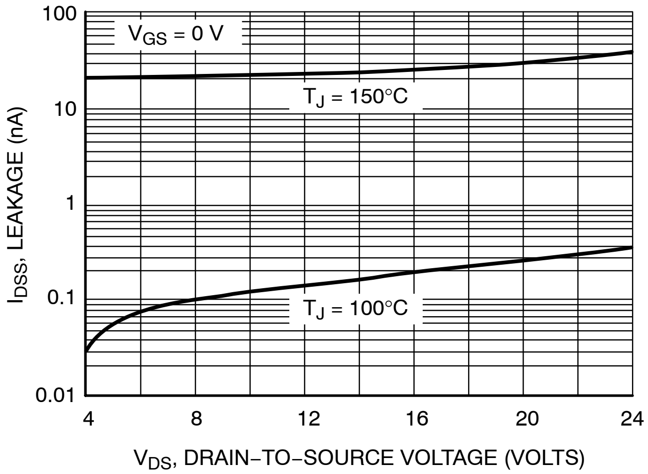


Figure 6. Drain−to−Source Leakage Current versus Voltage

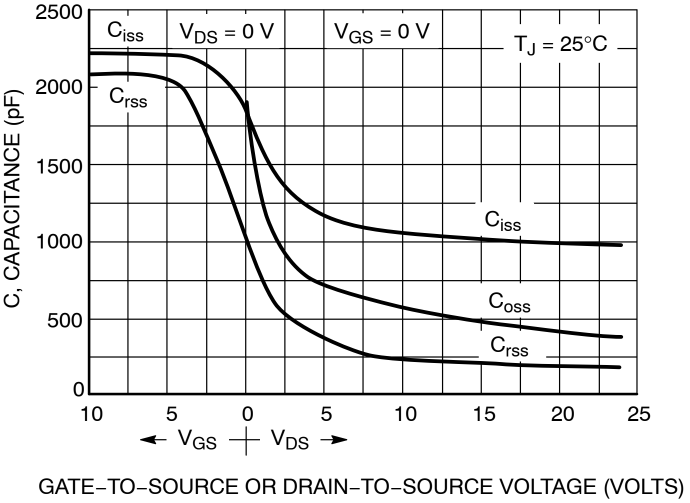
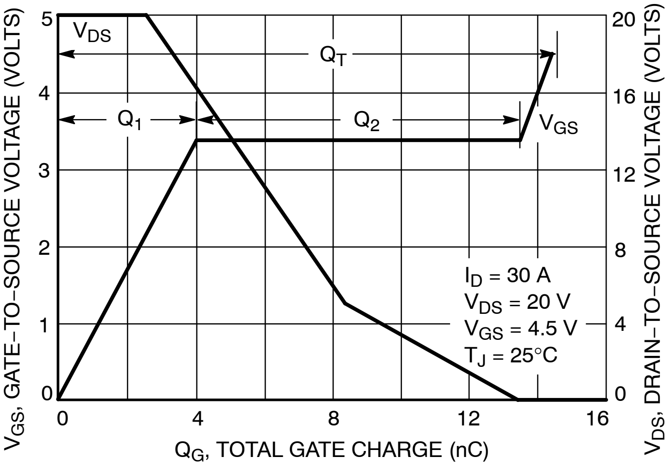


Figure 7. Capacitance Variation



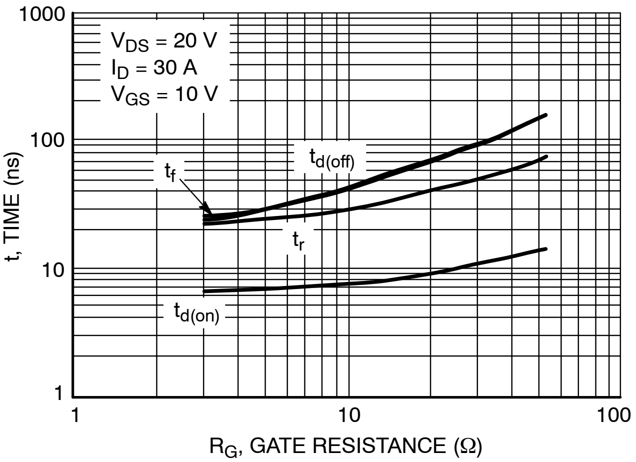


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

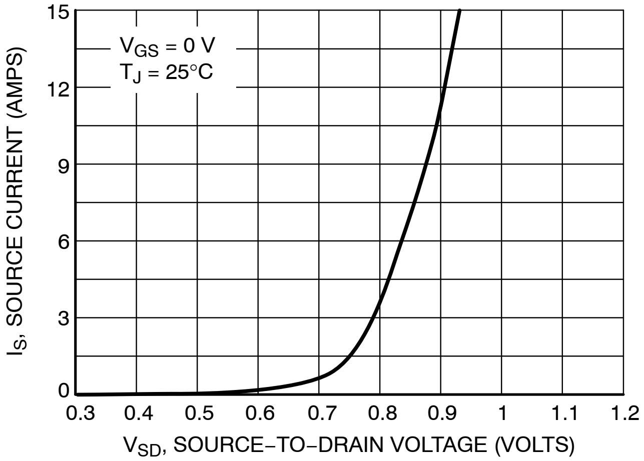
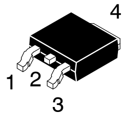


Figure 10. Diode Forward Voltage versus Current

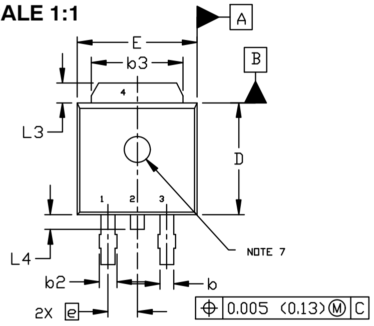
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



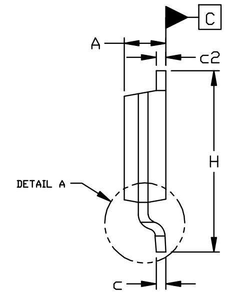
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

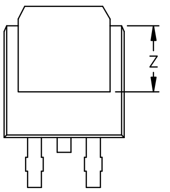


SIDE VIEW

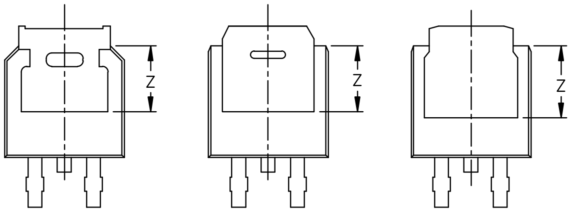
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

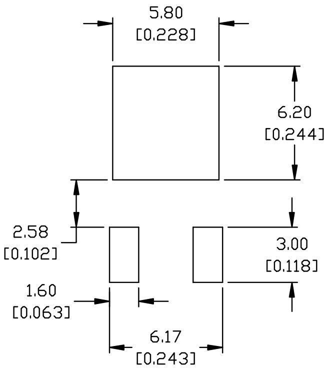


BOTTOM VIEW



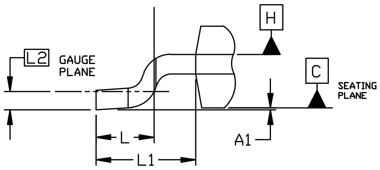
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



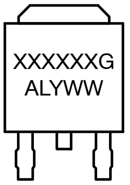
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

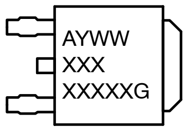


DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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