THE DATASHEET OF

CDCE72010RGCR

Ten Output High Performance Clock Synchronizer, Jitter Cleaner, and Clock Distributor

Check for Samples: CDCE72010

FEATURES

- High Performance LVPECL, LVDS, LVCMOS PLL Clock Synchronizer
- Two Reference Clock Inputs (Primary and Secondary Clock) for Redundancy Support with Manual or Automatic Selection
- Accepts Two Differential Input (LVPECL or LVDS) References up to 500MHz (or Two LVCMOS Inputs up to 250MHz) as PLL Reference
- VCXO_IN Clock is Synchronized to One of Two Reference Clocks
- VCXO_IN Frequencies up to 1.5GHz (LVPECL) 800MHz for LVDS and 250MHz for LVCMOS Level Signaling
- Outputs Can be a Combination of LVPECL, LVDS, and LVCMOS (Up to 10 Differential LVPECL or LVDS Outputs or up to 20 LVCMOS Outputs), Output 9 can be Converted to an Auxiliary Input as a 2nd VC(X)O.
- Output Divider is Selectable to Divide by 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 50, 56, 60, 64, 70, or 80 On Each Output Individually up to Eight Dividers. (Except for Output 0 and 9, Output 0 Follows Output 1 Divider and Output 9 Follows Output 8 Divider)
- SPI Controllable Device Setting
- Individual Output Enable Control via SPI Interface
- Integrated On-Chip Non-Volatile Memory (EEPROM) to Store Settings without the Need to Apply High Voltage to the Device
- Optional Configuration Pins to Select Between Two Default Settings Stored in EEPROM
- Efficient Jitter Cleaning from Low PLL Loop Bandwidth
- Very Low Phase Noise PLL Core
- Programmable Phase Offset (Input Reference to Outputs)
- Wide Charge-Pump Current Range From 200µA to 3mA
- Presets Charge-Pump to $V_{CC\_CP}/2$ for Fast Center-Frequency Setting of VC(X)O, Controlled Via the SPI Bus
- SERDES Startup Mode (Depending on VCXO Range)
- Auxiliary Input: Output 9 can Serve as 2nd VCXO Input to Drive All Outputs or to Serve as PLL Feedback Signal
- $\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$ Input Pin to Serve as Reset or Hold Functions
- REFERENCE SELECT for Manual Select Between Primary and Secondary Reference Clocks
- POWER DOWN ($\overline{\text{PD}}$) to Put Device in Standby Mode
- Analog and Digital PLL Lock Indicator
- Internally Generated VBB Bias Voltages for Single-Ended Input Signals
- Frequency Hold-Over Mode Activated by $\overline{\text{HOLD}}$ Pin or SPI Bus to Improve Fail-Safe Operation
- Input to All Outputs Skew Control
- Individual Skew Control for Each Output with Each Output Divider
- Packaged in a QFN-64 Package
- ESD Protection Exceeds 2kV HBM
- Industrial Temperature Range of –40°C to 85°

APPLICATIONS

- Low Jitter Clock Driver for High-End Telecom and Wireless Applications
- High Precision Test Equipment

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The CDCE72010 is a high-performance, low phase noise, and low skew clock synchronizer that synchronizes a VCXO (Voltage Controlled Crystal Oscillator) or VCO (Voltage Controlled Oscillator) frequency to one of two reference clocks. The clock path is fully programmable providing the user with a high degree of flexibility. The following relationship applies to the dividers:

Frequency (VCXO_IN or AUX_IN) / Frequency (PRI_REF or SEC_REF) = (P*N)/(R*M)

The VC(X)O_IN clock operates up to 1.5GHz through the selection of external VC(X)O and loop filter components. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements.

The CDCE72010 can lock to one of two reference clock inputs (PRI_REF and SEC_REF) and supports frequency hold-over mode for fail-safe and system redundancy. The outputs of the CDCE72010 are user definable and can be any combination of up to 10 LVPECL/LVDS outputs or up to 20 LVCMOS outputs. The built-in synchronization latches ensure that all outputs are synchronized for very low output skew.

All device settings, including output signaling, divider value selection, input selection, and many more, are programmable with the SPI (4-wire Serial Peripheral Interface). The SPI allows individual control of the device settings.

The device operates in a 3.3V environment and is characterized for operation from –40°C to +85°C.

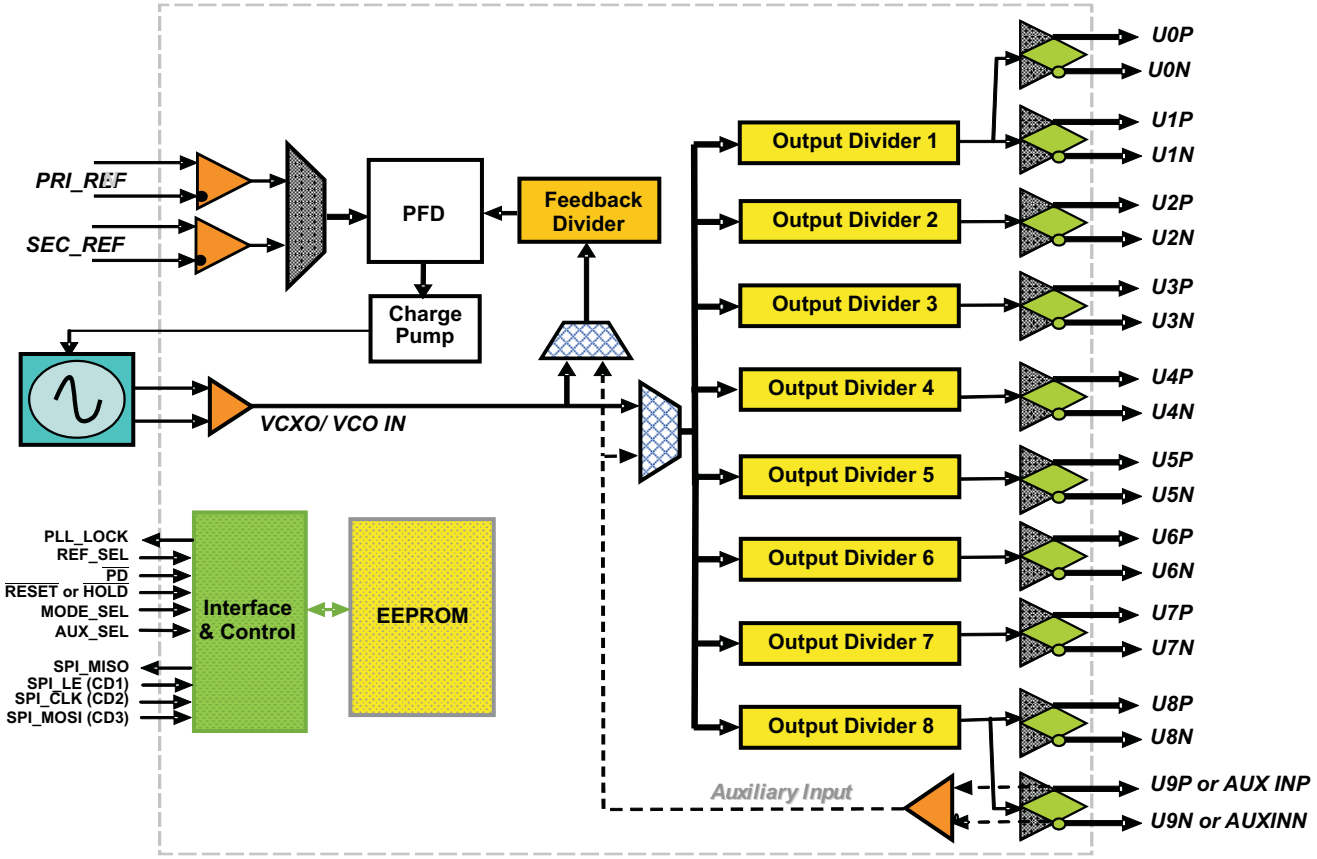
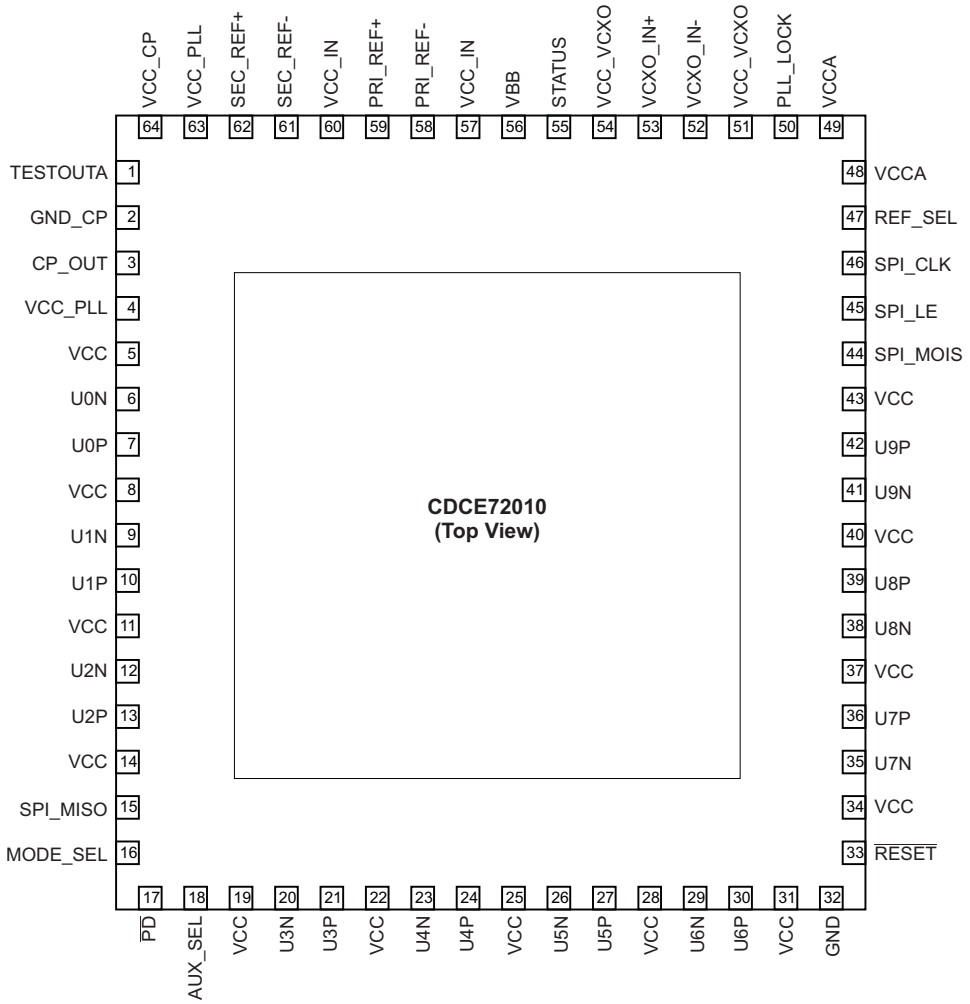
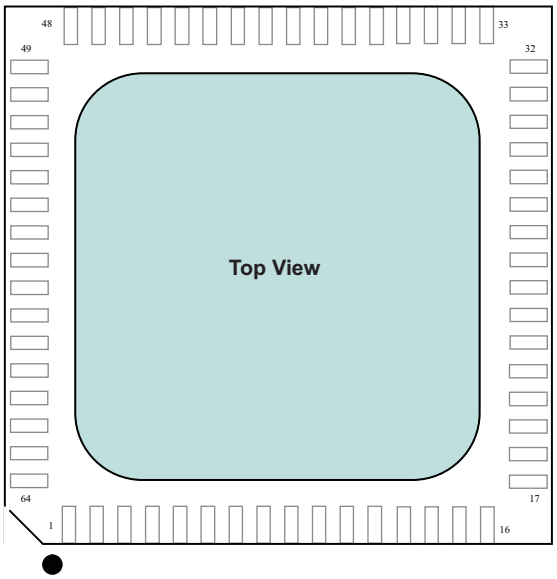


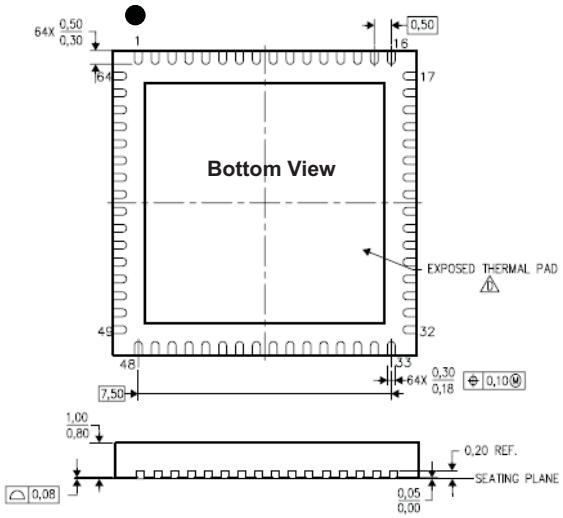
Figure 1. High Level Block Diagram of the CDCE72010


VCC_CP 64
VCC_PLL 63
SEC_REF+ 62
SEC_REF- 61
VCC_IN 60
PRI_REF+ 59
PRI_REF- 58
VCC_IN 57
VBB 56
STATUS 55
VCC_VCXO 54
VCXO_IN+ 53
VCXO_IN- 52
VCC_VCXO 51
PLL_LOCK 50
VCCA 49
TESTOUTA 1
GND_CP 2
CP_OUT 3
VCC_PLL 4
VCC 5
U0N 6
U0P 7
VCC 8
U1N 9
U1P 10
VCC 11
U2N 12
U2P 13
VCC 14
SPI_MISO 15
MODE_SEL 16
48 VCCA
47 REF_SEL
46 SPI_CLK
45 SPI_LE
44 SPI_MOIS
43 VCC
42 U9P
41 U9N
40 VCC
39 U8P
38 U8N
37 VCC
36 U7P
35 U7N
34 VCC
33 RESET
CDCE72010
(Top View)
17 PD
18 AUX_SEL
19 VCC
20 U3N
21 U3P
22 VCC
23 U4N
24 U4P
25 VCC
26 U5N
27 U5P
28 VCC
29 U6N
30 U6P
31 VCC
32 GND

PACKAGE

The CDCE72010 is available in a 64-pin lead-free “green” plastic quad flatpack package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments package designator is RGC (S-PQFP-N64).





PIN FUNCTIONS

PIN		I/O	DESCRIPTION(1)
NAME	NO.		
VCC	5, 8, 11, 14, 19 22, 25, 28, 31 34, 37, 40 and 43	Power	3.3V supply for the output buffers. (2)
VCC_PLL	4, 63	A. Power	3.3V PLL supply voltage for the PLL circuitry.
VCC_IN	57, 60	A. Power	3.3V reference input buffers and circuitry supply voltage.
VCC_VCXO	51, 54	A. Power	3.3V VCXO input buffer and circuitry supply voltage.
GND	32	Ground	Ground connected to thermal pad internally.
GND	PAD	Ground	Ground on thermal pad. See layout recommendations.
VCCA	48, 49	A. Power	3.3V for internal analog circuitry power supply
GND_CP	2	A. Ground	Analog ground for charge pump
VCC_CP	64	A. Power	Charge pump power supply pin used to have the same supply as the external VCO/VCXO. It can be set from 2.3V to 3.6V.
SPI_MISO	15	O	3-State LVCMOS output is enabled when SPI_LE is asserted low. It is the serial data output to the SPI bus interface.
SPI_LE *or CD1*	45	I	LVCMOS input, control latch enable for the Serial Programmable Interface (SPI), with hysteresis in SPI mode. *In configuration default mode this pin becomes CD1.*
SPI_CLK *or CD2*	46	I	LVCMOS input, serial control clock input for the SPI bus interface, with hysteresis. *In configuration default mode this pin becomes CD2.*
SPI_MOSI *or CD3*	44	I	LVCMOS input, master out slave in as a serial control data input to CDCE72010 for the SPI bus interface. *In configuration default mode this pin becomes CD3 and it should be tied to GND.*

(1) It is recommended to use supply filter to each VCC supply domain independently.
(2) Pin 5 and 8, pin 28 and 31, pin 40 and 43, pin 51 and 54, pin 4 and 63 and pin 60 and 57 are internally connected.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION(1)
NAME	NO.		
MODE_SEL	16	I	**SPI MODE = H**; when driven high or left unconnected, it defaults to SPI bus interface mode. **CD (Configuration Default) MODE = L**; If tied low the device goes into configuration default mode which is configured by CD1, CD2, CD3, and AUX_SEL. In configuration default mode the device loads various configuration defaults from the EEPROM into memory at start-up.
AUX_SEL	18	I	*This pin is used in CD mode only. If set to "1" or left unconnected, it disables output 9 and enables the AUXILIARY input to drive all outputs from output0 to output8 depending on the EEPROM configuration. If driven low in CD mode, it enables output 9 and makes all outputs driven by the VCXO Input depending on the internal EEPROM configuration.*
REF_SEL	47	I	If Auto Reference Select mode is OFF, this pin acts as an External Input Reference Select Pin; The REF_SEL signal selects one of two input clocks: REF_SEL [1]: PRI_REF is selected; REF_SEL [0]: SEC_REF is selected; The input has an internal 150-kΩ pull-up resistor and if left unconnected it will default to logic level "1". If Auto Reference Select mode in ON, this pin not used.
$\overline{PD}$	17	I	This pin is active low and can be activated externally or by the corresponding bit in the SPI register (in case of logic high, the SPI setting is valid). This pin switches the device into powerdown mode The input has an internal 150-kΩ pull-up resistor and if left unconnected it will default to logic level "1".
$\overline{RESET}$ or $\overline{HOLD}$	33	I	This LVCMOS input can be programmed (SPI) to act as $\overline{HOLD}$ or $\overline{RESET}$. $\overline{RESET}$ is the default function. This pin is active low and can be activated external or via the corresponding bit in the SPI register. In the case of $\overline{RESET}$, the CP (Charge Pump) is switched to 3-state and all counters are reset to zero. The LVPECL outputs are static low (N) and high (P) respectively, and the LVCMOS outputs are all low or high if inverted. In the case of $\overline{HOLD}$, the CP (Charge Pump) is switched into 3-state mode only. After $\overline{HOLD}$ is released and with the next valid reference clock cycle, the charge pump is switched back into normal operation (CP stays in 3-state as long as no reference clock is valid). During $\overline{HOLD}$, all outputs are at normal operation. This mode allows external control of "frequency hold-over" mode. The input has an internal 150-kΩ pull-up resistor.
VCXO_IN+	53	I	VCXO input (+) for LVPECL+, LVDS+, and LVCMOS level inputs.
VCXO_IN–	52	I	Complementary VCXO input for LVPECL-, LVDS- inputs. In the case of a LVCMOS level input on VCXO IN+, ground this pin through 1k resistor.
PRI_REF+	59	I	Universal input buffer (LVPECL, LVDS, LVCMOS) positive input for the Primary Reference Clock.
PRI_REF–	58	I	Universal input buffer (LVPECL, LVDS) negative input for the Primary Reference Clock. In the case of LVCMOS signaling, ground this pin through 1k resistor.
SEC_REF+	62	I	Universal input buffer (LVPECL, LVDS, LVCMOS) positive input for the Secondary Reference Clock.
SEC_REF–	61	I	Universal input buffer (LVPECL, LVDS,) negative input for the Secondary Reference Clock. In the case of LVCMOS signaling, ground this pin through 1k resistor.
TESTOUTA	1	A	Analog Test Point for TI internal testing. Connect a 1kΩ pull-down resistor or leave unconnected.
STATUS	55	O	LVCMOS output for TI internal testing. Leave unconnected unless it is configured as the IREF_CP pin. In this case it should be connected to a 12-kΩ resistor to GND.
CP_OUT	3	AO	Charge pump output
VBB	56	AO	Internal voltage bias analog output
PLL_LOCK	50	AO	LVCMOS output for PLL_LOCK information. This pin is set high if the PLL is in lock. This output can be programmed to be a digital lock detect or analog lock detect (see description of Analog Lock).
U0P:U0N U1P:U1N U2P:U2N U3P:U3N U4P:U4N U5P:U5N U6P:U6N U7P:U7N U8P:U8N	7, 6 10, 9 13, 12 21, 20 24, 23 27, 26 30, 29 36, 35 39, 38	O	The outputs of the CDCE72010 are user definable and can be any combination of up to 9 LVPECL outputs, 9 LVDS outputs, or up to 18 LVCMOS outputs. The outputs are selectable via the SPI interface. The power-up setting is EEPROM configurable.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION[1]
NAME	NO.		
U9P or AUXINP	42	I/O	Positive universal output buffer 9 can be 3-stated and used as a positive universal auxiliary input buffer (It requires external termination). The auxiliary input signal can be routed to drive the outputs or the feedback loop to the PLL.
U9N or AUXINN	41	I/O	Negative universal output buffer 9 can be 3-stated and used as a negative universal auxiliary input buffer (It requires external termination). The auxiliary input signal can be routed to drive the outputs or the feedback loop to the PLL.

PACKAGE THERMAL RESISTANCE FOR QFN (RGZ) PACKAGE[1] [2]

AIRFLOW (LFM)		θ_{JP} (°C/W)[3]	θ_{JA} (°C/W)
0	JEDEC compliant board (6×6 VIAs on PAD)	1.5	28
100	JEDEC compliant board (6×6 VIAs on PAD)	1.5	17.6
0	Recommended layout (10×10 VIAs on PAD)	1.5	22.8
100	Recommended layout (10×10 VIAs on PAD)	1.5	13.8

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) Connected to GND with 9 thermal vias (0.3 mm diameter).
(3) θ_{JP} (Junction – Pad) is used for the QFN package, because the main heat flow is from the junction to the GND-pad of the QFN.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}, AV_{CC}, V_{CC_CP}	Supply voltage range[1]		–0.5	4.6	V
V_I	Input voltage range[2]		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range[2]		–0.5	V_{CC} + 0.5	V
	Input current	V_I < 0, V_I > V_{CC}		±20	mA
	Output current for LVPECL/LVCMOS Outputs	0 < V_O < V_{CC}		±50	mA
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) All supply voltages have to be supplied simultaneously.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

for the CDCE72010 device for under the specified industrial temperature range of –40°C to 85°C

			MIN	NOM	MAX	UNIT
Power Supply						
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{CC_PLL}, V_{CC_IN}, V_{CC_VCXO}, V_{CCA}	Analog supply voltage		3	3.3	3.6	
V_{CC_CP}			2.3		V_{CC}	V
P_{LVPECL}	REF at 30.72MHz VCXO at 491.52MHz Outputs are LVPECL-HS	Divider 1 set to divide by 8 (DCR 30%) Divider 2 set to divide by 4 (DCR 30%) Divider 3 set to divide by 2 (DCR 30%) Divider 4 set to divide by 2 (DCR 30%) Divider 5 set to divide by 1 (DCR 30%) Divider 6 set to divide by 1 (DCR 0%) Divider 7 set to divide by 1 (DCR 0%) Divider 8 set to divide by 1 (DCR 0%) DCR: Divider Current Reduction Setting		2.9		W
P_{LVDS}	REF at 30.72MHz VCXO at 491.52MHz Outputs are LVDS-HS			2.0		W
P_{LVCMOS}	REF at 30.72MHz VCXO at 122.88MHz Outputs are LVCMOS			2.2		W
P_{OFF}	REF at 30.72MHz VCXO at 491.52MHz	Dividers are disabled. Outputs are disabled.		775		mW
P_{PD}		Device is powered down		30		mW
Typical Operating Conditions at V_{CC}= 3.3V and 25°C unless otherwise specified.						
Differential Input Mode (PRI_REF, SEC_REF, VCXO_IN and AUX_IN)						
V_{IN}	Differential input amplitude	(V_{INP} – V_{INN})	0.1		1.3	V
V_{ICM}	Common-mode input voltage		1.0		V_{CC}– 0.3	V
I_{IH}	Differential input current high (No internal termination)	V_I = V_{CC}, V_{CC} = 3.6 V			20	µA
I_{IL}	Differential input current low(No internal termination)	V_I = 0 V, V_{CC} = 3.6 V	–20		20	µA
	Input capacitance on PRI_REF, SEC_REF and VCXO_REF			3		pF
	Input capacitance on AUX_IN			7		pF
LVCMOS Input Mode (SPI_CLK, SPI_MOSI, SPI_LE, $\overline{PD}$, $\overline{RESET}$, REF_SEL, MODE_SEL)						
V_{IL}	Low-level input voltage LVCMOS		0		0.3 V_{CC}	V
V_{IH}	High-level input voltage LVCMOS		0.7 V_{CC}		V_{CC}	V
V_{IK}	LVCMOS input clamp voltage	V_{CC} = 3 V, II = –18 mA			–1.2	V
I_{IH}	LVCMOS input current	V_I = V_{CC}, V_{CC} = 3.6 V			20	µA
I_{IL}	LVCMOS input	V_I = 0 V, V_{CC} = 3.6 V	–10		–40	µA
C_I	Input capacitance (LVCMOS signals)	V_I = 0 V or V_{CC}		3		pF

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature(1) (2)

PARAMETER		MIN	TYP	MAX	UNIT
PRI_REF/SEC_REF					
$f_{REF - Single}$	For single-ended inputs (LVCMOS) on PRI_REF and SEC_REF			250	MHz
$f_{REF - Diff}$	For differential inputs (LVDS and LVPECL) on PRI_REF and SEC_REF (R divider set to DIV2)			500	MHz
Duty Cycle	Duty cycle of PRI_REF or SEC_REF	40%		60%	
t_{slew}	Input signal slew rate	1			V/ns
VCXO_IN, AUX_IN					
$f_{REF - Single}$	For single-ended inputs (LVCMOS)			250	MHz
$f_{REF - Diff}$	For differential inputs (LVDS and LVPECL)			1500	MHz
Duty Cycle	Duty cycle of PRI_REF or SEC_REF	40%		60%	
t_{slew}	Input signal slew rate	1			V/ns
$\overline{PD}$, $\overline{RESET}$, $\overline{Hold}$, REF_SEL					
t_r/t_f	Rise and fall time of the $\overline{PD}$, $\overline{RESET}$, $\overline{Hold}$, REF_SEL signal from 20% to 80% of the signal			4	ns

(1) From 250MHz to 500MHz is achieved by setting the divide by 2 in the R-divdier

(2) If the feedback clock (derived from the VCXO input) is less than 2MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_VCXO signal and PLL_LOCK signal to low. Both status signals are no longer relevant. This affects the HOLD-Over-Function as well as the PLL_LOCK signal is no longer valid.

AC/DC CHARACTERISTICS

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
SPI Output (MISO) / PLL_LOCK							
I_{OH}	High-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		33		mA
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = 3 V	I_{OH} = –100 µA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = 3 V	I_{OL} = 100 µA			0.3	V
C_O	Output capacitance on MISO	V_{CC} = 3.3 V; VO = 0 V or V_{CC}			3		pF
I_{OZH}	3-state output current	V_O = V_{CC}			5		µA
I_{OZL}		V_O = 0 V			–5		µA
EEPROM							
EEcyc	Programming cycle of EEPROM			100	1000		Cycles
EEret	Data retention			10			Years
VBB							
VBB	VCXO termination voltage depends on the settings of the VCXO/AUX_IN input buffers	IBB = –0.2mA Depending on the setting, Output impedance = 25 Ω		0.9		1.9	V
Input Buffers Internal Termination Resistors (VCXO_IN,PRI_REF and SEC_REF)							
	Termination resistance(2)	Single ended			53		Ω
Phase Detector							
f_{CPmax}	Maximum charge pump frequency	Default PFD pulse width delay				100	MHz
Charge Pump							
ICP3St	Charge pump 3-state current	0.5 V < VCP < V_{CC_CP} – 0.5 V			15		nA
ICPA	ICP absolute accuracy	V_{CP} = 0.5 V_{CC_CP}; internal reference resistor			20%		
ICPA	ICP absolute accuracy	VCP = 0.5 V_{CC_CP}; external reference resistor 12kΩ (1%)			5%		
ICPM	Sink/source current matching	0.5 V < VCP < V_{CC_CP} – 0.5 V, SPI default settings			%4		
IVCPM	ICP vs VCP matching	0.5 V < VCP < V_{CC_CP} – 0.5 V			6%		
$V_{I\_REF\_CP}$	Voltage on STATUS PIN when configured as I_REF_CP	12-kΩ resitor to GND (External current path for accurate charge pump current)			1.24		V

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Termination resistor can vary by 20%.

AC/DC CHARACTERISTICS (CONTINUED)

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
LVCMOS Output							
f_{clk}	Output frequency (see Figure 2)	Load = 5 pF to GND				250	MHz
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OH} = –100 µA	V_{CC} – 0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OL}=100 µA			0.3	V
I_{OH}	High-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		33		mA
t_{pho}	Phase offset without using available delay adjustment	VCXO at 491.52MHz, Output 1 is divide by 16 and reference at 30.72MHz, M and N delays are fixed to one value (set to 0).			13		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay from VCXO_IN to Outputs	Crosspoint to V_{CC}/2, load = 5 pF			3.3		ns
$t_{sk(o)}$	Skew, output-to-output LVCMOS single-ended output	Divide by 1 for all dividers			75		ps
		Divide by 16 for all dividers			75		
		Divide by 1 for divider 1 and divide by 16 for all other dividers			1400		
C_O	Output capacitance on Y0 to Y8	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			5		pF
C_O	Output capacitance on Y9	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			5		pF
I_{OZH}	3-state LVCMOS output current	V_O = V_{CC}			5		µA
I_{OZL}	3-state LVCMOS output current	V_O = 0V			–5		µA
I_{OPDH}	Power-down output current	V_O = V_{CC}				25	µA
I_{OPDL}	Power-down output current	V_O = 0V				5	µA
Duty cycle	LVCMOS	With 50% / 50% duty cycle of the VCXO input clock		45%		55%	
$t_{slew-rate}$	Output rise/fall slew rate			3.6		5.2	V/ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

AC/DC CHARACTERISTICS (CONTINUED)

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVDS Output						
f_{clk}	Output frequency		0		800	MHz
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω	160		270	mV
Δ_{VOD}	LVDS VOD magnitude change				50	mV
V_{OS}	Offset voltage	–40°C to 85°C		1.24		V
ΔV_{OS}	V_{OS} magnitude change			40		mV
	Short circuit V_{OUT+} to ground	V_{OUT} = 0			27	mA
	Short circuit $V_{OUT–}$ to ground	V_{OUT} = 0			27	mA
t_{pho} (2)	Reference to output phase offset without using available delay adjustment	VCXO at 491.52MHz, Output 1 is divide by 16 and reference at 30.72MHz, M and N delays are fixed to one value (set to 0), PFD: 240kHz, (M and N = 128)		14		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay time, VCXO_IN to output	Crosspoint to crosspoint, load		3.0		ns
tsk(o)(3)	Skew, output to output LVDS output	Divide by 1 for all dividers		45		ps
		Divide by 16 for all dividers		50		
		Divide by 1 for divider 1 Divide by 16 for all other dividers		2800		
C_O	Output capacitance on Y0 to Y8	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
C_O	Output capacitance on Y9	V_{CC} = 3.3 V; V_O = 0 V or V_{CC} 5		7		pF
I_{OPDH}	Power-down output current	V_O = V_{CC}			25	µA
I_{OPDL}	Power-down output current	V_O = 0V			5	µA
	Duty cycle		45		55	%
t_r/t_f	Rise and fall time	20% to 80% of V_{outpp}	110	140	160	ps
LVCMOS-TO-LVDS(4)						
tsk_{P_C}	Output skew between LVCMOS and LVDS outputs	Crosspoint to V_{CC}/2. Outputs are at the same output frequency and use the same output divider configuration.	0.9	1.4	1.9	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is valid only for same REF_IN clock and Y output clock frequency. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).
(3) The tsk(o) specification is only valid for equal loading of all outputs.
(4) The phase of LVCMOS is lagging in reference to the phase of LVDS.

AC/DC CHARACTERISTICS (CONTINUED)

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVDS Hi Swing Output						
f_{clk}	Output frequency		0		800	MHz
$\|V_{OD}\|$	Differential output voltage	R_L =100 Ω	270		550	mV
Δ_{VOD}	LVDS VOD magnitude change				50	mV
V_{OS}	Offset voltage	–40°C to 85°C		1.24		V
ΔV_{OS}	V_{OS} magnitude change			40		mV
	Short Circuit V_{OUT+} to ground	V_{OUT} = 0			27	mA
	Short Circuit $V_{OUT–}$ to ground	V_{OUT} = 0			27	mA
t_{pho} (2)	Reference to output phase offset without using available delay adjustment	VCXO at 491.52MHz, Output 1 is divide by 16 and reference at 30.72MHz. M and N delays are fixed to one value. (Set to 0) PFD: 240kHz, (M and N = 128)		14		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay time, VCXO_IN to output	Crosspoint to crosspoint		3.0		ns
$t_{sk(o)}$ (3)	LVDS output skew	Divide by 1 for all dividers		45		ps
		Divide by 16 for all dividers		50		
		Divide by 1 for divider 1 Divide by 16 for all other dividers		2800		
C_O	Output capacitance on Y0 to Y8	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
C_O	Output capacitance on Y9	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		7		pF
IOPDH	Power-down output current	V_O = V_{CC}			25	µA
IOPDL	Power-down output current	V_O = 0V			5	µA
Duty cycle			45		55	%
t_r/t_f	Rise and fall time	20% to 80% of V_{outpp}	110	160	190	ps
LVCMOS-TO-LVDS(4)						
tsk_{P_C}	Output skew between LVCMOS and LVDS outputs	Crosspoint to V_{CC}/2. Outputs are at the same output frequency and use the same output divider configuration with same output frequencies and divider values	0.9	1.4	1.9	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is valid only for same REF_IN clock and Y output clock frequency. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).
(3) The tsk(o) specification is only valid for equal loading of all outputs.
(4) The phase of LVCMOS is lagging in reference to the phase of LVDS.

AC/DC CHARACTERISTICS (CONTINUED)

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVPECL Output						
f_{clk}	Output frequency		0		1500	MHz
V_{OH}	LVPECL high-level output voltage	Load, see Figure 5	V_{CC} – 1.06		V_{CC} – 0.88	V
V_{OL}	LVPECL low-level output voltage	Load, see Figure 5	V_{CC} – 2.02		V_{CC} – 1.58	V
|VOD|	Differential output voltage	Load, see Figure 5	610		970	mV
t_{pho} (2)	Reference to output phase offset without using available delay adjustment	VCXO at 491.52MHz, Output 1 is divide by 16 and reference at 30.72MHz, M and N delays are fixed to one value (set to 0), PFD: 240kHz, (M and N = 128)		14		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay time, VCXO_IN to output	Crosspoint to crosspoint, load		3.4		ns
$t_{sk(o)}$ (3)	LVPECL output skew	Divide by 1 for all dividers		45		ps
		Divide by 16 for all dividers		50		
		Divide by 1 for divider 1 Divide by 16 for all other dividers		2700		
C_O	Output capacitance on Y0 to Y8	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
C_O	Output capacitance on Y9	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		7		pF
IOPDH	Power-down output current	V_O = V_{CC}			25	µA
IOPDL	Power-down output current	V_O = 0 V			5	µA
	Duty cycle		45		55	%
t_r/t_f	Rise and fall time	20% to 80% of V_{outpp}	55	75	135	ps
LVDS-TO-LVPECL						
tsk_{P_C}	Output skew between LVDS and LVPECL outputs	Crosspoint to Crosspoint with same output frequencies and divider values	0.9	1.1	1.3	ns
LVCMOS-TO-LVPECL						
tsk_{P_C}	Output skew between LVCMOS and LVPECL outputs	V_{CC}/2 to Crosspoint; With same output frequencies and divider values	–150	260	700	ps

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is valid only for same REF_IN clock and Y output clock frequency. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).
(3) The tsk(o) specification is only valid for equal loading of all outputs. :

AC/DC CHARACTERISTICS (CONTINUED)

over the specified industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVPECL Hi Swing Output						
f_{clk}	Output frequency		0		1500	MHz
V_{OH}	LVPECL high-level output voltage	Load, see Figure 5	V_{CC} – 1.11		V_{CC} – 0.87	V
V_{OL}	LVPECL low-level output voltage	Load, see Figure 5	V_{CC} – 2.06		V_{CC} – 1.73	V
|VOD|	Differential output voltage	Load, see Figure 5	760		1160	mV
t_{pho} (2)	Reference to output phase offset without using available delay adjustment	VCXO at 491.52MHz, Output 1 is divide by 16 and reference at 30.72MHz, M and N delays are fixed to one value (set to 0), PFD: 240kHz, (M and N = 128)		14		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay time, VCXO_IN to output	Crosspoint to crosspoint, load		3.4		ns
$t_{sk(o)}$ (3)	LVPECL output skew	Divide by 1 for all dividers		45		ps
		Divide by 16 for all dividers		50		
		Divide by 1 for divider 1 Divide by 16 for all other dividers		2700		
C_O	Output capacitance on Y0 to Y8	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
C_O	Output capacitance on Y9	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		7		pF
IOPDH	Power-down output current	V_O = V_{CC}			25	µA
IOPDL	Power-down output current	V_O = 0V			5	µA
	Duty cycle		45%		55%	
t_r/t_f	Rise and fall time	20% to 80% of V_{outpp}	55	75	135	ps
LVDS-TO-LVPECL						
tsk_{P_C}	Output skew between LVDS and LVPECL outputs	Crosspoint to Crosspoint; with same output frequencies and divider values	0.9	1.1	1.3	ns
LVCMOS-TO-LVPECL						
tsk_{P_C}	Output skew between LVCMOS and LVPECL outputs(4)	V_{CC}/2 to Crosspoint; With same output frequencies and divider values	–150	260	700	ps

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is valid only for same REF_IN clock and Y output clock frequency. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).
(3) The tsk(o) specification is only valid for equal loading of all outputs.
(4) The phase of LVCMOS is lagging in reference to the phase of LVDS and LVPECL.

PARAMETER MEASUREMENT INFORMATION

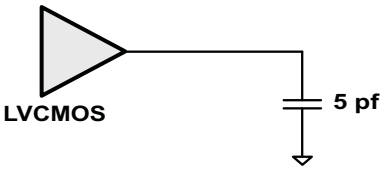


Figure 2. LVCMOS Output Test Setup

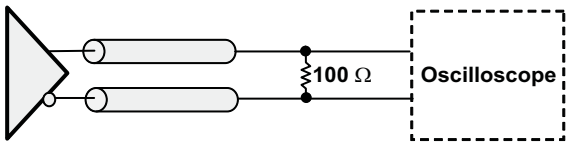


Figure 3. LVDS DC Test Setup

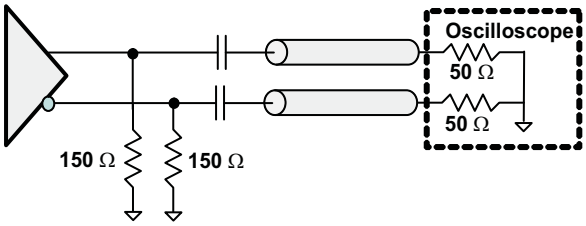


Figure 4. LVPECL AC Test Setup

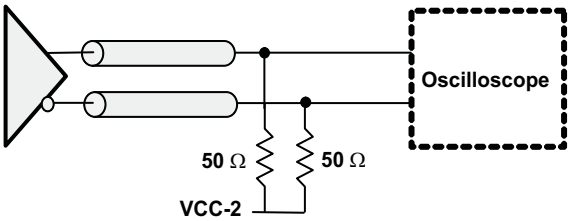


Figure 5. LVPECL DC Test Setup

TYPICAL CHARACTERISTICS

LVPECL OUTPUT SWING vs FREQUENCY

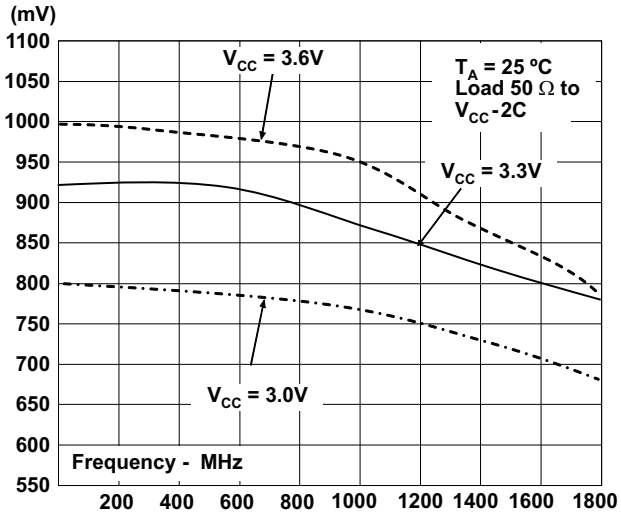


Figure 6.

Hi Swing LVPECL OUTPUT SWING vs FREQUENCY

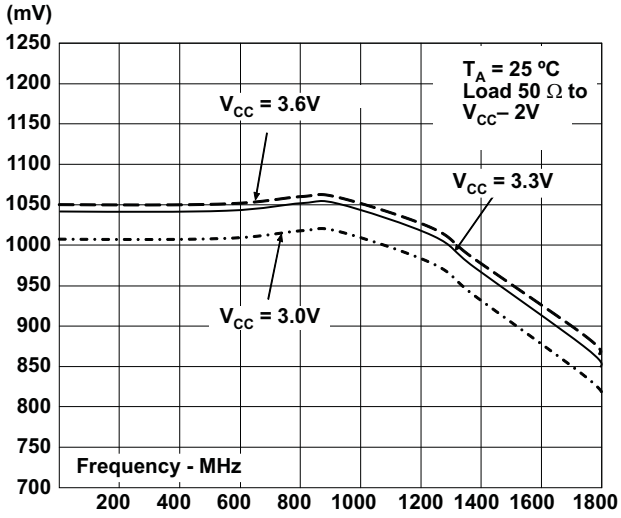


Figure 7.

LVDS OUTPUT SWING vs FREQUENCY

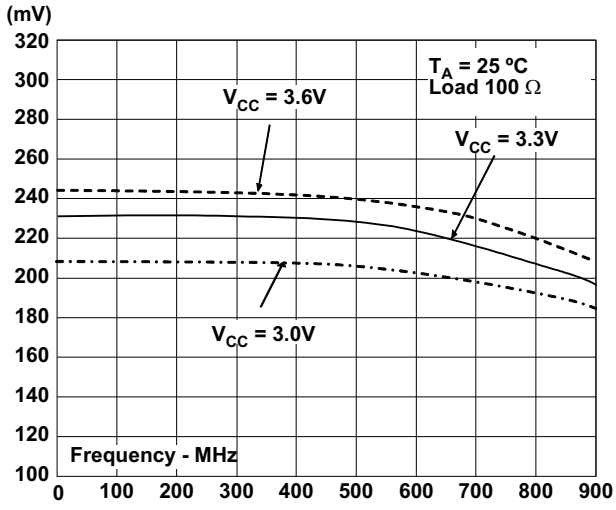


Figure 8.

Hi Swing LVDS OUTPUT SWING vs FREQUENCY

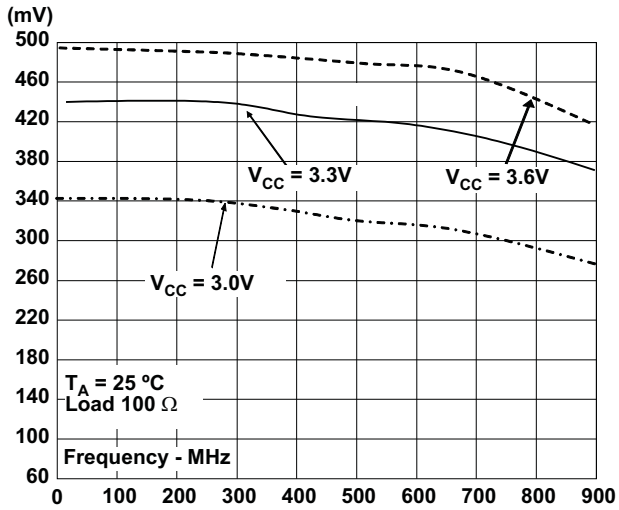


Figure 9.

TYPICAL CHARACTERISTICS (continued)

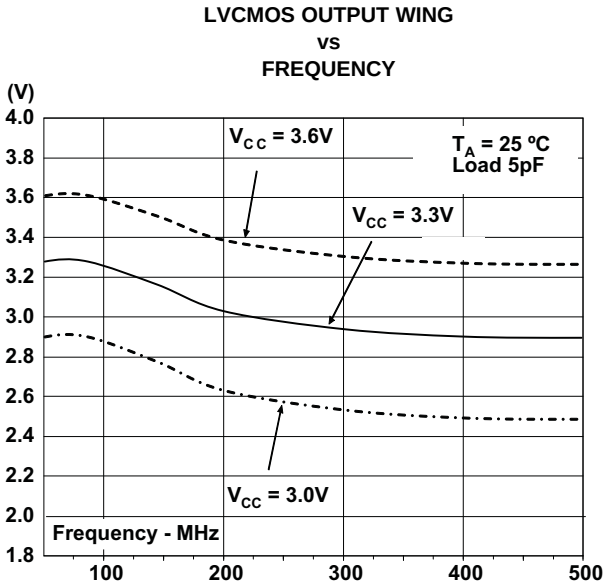


Figure 10.

APPLICATION INFORMATION

PHASE NOISE ANALYSIS

Phase noise is measured in a closed loop mode of 491.52MHz VCXO and 30.72MHz reference and a 100Hz loop. Output 1 is measured for divide by one, output 6 for divide by 4, and output 9 for divide by 16.

Table 1. Phase Noise for LVPECL High Swing

Phase Noise Specifications under following configuration: VCXO = 491.52MHz, REF = 30.72MHz, Divide by = 491.52MHz, Divide by 4 = 122.88MHz, Divide by 16 = 30.72MHz, PFD Frequency = 240KHz, Charge Pump Current = 2mA, Loop BW = 100Hz, Output 1 = 491.52 MHZ, Output Buffer: LVPECL-HS						
PHASE NOISE AT OFFSET	**VCXO OPEN LOOP**	**REFERENCE 30.72MHz**	**LVPECL-HS DIVIDE BY 1**	**LVPECL-HS DIVIDE BY 4**	**LVPECL-HS DIVIDE BY 16**	**UNIT**
10Hz	–64	–107	–80	–92	–105	dBc/Hz
100Hz	–99	–123	–92	–104	–116	dBc/Hz
1kHz	–113	–134	–115	–127	–139	dBc/Hz
10kHz	–135	–153	–135	–145	–158	dBc/Hz
100kHz	–148	–156	–146	–155	–162	dBc/Hz
1MHz	–148	–158	–146	–155	–162	dBc/Hz
10MHz	–149		–147	–156		dBc/Hz

Table 2. Phase Noise for LVDS High Swing

Phase Noise Specifications under following configuration: VCXO = 491.52MHz, REF = 30.72MHz, Divide by = 491.52MHz, Divide by 4 = 122.88MHz, DIvide by 16 = 30.72MHz, PFD Frequency = 240KHz, Charge Pump Current = 2mA Loop BW = 100Hz, Output 1 = 491.52 MHZ, Output Buffer: LVDS-HS						
PARAMETER	**VCXO OPEN LOOP**	**REFERENCE**	**LVDS–HS DIVIDE BY 1**	**LVDS-HS DIVIDE BY 4**	**LVDS-HS DIVIDE BY 16**	**UNIT**
10Hz	–64	–107	–82	–94	–104	dBc/Hz
100Hz	–99	–123	–92	–105	–117	dBc/Hz
1kHz	–113	–134	–114	–127	–139	dBc/Hz
10kHz	–135	–153	–135	–145	–151	dBc/Hz
100kHz	–148	–156	–145	–152	–153	dBc/Hz
1MHz	–148	–158	–146	–152	–153	dBc/Hz
10MHz	–149		–146	–152		dBc/Hz

Table 3. Phase Noise for LVCMOS

Phase Noise Specifications under following configuration: VCXO = 491.52MHz, REF = 30.72MHz, Divide by = 491.52MHz, Divide by 4 = 122.88MHz, DIvide by 16 = 30.72MHz, PFD Frequency = 240KHz, Charge Pump Current = 2mA, Loop BW = 100Hz, Output 1 = 491.52 MHZ, Output Buffer: LVCMOS						
PARAMETER	**VCXO OPEN LOOP**	**REFERENCE**	**N/A**	**LVCMOS DIVIDE BY 4**	**LVCMOS DIVIDE BY 16**	**UNIT**
10Hz	–64	–107		–91	–105	dBc/Hz
100Hz	–99	–123		–104	–116	dBc/Hz
1kHz	–113	–134		–127	–139	dBc/Hz
10kHz	–135	–153		–140	–151	dBc/Hz
100kHz	–148	–156		–151	–159	dBc/Hz
1MHz	–148	–158		–153	–160	dBc/Hz
10MHz	–149			–154		dBc/Hz

INTERFACE AND CONTROL BLOCK

The Interface & Control Block includes a SPI interface, four control pins, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in Static RAM. This RAM, also called the device registers, configures all hardware within the CDCE72010.

Serial Peripheral Interface (SPI)

The serial interface of CDCE72010 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE72010 is a slave. The SPI consists of four signals:

- **SPI_CLK:** Serial Clock (Output from Master) – the CDCE72010 and the master host clock data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock. (LVCMOS Input Buffer)
- **SPI_MOSI:** Master Output Slave Input (LVCMOS Input Buffer) .
- **SPI_MISO:** Master Input Slave Output
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place. (LVCMOS Input Buffer).

The CDCE72010 implements data fields that are 28-bits wide. In addition, it contains 12 registers, each comprising a 28 bit data field. Therefore, accessing the CDCE72010 requires that the host program append a 4-bit address field to the front of the data field as follows:

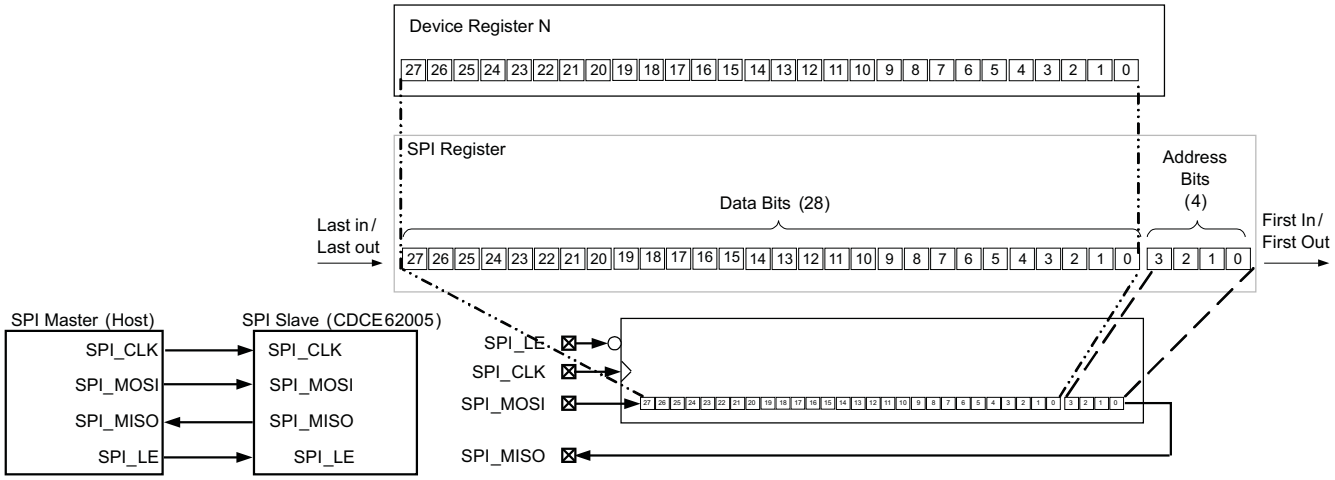


Figure 11. CDCE72010 SPI Communications Format

CDCE72010 SPI Command Structure

The CDCE72010 supports four commands issued by the Master via the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock
- Copy RAM to EEPROM – lock

Table 4 provides a summary of the CDCE72010 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a Read Command to initiate a data transfer from the CDCE72010 back to the host. This command specifies the address of the register of interest in the data field.

Table 4. CDCE72010 SPI Command Structure(1)

			Data Field (28 Bits)																												Addr Field (4 Bits)*			
Register	Operation	NVM	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	3	2	1	0
0	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
1	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1
2	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0
3	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1
4	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	0
5	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1
6	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0
7	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	1
8	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0
9	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1
10	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1	0
11	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1	1
12	Status/Control	No	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	0
Instruction	Read Command	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	A	A	A	1	1	1	0
Instruction	RAM → EEPROM	Unlock	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Instruction	RAM → EEPROM	Lock (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1

(1) **CAUTION:** In a read Cycle the Address Field should be ignored when accessing the CDCE72010 device.
(2) After execution of this command, the EEPROM is permanently locked. After locking EEPROM, device configuration can only be changed via Write into RAM after power up; however EEPROM can no longer be changed.

SPI Interface Master

The Interface master can be designed using a FPGA or a micro controller. The CDCE72010 acts as a slave to the SPI master. The SPI Master should be designed to issue none consecutive read or write commands. The SPI clock should start and stop with respect to the SPI_LE signal as shown in Figure 12. SPI_MOSI, SPI_CLK, and SPI_LE are generated by the SPI Master. SPI_MISO is gnererated by the SPI slave the CDCE72010.

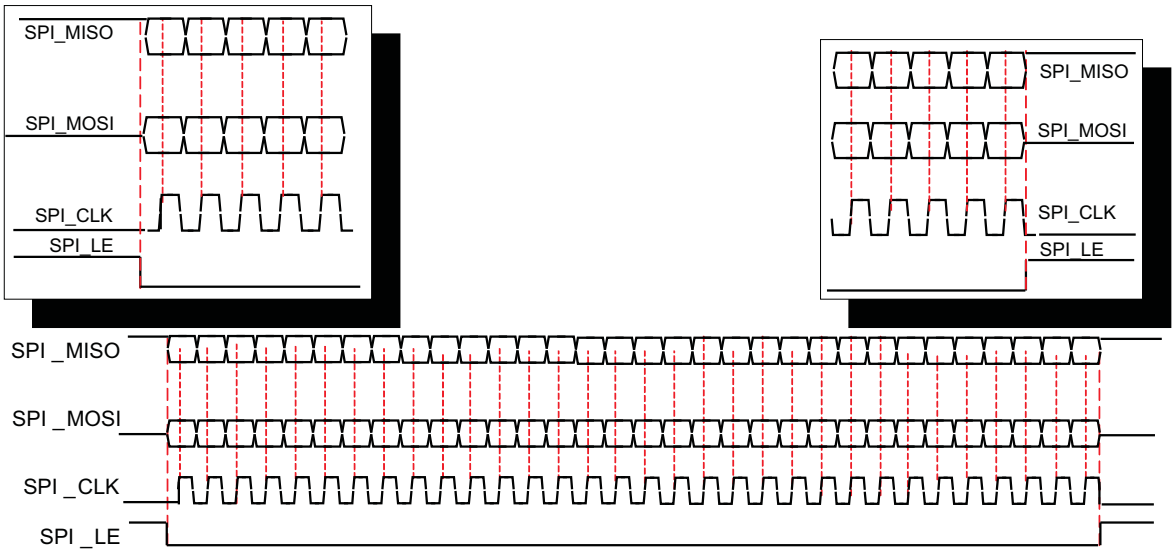


Figure 12. CDCE72010 SPI Read/Write Command

SPI Consecutive Read/Write Cycles to the CDCE72010

Figure 13 illustrates how two consecutive SPI cycles are performed between a SPI Master and the CDCE72010 SPI Slave.

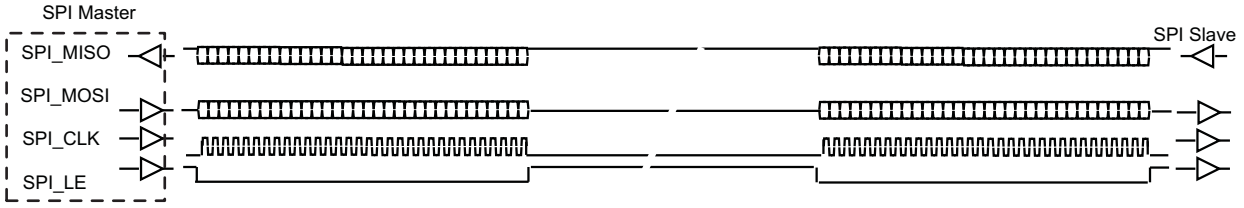


Figure 13. Consecutive Read/Write Cycles

Writing to the CDCE72010

Figure 14 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE72010, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE72010 that the transmission of the last bit in the stream (Bit 31) has occurred.

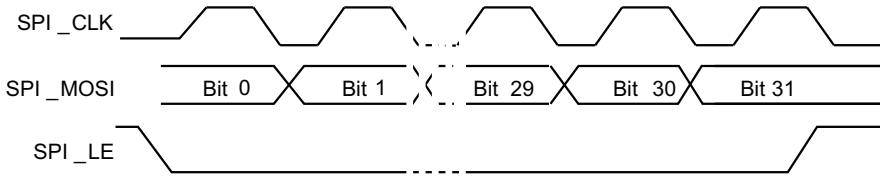


Figure 14. CDCE72010 SPI Write Operation

Reading from the CDCE72010

Figure 15 shows how the CDCE72010 executes a Read Command. The SPI master first issues a Read Command to initiate a data transfer from the CDCE72010 back to the host (see Table 4).This command specifies the address of the register of interest (marked as AAAA in Table 1). By transitioning SPI_LE from a low to a high, the CDCE72010 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE72010 presents the data present in the register specified in the Read Command on SPI_MISO.

IMPORTANT NOTE: The read instruction does not return SPI_MISO Bit 0 properly. This bit is stuck with zero. The host should ignore this bit when accessing the CDCE72010.

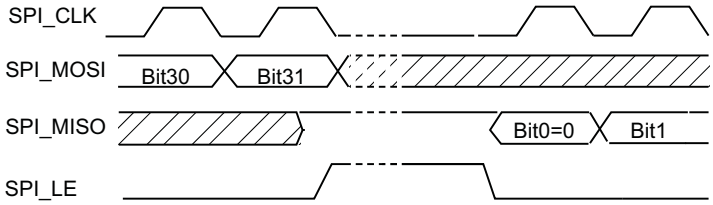


Figure 15. CDCE72010 SPI Read Operation

Writing to EEPROM

After the CDCE72010 detects a power-up and completes a reset cycle, the device copies the contents of the on-board EEPROM into the Device Registers. (SPI_LE signal has to be HIGH in order for the EEPROM to load correctly during the rising edge of Power_Down signal).

The host issues one of two special commands shown in Table 4 to copy the contents of Device Registers 0 through 11 (a total of 336 bits) into EERPOM. They include:

- Copy RAM to EEPROM – Unlock, Execution of this command can happen many times.
- Copy RAM to EEPROM – Lock: Execution of this command can happen only once; after which the EEPROM is **permanently locked**.

After either command is initiated, power must remain stable and the host must not access the CDCE72010 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

SPI CONTROL INTERFACE TIMING

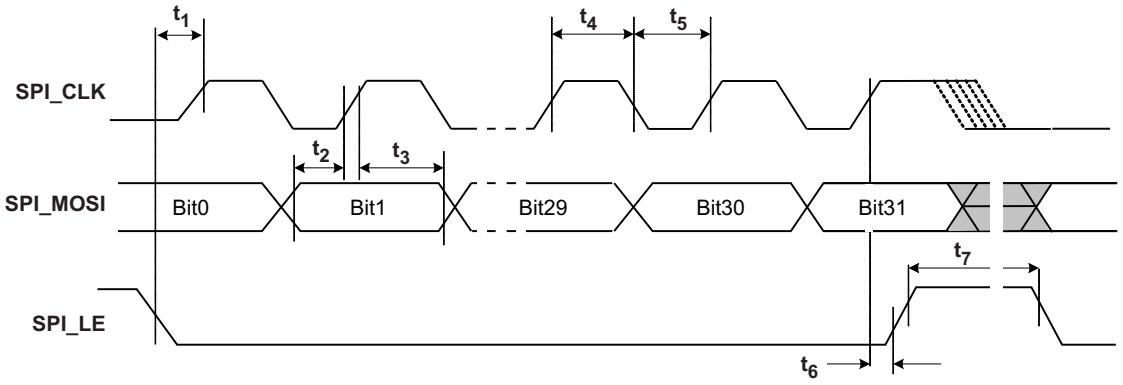


Figure 16. Timing Diagram for SPI Write Command

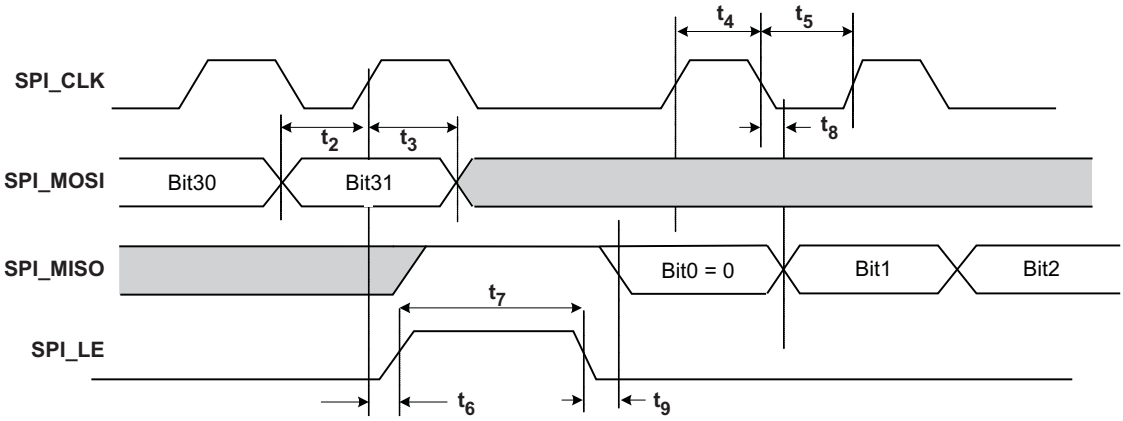


Figure 17. Timing Diagram for SPI Read Command

Table 5. SPI Bus Timing Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
f_{Clock}	Clock Frequency for the SPI_CLK			20	MHz
t_1	SPI_LE to SPI_CLK setup time	10			ns
t_2	SPI_MOSI to SPI_CLK setup time	10			ns
t_3	SPI_MOSI to SPI_CLK hold time	10			ns
t_4	SPI_CLK high duration	25			ns
t_5	SPI_CLK low duration	25			ns
t_6	SPI_CLK to SPI_LE Hold time	10			ns
t_7	SPI_LE Pulse Width	20			ns
t_8	SPI_CLK to MISO data valid			10	ns
t_9	SPI_LE to SPI_MISO Data Valid			10	ns

CDCE72010 Default Configuration

The CDCE72010 on-chip EEPROM has been factory preset to the default settings listed in Table 6

Table 6. CDCE72010 Default Configuration Settings

REGISTER	DEFAULT SETTING	REGISTER	DEFAULT SETTING
REG0000	002C0040	REG0007	EB040717
REG0001	83840051	REG0008	010C0158
REG0002	83400002	REG0009	01000049
REG0003	83400003	REG0010	0BFC07CA
REG0004	81800004	REG0011	8000058B
REG0005	81800005	REG0012	Undetermined
REG0006	EB040006		

The default configuration programmed in the EEPROM is: a 10MHz primary reference single ended LVCMOS, a 491.52MHz LVPECL VCXO running at 80kHz PFD with a 10Hz loop bandwidth. Reference Auto Select is off, M divider is set for 125, N divider is set to 768, charge pump current is set to 2.2mA, and feedback divider is set to divide by 8. Divider 1 is set to divide by 4, Dividers 2 and 3 are set to divide by 1, Dividers 4 and 5 are set to divide by 2, Dividers 6 and 7 are set to divide by 8, and Divider 8 is set to divide by 16.Output0:LVCMOS, Output1:Hi-LVPECL, Output2: Hi-LVPECL, Output3:Hi_LVPECL, Output4:LVPECL, Output5:LVPECL, Output6:Hi-LVDS, Output7:Hi-LVDS, Output8:LVCMOS and Output9:LVCMOS.

Register 0 Address 0x00: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	INBUFSELX	Reference Input Buffers	Primary and secondary Buffer Type Select (LVPECL,LVDS or LVCMOS) XY(10) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive pin	EEPROM
1	INBUFSELY			
2	PRISEL	Reference Input Buffer	When REFSELCNTRL is set to 1, the following settings apply: If Bits (2,3): 00 – No input buffer is selected/active If Bits (2,3): 10 – PRI_REF is selected, SEC_REF is powered down If Bits (2,3): 01 – SEC_REF is selected, PRI_REF is powered down(1) If Bits (2,3): 11 – Auto Select (PRI then SEC).	EEPROM
3	SECSEL			
4	VCXOSEL	Divider START DETERM-Block	When set to 0, PRI- or SEC-clock is selected, depending on bits 2 and 3 (default) When set to 1, VCXO/AUX-clock is selected, overwrites bits 2 and 3	EEPROM
5	REFSELCNTRL	Reference Selection Control	Reference Select Control to select if the control of the reference is from the internal bit in Register 0 bits 2 and 3 or from the external select pin. - When set to 0: the external pin REF_SEL takes over the selection between PRI and SEC. Autoselect is not available. - When set to 1: The external pin REF_SEL is ignored. The table in (Register 0 <2 and 3>) describes which reference input clock is selected and available (none, PRI, SEC or Autoselect). In autoselect mode, refer to the timing diagram.	EEPROM
6	DELAY_PFD0	PFD	PFD pulse width PFD bit 0 PFD pulse width PFD bit 1	EEPROM
7	DELAY_PFD1			
8	Reserved		Must be set 0	EEPROM
9	CP_DIR	Charge Pump	Determines which direction CP current will regulate (Reference Clock leads to Feedback Clock, Positive CP output current [0], Negative CP output current [1])	EEPROM
10	*CP_SRC*	*Charge Pump Diagnostics*	*Switches the current source in the charge pump on when set to 1 (TI Test-GTME)*	EEPROM
11	*CP_SNK*		*Switches the current sink in the charge pump on when set to 1 (TI Test-GTME)*	EEPROM
12	*CP_OPA*		*Switches the charge pump op-amp off when set to 1 (TI Test-GTME)*	EEPROM
13	CP_PRE	Charge Pump	Preset charge pump output voltage to V_{CC_CP}/2, on [1], off [0]	EEPROM
14	ICP0		CP current setting bit 0	EEPROM
15	ICP1		CP current setting bit 1	EEPROM
16	ICP2		CP current setting bit 2	EEPROM
17	ICP3		CP current setting bit 3	EEPROM
18	RESERVED		Must be set to 0	EEPROM
19	RESERVED		Must be set to 0	EEPROM
20	*IREFRES*	*Charge Pump Diagnostics*	*Enables the 12-kΩ pull-down resistor at I_REF_CP pin when set to 1 (TI Test-GTME)*	EEPROM
21	PECL0HISWING	Output 0	High output voltage swing in LVPECL/LVDS mode if set to 1	EEPROM
22	CMOSMODE0PX	Output 0	LVCMOS mode select for OUTPUT 0 positive pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE0PY			
24	CMOSMODE0NX	Output 0	LVCMOS mode select for OUTPUT 0 negative pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE0NY			

26	OUTBUFSEL0X	Output 0	**OUTPUT TYPE**	**REGISTER BITS**						EEPROM
				22	**23**	**24**	**25**	**26**	**27**	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL0Y	Output 0	**LVDS**	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(2)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) This setting is only available if the Register 11 Bit 3 is set to 0 (Feedback Divider clock is set to CMOS type).
(2) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs.

Register 1 Address 0x01: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	ACDCSEL	Input Buffers	If set to 0 AC Termination, If set to 1 DC termination	EEPROM
1	HYSTEN	Input Buffers	If set to 1 Input Buffers Hysteresis enabled	EEPROM
2	TERMSEL	Input Buffers	If set to 0 Input Buffer Internal Termination enabled	EEPROM
3	PRIINVBB	Input Buffers	If set to 1 Primary Input Negative pin biased with internal VBB voltage	EEPROM
4	SECINVBB	Input Buffers	If set to 1 Secondary Input Negative pin biased with internal VBB voltage	EEPROM
5	FAILSAFE	Input Buffers	If set to 1 Fail Safe is enabled for all input buffers	EEPROM
6	PH1ADJC0	Output 0 and 1	Coarse phase adjust select for Output Divider 1	EEPROM
7	PH1ADJC1			
8	PH1ADJC2			
9	PH1ADJC3			
10	PH1ADJC4			
11	PH1ADJC5			
12	PH1ADJC6			
13	OUT1DIVRSEL0	Output 0 and 1	Output Divider 1 ratio select (seeTable 8)	EEPROM
14	OUT1DIVRSEL1			
15	OUT1DIVRSEL2			
16	OUT1DIVRSEL3			
17	OUT1DIVRSEL4			
18	OUT1DIVRSEL5			
19	OUT1DIVRSEL6			
20	EN01DIV	Output 0 and 1	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL1HISWING	Output 1	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE1PX	Output 1	LVCMOS mode select for OUTPUT 1 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE1PY			
24	CMOSMODE1NX	Output 1	LVCMOS mode select for OUTPUT 1 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE1NY			

26	OUTBUFSEL1X	Output 1	OUTPUT TYPE	REGISTER BITS						EEPROM
				22	23	24	25	26	27	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL1Y	Output 1	LVDS	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs.

Register 2 Address 0x01: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	DLYM0	DELAY M	Reference phase delay M bit0	EEPROM
1	DLYM1		Reference phase delay M bit1	
2	DLYM2		Reference phase delay M bit2	
3	DLYN0	DELAY N	Feedback phase delay N bit0	EEPROM
4	DLYN1		Feedback phase delay N bit1	
5	DLYN2		Feedback phase delay N bit2	
6	PH2ADJC0	Output 2	Coarse phase adjust select for output divider 2	EEPROM
7	PH2ADJC1			
8	PH2ADJC2			
9	PH2ADJC3			
10	PH2ADJC4			
11	PH2ADJC5			
12	PH2ADJC6			
13	OUT2DIVRSEL0	Output 2	Output Divider 2 ratio select (seeTable 8)	EEPROM
14	OUT2DIVRSEL1			
15	OUT2DIVRSEL2			
16	OUT2DIVRSEL3			
17	OUT2DIVRSEL4			
18	OUT2DIVRSEL5			
19	OUT2DIVRSEL6			
20	EN2DIV	Output 2	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL2HISWING	Output 2	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE2PX	Output 2	LVCMOS mode select for OUTPUT 2 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE2PY			
24	CMOSMODE2NX	Output 2	LVCMOS mode select for OUTPUT 2 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE2NY			
26	OUTBUFSEL2X	Output 2	**OUTPUT TYPE** / **REGISTER BITS**	EEPROM
27	OUTBUFSEL2Y		

OUTPUT TYPE	22	23	24	25	26	27
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	See Settings Above(1)				0	0
All Outputs Disabled	0	1	0	1	1	0

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs.

Register 3 Address 0x03: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	DIS_FDET_REF	PLL Freq. Detect	When set to 0, the REF-clock frequency detector is ON When set to 1, it is switched OFF	EEPROM
1	DIS_FDET_FB	Diagnostics	When set to 1, the feedback path frequency detector is switched OFF (TI Test-GTME)	EEPROM
2	BIAS_DIV01<0>	Output Divider 0 and 1	When BIAS_DIV01<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
3	BIAS_DIV01<1>			
4	BIAS_DIV23<0>	Output Divider 2 and 3	When BIAS_DIV23<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
5	BIAS_DIV23<1>			
6	PH3ADJC0	Output 3	Coarse phase adjust select for Output Divider 3	EEPROM
7	PH3ADJC1			
8	PH3ADJC2			
9	PH3ADJC3			
10	PH3ADJC4			
11	PH3ADJC5			
12	PH3ADJC6			
13	OUT3DIVRSEL0	Output 3	Output Divider 3 ratio select (seeTable 8)	EEPROM
14	OUT3DIVRSEL1			
15	OUT3DIVRSEL2			
16	OUT3DIVRSEL3			
17	OUT3DIVRSEL4			
18	OUT3DIVRSEL5			
19	OUT3DIVRSEL6			
20	EN3DIV	Output 3	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL3HISWING	Output 3	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE3PX	Output 3	LVCMOS mode select for OUTPUT 3 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE3PY			
24	CMOSMODE3NX	Output 3	LVCMOS mode select for OUTPUT 3 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE3NY			
26	OUTBUFSEL3X	Output 3	**OUTPUT TYPE** / **REGISTER BITS** (22, 23, 24, 25, 26, 27)	EEPROM
			LVPECL 0 0 0 0 0 1	
27	OUTBUFSEL3Y	Output 3	**LVDS** 0 1 0 1 1 1	EEPROM
			LVCMOS See Settings Above(1) 0 0	
			All Outputs Disabled 0 1 0 1 1 0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 4 Address 0x04: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	RESERVED		Must be set '0'	EEPROM
1	RESERVED		Must be set '0'	EEPROM
2	RESERVED		Must be set '0'	EEPROM
3	RESERVED		Must be set '0'	EEPROM
4	HOLDONLOR	HOLD_OVER	If set to 0, CP remains active and will discharge loop filter if input reference clock is lost	EEPROM
5	RESERVED			EEPROM
6	PH4ADJC0	Output 4	Coarse phase adjust select for Output Divider 4	EEPROM
7	PH4ADJC1			
8	PH4ADJC2			
9	PH4ADJC3			
10	PH4ADJC4			
11	PH4ADJC5			
12	PH4ADJC6			
13	OUT4DIVRSEL0	Output 4	Output Divider 4 ratio select (seeTable 8)	EEPROM
14	OUT4DIVRSEL1			
15	OUT4DIVRSEL2			
16	OUT4DIVRSEL3			
17	OUT4DIVRSEL4			
18	OUT4DIVRSEL5			
19	OUT4DIVRSEL6			
20	EN4DIV	Output 4	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL4HISWING	Output 4	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE4PX	Output 4	LVCMOS mode select for OUTPUT 4 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE4PY			
24	CMOSMODE4NX	Output 4	LVCMOS mode select for OUTPUT 4 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE4NY			

26	OUTBUFSEL4X	Output 4	OUTPUT TYPE	REGISTER BITS						EEPROM
				22	23	24	25	26	27	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL4Y	Output 4	**LVDS**	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 5 Address 0x05: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	BIAS_DIV45<0>	Output Divider 4 and 5	When BIAS_DIV45<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
1	BIAS_DIV45<1>			
2	BIAS_DIV67<0>	Output Divider 6 and 7	When BIAS_DIV67<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
3	BIAS_DIV67<1>			
4	RESERVED			EEPROM
5	RESERVED			EEPROM
6	PH5ADJC0	Output 5	Coarse phase adjust select for Output Divider 5	EEPROM
7	PH5ADJC1			
8	PH5ADJC2			
9	PH5ADJC3			
10	PH5ADJC4			
11	PH5ADJC5			
12	PH5ADJC6			
13	OUT5DIVRSEL0	Output 5	Output Divider 5 ratio select (seeTable 8)	EEPROM
14	OUT5DIVRSEL1			
15	OUT5DIVRSEL2			
16	OUT5DIVRSEL3			
17	OUT5DIVRSEL4			
18	OUT5DIVRSEL5			
19	OUT5DIVRSEL6			
20	EN5DIV	Output 5	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL5HISWING	Output 5	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE5PX	Output 5	LVCMOS mode select for OUTPUT 5 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE5PY			
24	CMOSMODE5NX	Output 5	LVCMOS mode select for OUTPUT 5 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE5NY			
26	OUTBUFSEL5X	Output 5	**OUTPUT TYPE** / **REGISTER BITS** (22, 23, 24, 25, 26, 27)	EEPROM
27	OUTBUFSEL5Y	Output 5		EEPROM

OUTPUT TYPE	22	23	24	25	26	27
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	See Settings Above(1)				0	0
All Outputs Disabled	0	1	0	1	1	0

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 6 Address 0x06: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	FB_FD_DESEL	LOCK-DET	0 Feedback Frequency Detector is connected to the Lock Detector 1 Feedback Frequency Detector is disconnected from the Lock Detector	EEPROM
1	RESERVED		Set to 0	
2	FBDETERM_DIV_SEL	FB-Divider/ Deterministic Blocks	0 FB-Deterministic Clock divided by 1 1 FB- Deterministic Clock divided by 2	EEPROM
3	FBDETERM_DIV2_DIS		0 FB-Deterministic-DIV2-Block in normal operation 1 FB-Deterministic-DIV2 reset (here REG6_RB<2> == 0)	
4	FB_START_BYPASS		0 FB-Divider started with delay block (RC), normal operation 1 FB-Divider can be started with external REF_SEL-signal (pin)	
5	DET_START_BYPASS	All Output Dividers	0 Output-Dividers started with delay block (RC), normal operation 1 Output-Dividers can be started with external NRESET-signal (pin)	EEPROM
6	PH6ADJC0	Output 6	Coarse phase adjust select for Output Divider 6	EEPROM
7	PH6ADJC1			
8	PH6ADJC2			
9	PH6ADJC3			
10	PH6ADJC4			
11	PH6ADJC5			
12	PH6ADJC6			
13	OUT6DIVRSEL0	Output 6	Output Divider 6 ratio select (seeTable 8)	EEPROM
14	OUT6DIVRSEL1			
15	OUT6DIVRSEL2			
16	OUT6DIVRSEL3			
17	OUT6DIVRSEL4			
18	OUT6DIVRSEL5			
19	OUT6DIVRSEL6			
20	EN6DIV	Output 6	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL6HISWING	Output 6	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE6PX	Output 6	LVCMOS mode select for OUTPUT 6 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE6PY			
24	CMOSMODE6NX	Output 6	LVCMOS mode select for OUTPUT 6 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE6NY			

26	OUTBUFSEL6X	Output 6	**OUTPUT TYPE**	**REGISTER BITS**						EEPROM
				22	**23**	**24**	**25**	**26**	**27**	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL6Y	Output 6	**LVDS**	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24 and 25 for setting the LVCMOS outputs

Register 7 Address 0x07: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	LOCKW 0	LOCK-DET	Lock-detect window Bit 0 (Refer to Reg 9 Bits 6 and 7)	EEPROM
1	LOCKW 1		Lock-detect window Bit 1 (Refer to Reg 9 Bits 6 and 7)	EEPROM
2	RESERVED		Set to 0	
3	LOCKC0		Number of coherent lock events Bit 0	
4	LOCKC1		Number of coherent lock events Bit 1	
5	ADLOCK		Selects Digital PLL_LOCK 0, Selects Analog PLL_LOCK 1	
6	PH7ADJC0	Output 7	Coarse phase adjust select for Output Divider 7	EEPROM
7	PH7ADJC1			
8	PH7ADJC2			
9	PH7ADJC3			
10	PH7ADJC4			
11	PH7ADJC5			
12	PH7ADJC6			
13	OUT7DIVRSEL0	Output 7	Output Divider 7 ratio select (seeTable 8)	EEPROM
14	OUT7DIVRSEL1			
15	OUT7DIVRSEL2			
16	OUT7DIVRSEL3			
17	OUT7DIVRSEL4			
18	OUT7DIVRSEL5			
19	OUT7DIVRSEL6			
20	EN7DIV	Output 7	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL7HISWING	Output 7	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE7PX	Output 7	LVCMOS mode select for OUTPUT 7 Positive Pin (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE7PY			
24	CMOSMODE7NX	Output 7	LVCMOS mode select for OUTPUT 7 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE7NY			

26	OUTBUFSEL7X	Output 7	OUTPUT TYPE	REGISTER BITS 22	23	24	25	26	27	EEPROM
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL7Y	Output 7	**LVDS**	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 8 Address 0x08: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	VCXOBUFSELX	VCXO and AUX Input Buffers	VCXO and AUX Input Buffer Type Select (LVPECL,LVDS or LVCMOS) XY(10) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin	EEPROM
1	VCXOBUFSELY			
2	VCXOACDCSEL		If Set to 0 AC Termination, If set to 1 DC Termination	
3	VCXOHYSTEN		If Set to 1 Input Buffers Hysteresis enabled	
4	VCXOTERMSEL		If Set to 0 Input Buffer Internal Termination enabled	
5	VCXOINVBB	VCXO Input Buffer	If Set to 1 It Biases VCXO Input negative pin with internal VCXOVBB Voltage	EEPROM
6	PH8ADJC0	Output 8 and 9	Coarse phase adjust select for Output Divider 8	EEPROM
7	PH8ADJC1			
8	PH8ADJC2			
9	PH8ADJC3			
10	PH8ADJC4			
11	PH8ADJC5			
12	PH8ADJC6			
13	OUT8DIVRSEL0	Output 8 and 9	Output Divider 8 ratio select (seeTable 8)	EEPROM
14	OUT8DIVRSEL1			
15	OUT8DIVRSEL2			
16	OUT8DIVRSEL3			
17	OUT8DIVRSEL4			
18	OUT8DIVRSEL5			
19	OUT8DIVRSEL6			
20	EN89DIV	Output 8 and 9	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL8HISWING	Output 8	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE8PX	Output 8	LVCMOS mode select for OUTPUT 8 Positive Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE8PY			
24	CMOSMODE8NX	Output 8	LVCMOS mode select for OUTPUT 8 Negative Pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE8NY			

26	OUTBUFSEL8X	Output 8	OUTPUT TYPE	REGISTER BITS						EEPROM
				22	23	24	25	26	27	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL8Y	Output 8	LVDS	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 9 Address 0x09: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	HOLDF	HOLD-Over	Enables the Frequency Hold-Over (External Hold Over Function based on the external circuitry) on 1, off 0	EEPROM
1	RESERVED			
2	$\overline{\text{HOLD}}$		3-State Charge Pump 0 - (equal to $\overline{\text{HOLD}}$ pin function)	
3	HOLDTR		HOLD function always activated 1 (recommended for test purposes, only) Triggered by analog PLL Lock detect outputs If analog PLL Lock Signal is [1] (PLL locked), HOLD is activated If analog PLL Lock Signal is [0] (PLL not lock), HOLD is deactivated	
4	HOLD_CNT0		HOLD Function is reactivated after X Ref Clock Cycles. Defined by (HOLD_CNT0,HOLD_CNT1) : X = Number of Clock Cycles. For (00) : X = 64, (01) : X = 128, (10) : X = 256, (11) : X = 512 Clock Cycles	
5	HOLD_CNT1			
6	LOCKW 2	LOCK-DET	Extended Lock-detect window Bit 2 (also refer to Reg 7 Bits 0 and 1)	EEPROM
7	LOCKW 3		Extended Lock-detect window Bit 3 (also refer to Reg 7 Bits 0 and 1)	
8	NOINV_RESHOL_INT	Chip CORE	When set to 0, SPI/HOLD_INT and SPI/RESET_INT inverted (default) When set to 1, SPI/HOLD_INT and SPI/RESET_INT not inverted	EEPROM
9	DIVSYNC_DIS	*Diagnostic: PLL N/M Divider*	When GTME = 0, this Bit has no functionality, But when GTME = 1, then: When set to 0, START-Signal is synchronized to N/M Divider Input Clocks When set to 1, START-Sync N/M Divider in PLL are bypassed	EEPROM
10	START_BYPASS	Divider START DETERM-Block	When set to 0, START-Signal is synchronized to VCXO-Clock When set to 1, START-Sync Block is bypassed	EEPROM
11	INDET_BP	Divider START DETERM-Block	When set to 0, Sync Logic active when VCXO/AUX-Clocks are available When set to 1, Sync Logic is independent from VCXO- and/or AUX-Clocks	EEPROM
12	PLL_LOCK_BP	Divider START DETERM-Block	When set to 0, Sync Logic waits for 1st PLL_LOCK state When set to 1, Sync Logic independent from 1st PLL_LOCK	EEPROM
13	LOW_FD_FB_EN	Divider START DETERM-Block	When set to 0, Sync Logic is independent from VCXO/DIV_FB freq. (PLL-FD) When set to 1, Sync Logic is started for VCXO/DIV_FB > ~600KHz, stopped for VCXO/DIV_FB < ~600KHz	EEPROM
14	NPRESET_MDIV	PLL M/FB-Divider	When set to 0, M-Divider uses NHOLD as NPRESET When set to 1, M-Divider NOT preseted by NHOLD	EEPROM
15	BIAS_DIV_FB<0>	Feedback Divider	When BIAS_DIV_FB<1:0> = 00, No current reduction for FB-Divider 01, Current reduction for FB-Divider by about 20% 10, Current reduction for FB-Divider by about 30%	EEPROM
16	BIAS_DIV_FB<1>			
17	BIAS_DIV89<0>	Output Divider 8 and 9	When BIAS_DIV89<1:0> = 00, No current reduction for all output-rivider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
18	BIAS_DIV89<1>			
19	AUXINVBB	AUX Input Buffer	If set to 1 it biases AUX Input Negative pin with internal VCXOVBB voltage.	EEPROM
20	DIS_AUX_Y9		If set to 1 AUX in Input Mode Buffer Is disabled. If set to 0 it follows the behavior of FB_MUX_SEL and OUT_MUX_SEL bits settings.	
21	PECL9HISWING	Output 9	High output voltage swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	CMOSMODE9PX	Output 9	LVCMOS mode select for OUTPUT 9 Positive pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
23	CMOSMODE9PY			
24	CMOSMODE9NX	Output 9	LVCMOS mode select for OUTPUT 9 Negative pin. (X,Y) = 00: Active, 10: Inverting, 11: Low, 01: 3-State	EEPROM
25	CMOSMODE9NY			

26	OUTBUFSEL9X	Output 9	**OUTPUT TYPE**	**REGISTER BITS**						EEPROM
				22	**23**	**24**	**25**	**26**	**27**	
			LVPECL	0	0	0	0	0	1	
27	OUTBUFSEL9Y	Output 9	**LVDS**	0	1	0	1	1	1	EEPROM
			LVCMOS	See Settings Above(1)				0	0	
			All Outputs Disabled	0	1	0	1	1	0	

(1) Use description for bits 22, 23, 24, and 25 for setting the LVCMOS outputs

Register 10 Address 0x0A: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	M0	Reference (PRI/SEC) Divider M	Reference Divider M Bit 0	EEPROM
1	M1		Reference Divider M Bit 1	
2	M2		Reference Divider M Bit 2	
3	M3		Reference Divider M Bit 3	
4	M4		Reference Divider M Bit 4	
5	M5		Reference Divider M Bit 5	
6	M6		Reference Divider M Bit 6	
7	M7		Reference Divider M Bit 7	
8	M8		Reference Divider M Bit 8	
9	M9		Reference Divider M Bit 9	
10	M10		Reference Divider M Bit 10	
11	M11		Reference Divider M Bit 11	
12	M12		Reference Divider M Bit 12	
13	M13		Reference Divider M Bit 13	
14	N0	VCXO/AUX/SEC Divider N	VCXO Divider N Bit 0	EEPROM
15	N1		VCXO Divider N Bit 1	
16	N2		VCXO Divider N Bit 2	
17	N3		VCXO Divider N Bit 3	
18	N4		VCXO Divider N Bit 4	
19	N5		VCXO Divider N Bit 5	
20	N6		VCXO Divider N Bit 6	
21	N7		VCXO Divider N Bit 7	
22	N8		VCXO Divider N Bit 8	
23	N9		VCXO Divider N Bit 9	
24	N10		VCXO Divider N Bit 10	
25	N11		VCXO Divider N Bit 11	
26	N12		VCXO Divider N Bit 12	
27	N13		VCXO Divider N Bit 13	

Register 11 Address 0x0B: SPI Mode

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	PRI_DIV2	Input Buffers	If set to 1 enables Primary Reference Divide by 2	EEPROM
1	SEC_DIV2	Input Buffers	If set to 1 enables Secondary Reference Divide by 2	EEPROM
2	FB_DIS	FB Path Integer Counter 32	When set to 0, FB divider is active When set to 1, FB divider is disabled	EEPROM
3	FB_CML_SEL	FB Path Integer Counter 32	When set to 0, FB clock is CMOS type(1) When set to 1, FB clock is CML type and uses CML2CMOS converter in PLL	EEPROM
4	FB_INCLK_INV	FB-Divider/ Deterministic Blocks	When set to 0, Input clock for FB not inverted (normal mode, low speed) When set to 1, Input clock for FB inverted (higher speed mode)	EEPROM
5	FB_COUNT32_0	FB Path Integer Counter 32	Feedback Counter Bit0	EEPROM
6	FB_COUNT32_1		Feedback Counter Bit1	
7	FB_COUNT32_2		Feedback Counter Bit2	
8	FB_COUNT32_3		Feedback Counter Bit3	
9	FB_COUNT32_4		Feedback Counter Bit4	
10	FB_COUNT32_5		Feedback Counter Bit5	
11	FB_COUNT32_6		Feedback Counter Bit6	
12	FB_PHASE0	FB Path Integer Counter 32	Feedback Phase Adjust Bit0	EEPROM
13	FB_PHASE1		Feedback Phase Adjust Bit1	
14	FB_PHASE2		Feedback Phase Adjust Bit2	
15	FB_PHASE3		Feedback Phase Adjust Bit3	
16	FB_PHASE4		Feedback Phase Adjust Bit4	
17	FB_PHASE5		Feedback Phase Adjust Bit5	
18	FB_PHASE6		Feedback Phase Adjust Bit6	
19	PD_PLL	PLL	If set to 0, PLL is in normal mode If set to 1, PLL is powered down	EEPROM
20	FB_MUX_SEL See Table 7	Clock Tree and Deterministic Block	When set to 0, the VCXO Clock is selected for the Clock Tree and FB-Div and Det When set to 1, the AUX Clock is selected for the Clock Tree and FB-Div and Det	EEPROM
21	OUT_MUX_SEL See Table 7	Clock Tree	If Set to 0 it selects the VCXO Clock and if Set to 1 it selects the AUX Clock	EEPROM
22	*FB_SEL*	*Diagnostics*	*Feed Back Path Selects FB/VCXO-Path when set to 0 (TI Test-GTME)* *The Secondary Reference clock input is selected when set to 1 (TI Test-GTME)*	EEPROM
23	NRESHAPE1	Reference Selection Control	Reshapes the Reference Clock Signal 0, Disable Reshape 1	EEPROM
24	SEL_DEL1		If set to 0 it enables short delay for fast operation If Set to 1 Long Delay recommended for Input References below 150Mhz	EEPROM
25	RESET_HOLD_MODE	Reset Circuitry	If set to 1 the RESET or HOLD pin acts as $\overline{\text{HOLD}}$, set to 0 it acts as $\overline{\text{RESET}}$	EEPROM
26	EPLOCK	Status	Read only. If EPLOCK reads a 0, the EEPROM is unlocked. If EPLOCK reads a 1, then the EEPROM is locked.	EEPROM
27	Reserved	read only	Read only; always reads '1'	EEPROM

(1) When Feedback Divider clock is set to CMOS type, only feedback divider values greater than 5 are available.

Table 7. Output Buffers Source Feed, PLL Source Feed, and AUX IN/OUTPUT 9 Selection

FB_MUX_SEL	OUT_MUX_SEL	PLL FEED AND OUTPUTS FEED	AUX INPUT OR OUTPUT 9
0	0	VCXO::PLL, VCXO::Y0…Y9 and Deterministic Block	OUTPUT 9 is enabled
1	0	AUXIN::PLL, VCXO::Y0…Y8 and Deterministic Block	AUX IN is enabled
0	1	VCXO::PLL, AUXIN::Y0…Y8 and Deterministic Block	AUX IN is enabled
1	1	AUXIN::PLL, AUXIN::Y0…Y8 and Deterministic Block	AUX IN is enabled

Register 12 Address 0x0C: SPI Mode (RAM only Register)

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POR DEFAULT	
0	RESERVED		Must be set '0'		RAM
1	RESERVED		Must be set '0'		RAM
2	RESERVED		Must be set '0'		RAM
3	RESERVED		Must be set '0'		RAM
4	INDET_AUX	Status (Read Only)	It indicates that a clock is present at AUX-input (Y9) , when set to 1		RAM
5	INDET_VCXO	Status (Read Only)	It indicates that a clock is present at VCXO-input , when set to 1		RAM
6	PLL_LOCK	Status (Read Only)	It indicates that the PLL is locked when set to 1		RAM
7	$\overline{\text{SLEEP}}$	Power Down	Power-down mode on when set to 0, Off when set to 1	1	RAM
8	$\overline{\text{RESET\_HOLD}}$	Reset	If set to 0 this bit forces "$\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$" depending on the setting of RESET_HOLD_MODE bit in Register 11. If set to 0 $\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$ are asserted. Set for 1 for normal operation.	1	RAM
9	*GTME*	*Diagnostics*	*General Test Mode Enable, Test Mode is only enabled, if this bit is set to 1 This bit controls many test modes on the device.*	0	RAM
10	*REVISION0*	*Status*	*Read only: Revision Control Bit 0*		RAM
11	*REVISION1*	*Status*	*Read only: Revision Control Bit 1*		RAM
12	*REVISION2*	*Status*	*Read only: Revision Control Bit 2*		RAM
13	*PD_IO*	*Diagnostics*	*When set to 0, all blocks are on. (TI Test-GTME) When set to 1, the VCXO Input, AUX Input and all output buffers and divider blocks are disabled. This test is done to measure the effect of the I/O circuitry on the Charge Pump. (TI Test-GTME)*	0	RAM
14	*SXOIREF*	*Diagnostics*	*If set to 0 that Status pin is used as CMOS output to enable TI test modes. Set to 1 when IREFRES is set to 1 and 12-KΩ resistor is connected. (TI Test-GTME)*	0	RAM
15	*SHOLD*	*Diagnostics*	*Routes the HOLD signal to the PLL_LOCK pin when set to 1 (TI Test-GTME)*	0	RAM
16	*RESERVED*		Must be set '0'	0	RAM
17	*STATUS0*	*Diagnostics*	TI test registers. For TI use only Route internal signals to external STATUS pin. STATUS3, STATUS2, STATUS1, STATUS0 (S3, S2, S1, S0) will select that internal status signal that will be routed to the external STATUS pin.	1	RAM
18	*STATUS1*				
19	*STATUS2*				
20	*STATUS3*				
21	*TITSTCFG0*	*Diagnostics*	*TI test registers. For TI use only*	0	RAM
22	*TITSTCFG1*	*Diagnostics*	*TI test registers. For TI use only*	0	RAM
23	*TITSTCFG2*	*Diagnostics*	*TI test registers. For TI use only*	0	RAM
24	*TITSTCFG3*	*Diagnostics*	*TI test registers. For TI use only*	0	RAM
25	PRIACTIVITY	Status	It indicates activity on the Primary when set to - (read only bit)		RAM
26	SECACTIVITY	Status	It indicates activity on the Secondary when set to - (read only bit)		RAM
27	RESERVED				RAM

NOTE

If TI test bits (Register 12< bits 17,18,19, 20> are set to 1000, Reference Select from the Smart Mux will show on the STATUS pin (High = Primary REF is selected and Low = Secondary REF is selected).

When TI test bits are set to 0000 the Reference Clock Frequency Detector shows up on the STATUS pin. In this mode the STATUS pin goes high if a clock is detected and low if a clock is not detected. In this configuration Register 3 Bit 0 should be set to 0.

OUTPUT DIVIDERS SETTINGS

The CDCE72010 has a complex multi stage output divider. The table below describes the setting of Bits 13:19 of Register 1 to 8 and the setting for the feedback divider bits 5:11 of register 11. The table below describes divider settings and the phase relation of the outputs with respect to divide by one clock. To calculate the phase relation between 2 different dividers see Output Divider and Phase Adjust Section in this document.

Table 8. Output Dividers and Feedback Divide Settings and Phase Output

FOR REGISTER 1 TO 8 BITS {19[BIT6] TO 13[BIT0]} FOR REGISTER 11 BITS {11[BIT6] TO 5[BIT0]}							DIVIDE BY TOTAL
[Bit 6]	[Bit 5]	[Bit 4]	[Bit 3]	[Bit 2]	[Bit 1]	[Bit 0]	
0	1	0	0	0	0	0	1
1	0	0	0	0	0	0	2
1	0	0	0	0	0	1	3
1	0	0	0	0	1	0	4
1	0	0	0	0	1	1	5
0	0	0	0	0	0	0	4'
0	0	0	0	0	0	1	6
0	0	0	0	0	1	0	8
0	0	0	0	0	1	1	10
0	0	0	0	1	0	0	8'
0	0	0	0	1	0	1	12
0	0	0	0	1	1	0	16
0	0	0	0	1	1	1	20
0	0	0	1	0	0	0	12'
0	0	0	1	0	0	1	18
0	0	0	1	0	1	0	24
0	0	0	1	0	1	1	30
0	0	0	1	1	0	0	16'
0	0	0	1	1	0	1	24'
0	0	0	1	1	1	0	32
0	0	0	1	1	1	1	40
0	0	1	0	0	0	0	20'
0	0	1	0	0	0	1	30'
0	0	1	0	0	1	0	40'
0	0	1	0	0	1	1	50
0	0	1	0	1	0	0	24'
0	0	1	0	1	0	1	36
0	0	1	0	1	1	0	48
0	0	1	0	1	1	1	60
0	0	1	1	0	0	0	28
0	0	1	1	0	0	1	42
0	0	1	1	0	1	0	56
0	0	1	1	0	1	1	70
0	0	1	1	1	0	0	32'
0	0	1	1	1	0	1	48'
0	0	1	1	1	1	0	64
0	0	1	1	1	1	1	80

CONFIGURATION DEFAULT MODE (CD MODE)

The CDCE72010 has two modes of operation, SPI Interface and Configuration Default Mode. The Configuration Default mode is selected when MODE_SEL Pin is driven low and it is used where SPI interface is not available. In the CD Mode configuration, the SPI interface Pins become static control pins CD1, CD2, CD3 and AUX_SEL as shown in the Pin description. The CD Mode signals are sampled only at power up or after Power Down are asserted.

In CD Mode, CD1 and CD2 are used to switch between EEPROM saved configurations.

- CD1 allows swapping Divider and Phase Adjust value between output couples
- CD2 allows changing the output type for each output.
- AUX_SEL Controls the Output Mux between VCXO and AUX Input.
- CD3 must be grounded in CD Mode.

Without any interface a single device with a single program can have multiple configurations that can be implemented on more than one socket.

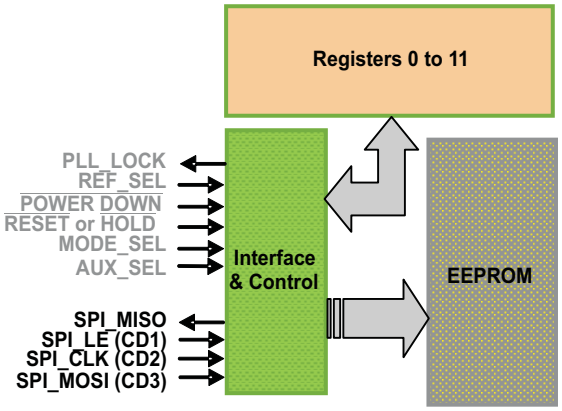


Figure 18. Writing to EEPROM via SPI Bus

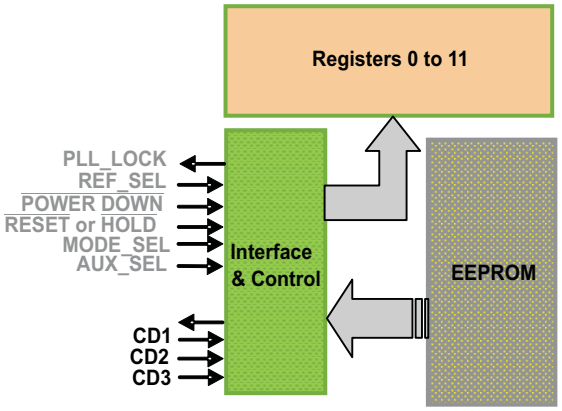


Figure 19. Using CD1, CD2 to Control What is Copied From EEPROM Into Registers at Power Up

Register 0 Address 0x00: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	INBUFSELX	Reference Input Buffers	Primary and Secondary Buffer Type Select (LVPECL,LVDS or LVCMOS) XY(10) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin	EEPROM
1	INBUFSELY			
2	PRISEL	Reference Input Buffer	When REFSELCNTRL is set to 1 the following settings apply: If Bit (2,3): 00 – no Input Buffer is selected/active If Bit (2,3): 10 – PRI_REF is selected, SEC_BUF is powered down If Bit (2,3): 01 – SEC_REF is selected, PRI_BUF is powered down(1) If Bit (2,3): 11 – Auto Select (PRI then SEC).	EEPROM
3	SECSEL			
4	VCXOSEL	Divider START DETERM-Block	When set to 0, PRI- or SEC-Clocks are selected, depending on Bits 2 and 3 (default) When set to 1, VCXO/AUX-clock selected, overwrites Bits 2 and 3	EEPROM
5	REFSELCNTRL	Reference Selection Control	Reference Select Control to select if the control of the reference is from the internal bit in Register 0 bits 2 and 3 or from the external select pin. – When set to 0: The external pin REF_SEL takes over the selection between PRI and SEC. Autoselect is not available. – When set to 1 R0.2 and R0.3 bits must be set '1': The external pin REF_SEL is ignored. The Table in (Register 0 <2 and 3>) describes, which reference input clock is selected and available at (none, PRI, SEC or Autoselect). In autoselect mode, refer to the timing diagram	EEPROM
6	DELAY_PFD0	PFD	PFD Pulse Width PFD Bit 0	EEPROM
7	DELAY_PFD1	PFD	PFD Pulse Width PFD Bit 1	EEPROM
8	RESERVED		Must be set '0'	EEPROM
9	CP_DIR	Charge Pump	Determines in which direction CP current will regulate (Reference Clock leads to Feedback Clock; Positive CP output current [0]; Negative CP output current [1]	EEPROM
10	*CP_SRC*	*Diagnostics*	*Switches the current source in the Charge Pump on when set to 1 (TI Test-GTME)*	EEPROM
11	*CP_SNK*		*Switches the current sink in the Charge Pump on when set to 1 (TI Test-GTME)*	EEPROM
12	*CP_OPA*		*Switches the Charge Pump op-amp off when set to 1 (TI Test-GTME)*	EEPROM
13	CP_PRE	Charge Pump	Preset Charge Pump output voltage to V_{CC_CP}/2, on [1], off [0]	EEPROM
14	ICP0		CP Current Setting Bit 0	EEPROM
15	ICP1		CP Current Setting Bit 1	EEPROM
16	ICP2		CP Current Setting Bit 2	EEPROM
17	ICP3		CP Current Setting Bit 3	EEPROM
18	RESERVED		Must be set '0'	EEPROM
19	RESERVED		Must be set '0'	EEPROM
20	*IREFRES*	*Diagnostics*	*Enables the 12k pull-down resistor at I_REF_CP Pin when set to 1 (TI Test-GTME)*	EEPROM
21	PECL0HISWING	Output 0	High output voltage swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	RESERVED			EEPROM
23	RESERVED			EEPROM
24	OUTBUF0CD2LX	CD2 Low	Output Buffer 0 Signaling Selection when CD2 In low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF0CD2LY			
26	OUTBUF0CD2HX	CD2 High	Output Buffer 0 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: output disable	EEPROM
27	OUTBUF0CD2HY			

(1) This setting is only avaiable if the Register 11 Bit 3 is set to 0 (Feedback Divider clock is set to CMOS type).

Register 1 Address 0x01: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	ACDCSEL	Input Buffers	If Set to 0 AC Termination, If set to 1 DC termination	EEPROM
1	HYSTEN	Input Buffers	If Set to 1 Input Buffers Hysteresis enabled	EEPROM
2	TERMSEL	Input Buffers	If Set to 0 Input Buffer Internal Termination enabled	EEPROM
3	PRIINVBB	Input Buffers	If Set to 1 Primary Input Negative Pin biased with internal VBB voltage.	EEPROM
4	SECINVBB	Input Buffers	If Set to 1 Secondary Input Negative Pin biased with internal VBB voltage	EEPROM
5	FAILSAFE	Input Buffers	If Set to 1 Fail Safe is enabled for all input buffers.	EEPROM
6	PH1ADJC0	Output 0 and 1	Coarse phase adjust select for output divider 1	EEPROM
7	PH1ADJC1			
8	PH1ADJC2			
9	PH1ADJC3			
10	PH1ADJC4			
11	PH1ADJC5			
12	PH1ADJC6			
13	OUT1DIVRSEL0	Output 0 and 1	OUTPUT DIVIDER 1 Ratio Select (See Table 8)	EEPROM
14	OUT1DIVRSEL1			
15	OUT1DIVRSEL2			
16	OUT1DIVRSEL3			
17	OUT1DIVRSEL4			
18	OUT1DIVRSEL5			
19	OUT1DIVRSEL6			
20	EN01DIV	Output 0 and 1	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL1HISWING	Output 1	High output voltage swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA1CD1H	CD1 High	CD1 PIN is high and DIVPHA1CD1H is set to low Loads Output Divider 1 and Phase Adjust 1 into OUTPUT 1 CD1 PIN is high and DIVPHA1CD1H is set to high Loads Output Divider 2 and Phase Adjust 2 into OUTPUT 1	EEPROM
23	DIVPHA1CD1L	CD1 Low	CD1 PIN is low and DIVPHA1CD1L is set to low Loads Output Divider 1 and Phase Adjust 1 into OUTPUT 1 CD1 PIN is low and DIVPHA1CD1L is set to high Loads Output Divider 2 and Phase Adjust 2 into OUTPUT 1	EEPROM
24	OUTBUF1CD2LX	CD2 Low	Output Buffer 1 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF1CD2LY			
26	OUTBUF1CD2HX	CD2 High	Output Buffer 1 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF1CD2HY			

Register 1 Address 0x01: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	DLYM0	DELAY M	Reference Phase Delay M Bit0	EEPROM
1	DLYM1		Reference Phase Delay M Bit1	
2	DLYM2		Reference Phase Delay M Bit2	
3	DLYN0	DELAY N	Feedback Phase Delay N Bit0	EEPROM
4	DLYN1		Feedback Phase Delay N Bit1	
5	DLYN2		Feedback Phase Delay N Bit2	
6	PH2ADJC0	Output 2	Coarse phase adjust select for output divider 2	EEPROM
7	PH2ADJC1			
8	PH2ADJC2			
9	PH2ADJC3			
10	PH2ADJC4			
11	PH2ADJC5			
12	PH2ADJC6			
13	OUT2DIVRSEL0	Output 2	OUTPUT DIVIDER 2 Ratio Select (See Table 8)	EEPROM
14	OUT2DIVRSEL1			
15	OUT2DIVRSEL2			
16	OUT2DIVRSEL3			
17	OUT2DIVRSEL4			
18	OUT2DIVRSEL5			
19	OUT2DIVRSEL6			
20	EN2DIV	Output 2	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL2HISWING	Output 2	High output voltage swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA2CD1H	CD1 High	CD1 PIN is high and DIVPHA2CD1H is set to low Loads Output Divider 2 and Phase Adjust 2 into OUTPUT 2 CD1 PIN is high and DIVPHA2CD1H is set to high Loads Output Divider 1 and Phase Adjust 1 into OUTPUT 2	EEPROM
23	DIVPHA2CD1L	CD1 Low	CD1 PIN is low and DIVPHA2CD1L is set to low Loads Output Divider 2 and Phase Adjust 2 into OUTPUT 2 CD1 PIN is low and DIVPHA2CD1L is set to high Loads Output Divider 1 and Phase Adjust 1 into OUTPUT 2	EEPROM
24	OUTBUF2CD2LX	CD2 Low	Output Buffer 2 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF2CD2LY			
26	OUTBUF2CD2HX	CD2 High	Output Buffer 2 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF2CD2HY			

Register 3 Address 0x03: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	DIS_FDET_REF	PLL Freq. Detect	When set to 0, the REF-clock frequency detector is ON When set to 1, it is switched OFF	EEPROM
1	*DIS_FDET_FB*	*Diagnostics*	*When set to 1, the feedback path frequency detector is switched OFF* *(TI Test-GTME)*	EEPROM
2	BIAS_DIV01<0>	Output Divider 0 and 1	When BIAS_DIV01<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
3	BIAS_DIV01<1>			EEPROM
4	BIAS_DIV23<0>	Output Divider 2 and 3	When BIAS_DIV23<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
5	BIAS_DIV23<1>			EEPROM
6	PH3ADJC0	Output 3	Coarse phase adjust select for output divider 3	EEPROM
7	PH3ADJC1			
8	PH3ADJC2			
9	PH3ADJC3			
10	PH3ADJC4			
11	PH3ADJC5			
12	PH3ADJC6			
13	OUT3DIVRSEL0	Output 3	OUTPUT DIVIDER 3 Ratio Select (See Table 8)	EEPROM
14	OUT3DIVRSEL1			
15	OUT3DIVRSEL2			
16	OUT3DIVRSEL3			
17	OUT3DIVRSEL4			
18	OUT3DIVRSEL5			
19	OUT3DIVRSEL6			
20	EN3DIV	Output 3	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL3HISWING	Output 3	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA3CD1H	CD1 High	CD1 PIN is high and DIVPHA3CD1H is set to low Loads Output Divider 3 and Phase Adjust 3 into OUTPUT 3 CD1 PIN is high and DIVPHA3CD1H is set to high Loads Output Divider 4 and Phase Adjust 4 into OUTPUT 3	EEPROM
23	DIVPHA3CD1L	CD1 Low	CD1 PIN is Low and DIVPHA3CD1L is set to low Loads Output Divider 3 and Phase Adjust 3 into OUTPUT 3 CD1 PIN is Low and DIVPHA3CD1L is set to high Loads Output Divider 4 and Phase Adjust 4 into OUTPUT 3	EEPROM
24	OUTBUF3CD2LX	CD2 Low	Output Buffer 3 Signaling Selection when CD2 in low (X,Y) = 01:LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF3CD2LY			
26	OUTBUF3CD2HX	CD2 High	Output Buffer 3 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF3CD2HY			

Register 4 Address 0x04: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	RESERVED		Must be set '0'	EEPROM
1	RESERVED		Must be set '0'	EEPROM
2	RESERVED		Must be set '0'	EEPROM
3	RESERVED		Must be set '0'	EEPROM
4	HOLDONLOR	HOLD_OVER	If set to 0, CP remains active and will discharge loop filter if input reference clock is lost. If set to 1 it will 3-state the charge pump to act as a HOLD on Loss of Reference Clocks (Primary and Secondary)	EEPROM
5	RESERVED			EEPROM
6	PH4ADJC0	Output 4	Coarse phase adjust select for output divider 4	EEPROM
7	PH4ADJC1			
8	PH4ADJC2			
9	PH4ADJC3			
10	PH4ADJC4			
11	PH4ADJC5			
12	PH4ADJC6			
13	OUT4DIVRSEL0	Output 4	OUTPUT DIVIDER 4 Ratio Select (See Table 8)	EEPROM
14	OUT4DIVRSEL1			
15	OUT4DIVRSEL2			
16	OUT4DIVRSEL3			
17	OUT4DIVRSEL4			
18	OUT4DIVRSEL5			
19	OUT4DIVRSEL6			
20	EN4DIV	Output 4	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL4HISWING	Output 4	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA4CD1H	CD1 High	CD1 PIN is high and DIVPHA4CD1H is set to low Loads Output Divider 4 and Phase Adjust 4 into OUTPUT 4 CD1 PIN is high and DIVPHA4CD1H is set to high Loads Output Divider 3 and Phase Adjust 3 into OUTPUT 4	EEPROM
23	DIVPHA4CD1L	CD1 Low	CD1 PIN is low and DIVPHA4CD1L is set to low Loads Output Divider 4 and Phase Adjust 4 into OUTPUT 4 CD1 PIN is low and DIVPHA4CD1L is set to high Loads Output Divider 3 and Phase Adjust 3 into OUTPUT 4	EEPROM
24	OUTBUF4CD2LX	CD2 Low	Output Buffer 4 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF4CD2LY			
26	OUTBUF4CD2HX	CD2 High	Output Buffer 4 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF4CD2HY			

Register 5 Address 0x05: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	BIAS_DIV45<0>	Output Divider 4 and 5	When BIAS_DIV45<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
1	BIAS_DIV45<1>			
2	BIAS_DIV67<0>	Output Divider 6 and 7	When BIAS_DIV67<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
3	BIAS_DIV67<1>			
4	RESERVED			EEPROM
5	RESERVED			EEPROM
6	PH5ADJC0	Output 5	Coarse phase adjust select for output divider 5	EEPROM
7	PH5ADJC1			
8	PH5ADJC2			
9	PH5ADJC3			
10	PH5ADJC4			
11	PH5ADJC5			
12	PH5ADJC6			
13	OUT5DIVRSEL0	Output 5	OUTPUT DIVIDER 5 Ratio Select (See Table 8)	EEPROM
14	OUT5DIVRSEL1			
15	OUT5DIVRSEL2			
16	OUT5DIVRSEL3			
17	OUT5DIVRSEL4			
18	OUT5DIVRSEL5			
19	OUT5DIVRSEL6			
20	EN5DIV	Output 5	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL5HISWING	Output 5	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA5CD1H	CD1 High	CD1 PIN is high and DIVPHA5CD1H is set to low Loads Output Divider 5 and Phase Adjust 5 into OUTPUT 5 CD1 PIN is high and DIVPHA5CD1H is set to high Loads Output Divider 6 and Phase Adjust 6 into OUTPUT 5	EEPROM
23	DIVPHA5CD1L	CD1 Low	CD1 PIN is low and DIVPHA5CD1L is set to low Loads Output Divider 5 and Phase Adjust 5 into OUTPUT 5 CD1 PIN is low and DIVPHA5CD1L is set to high Loads Output Divider 6 and Phase Adjust 6 into OUTPUT 5	EEPROM
24	OUTBUF5CD2LX	CD2 Low	Output Buffer 5 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF5CD2LY			
26	OUTBUF5CD2HX	CD2 High	Output Buffer 5 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF5CD2HY			

Register6 Address 0x06: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	FB_FD_DESEL	LOCK-DET	0 Feedback Frequency Detector is connected to the Lock Detector 1 Feedback Frequency Detector is disconnected from the Lock Detector	EEPROM
1	RESERVED		Set to “0”	
2	FBDETERM_DIV_SEL	FB-Divider / Deterministic Blocks	0 FB-Deterministic Clock divided by 1 1 FB- Deterministic Clock divided by 2	EEPROM
3	FBDETERM_DIV2_DIS		0 FB-Deterministic-DIV2-Block in normal operation 1 FB-Deterministic-DIV2 reset (here REG6_RB<2> == “0”)	
4	FB_START_BYPASS		0 FB-Divider started with delay block (RC), normal operation 1 FB-Divider can be started with external REF_SEL-signal (pin)	
5	DET_START_BYPASS	All Output Dividers	0 Output-Dividers started with delay block (RC), normal operation 1 Output-Dividers can be started with external NRESET-signal (pin)	EEPROM
6	PH6ADJC0	Output 6	Coarse phase adjust select for output divider 6	EEPROM
7	PH6ADJC1			
8	PH6ADJC2			
9	PH6ADJC3			
10	PH6ADJC4			
11	PH6ADJC5			
12	PH6ADJC6			
13	OUT6DIVRSEL0	Output 6	OUTPUT DIVIDER 6 Ratio Select (See Table 8)	EEPROM
14	OUT6DIVRSEL1			
15	OUT6DIVRSEL2			
16	OUT6DIVRSEL3			
17	OUT6DIVRSEL4			
18	OUT6DIVRSEL5			
19	OUT6DIVRSEL6			
20	EN6DIV	Output 6	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL6HISWING	Output 6	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA6CD1H	CD1 High	CD1 PIN is high and DIVPHA6CD1H is set to low Loads Output Divider 6 and Phase Adjust 6 into OUTPUT 6 CD1 PIN is high and DIVPHA6CD1H is set to high Loads Output Divider 5 and Phase Adjust 5 into OUTPUT 6	EEPROM
23	DIVPHA6CD1L	CD1 Low	CD1 PIN is low and DIVPHA6CD1L is set to low Loads Output Divider 6 and Phase Adjust 6 into OUTPUT 6 CD1 PIN is low and DIVPHA6CD1L is set to high Loads Output Divider 5 and Phase Adjust 5 into OUTPUT 6	EEPROM
24	OUTBUF6CD2LX	CD2 Low	Output Buffer 6 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF6CD2LY			
26	OUTBUF6CD2HX	CD2 High	Output Buffer 6 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF6CD2HY			

Table 9. Register 7 Address 0x07: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	LOCKW 0	LOCK-DET	Lock-detect window bit 0 (Refer to Reg 9 Bits 6 and 7)	EEPROM
1	LOCKW 1		Lock-detect window bit 1 (Refer to Reg 9 Bits 6 and 7)	
2	RESERVED		Set to 0	
3	LOCKC0		Number of coherent lock events bit 0	
4	LOCKC1		Number of coherent lock events bit 1	
5	ADLOCK		Selects Digital PLL_LOCK 0 ,Selects Analog PLL_LOCK 1	
6	PH7ADJC0	Output 7	Coarse phase adjust select for output divider 7	EEPROM
7	PH7ADJC1			
8	PH7ADJC2			
9	PH7ADJC3			
10	PH7ADJC4			
11	PH7ADJC5			
12	PH7ADJC6			
13	OUT7DIVRSEL0	Output 7	OUTPUT DIVIDER 7 Ratio Select (See Table 8)	EEPROM
14	OUT7DIVRSEL1			
15	OUT7DIVRSEL2			
16	OUT7DIVRSEL3			
17	OUT7DIVRSEL4			
18	OUT7DIVRSEL5			
19	OUT7DIVRSEL6			
20	EN7DIV	Output 7	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL7HISWING	Output 7	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA7CD1H	CD1 High	CD1 PIN is high and DIVPHA7CD1H is set to low Loads Output Divider 7 and Phase Adjust 7 into OUTPUT 7 CD1 PIN is high and DIVPHA7CD1H is set to high Loads Output Divider 8 and Phase Adjust 8 into OUTPUT 7	EEPROM
23	DIVPHA7CD1L	CD1 Low	CD1 PIN is low and DIVPHA7CD1L is set to low Loads Output Divider 7 and Phase Adjust 7 into OUTPUT 7 CD1 PIN is low and DIVPHA7CD1L is set to high Loads Output Divider 8 and Phase Adjust 8 into OUTPUT 7	EEPROM
24	OUTBUF7CD2LX	CD2 Low	Output Buffer 7 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF7CD2LY			
26	OUTBUF7CD2HX	CD2 High	Output Buffer 7 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF7CD2HY			

Register 8 Address 0x08: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	VCXOBUFSELX	VCXO and AUX Input Buffers VCXO Input Buffer	VCXO and AUX Input Buffer Type Select (LVPECL,LVDS or LVCMOS)	EEPROM
1	VCXOBUFSELY		XY(10) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin	
2	VCXOACDCSEL		If Set to 0 AC Termination, If set to 1 DC Termination	
3	VCXOHYSTEN		If Set to 1 Input Buffers Hysteresis enabled	
4	VCXOTERMSEL		If Set to 0 Input Buffer Internal Termination enabled	
5	VCXOINVBB	VCXO Input Buffer	If Set to 1 It biases VCXO Input negative pin with internal VCXOVBB voltage	EEPROM
6	PH8ADJC0	Output 8 and 9	Coarse phase adjust select for output divider 8 and 9	EEPROM
7	PH8ADJC1			
8	PH8ADJC2			
9	PH8ADJC3			
10	PH8ADJC4			
11	PH8ADJC5			
12	PH8ADJC6			
13	OUT8DIVRSEL0	Output 8 and 9	OUTPUT DIVIDER 8 and 9 Ratio Select (See Table 8)	EEPROM
14	OUT8DIVRSEL1			
15	OUT8DIVRSEL2			
16	OUT8DIVRSEL3			
17	OUT8DIVRSEL4			
18	OUT8DIVRSEL5			
19	OUT8DIVRSEL6			
20	EN89DIV	Output 8 and 9	When set to 0, the divider is disabled When set to 1, the divider is enabled	EEPROM
21	PECL8HISWING	Output 8	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	DIVPHA8CD1H	CD1 High	CD1 PIN is high and DIVPHA8CD1H is set to low Loads Output Divider 8 and Phase Adjust 8 into OUTPUT 8 CD1 PIN is high and DIVPHA8CD1H is set to high Loads Output Divider 7 and Phase Adjust 7 into OUTPUT 8	EEPROM
23	DIVPHA8CD1L	CD1 Low	CD1 PIN is low and DIVPHA8CD1L is set to low Loads Output Divider 8 and Phase Adjust 8 into OUTPUT 8 CD1 PIN is low and DIVPHA8CD1L is set to high Loads Output Divider 7 and Phase Adjust 7 into OUTPUT 8	EEPROM
24	OUTBUF8CD2LX	CD2 Low	Output Buffer 8 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF8CD2LY			
26	OUTBUF8CD2HX	CD2 High	Output Buffer 8 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF8CD2HY			

Register 9 Address 0x09: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	HOLDF1	HOLD- Over	Enables the Frequency Hold-Over Function 1 on 1, off 0	EEPROM
1	HOLDF2		Enables the Frequency Hold-Over Function 2 on 1, off 0	
2	$\overline{\text{HOLD}}$		3-State Charge Pump 0 - (equal to $\overline{\text{HOLD}}$-Pin function)	
3	HOLDTR		HOLD function always activated “1” (recommended for test purposes, only) Triggered by analog PLL Lock detect outputs If analog PLL Lock Signal is [1] (PLL locked), HOLD is activated If analog PLL Lock Signal is [0] (PLL not lock), HOLD is deactivated	
4	HOLD_CNT0		HOLD1 Function is reactivated after X Ref Clock Cycles. Defined by (HOLD_CNT0,HOLD_CNT1)::X= Number of Clock Cycles. For (00)::X=64, (01) ::X=128, (10)::X=256, (11)::X=512 Clock Cycles.	
5	HOLD_CNT1			
6	LOCKW 2	LOCK-DET	Extended Lock-detect window Bit 2 (Also refer to Reg 7 Bits 0 and 1)	EEPROM
7	LOCKW 3		Extended Lock-detect window Bit 3 (Also refer to Reg 7 Bits 0 and 1)	
8	NOINV_RESHOL_INT	Chip CORE	When set to 0, SPI/HOLD_INT and SPI/RESET_INT inverted (default) When set to 1, SPI/HOLD_INT and SPI/RESET_INT not inverted	EEPROM
9	DIVSYNC_DIS	*Diagnostic: PLL N/M Divider*	*When GTME = 0, this bit has no functionality, But when GTME = 1, then:* *When set to 0, START-Signal is synchronized to N/M Divider Input Clocks* *When set to 1, START-Sync N/M Divider in PLL are bypassed*	EEPROM
10	START_BYPASS	Divider START DETERM-Block	When set to 0, START-Signal is synchronized to VCXO-Clock When set to 1, START-Sync Block is bypassed	EEPROM
11	INDET_BP	Divider START DETERM-Block	When set to 0, Sync Logic active when VCXO/AUX-Clocks are available When set to 1, Sync Logic is independent from VCXO- and/or AUX-Clocks	EEPROM
12	PLL_LOCK_BP	Divider START DETERM-Block	When set to 0, Sync Logic waits for 1st PLL_LOCK state When set to 1, Sync Logic independent from 1st PLL_LOCK	EEPROM
13	LOW_FD_FB_EN	Divider START DETERM-Block	When set to 0, Sync Logic is independent from VCXO/DIV_FB freq. (PLL-FD) When set to 1, Sync Logic is started for VCXO/DIV_FB > ~600KHz, stopped for VCXO/DIV_FB < ~600KHz	EEPROM
14	NPRESET_MDIV	PLL M/FB-Divider	When set to 0, M-Divider uses NHOLD1 as NPRESET When set to 1, M-Divider NOT preseted by NHOLD1	EEPROM
15	BIAS_DIV_FB<0>	Feedback Divider	When BIAS_DIV_FB<1:0> = 00, No current reduction for FB-Divider 01, Current reduction for FB-Divider by about 20% 10, Current reduction for FB-Divider by about 30%	EEPROM
16	BIAS_DIV_FB<1>			
17	BIAS_DIV89<0>	Output Divider 8 and 9	When BIAS_DIV89<1:0> = 00, No current reduction for all output-divider 01, Current reduction for all output-divider by about 20% 10, Current reduction for all output-divider by about 30%	EEPROM
18	BIAS_DIV89<1>			
19	AUXINVBB	AUX Buffer	If Set to 1 it Biases AUX Input Negative Pin with internal VCXOVBB voltage.	EEPROM
20	DIS_AUX_Y9		If Set to 1 AUX in input Mode Buffer is disabled. If Set to 0 it follows the behavior of FB_MUX_SEL and OUT_MUX_SEL bits settings.	
21	PECL9HISWING	Output 9	High Output Voltage Swing in LVPECL/LVDS Mode if set to 1	EEPROM
22	RESERVED			EEPROM
23	RESERVED			EEPROM
24	OUTBUF9CD2LX	CD2 Low	Output Buffer 9 Signaling Selection when CD2 in low (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
25	OUTBUF9CD2LY			
26	OUTBUF9CD2HX	CD2 High	Output Buffer 9 Signaling Selection when CD2 in high (X,Y) = 01: LVPECL, 11: LVDS, 00: LVCMOS, 10: Output Disable	EEPROM
27	OUTBUF9CD2HY			

Register 10 Address 0x0A: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	M0	Reference (PRI/SEC) Divider M	Reference Divider M bit 0	EEPROM
1	M1		Reference Divider M bit 1	
2	M2		Reference Divider M bit 2	
3	M3		Reference Divider M bit 3	
4	M4		Reference Divider M bit 4	
5	M5		Reference Divider M bit 5	
6	M6		Reference Divider M bit 6	
7	M7		Reference Divider M bit 7	
8	M8		Reference Divider M bit 8	
9	M9		Reference Divider M bit 9	
10	M10		Reference Divider M bit 10	
11	M11		Reference Divider M bit 11	
12	M12		Reference Divider M bit 12	
13	M13		Reference Divider M bit 13	
14	N0	VCXO/AUX/SEC Divider N	VCXO Divider N bit 0	EEPROM
15	N1		VCXO Divider N bit 1	
16	N2		VCXO Divider N bit 2	
17	N3		VCXO Divider N bit 3	
18	N4		VCXO Divider N bit 4	
19	N5		VCXO Divider N Bit 5	
20	N6		VCXO Divider N Bit 6	
21	N7		VCXO Divider N Bit 7	
22	N8		VCXO Divider N Bit 8	
23	N9		VCXO Divider N Bit 9	
24	N10		VCXO Divider N Bit 10	
25	N11		VCXO Divider N Bit 11	
26	N12		VCXO Divider N Bit 12	
27	N13		VCXO Divider N Bit 13	

Register 11 Address 0x0B: CD Mode

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	POWER UP CONDITION
0	PRI_DIV2	Input Buffers	If set to 1 Enables Primary Reference Divide by 2	EEPROM
1	SEC_DIV2	Input Buffers	If set to 1 Enables Secondary Reference Divide by 2	EEPROM
2	FB_DIS	FB Path Integer Counter 32	When set to 0, FB divider is active When set to 1, FB divider is disabled	EEPROM
3	FB_CML_SEL	FB Path Integer Counter 32	When set to 0, FB clock is CMOS type When set to 1, FB clock is CML type and uses CML2CMOS converter in PLL	EEPROM
4	FB_INCLK_INV	FB-Divider / Deterministic Blocks	When set to 0, Input clock for FB not inverted (normal mode, low speed) When set to 1, Input clock for FB inverted (higher speed mode)	EEPROM
5	FB_COUNT32_0	FB Path Integer Counter 32 (P divider)	Feedback Counter Bit0	EEPROM
6	FB_COUNT32_1		Feedback Counter Bit1	
7	FB_COUNT32_2		Feedback Counter Bit2	
8	FB_COUNT32_3		Feedback Counter Bit3	
9	FB_COUNT32_4		Feedback Counter Bit4	
10	FB_COUNT32_5		Feedback Counter Bit5	
11	FB_COUNT32_6		Feedback Counter Bit6	
12	FB_PHASE0	FB Path Integer Counter 32 (P Divider)	Feedback Phase Adjust Bit0	EEPROM
13	FB_PHASE1		Feedback Phase Adjust Bit1	
14	FB_PHASE2		Feedback Phase Adjust Bit2	
15	FB_PHASE3		Feedback Phase Adjust Bit3	
16	FB_PHASE4		Feedback Phase Adjust Bit4	
17	FB_PHASE5		Feedback Phase Adjust Bit5	
18	FB_PHASE6		Feedback Phase Adjust Bit6	
19	PD_PLL	PLL	If set to 0, PLL is in normal mode If set to 1, PLL is powered down	EEPROM
20	FB_MUX_SEL Table 10	Clock Tree and Deterministic Block	When set to 0, the VCXO Clock is selected for the Clock Tree and FB-Div/Det When set to 1, the AUX Clock is selected for the Clock Tree and FB-Div/Det.	EEPROM
21	OUT_MUX_SEL Table 10		If Set to 0 it selects the VCXO Clock and if Set to 1 it selects the AUX Clock	EEPROM
22	*FB_SEL*	*Diagnostics*	*Feed Back Path Selects FB/VCXO-Path when set to 0 (TI Test-GTME)* *The Secondary Reference clock input is selected when set to 1 (TI Test-GTME)*	EEPROM
23	NRESHAPE1	Reference Selection Control	Reshapes the Reference Clock Signal 0, Disable Reshape 1	EEPROM
24	SEL_DEL1		If set to 0 it enables short delay for fast operation If Set to 1 Long Delay recommended for input references below 150Mhz.	
25	RESET_HOLD	Reset Circuitry	If set to 1 the RESET or HOLD pin acts as $\overline{\text{HOLD}}$, set to 0 it acts as $\overline{\text{RESET}}$.	EEPROM
26	EPLOCK	Status	Read only. If EPLOCK reads a 0, the EEPROM is unlocked. If EPLOCK reads a 1, then the EEPROM is locked.	EEPROM
27	EPSTATUS	Status	EEPROM Status	EEPROM

Table 10. Output Buffers Source Feed, PLL Source Feed, and AUX IN/OUTPUT 9 Selection

FB_MUX_SEL	OUT_MUX_SEL	PLL FEED AND OUTPUT FEED	AUX INPUT OR OUTPUT 9
0	0	VCXO::PLL, VCXO::Y0…Y9 and Deterministic Block	OUTPUT 9 is Enabled(1)
1	0	AUXIN::PLL, VCXO::Y0…Y8 and Deterministic Block	AUX IN is Enabled
0	1	VCXO::PLL, AUXIN::Y0…Y8 and Deterministic Block	AUX IN is Enabled
1	1	AUXIN::PLL, AUXIN::Y0…Y8 and Deterministic Block	AUX IN is Enabled

(1) Default

INTERFACE, CONFIGURATION, AND CONTROL

The CDCE72010 is designed to support various applications with SPI bus interface and without. In the case where systems lack the SPI bus or a Boot up configuration is required at start up before the management layer is up the built in EEPROM is used to provide this function.

The Interface bus takes the serialized address and data and writes to the specified Register bits. The content of the RAM bits are connected to logical functions in the device. Changing the content of the Register bits (high or low) instantly changes the logical functions inside the device.

At power up or after power down is de-asserted the contents of the EEPROM bits are copied to their corresponding Register bits. After that the content of Register can be changed via the SPI bus. When writing to EEPROM commands are detected on the SPI bus the control logic begins writing the content of the Register bits into the corresponding EEPROM bits. This process takes about 50ms. During this time the power supply should be above 3.2V.

The on-chip EEPROM can be operated in its unlocked or locked mode. An unlocked EEPROM indicates that the stored bit values can be changed on another EEPROM write sequence (available for up to a 100 EEPROM write sequences). A locked EEPROM indicates that the stored bit values cannot be changed on another EEPROM write sequence.

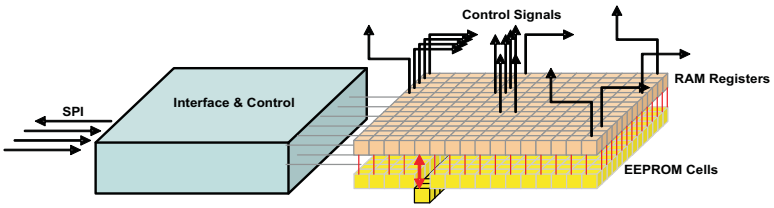


Figure 20. Interface Control

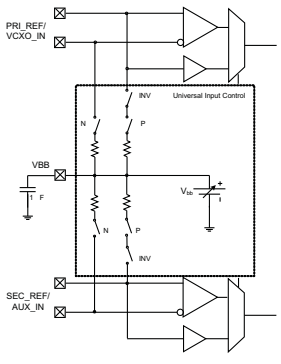
UNIVERSAL INPUT AND REFERENCE CLOCK BUFFERS

The CDCE72010 is designed to support what is referred to as a Universal Input Buffer structure. This type of buffer is designed to accept Differential or single ended inputs and it is sensitive enough to act as a LVPECL or LVDS in differential mode and LVCMOS in Single ended mode. With the proper external termination various types of inputs signals can be supported.

The CDCE72010 has two internal voltage biasing circuitries. One to set the termination voltage for references (PRI_REF and SEC_REF) and the second biasing circuitry is to set the termination voltage to the VCXO_IN and AUX_IN. This means that we can only have one type of differential signal on PRI_REF and SEC_REF and only one type of differential signal on VCXO_IN and AUX_IN.

PRE_REF & SEC_REF Input Buffer Settings

Settings						Configuration				
0.0	0.1	1.0	1.1	1.2	1.3/4	Hyst	Mode	Coup	Term	Vbb
0	0	X	1	X	X	ON	LVCMOS	DC	N/A	--
1	0	0	1	0	0	ON	LVPECL	AC	Internal	1.9V
1	0	1	1	0	0	ON	LVPECL	DC	Internal	1.2V
1	0	X	1	1	X	ON	LVPECL	--	External	--
1	1	0	1	0	0	ON	LVDS	AC	Internal	1.2V
1	1	1	1	0	0	ON	LVDS	DC	Internal	1.2V
1	1	X	1	1	X	ON	LVDS	--	External	--
X	X	X	0	X	X	OFF	--	--	--	--
X	X	X	1	X	X	ON	--	--	--	--



PRE_REF Buffer Settings

Register / Bits				Switch		
0.0	0.1	1.2	1.3	P	N	INV
0	0	X	X	O	O	O
X	X	1	X	O	O	O
X	1	0	0	C	C	C
X	1	0	1	C	C	O

SEC_REF Buffer Settings

Register / Bits				Switch		
0.0	0.1	1.2	1.4	P	N	INV
0	0	X	X	O	O	O
X	X	1	X	O	O	O
X	1	0	0	C	C	C
X	1	0	1	C	C	O

O - OPEN **C** - CLOSED

Figure 21. CDCE72010 REF Voltage Biasing Circuitry

VCXO & AUX Input Buffer Settings

Settings						Configuration				
8.0	8.1	8.2	8.3	8.4	8.5/9.19	Hyst	Mode	Coup	Term	Vbb
0	0	X	1	X	X	ON	LVCMOS	DC	N/A	--
1	0	0	1	0	0	ON	LVPECL	AC	Internal	1.9V
1	0	1	1	0	0	ON	LVPECL	DC	Internal	1.2V
1	0	X	1	1	X	ON	LVPECL	--	External	--
1	1	0	1	0	0	ON	LVDS	AC	Internal	1.2V
1	1	1	1	0	0	ON	LVDS	DC	Internal	1.2V
1	1	X	1	1	X	ON	LVDS	--	External	--
X	X	X	0	X	X	OFF	--	--	--	--
X	X	X	1	X	X	ON	--	--	--	--

AUX_IN Input Buffer Settings

Register / Bits				Switch		
8.0	8.1	8.4	9.19	P	N	INV
0	0	X	X	O	O	O
X	X	1	X	O	O	O
X	1	0	0	C	C	C
X	1	0	1	C	C	O

VCXO Input Buffer Settings

Register / Bits				Switch		
8.0	8.1	8.4	8.5	P	N	INV
0	0	X	X	O	O	O
X	X	1	X	O	O	O
X	1	0	0	C	C	C
X	1	0	1	C	C	O

O - OPEN **C** - CLOSED

NOTE: Using INV switch, negative input can be biased properly (either 1.2V or 1.9V) and single ended clock signal (whose common mode is already set to either 1.2V for LVDS clock or 1.9V for LVPECL clock) can be applied to positive input.

Figure 22. CDCE72010 Inputs Configuration

AUTOMATIC/MANUAL REFERENCE CLOCK SWITCHING (SMART MUX)

The CDCE72010 supports two reference clock inputs, the primary clock input, PRI_REF, and the secondary clock input, SEC_REF. The clocks can be selected manually or automatically. The respective mode is selected by the dedicated register. In the manual mode the external REF_SEL signal selects one of the two input clocks

In the automatic mode the primary clock is selected by default even if both clocks are available. In case the primary clock is not available or fails, then the input switches to the secondary clock until the primary clock is back. The figure below shows the automatic clock selection.

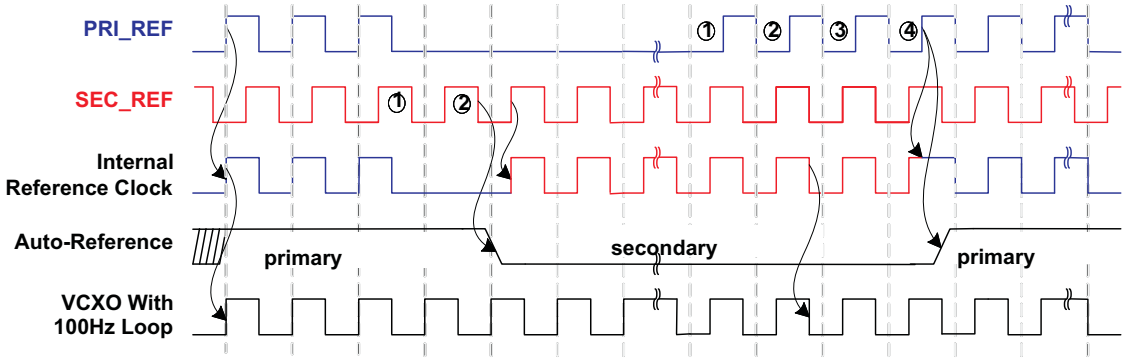


Figure 23. Automatic Clock Select Timing

In the automatic mode the frequencies of both clock signals has to be similar but may differ by up to 20%. There is no limitation placed on the phase relationship between the two inputs.

The clock input circuitry is designed to suppress glitches during switching between the primary and secondary clock in the manual and automatic mode. This insures that the clock outputs continue to clock reliably when a transition from a clock input occurs.

The phase of the output clock will slowly follow the new input phase. The speed of this transition is determined by the loop bandwidth. However, there is no phase build-out function supported (like in SONET/SDH applications).

PHASE FREQUENCY DETECTOR

The main function of the CDCE72010 device is to synchronize a Voltage Control Oscillator (VCO) or a Voltage Control Crystal Oscillator (VCXO) output to a reference clock input. The phase detector compares 2 signals and outputs the difference between them. It is symbolized by an XOR. The compared signals are derived from the Reference clock and from the VCO/VCXO clocks. The Reference clock is divided by the “R” Divider (1 or 2) and “M” divider (14 Bits) and presented to the PFD. The VCO/VCXO clock is divided by the Feedback Divider “P” (1 to 80) and the “N” Divider (14 Bits) and presented to the PFD.

Frequency (VCXO_IN or AUX_IN) / Frequency (PRI_REF or SEC_REF) = (P*N)/(R*M)

The PFD is a classical style with UP and DOWN signals generating flip-flops and a common reset path. Some special functions were implemented:

- Bit CP_DIR (register 0 bit<9> can swap internally the REF- and FB-CLK inputs to the PFD flip-flops.
- The reset path can be typically delayed with the bits DELAY_PFD <1:0> (register 0 bit<7:6>) from 1.5ns to 6.0ns.

PFD Pulse Width Delay (Register 0 Bits [7:6])

The “PFD pulse width delay” gets around the dead zone of the PFD transfer function and reduces phase noise and reference spurs.

Table 11. PFD Pulse Width Delay

PFD1	PFD0	PFD PULSE WIDTH DELAY
0	0	1.5ns(1)
0	1	3.0ns
1	0	4.5ns
1	1	6.0ns

(1) Default

The PFD receives two clocks of the similar frequencies and decides if one is lagging or leading. This Lagging/Leading signals are feed to the Charge Pump. The Charge Pump in its turn takes the Lagging/Leading signals and translate them into current pulses that are feed to the external filter. The Output of the external filter is a DC level that controls the Voltage reference of the VCO/VCXO sitting outside and feeding the CDCE72010 at the VCXO Input. The VCO/VCXO drifts its outputs frequency with respect to the voltage applied to its Voltage Control pin. This is how the loop is closed.

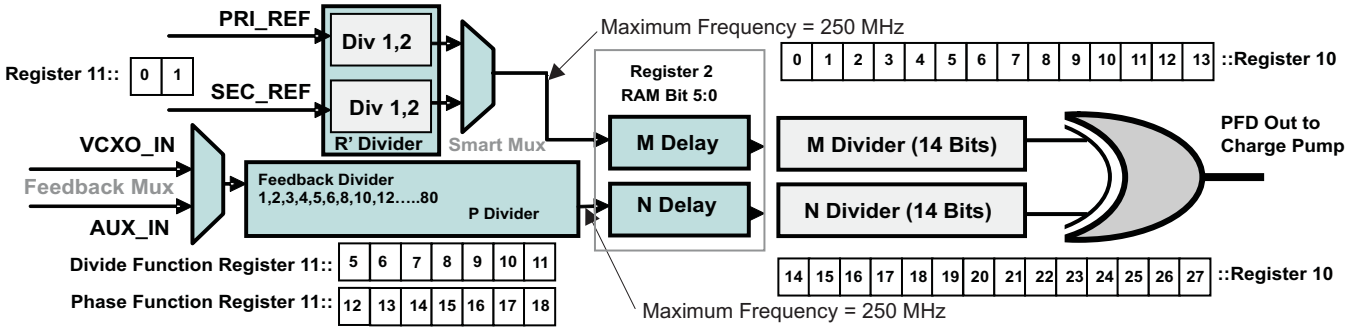


Figure 24. Phase Frequency Detection

Table 12. Feedback Divider Settings

FEEDBACK DIVIDER SETTINGS (REGISTER 11: BITS)							DIVIDER SETTING
11	10	9	8	7	6	5	
0	1	0	0	0	0	0	1
1	0	0	0	0	0	0	2
1	0	0	0	0	0	1	3
1	0	0	0	0	1	0	4
1	0	0	0	0	1	1	5
0	0	0	0	0	0	0	4'
0	0	0	0	0	0	1	6
0	0	0	0	0	1	0	8
0	0	0	0	0	1	1	10
0	0	0	0	1	0	0	8'
0	0	0	0	1	0	1	12
0	0	0	0	1	1	0	16
0	0	0	0	1	1	1	20
0	0	0	1	0	0	0	12'
0	0	0	1	0	0	1	18
0	0	0	1	0	1	0	24
0	0	0	1	0	1	1	30
0	0	0	1	1	0	0	16'
0	0	0	1	1	0	1	24'
0	0	0	1	1	1	0	32
0	0	0	1	1	1	1	40
0	0	1	0	0	0	0	20'
0	0	1	0	0	0	1	30'
0	0	1	0	0	1	0	40'
0	0	1	0	0	1	1	50
0	0	1	0	1	0	0	24'
0	0	1	0	1	0	1	36
0	0	1	0	1	1	0	48
0	0	1	0	1	1	1	60
0	0	1	1	0	0	0	28
0	0	1	1	0	0	1	42
0	0	1	1	0	1	0	56
0	0	1	1	0	1	1	70
0	0	1	1	1	0	0	32'
0	0	1	1	1	0	1	48'
0	0	1	1	1	1	0	64
0	0	1	1	1	1	1	80

PHASE DELAY FOR M AND N

Delay Block in M/N Path

Table 13. Reference Delay M (PRI_REF or SEC_REF) and Feedback Delay N (VCXO) Phase Adjustment (Register 2 Bits [5:0]) (1)

DLYM2/DLYN2	DLYM1/DLYN1	DLYM0/DLYN0	PHASE OFFSET
0	0	0	0ps(2)
0	0	1	±160ps
0	1	0	±320ps
0	1	1	±480ps
1	0	0	±830ps
1	0	1	±1130ps
1	1	0	±1450ps
1	1	1	±1750ps

(1) If Progr Delay M is set, all Yx outputs are lagging to the Reference Clock according to the value set. If Progr Delay N is set, all Yx outputs are leading to the Reference Clock according to the value set. Above are typical values at V_{CC} = 3.3 V, T_A = 25°C, PECL-output relate to Div4 mode.
(2) Default

Table 14. Input and Feedback Divider: 14-Bit (Register 10 Bits [13:0] for M and Bits [27:14] for N)

N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	DIV BY(1)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	0	1	1	4
								• • •						
0	0	0	0	0	0	0	1	1	1	1	1	0	0	125(2)
								• • •						
1	1	1	1	1	1	1	1	1	1	1	1	0	1	16382
1	1	1	1	1	1	1	1	1	1	1	1	1	0	16383
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16384

(1) If the divider value is Q, then the code will be the binary value of (Q - 1).
(2) Factory EEPROM Default values M = 125 and N = 768

CHARGE PUMP

The Charge Pump drives the loop filter that controls the external VCO/VCXO. The Charge pump operates at the PFD frequency since the function of the charge pump is to translate the UP DOWN signals of the PFD into current pulses that drives the external filter. The Charge pump current is set by the control vector ICP [3:0].

Table 15. CP, Charge Pump Current (Register 0 RAM Bits [17:14])

ICP3	ICP2	ICP1	ICP0	TYPICAL CHARGE PUMP CURRENT
0	0	0	0	0 µA (3-State)
0	0	0	1	200 µA
0	0	1	0	400 µA
0	0	1	1	600 µA
0	1	0	0	800 µA
0	1	0	1	1.0 mA
0	1	1	0	1.2 mA
0	1	1	1	1.4 mA
1	0	0	0	1.6 mA
1	0	0	1	1.8 mA
1	0	1	0	2.0 mA
1	0	1	1	2.2 mA(1)
1	1	0	0	2.4 mA
1	1	0	1	2.6 mA
1	1	1	0	2.8 mA
1	1	1	1	3.0 mA

(1) Default

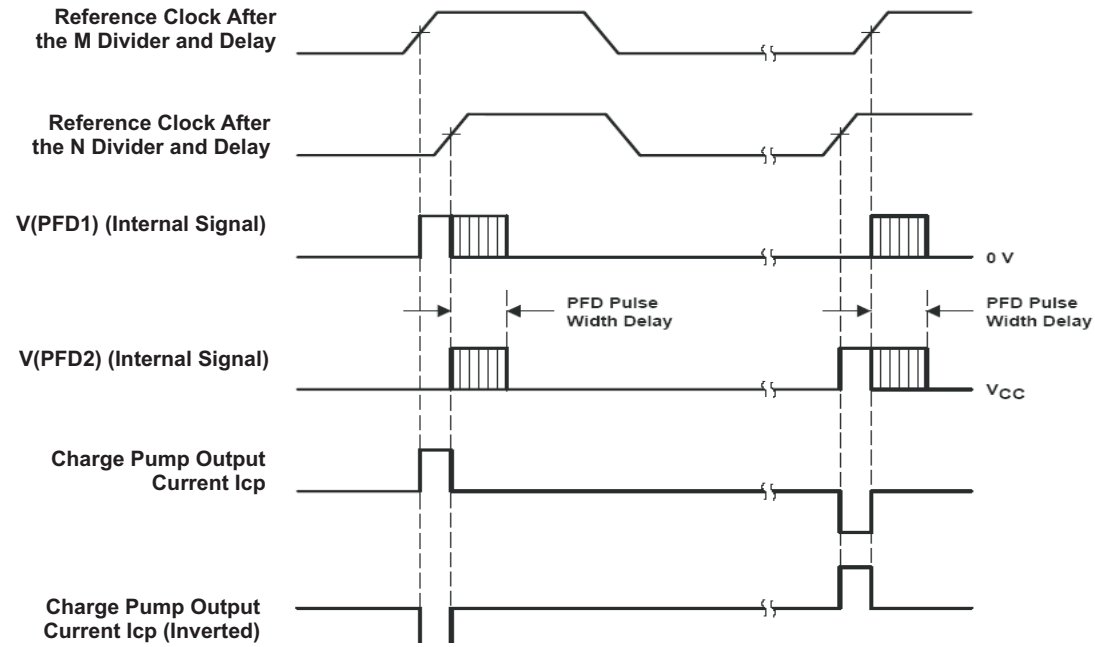
The CP_PRE register bit R0.13 is a useful feature to quickly set the center frequency of the VC(X)O after Power-up or Reset. The adequate control voltage for the VC(X)O will be provided to the Charge-Pump output by an internal voltage divider of 1KΩ/1KΩ to V_{CC_CP} and GND (V_{CC_CP}/2). The CP_PRE register bit must be reset to "0" in order for the PLL to achieve lock.

This feature helps to get the initial frequency accuracy, i.e. required at CPRI (Common Public Radio Interface) or OBSAI (Open Base Station Architecture Initiative).

The Preset Charge-Pump to V_{CC_CP}/2 can be set and reset by register.

Charge-Pump Current Direction

The direction of the charge-pump (CP) current pulse can be changed by the register settings. It determines in which direction CP current will regulate (Reference Clock leads to Feedback Clock). Most applications use the positive CP output current (power-up condition) because of the use of a passive loop filter. The negative CP current is useful when using an active loop filter concept with inverting operational amplifier. The Figure below shows the internal PFD signal and the corresponding CP current.



PFD pulse width delay improves spurious suppression.

Figure 25. Charge Pump

PLL LOCK FOR ANALOG AND DIGITAL DETECT

The CDCE72010 supports two PLL Lock indications: the digital lock signal or the analog lock signal. Both signals indicate logic high-level at PLL_LOCK if the PLL locks according the selected lock condition.

The PLL is locked (set high), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD (Phase Frequency Detect) are inside a predefined lock detect window for a pre-defined number of successive clock cycles.

The PLL is out-of-lock (set low), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD are outside the predefined lock detect window.

Both, the lock detect window and the number of successive clock cycles are user definable in the register settings.

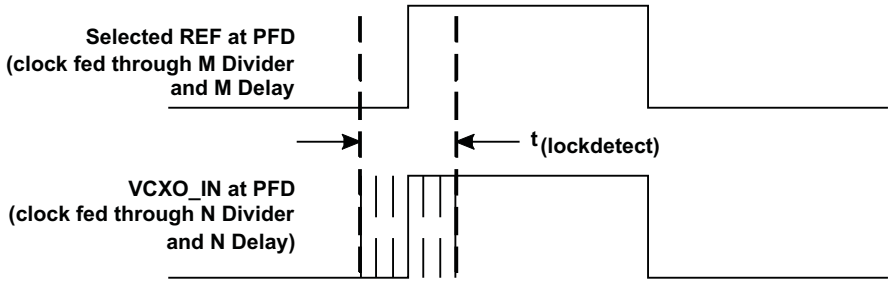


Figure 26. PLL Lock

The lock detect window describes the maximum allowed time difference for lock detect between the rising edge of PRI_REF or SEC_REF and VCXO_IN. The time difference is detected at the phase frequency detector. The rising edge of PRI_REF or SEC_REF is taken as reference. The rising edge of VCXO_IN is outside the lock detect window, if there is a phase displacement of more than $+0.5*t_{(lockdetect)}$ or $-0.5*t_{(lockdetect)}$.

Table 16. Lock-Detect Window (Register 7 Bits [1:0] and Register 9 Bits [7:6])

LOCKW3 [7]	LOCKW2 [6]	LOCKW1 [1]	LOCKW0 [0]	PHASE-OFFSET AT PFD-INPUT(1)
0	0	0	0	1.5 ns
0	0	0	1	5.8 ns(2)
0	0	1	0	15.1 ns
0	0	1	1	Reserved
0	1	0	0	3.4 ns
0	1	0	1	7.7 ns
0	1	1	0	17.0 ns
0	1	1	1	Reserved
1	0	0	0	5.4 ns
1	0	0	1	9.7 ns
1	0	1	0	19.0 ns
1	0	1	1	Reserved
1	1	0	0	15.0 ns
1	1	0	1	19.3 ns
1	1	1	0	28.6 ns
1	1	1	1	Reserved

(1) Typical values at V_{CC} = 3.3 V, T_A = 25°C
(2) Default

Table 17. Number of Successive Lock Events Inside the Lock Detect Window (Register 7 Bits [4:3]) the PLL Lock Signal is Delayed for Number of FB_CLK Events

LOCKC1	LOCKC0	NO. OF SUCCESSIVE LOCK EVENTS
0	0	1
0	1	16
1	0	64 (1)
1	1	256

(1) Default

DIGITAL LOCK DETECT

When selecting the digital PLL lock option, PLL_LOCK will possibly jitter several times between lock and out of lock until a stable lock is detected. A single “low-to-high” step can be reached with a wide lock detect window and high number of successive clock cycles. PLL_LOCK will return to out of lock if just one cycle is outside the lock detect window.

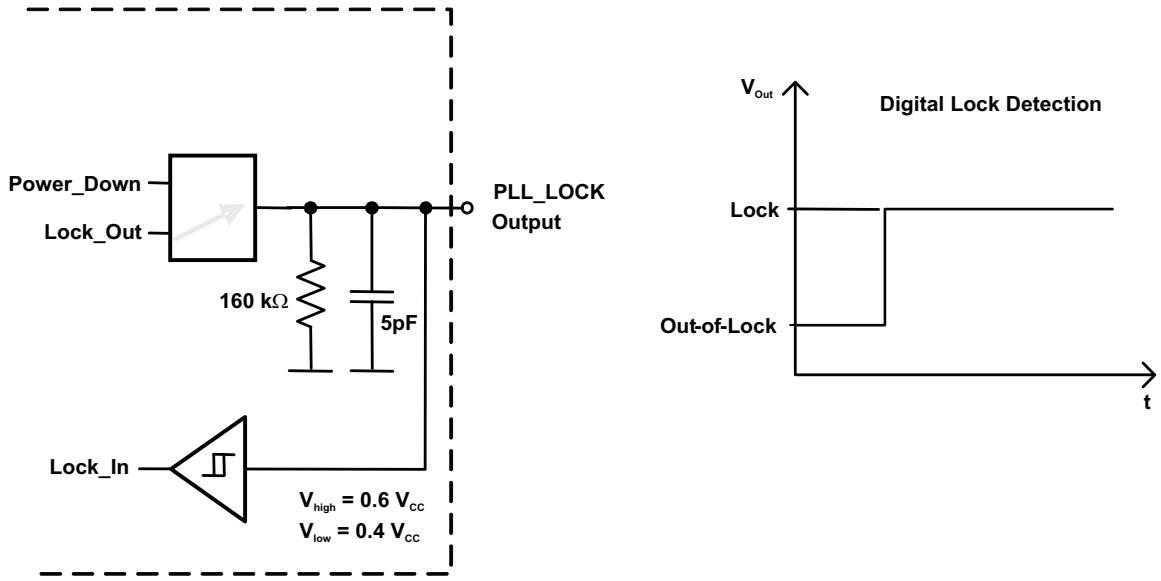


Figure 27. Digital Lock

ANALOG LOCK DETECT

When selecting the analog PLL Lock option, the high-pulses load the external capacitor via the internal 110 µA current source until logic high-level is reached. Therefore, more time is needed to detect logic high level, but jittering of PLL_LOCK will be suppressed like possible in case of digital lock. The time PLL_LOCK needs to return to out of lock depends on the level of V_{OUT}, when the current source starts to unload the external capacitor.

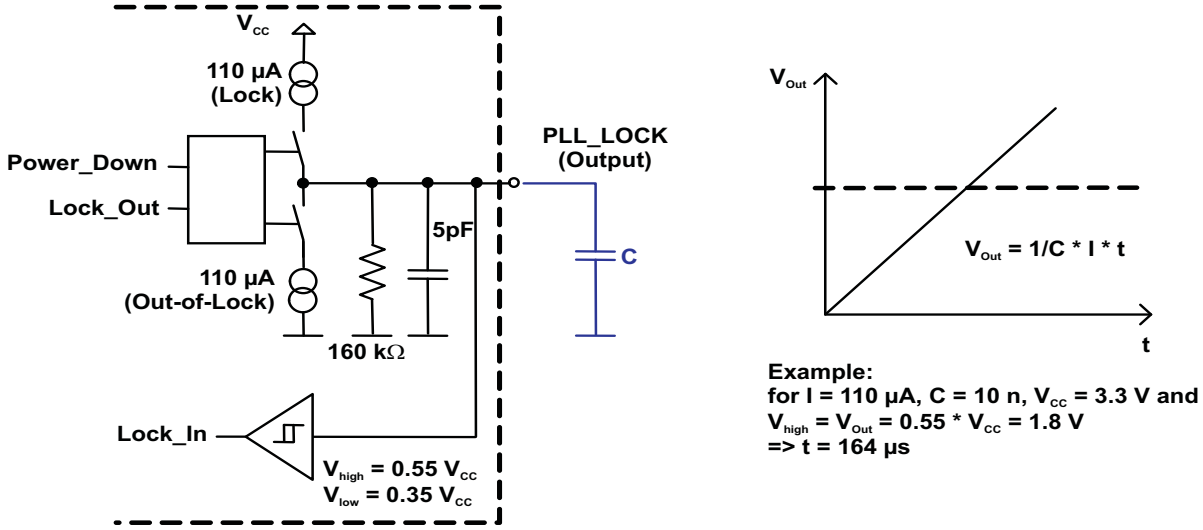


Figure 28. Analog Lock

FREQUENCY HOLD-OVER MODE

The HOLD-Function is a CDCE72010 feature that helps to improve system reliability. The HOLD-Function holds the output frequency in case the input reference clock fails or is disrupted. During HOLD, the Charge-Pump is switched off (3-State) freezing the last valid output frequency. The Hold-Function will be released after a valid reference clock is reapplied to the clock input and detected by the CDCE72010. For proper HOLD function, the Analog PLL-Lock-Detect mode has to be active. The following settings are involved with the HOLD Function:

- Lock Detect Window: Defines the window in ns inwhich the Lock is valid. The size is 3.5ns, 8.5ns, 18.5ns. Lock is set if Reference Clock and Feedback Clock are inside this predefined Lock-Detect Window for a pre-selected number of successive cycles.
- Out-of-Lock: Defines the out-of-lock condition: If the Reference Clock and the Feedback Clock at the PFD are outside the predefined Lock Detect Window.
- Number of Clock Cycles: Defines the number of successive PFD cycles which have to occur inside the lock window to set Lock detect. This does not apply for Out-of-Lock condition.
- Hold-Function: Selects HOLD-Function (see more details below).
- Hold-Trigger: Defines whether the HOLD-Function is always activated or whether it is dependent on the state of the analog PLL Lock detect output. In the latter case, HOLD is activated if Lock is set (high) and de-activated if Lock is reset (low).
- Analog PLL Lock Detect: Analog Lock output charges or discharges an external capacitor with every valid Lock cycle. The time constant for Lock detect can be set by the value of the capacitor.

The CDCE72010 supports two types of HOLD functions, one external controllable $\overline{\text{HOLD}}$ mode and one internal mode, HOLD.

EXTERNAL/HOLD FUNCTION

The Charge Pump can directly be switched into 3-State. This function is also available via register. If logic low is applied to $\overline{\text{HOLD}}$ pin the Charge Pump will be switched to 3-State. After $\overline{\text{HOLD}}$ pin is released, the charge pump is switched back in to normal operation, with the next valid reference clock cycle at PRI_REF or SEC_REF and the next valid feedback clock cycle at the PFD. During $\overline{\text{HOLD}}$, all divider and all outputs are at normal operation.

INTERNAL/HOLD FUNCTION

In Internal $\overline{\text{HOLD}}$ Function or HOLD-Over-Function the PLL has to be in lock to start the HOLD function. It switches the Charge Pump in to 3-State when an 'out-of-lock' event occurs. It leaves the '3-State Charge Pump' state when the Reference Clock is back. Then it starts a locking sequence of 64 cycles before it goes back to the beginning of the HOLD-Over loop.

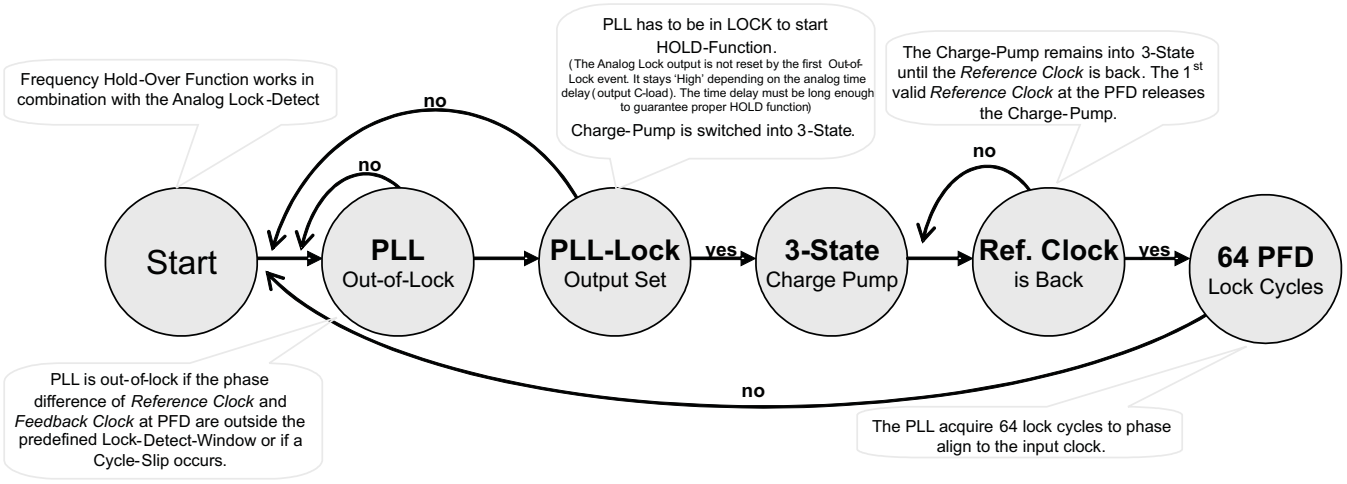


Figure 29. Frequency Hold Over

OUTPUT DIVIDERS AND PHASE ADJUST

The CDCE72010 is designed with individual Output Dividers for Outputs 1 to 8. Output Divider 1 drives Output 1 and Output 0 and Output Divider 8 drives Output 8 and Output 9. Each output divider has a bypass function or it is referred to as divide by “one”. Since divide by one bypasses the divider block it can address higher operating frequencies.

The output divider is designed to address divide by 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 50, 56, 60, 64, 70 and 80.The output divider includes a coarse phase adjust that shifts the divided clock signal. The phase adjust resolution is a function of the divide function. The maximum number of phase steps equals to the divider setting.

If the output is divide by 2, then two phase adjustment settings (0 and 180 degrees) are available. The resolution of phase adjustment is related to the output divider setting by the following: Phase adjust resolution = (1/Output Divider settings) X 360 Degrees.

Example: For a 491.52MHz VCXO where one of the outputs of the device is set to divide by 16 for a 30.72MHz desired output, this will mean that the 30.72MHz clock will have (1/16) X 360 = 22.5 Degrees of phase adjustment resolution.

Output Divide Select (OUT#DIVSEL#) and Coarse Phase Adjust Select (PH#ADJC#) registers are located in Register 1 thought 8 for Output 1 thought 8 respectively.

The Phase difference between 2 divider settings on different output can be calculated using the following formula and referring to the Phase Lag number in the Output Divider Table (see Table 8).

Integer Remainder of [(Phase Lag X - Phase Lag Y)/ Divide X] as an example if we need to calculate the phase difference between divide by 4 and divide by 8 with respect to divide by 4 clock.

The Integer Remainder [(28.5 - 0.5)/4] = 0. This means there is 0 Cycle phase delay between Divide by 4 and Divide by 8 with respect to Divide by 4 Clock.

If we need to do the same calculation with respect to Divide by 8 we will have Intger Remainder [(28.5 – 0.5)/8] = 0.5 that means that there is 0.5 Cycles between Divide by 4 and divide by 8 with respect to a divide by 8 clock.

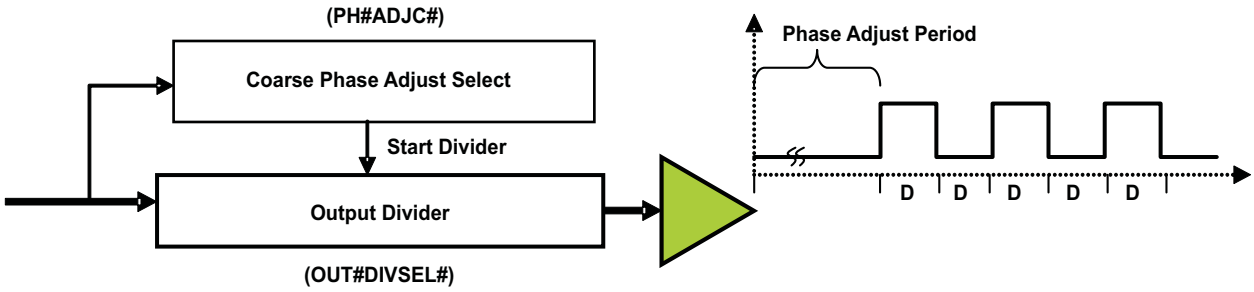


Figure 30. Maximum Output Frequency With Phase Alighment

FREQUENCY DETECTION CIRCUIT

The Frequency detector circuit can detect the input clock signal and provide the indications at STATUS pin depending on Register 12 and 3 settings (see notes in page 33). The STATUS pin will set to HIGH if a valid input clock is detected. And LOW if valid input clock is absent or missing.

The frequency detector circuit is located in between the SMART MUX and the M divider (see Figure 31).

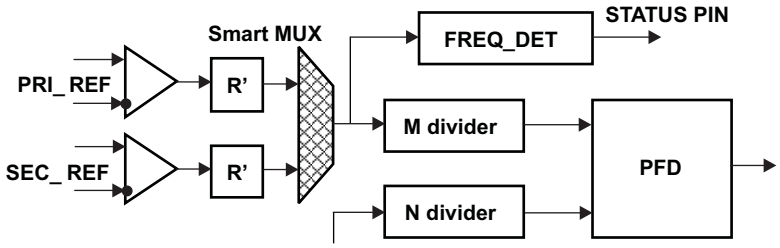


Figure 31. Location of the Frequency Detector Circuit

The detection circuit is RC-based analog circuit. The response time to detect a new clock signal is clock-frequency dependent (min. 3.125µs at 0.8MHz). With higher clock frequency the response time will be faster as well.

If the input clock goes away, the detector reports the event within 5.2 µs independent of clock frequency.

Table 18. Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Frequency detection threshold (1)	800			kHz
Response time (clock absence) (1)	2.62		5.2	µs
Response time (clock resumes) at 0.8 MHz (1)	3.125		29	µs
Clock cycles (clock resumes) at 0.8 MHz (2)	2.5		23	cycles

(1) Received values from simulation
(2) Received values from simulation

DEVICE LAYOUT

The CDCE72010 is a high performance device packaged in a QFN-64. The die has all the ground pins bounded to the thermal PAD on the bottom of the package. Therefore it is essential that the connection from the thermal PAD to the ground layers should be low impedance. In addition, the thermal path in a QFN package is via the thermal PAD on the bottom of the package. Therefore, the layout of the PAD is very important and it will affect the thermal performance as well as the overall performance of the device. The illustration shown provides optimal performance in terms of thermal issues, inductance and power supply bypassing. The 10 X 10 Filled VIA pattern recommended allows for a low inductance connection between the thermal ground pad and the ground plane of the board. This pattern forms a low thermal resistive path for the heat generated by the die to get dissipated through the ground plane and to the exposed bottom side ground pad. It is recommended that solder mask not be used on this bottom side pad to maximize its effectiveness as a thermal heat sink. The recommended layout drives the thermal conductivity to 22.8 C°/W in still air and 13.8 C°/W in a 100LFM air flow if implemented on a JEDEC compliant test thermal board.

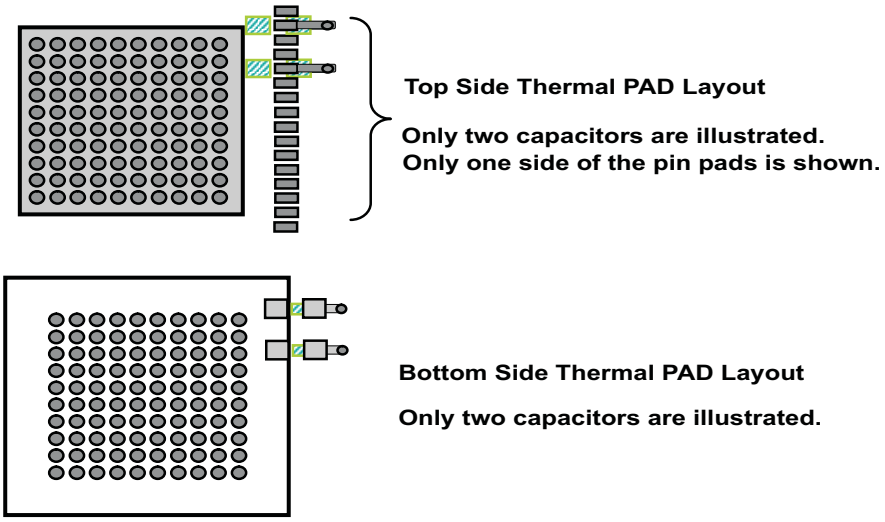


Figure 32. Device Layout

DEVICE POWER

The CDCE72010 is designed as a high performance device, therefore careful attention must be paid to device configuration with respect to power consumption. Total power consumption of the device can be estimated by adding up the total power consumed by each block in the device.

The Table below describes the blocks used and power consumed per block. The total power of the device can be calculated by multiplying the number of blocks used by the power consumption per block.

Table 19. Device Power

Internal Block Power at 3.3V (typ.)		Power Dissipation/ Block	Number of Blocks
PLL Core, Input and Feedback		530 mW	1
Output Dividers	Divider = 1	82 mW	8
	Divider > 1	180 mW	
LVPECL Output Buffer		75 mW(1)	10
LVDS Output Buffer		75 mW	10
LVCMOS Output Buffer	Static	7 mW	20
	Transient, 'C_L' load, 'f_{OUT}' MHz output frequency, 'V' output swing	$V_{DD} \times V \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	20

(1) Approximately 50 mW power dissipates externally at termination resistors per LVPECL output pair.

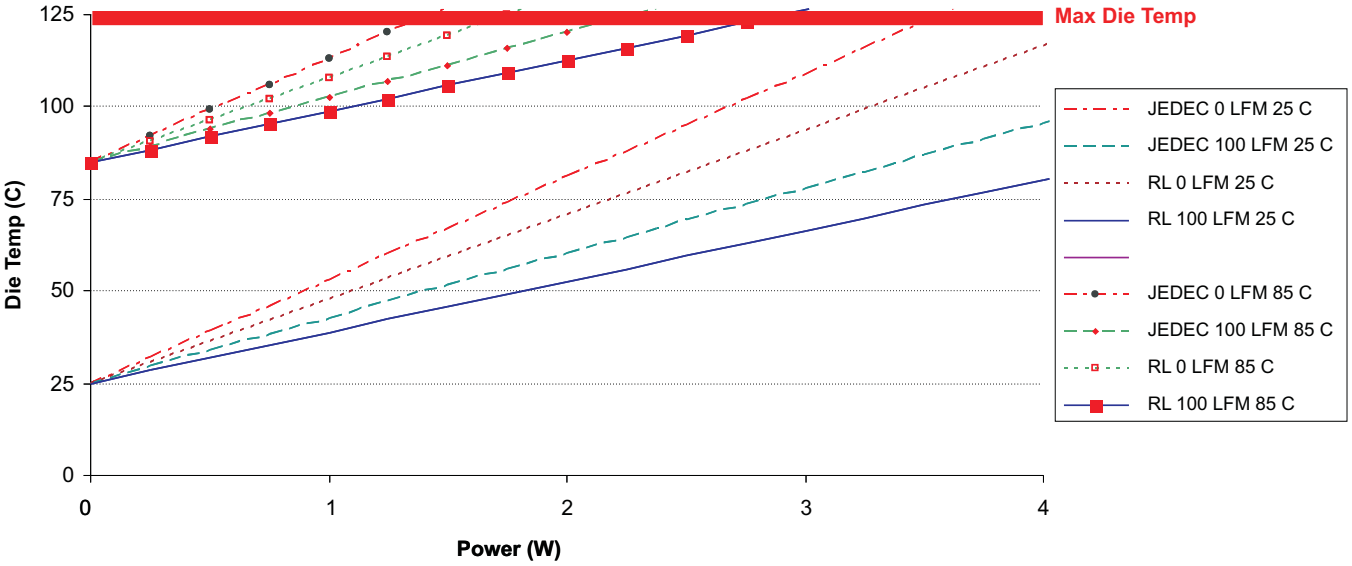


Figure 33. Die Temperature

LOOP FILTER

The CDCE72010 is designed to control an external Voltage Controlled Oscillator (VCO) or a Voltage Controlled Crystal Oscillator (VCXO) and to synchronize the controlled oscillators to the input reference. Controlling the Oscillator happens via a DC voltage that is applied to the Voltage control pin. This DC voltage is generated by the CDCE72010 in the form of AC pulses that get filtered by the external loop filter.

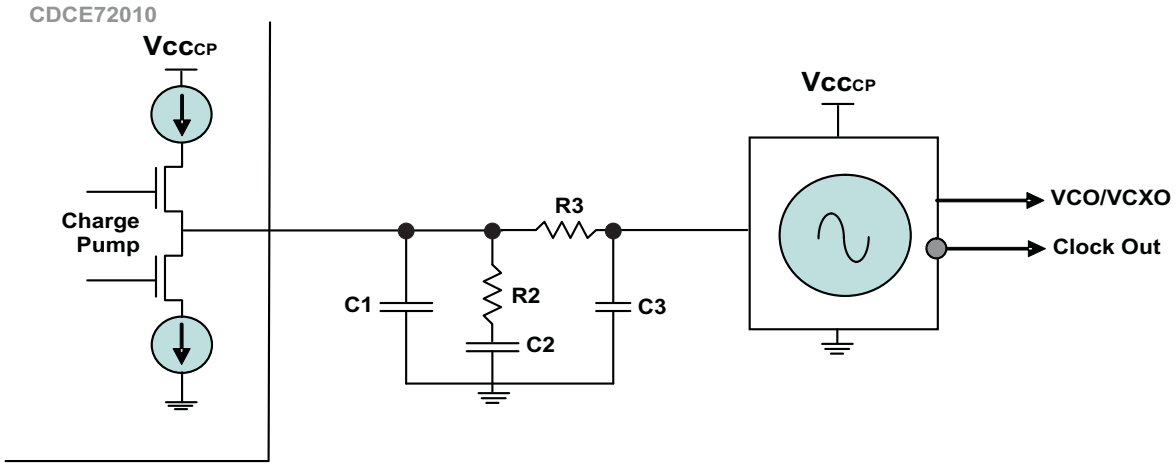


Figure 34. Loop Filter

UNIVERSAL OUTPUT BUFFERS

The CDCE72010 is designed to drive three types of clock signaling, LVPECL, LVDS, and LVCMOS from each of the ten outputs. This super buffer that contains all three drivers is refered to as the Universal Output Buffer. Only one driver can be enabled at one time. Each universal output buffer is made from four independent buffers in parallel. When LVPECL mode is selected, only the LVPECL Buffer is enabled and the rest of the buffers are 3-stated and in low power mode. When Selecting LVDS, only the LVDS Buffer is enabled and the rest of the buffers are 3-stated and in low power mode. When LVCMOS mode is selected, both LVCMOS drivers are enabled. One LVCMOS buffer drives the negative side and the other buffer drives the positive pin.

The LVCMOS drivers are driven from the same output divider but have separate control bits. In SPI Mode, bits 22, 23, 24, and 25 of Registers 0 to 9 are used to put the LVCMOS buffer in active, inverting, low, or 3-state. In CD Mode, those bits are used for different functions and the LVCMOS buffer can be active when selected or 3-state when their not.

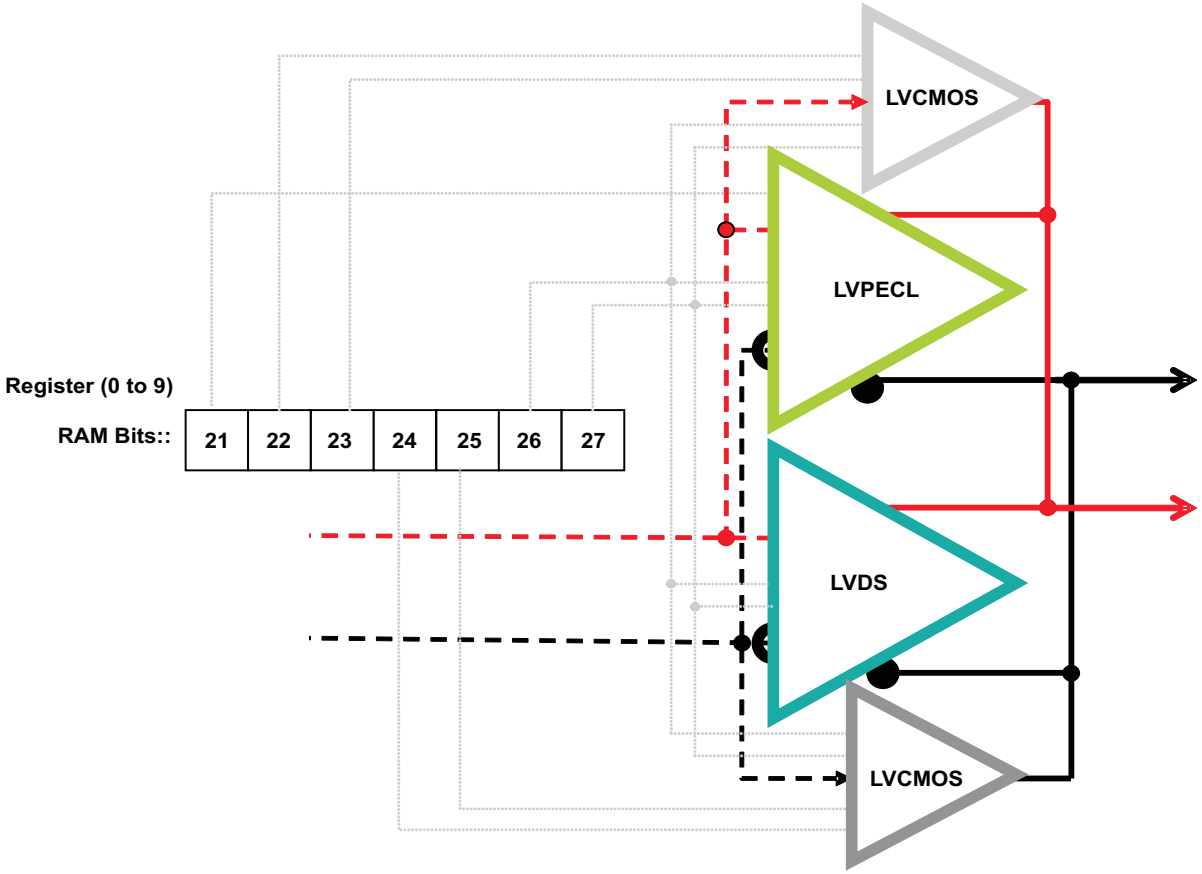


Figure 35. Universal Output Buffer

Output Dividers Synchronization

The CDCE72010 is a 10 output clock device with 8 output dividers and to insure that all the outputs are synchronous a synchronization startup circuitry is used. The synchronization circuitry generates a pulse to reset all the dividers in a way, that a predictable synchronous output is generated. The Synchronization signal can be generated from different sources and can be synchronized to a specific clock. The Block diagram below illustrates the signal path of the Output Divider Sync Signal. This function is assured up to 500 MHz.

NOTE

The minimum frequency required for the output synchronization block to work properly is 1 MHz.

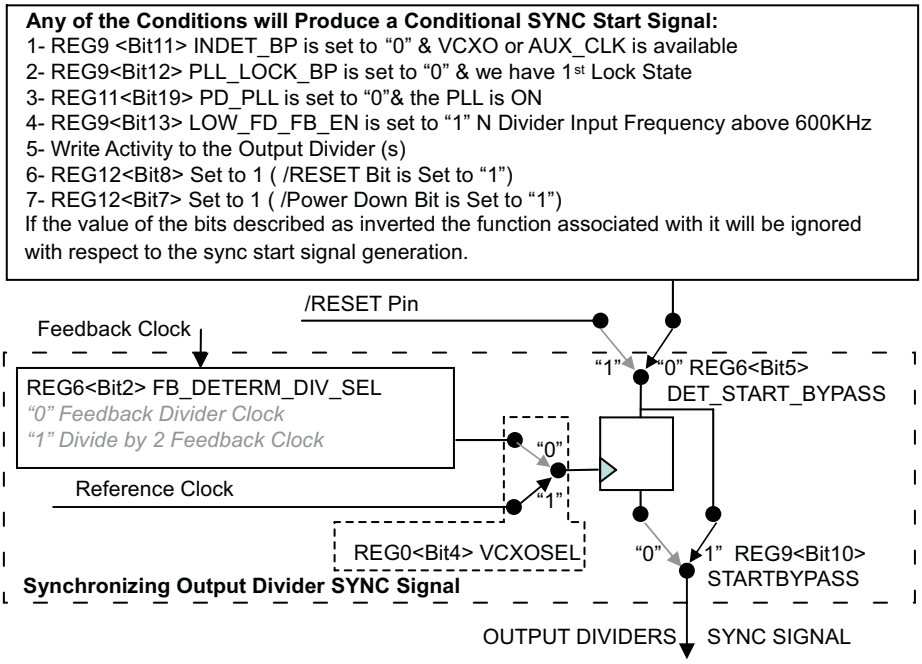


Figure 36. Output Divider Synchronization Block Diagram

POWER UP RESET, POWER DOWN MODE AND RESET OR HOLD

The CDCE72010 is designed to address various clock synchronization applications. Some functions can be set to be in automatic and manual mode or some functions can be controlled by software or by the internal circuitry.

Table 20 explains the various functionalities of power up reset internal circuitry functionality, power down functionality and reset functionality. The hold function shares the same block with Reset and one bit in the EEPROM will select either function.

Table 20. RESET_HOLD_STATE

RESET_HOLD_MODE (R11.25)	$\overline{\text{SLEEP}}$ (R12.7)	RESET_HOLD (R12.8)	RESET/HOLD (pin #33)	$\overline{\text{PD}}$ (pin #17)	MODE
X	X	X	X	0	Device in Power down. On Power down exit, register reset to EEPROM defaults.
X	0	X	X	1	Device in SLEEP Mode. It's the same as power down but upon exit of this mode, the registers will retain their previous state (no EEPROM reload).
0	1	00 01 10		1	Device in RESET. Power consumption minimized outputs tri-state. Upon exit of this mode, the registers will retain their previous state (no EEPROM reload).
1	1	00 01 10		1	Device in HOLD mode. The CP output is tri-stated.
X	1	11		1	Normal Mode.

REVISION HISTORY

Changes from Original (June 2008) to Revision A **Page**

- Changed Frequency equation result from (R*M)/(P*N) to (P*N)/(R*M) 2
- Added table note to Register 0: SPI Mode table description 24
- Changed Register 12: SPI Mode (RAM only Register) Note 36
- Added table note to Register 0:CD Mode table description 39
- Added additional information to INTERFACE, CONFIGURATION, AND CONTROL description 51
- Changed Figure 22 52
- Added “P” to PHASE FREQUENCY DETECTOR feedback divider description 53
- Changed Frequency equation from (R*M)/(P*N) to (P*N)/(R*M) 53
- Deleted P is the product of X Divider and FB Divider R and X Divider is set to be divide by 1 or 2 53
- Changed Figure 24 by adding maximum frequency = 250 MHz 53
- Added note to Output Dividers Synchronization description 68

Changes from Revision A (June 2008) to Revision B **Page**

- Changed many instances in rev B of this data sheet (major changes/additions to this data sheet) 1
- Deleted "Dedicated Charge-Pump.....VCOs" from FEATURES 1
- Changed Figure 1 2
- Changed Pin Functions table 4
- Changed Pin Functions table 5
- Changed Pin Functions table 6
- Changed Recommended Operating Conditions table 7
- Changed Timing Requirements table 8
- Changed AC/DC Characteristics table 9
- Added new section "INTERFACE AND CONTROL BLOCK" including figures/tables 19
- Changed Table 6 23
- Changed Table 6 23
- Changed text/rows in all Register tables 24
- Changed $\overline{\text{SLEEP}}$ and $\overline{\text{RESET\_HOLD}}$ 36
- Changed "Universal Input and Reference Clock Buffers" section including figures 51
- Changed Figure 21 51
- Changed Figure 22 52
- Changed tables in "PHASE DELAY for M and N" section 55
- Deleted 0 from N1 and N0 55
- Changed text in "CHARGE PUMP" section 56
- Changed text in CHARGE PUMP section 56
- Changed Table 19 65
- Changed SLEEP in Table 20 to active low 69

Changes from Revision B (August 2011) to Revision C **Page**

- Changed Pin 3 and 58 to Pin 5 and 8 in PIN FUNCTIONS note 4
- Changed in Table 6, Reg 11 from 81E09B0C to 8000058B 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCE72010RGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples
CDCE72010RGCRG4	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples
CDCE72010RGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples
CDCE72010RGCTG4	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE72010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

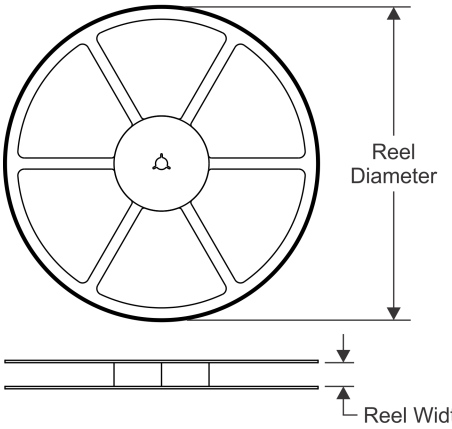
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

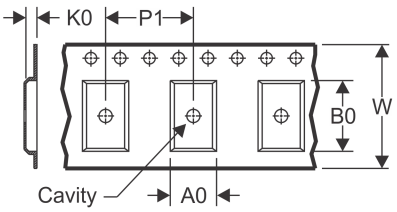
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

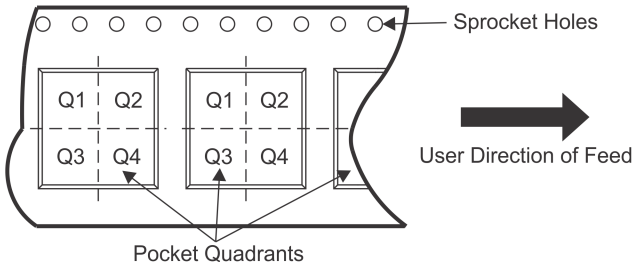


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

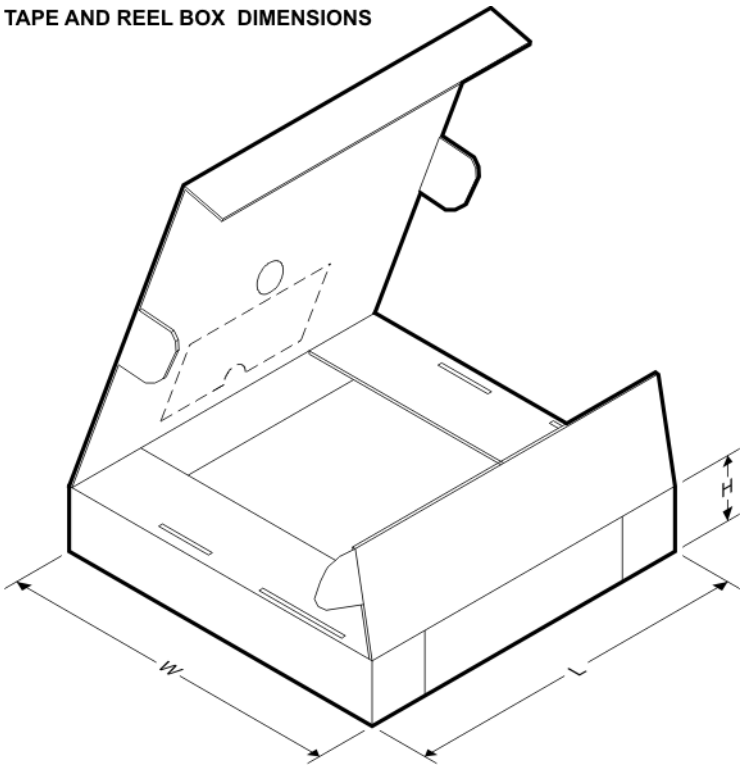
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE72010RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
CDCE72010RGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE72010RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
CDCE72010RGCT	VQFN	RGC	64	250	367.0	367.0	38.0

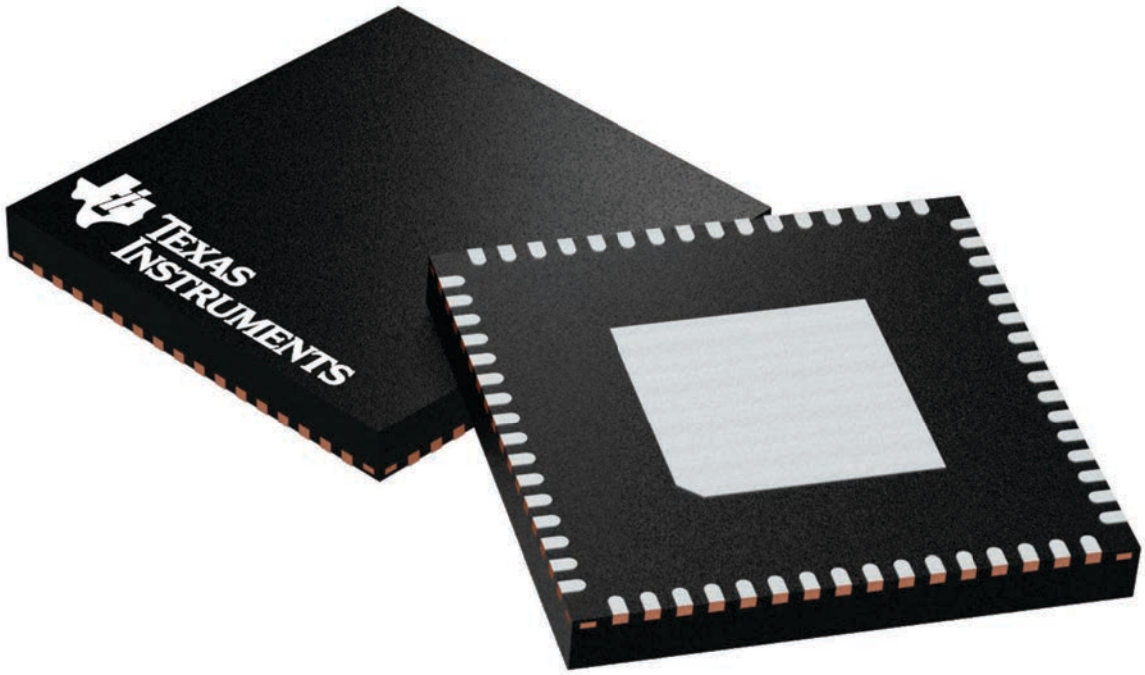
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

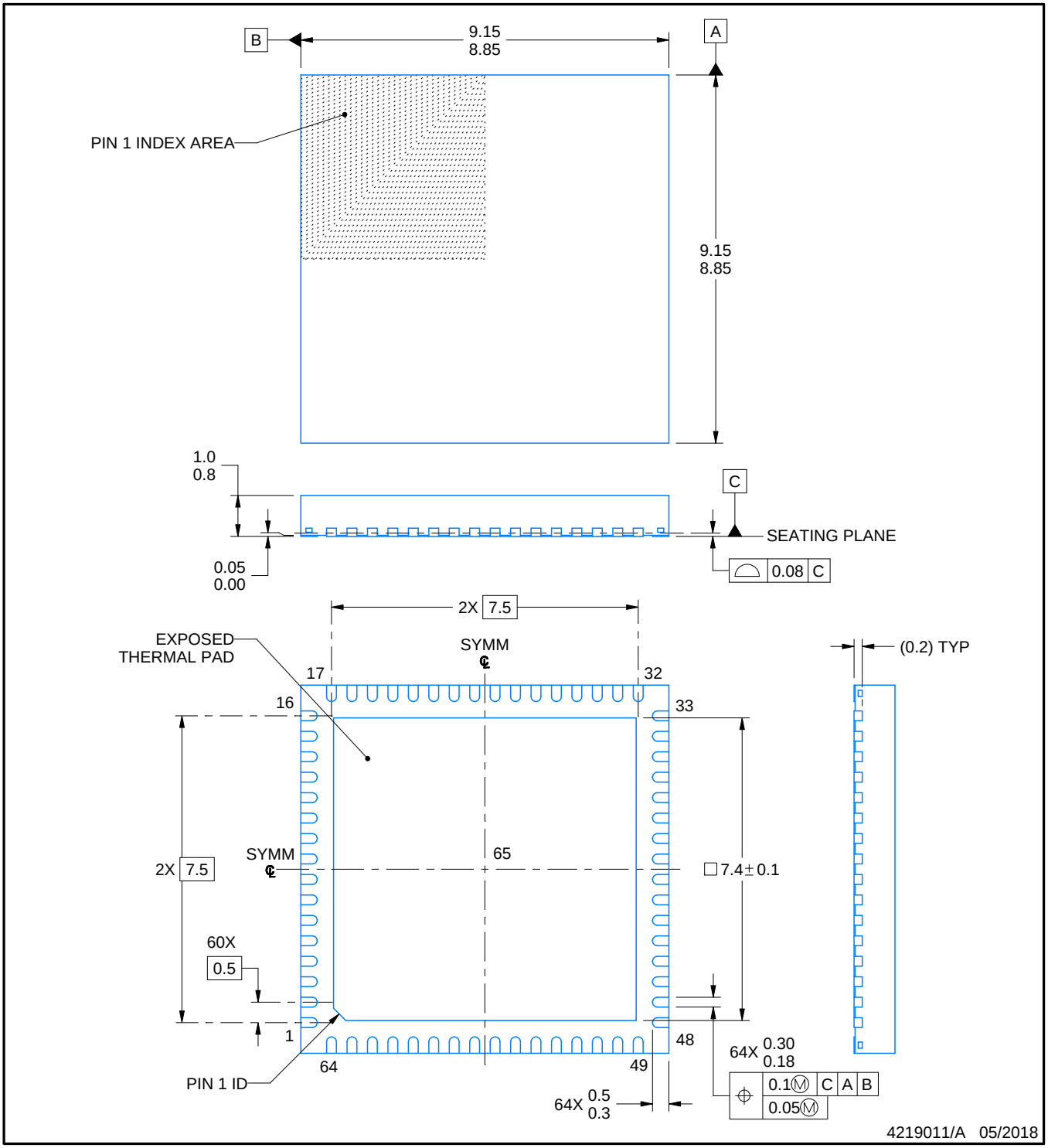
4224597/A

RGC0064H

PACKAGE OUTLINE

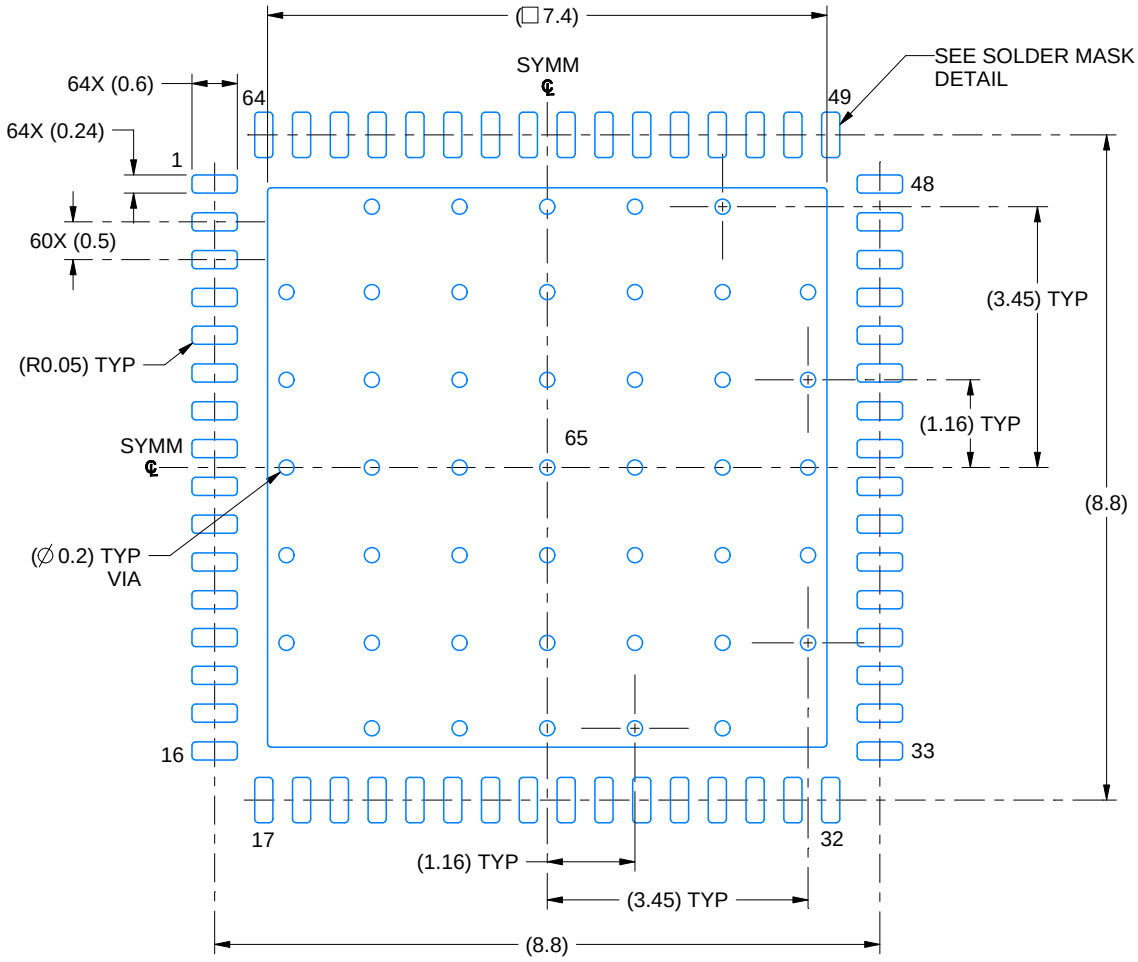
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

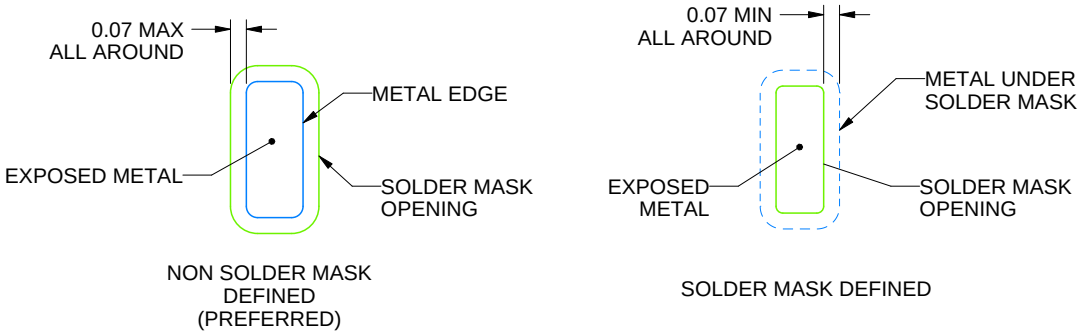


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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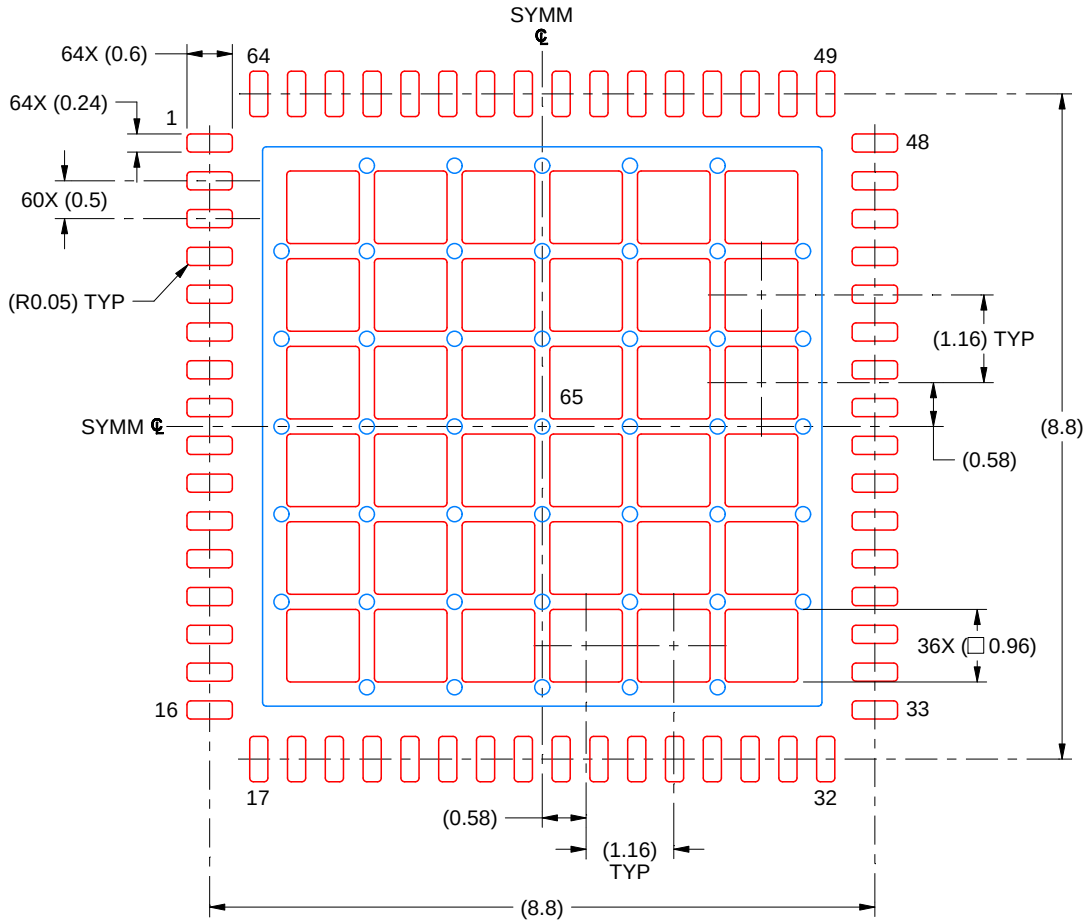
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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