



**THE DATASHEET OF
TC7920K6-G**



Two Pair, N- and P-Channel Enhancement-Mode MOSFET with Drain-Diodes

Features

- ▶ High voltage Vertical DMOS technology
- ▶ Integrated drain output high voltage diodes
- ▶ Integrated gate-to-source resistor
- ▶ Integrated gate-to-source Zener diode
- ▶ Low threshold, Low on-resistance
- ▶ Low input & output capacitance
- ▶ Fast switching speeds
- ▶ Electrically isolated N- and P-MOSFET pairs

Applications

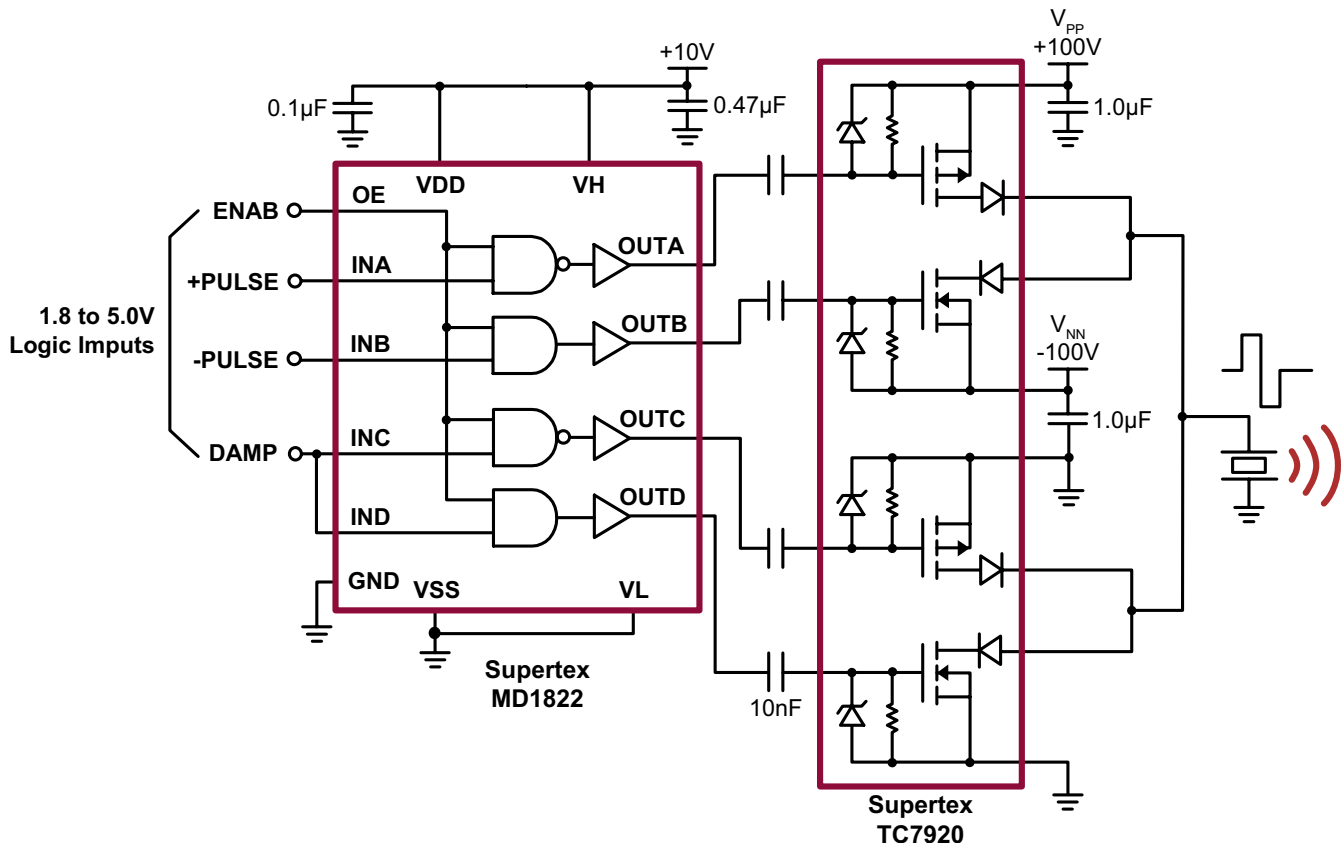
- ▶ High voltage pulsers
- ▶ Amplifiers
- ▶ Buffers
- ▶ Piezoelectric transducer drivers
- ▶ General purpose line drivers
- ▶ Logic level interfaces

General Description

The Supertex TC7920 consists of two pairs of high voltage, low threshold N-channel and P-channel MOSFETs in a 12-Lead DFN package. All MOSFETs have integrated the output drain high voltage diodes, gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high voltage pulser applications. The complimentary, high-speed, high voltage, gate-clamped N and P-channel MOSFET pairs utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices.

Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown. Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input and output capacitance, and fast switching speeds are desired.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
TC7920K6-G	12-Lead DFN	3000/Reel

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

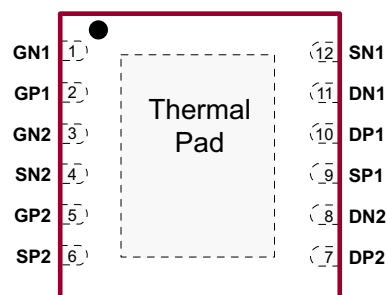
Package	θ_{ja}
12-Lead DFN	42°C/W

Note:
1.0oz, 4-layer, 3"x4" PCB.

Product Summary

BV_{DSS}/BV_{DGS}		$R_{DS(ON)}$ (max)	
N-Channel	P-Channel	N-Channel	P-Channel
200V	-200V	7.0Ω	8.0Ω

Pin Configuration



12-Lead DFN
(top view)

Package Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
— = "Green" Packaging

Package may or may not include the following marks: Si or

12-Lead DFN

Drain Output Diodes

Sym	Parameter	Min	Typ	Max	Unit	Condition
V_R	Breakdown voltage	200	-	-	V	$I_R = 100\mu A$
VF	Forward voltage	-	1.25	-	V	$I_F = 100mA$
I_{FM}	Park forward current	-	3.0	-	A	Pulse width = 1.0μs, D% = 1%, One diode
I_R	Reverse current	-	1.0	-	μA	$V_R = 100 V, T_A = 25^\circ C$
		-	100	-		$V_R = 100 V, T_A = 125^\circ C$
t_{tr}	Reverse recovery time	-	1.0	-	μs	$I_F = I_R = 10mA, I_{RR} = 1.0 mA, R_L = 100\Omega$

Pin Description

Pin #	Function	Description	Pin #	Function	Description
1	GN1	Gate of N-MOSFET 1	7	DP2	Drain of P-MOSFET 2
2	GP1	Gate of P-MOSFET 1	8	DN2	Drain of N-MOSFET 2
3	GN2	Gate of N-MOSFET 2	9	SP1	Source of P-MOSFET 1
4	SN2	Source of N-MOSFET 2	10	DP1	Drain of P-MOSFET 1
5	GP2	Gate of P-MOSFET 2	11	DN1	Drain of N-MOSFET 1
6	SP2	Source of P-MOSFET 2	12	SN1	Source of N-MOSFET 1
Thermal Pad		Die attachment substrate, must be grounded externally			

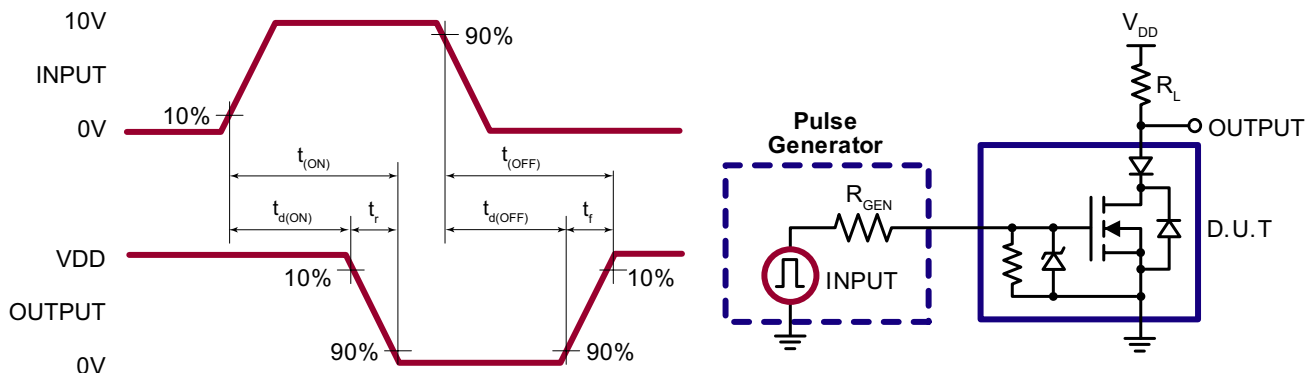
N-Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	200	-	-	V	$V_{GS} = 0V, I_D = 2.0mA$
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.4	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
R_{GS}	Gate-to-source shunt resistor	10	-	50	K Ω	$I_{GS} = 100\mu A$
VZ_{GS}	Gate-to-source Zener voltage	13.2	-	25	V	$I_{GS} = 2.0mA$
I_{DSS}	Zero gate voltage drain current	-	-	10.0	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.9	-	-	A	$V_{GS} = 5.0V, V_{DS} = 25V$
		2.0	-	-		$V_{GS} = 10V, V_{DS} = 50V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	13	Ω	$V_{GS} = 5.0V, I_D = 150mA$
		-	-	10		$V_{GS} = 10V, I_D = 1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	$V_{GS} = 5.0V, I_D = 150mA$
G_{FS}	Forward transconductance	300	-	-	mmho	$V_{DS} = 25V, I_D = 500mA$
C_{ISS}	Input capacitance	-	52	-	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
C_{OSS}	Common source output capacitance	-	6.9	-		
C_{RSS}	Reverse transfer capacitance	-	1.3	-		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 500mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

N-Channel Switching Waveforms and Test Circuit



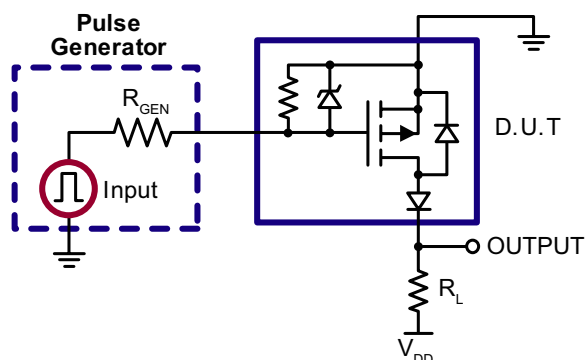
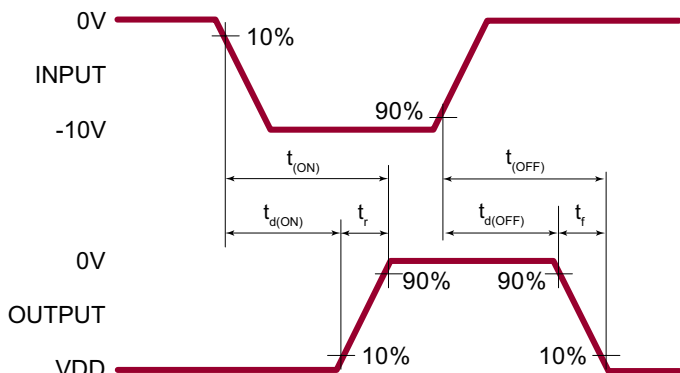
P-Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-200	-	-	V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	$V_{GS} = V_{DS}, I_D = -1.0mA$
R_{GS}	Gate-to-source shunt resistor	10	-	50	K Ω	$I_{GS} = 100\mu A$
VZ_{GS}	Gate-to-source Zener voltage	13.2	-	25	V	$I_{GS} = -2.0mA$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.7	-	-	A	$V_{GS} = -5.0V, V_{DS} = -25V$
		-2.0	-	-		$V_{GS} = -10V, V_{DS} = -50V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	15	Ω	$V_{GS} = -5.0V, I_D = -150mA$
		-	-	12		$V_{GS} = -10V, I_D = -1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	$V_{GS} = -10V, I_D = -200mA$
G_{FS}	Forward transconductance	300	-	-	mmho	$V_{DS} = -25V, I_D = -500mA$
C_{ISS}	Input capacitance	-	54	-	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
C_{OSS}	Common source output capacitance	-	7.5	-		
C_{RSS}	Reverse transfer capacitance	-	2.6	-		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25V, I_D = -1.0A, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -500mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -500mA$

Notes:

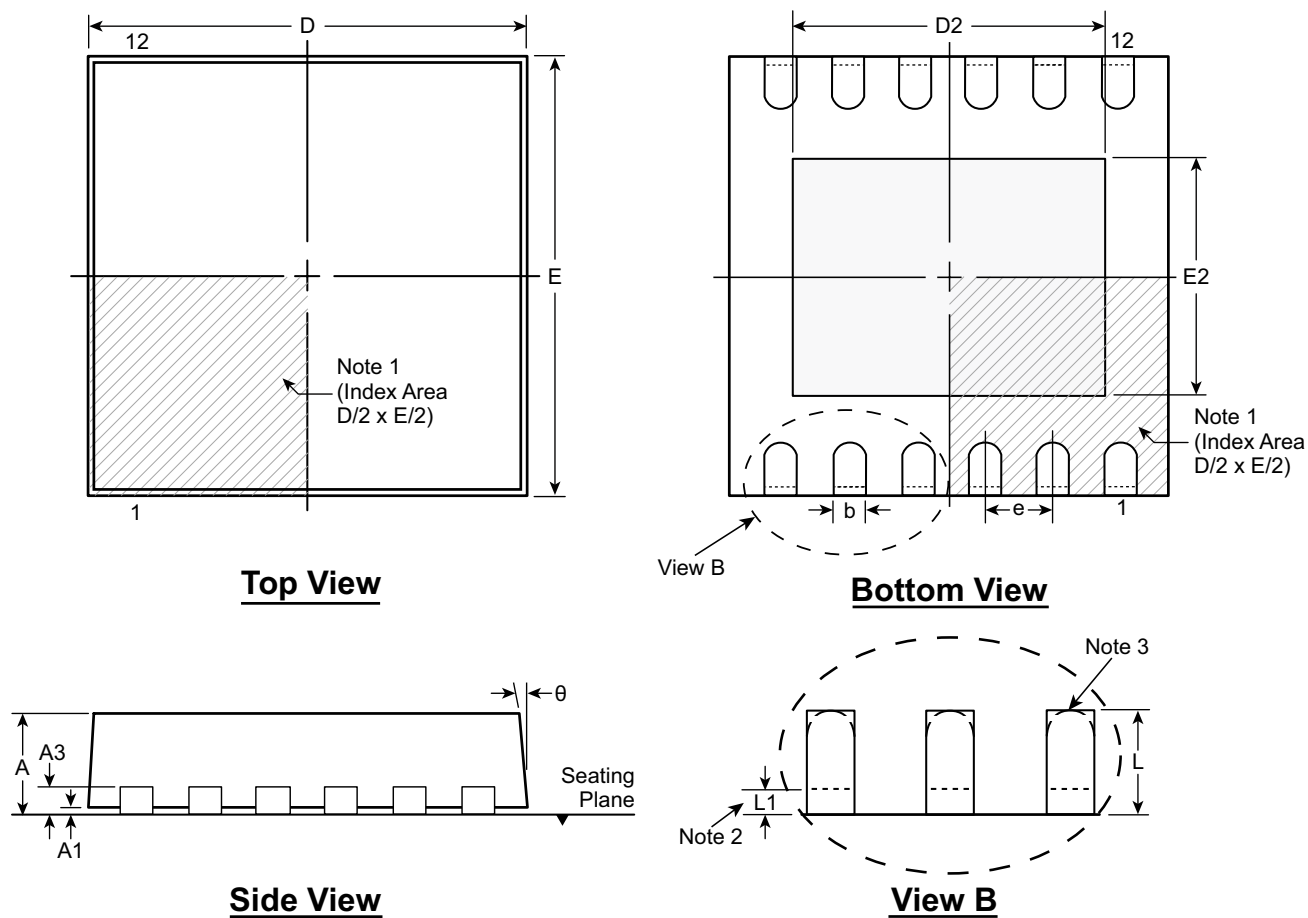
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

P-Channel Switching Waveforms and Test Circuit



12-Lead DFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	3.85	3.19	3.85	2.29	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	4.00	3.34	4.00	2.44		0.40	-	-
	MAX	1.00	0.05		0.30	4.15	3.44	4.15	2.54		0.50	0.15	14°

Drawings not to scale.

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(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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