THE DATASHEET OF

OPA380AIDGKT

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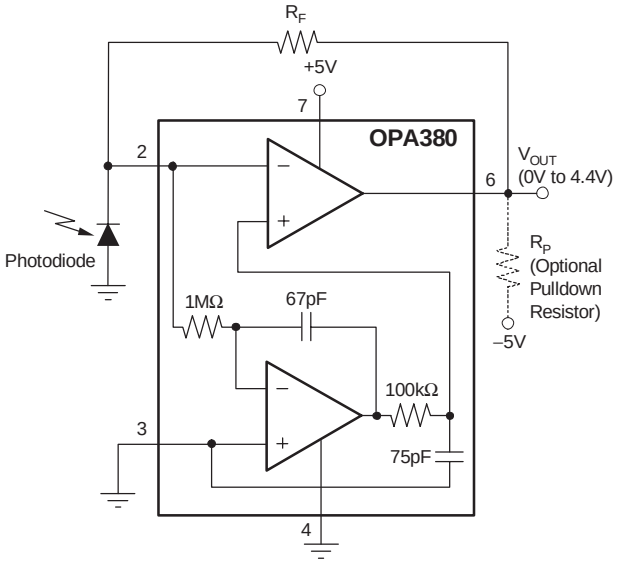
Precision, High-Speed Transimpedance Amplifier

FEATURES

- **> 1MHz TRANSIMPEDANCE BANDWIDTH**
- **EXCELLENT LONG-TERM V_{OS} STABILITY**
- **BIAS CURRENT: 50pA (max)**
- **OFFSET VOLTAGE: 25μV (max)**
- **DYNAMIC RANGE: 4 to 5 Decades**
- **DRIFT: 0.1μV/°C (max)**
- **GAIN BANDWIDTH: 90MHz**
- **QUIESCENT CURRENT: 7.5mA**
- **SUPPLY RANGE: 2.7V to 5.5V**
- **SINGLE AND DUAL VERSIONS**
- ***Micro*Size PACKAGE: MSOP-8**

APPLICATIONS

- **PHOTODIODE MONITORING**
- **PRECISION I/V CONVERSION**
- **OPTICAL AMPLIFIERS**
- **CAT-SCANNER FRONT-END**



DESCRIPTION

The OPA380 family of transimpedance amplifiers provides high-speed (90MHz Gain Bandwidth [GBW]) operation, with extremely high precision, excellent long-term stability, and very low 1/f noise. It is ideally suited for high-speed photodiode applications. The OPA380 features an offset voltage of 25μV, offset drift of 0.1μV/°C, and bias current of 50pA. The OPA380 far exceeds the offset, drift, and noise performance that conventional JFET op amps provide.

The signal bandwidth of a transimpedance amplifier depends largely on the GBW of the amplifier and the parasitic capacitance of the photodiode, as well as the feedback resistor. The 90MHz GBW of the OPA380 enables a transimpedance bandwidth of > 1MHz in most configurations. The OPA380 is ideally suited for fast control loops for power level on an optical fiber.

As a result of the high precision and low-noise characteristics of the OPA380, a dynamic range of 4 to 5 decades can be achieved. For example, this capability allows the measurement of signal currents on the order of 1nA, and up to 100μA in a single I/V conversion stage. In contrast to logarithmic amplifiers, the OPA380 provides very wide bandwidth throughout the full dynamic range. By using an external pull-down resistor to –5V, the output voltage range can be extended to include 0V.

The OPA380 (single) is available in MSOP-8 and SO-8 packages. The OPA2380 (dual) is available in the miniature MSOP-8 package. They are specified from –40°C to +125°C.

OPA380 RELATED DEVICES

PRODUCT	FEATURES
OPA300	150MHz CMOS, 2.7V to 5.5V Supply
OPA350	500μV V_{OS}, 38MHz, 2.5V to 5V Supply
OPA335	10μV V_{OS}, Zero-Drift, 2.5V to 5V Supply
OPA132	16MHz GBW, Precision FET Op Amp, ±15V
OPA656/7	230MHz, Precision FET, ±5V
LOG112	LOG amp, 7.5 decades, ±4.5V to ±18V Supply
LOG114	LOG amp, 7.5 decades, ±2.25V to ±5.5V Supply
IVC102	Precision Switched Integrator
DDC112	Dual Current Input, 20-Bit ADC

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS(1)

Voltage Supply	+7V
Signal Input Terminals(2), Voltage	−0.5V to (V+) + 0.5V
Current	±10mA
Short-Circuit Current(3)	Continuous
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	2000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

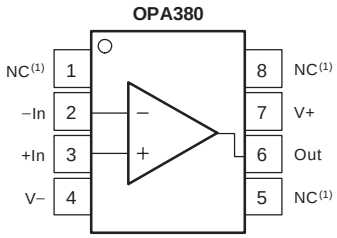
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
OPA380	MSOP-8	AUN
OPA380	SO-8	OPA380A
OPA2380	MSOP-8	BBX

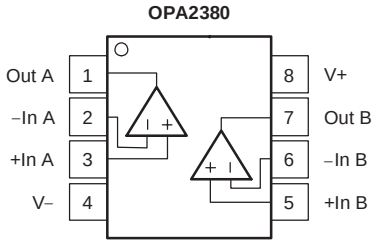
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN ASSIGNMENTS

Top View



MSOP-8, SO-8



MSOP-8

NOTES: (1) NC indicates no internal connection.

ELECTRICAL CHARACTERISTICS: OPA380 (SINGLE), V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +125°C**.

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA380 MIN	OPA380 TYP	OPA380 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V, V_{CM} = 0V		4	25	µV
Drift	**dV_{OS}/dT**			**0.03**	**0.1**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = 0V		2.4	10	µV/V
Over Temperature		**V_S = +2.7V to +5.5V, V_{CM} = 0V**			**10**	**µV/V**
Long-Term Stability(1)				See Note (1)		
Channel Separation, dc				1		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		3	±50	pA
Over Temperature				Typical Characteristics		
Input Offset Current	I_{OS}	V_{CM} = V_S/2		6	±100	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n	V_S = +5V, V_{CM} = 0V		3		μV_{PP}
Input Voltage Noise Density, f = 10kHz	e_n	V_S = +5V, V_{CM} = 0V		67		$nV/\sqrt{Hz}$
Input Voltage Noise Density, f > 1MHz	e_n	V_S = +5V, V_{CM} = 0V		5.8		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 10kHz	i_n	V_S = +5V, V_{CM} = 0V		10		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		V−		(V+) − 1.8V	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) < V_{CM} < (V+) − 1.8V**	**100**	**110**		**dB**
INPUT IMPEDANCE						
Differential Capacitance				1.1		pF
Common-Mode Resistance and Inverting Input Capacitance				10^{13} || 3		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**0.1V < V_O < (V+) − 0.7V, V_S = 5V, V_{CM} = V_S/2**	**110**	**130**		**dB**
		0.1V < V_O < (V+) − 0.6V, V_S = 5V, V_{CM} = V_S/2, T_A = −40°C to +85°C	110	130		dB
		0V < V_O < (V+) − 0.7V, V_S = 5V, V_{CM} = 0V, R_P = 2kΩ to −5V(2)	**106**	**120**		**dB**
		0V < V_O < (V+) − 0.6V, V_S = 5V, V_{CM} = 0V, R_P = 2kΩ to −5V(2), T_A = −40°C to +85°C	106	120		dB
FREQUENCY RESPONSE		C_L = 50pF				
Gain-Bandwidth Product	GBW			90		MHz
Slew Rate	SR	G = +1		80		V/µs
Settling Time, 0.01%(3)	t_S	V_S = +5V, 4V Step, G = +1		2		µs
Overload Recovery Time(4)(5)		$V_{IN} \times G$ = > V_S		100		ns
OUTPUT						
Voltage Output Swing from Positive Rail		**R_L = 2kΩ**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_L = 2kΩ**		**60**	**100**	**mV**
Voltage Output Swing from Positive Rail		**R_P = 2kΩ to −5V(2)**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_P = 2kΩ to −5V(2)**		**−20**	**0**	**mV**
Output Current	I_{OUT}			See Typical Characteristics		
Short-Circuit Current	I_{SC}			150		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
Open-Loop Output Impedance	R_O	f = 1MHz, I_O = 0A		40		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Quiescent Current	I_Q	I_O = 0A		7.5	9.5	mA
Over Temperature					**10**	**mA**
TEMPERATURE RANGE						
Specified and Operating Range			−40		+125	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8, SO-8				150		°C/W

(1) 300-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of 1µV.
(2) Tested with output connected only to R_P, a pulldown resistor connected between V_{OUT} and −5V, as shown in Figure 5. See also applications section, *Achieving Output Swing to Ground*.
(3) Transimpedance frequency of 1MHz.
(4) Time required to return to linear operation.
(5) From positive rail.

ELECTRICAL CHARACTERISTICS: OPA2380 (DUAL), V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +125°C**.

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

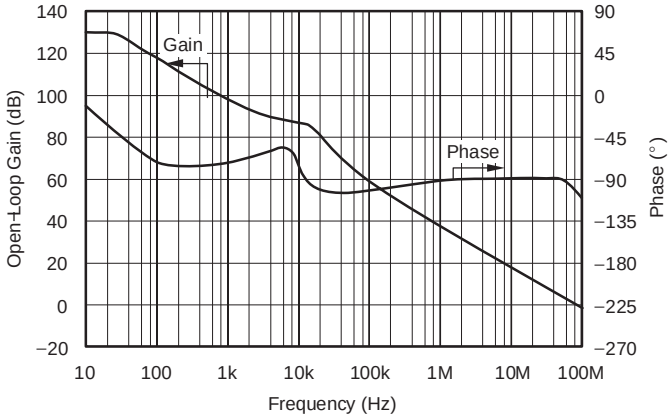
PARAMETER		CONDITION	OPA2380 MIN	OPA2380 TYP	OPA2380 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V, V_{CM} = 0V		4	25	µV
Drift	**dV_{OS}/dT**			**0.03**	**0.1**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = 0V		2.4	10	µV/V
Over Temperature		**V_S = +2.7V to +5.5V, V_{CM} = 0V**			**10**	**µV/V**
Long-Term Stability(1)				See Note (1)		
Channel Separation, dc				1		µV/V
INPUT BIAS CURRENT						
Input Bias Current, Inverting Input	I_B	V_{CM} = V_S/2		3	±50	pA
Noninverting Input	I_B	V_{CM} = V_S/2		3	±200	pA
Over Temperature				Typical Characteristics		
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n	V_S = +5V, V_{CM} = 0V		3		$µV_{PP}$
Input Voltage Noise Density, f = 10kHz	e_n	V_S = +5V, V_{CM} = 0V		67		nV/√Hz
Input Voltage Noise Density, f > 1MHz	e_n	V_S = +5V, V_{CM} = 0V		5.8		nV/√Hz
Input Current Noise Density, f = 10kHz	i_n	V_S = +5V, V_{CM} = 0V		10		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		V−		(V+) − 1.8V	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) < V_{CM} < (V+) − 1.8V**	**95**	**105**		**dB**
INPUT IMPEDANCE						
Differential Capacitance				1.1		pF
Common-Mode Resistance and Inverting Input Capacitance				10^{13} || 3		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**0.12V < V_O < (V+) − 0.7V, V_S = 5V, V_{CM} = V_S/2**	**110**	**130**		**dB**
		0.12V < V_O < (V+) − 0.6V, V_S = 5V, V_{CM} = V_S/2, T_A = −40°C to +85°C	110	130		dB
		0V < V_O< (V+) − 0.7V, V_S = 5V, V_{CM} = 0V, R_P = 2kΩ to −5V(2)	**106**	**120**		**dB**
		0V < V_O < (V+) − 0.6V, V_S = 5V, V_{CM} = 0V, R_P = 2kΩ to −5V(2), T_A = −40°C to +85°C	106	120		dB
FREQUENCY RESPONSE		C_L = 50pF				
Gain-Bandwidth Product	GBW			90		MHz
Slew Rate	SR	G = +1		80		V/µs
Settling Time, 0.01%(3)	t_S	V_S = +5V, 4V Step, G = +1		2		µs
Overload Recovery Time(4)(5)		V_{IN} × G = > V_S		100		ns
OUTPUT						
Voltage Output Swing from Positive Rail		**R_L = 2kΩ**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_L = 2kΩ**		**80**	**120**	**mV**
Voltage Output Swing from Positive Rail		**R_P = 2kΩ to −5V(2)**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_P = 2kΩ to −5V(2)**		**−20**	**0**	**mV**
Output Current	I_{OUT}			See Typical Characteristics		
Short-Circuit Current	I_{SC}			150		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
Open-Loop Output Impedance	R_O	f = 1MHz, I_O = 0A		40		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Quiescent Current (per amplifier)	I_Q	I_O = 0A		7.5	9.5	mA
Over Temperature					**10**	**mA**
TEMPERATURE RANGE						
Specified and Operating Range			−40		+125	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8				150		°C/W

(1) 300-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of 1µV.
(2) Tested with output connected only to R_P, a pulldown resistor connected between V_{OUT} and −5V, as shown in Figure 5. See also applications section, *Achieving Output Swing to Ground.*
(3) Transimpedance frequency of 1MHz.
(4) Time required to return to linear operation.
(5) From positive rail.

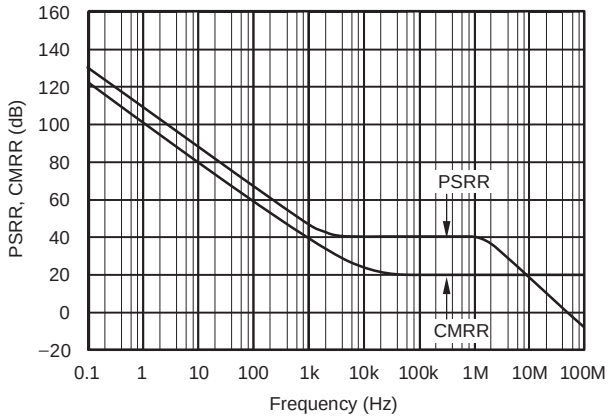
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

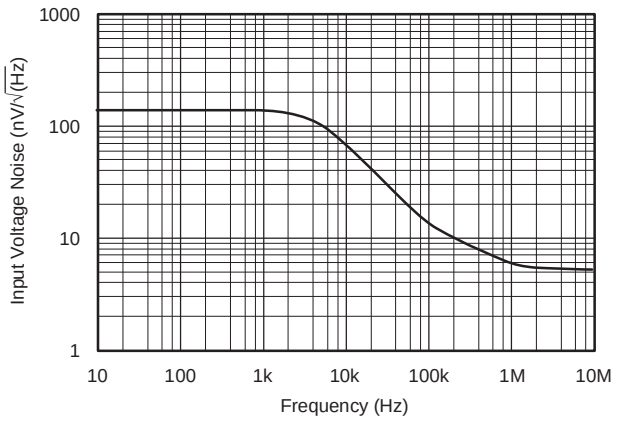
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



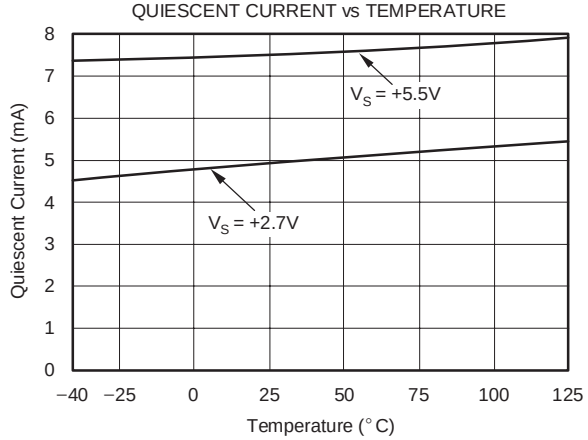
POWER−SUPPLY REJECTION RATIO AND COMMON−MODE REJECTION vs FREQUENCY



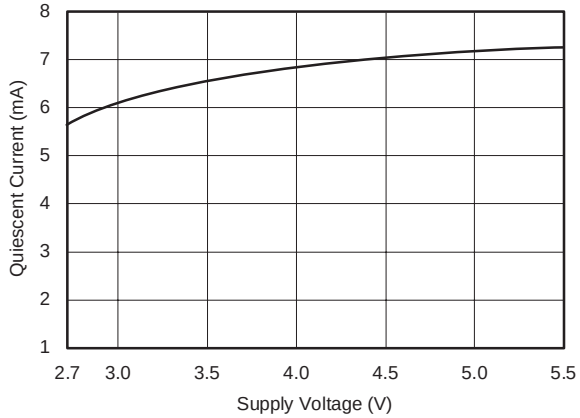
INPUT VOLTAGE NOISE SPECTRAL DENSITY



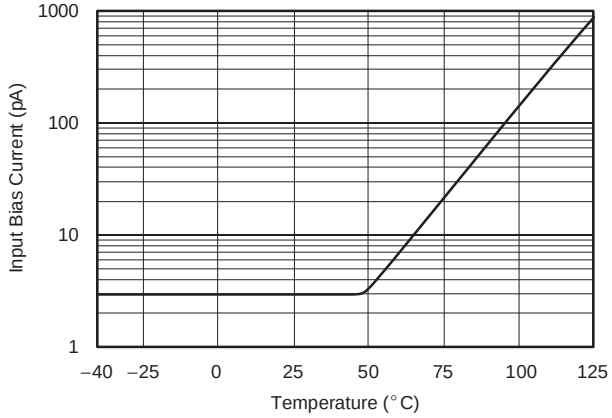
QUIESCENT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



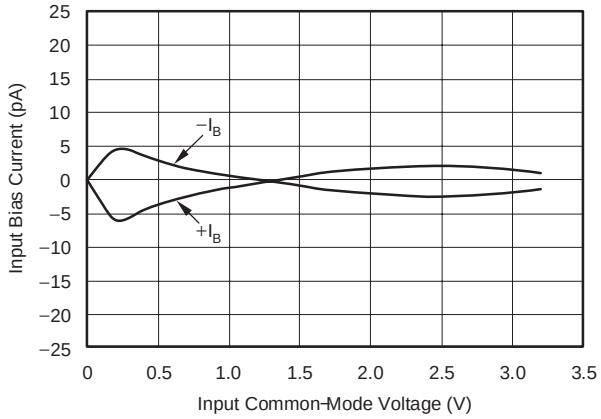
INPUT BIAS CURRENT vs TEMPERATURE



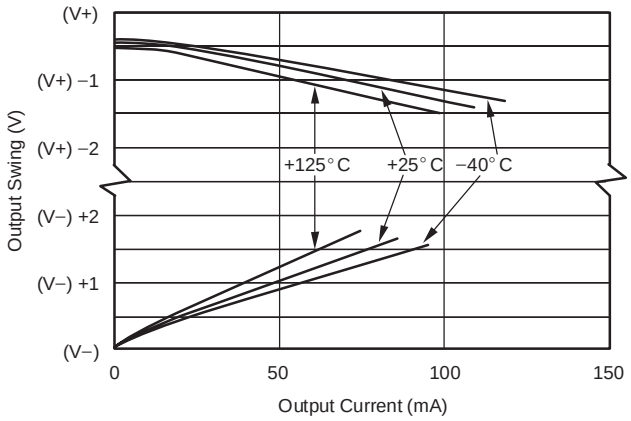
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (continued)

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

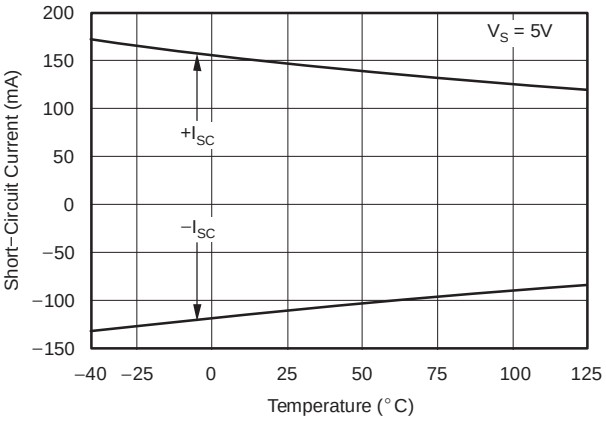
INPUT BIAS CURRENT
vs INPUT COMMON−MODE VOLTAGE



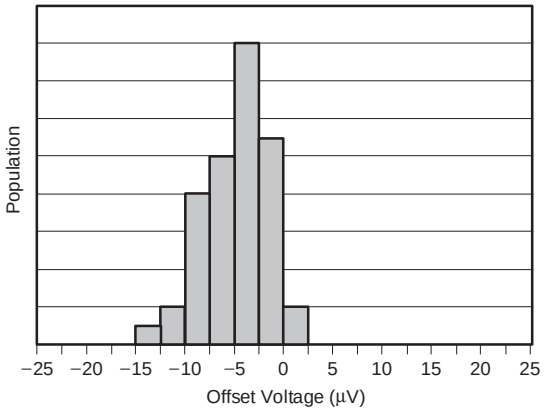
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



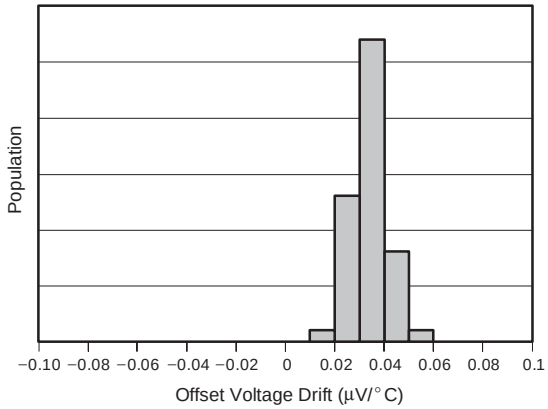
SHORT−CIRCUIT CURRENT vs TEMPERATURE



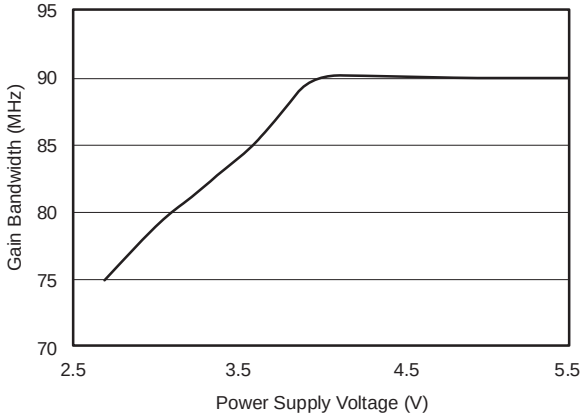
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



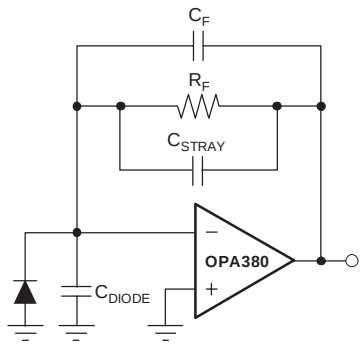
GAIN BANDWIDTH vs POWER SUPPLY VOLTAGE



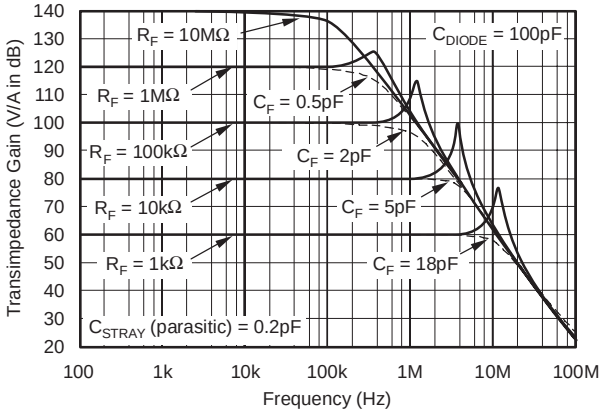
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (continued)

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

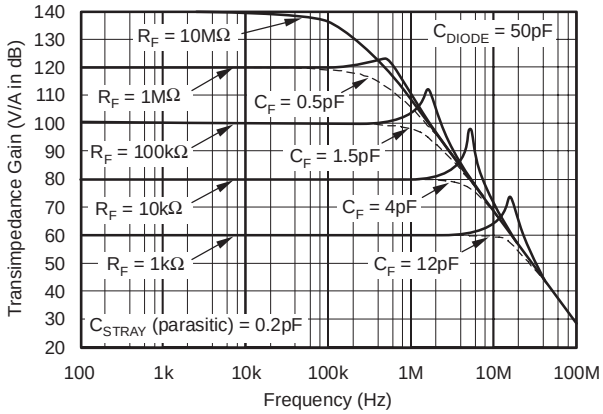
Circuit for *Transimpedance Amplifier Characteristic* curves on this page.



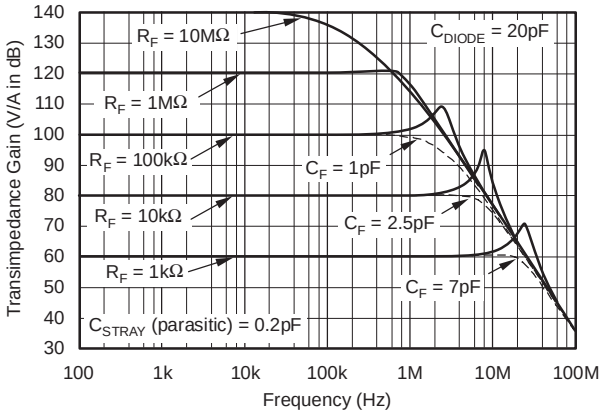
TRANSIMPEDANCE AMP CHARACTERISTIC



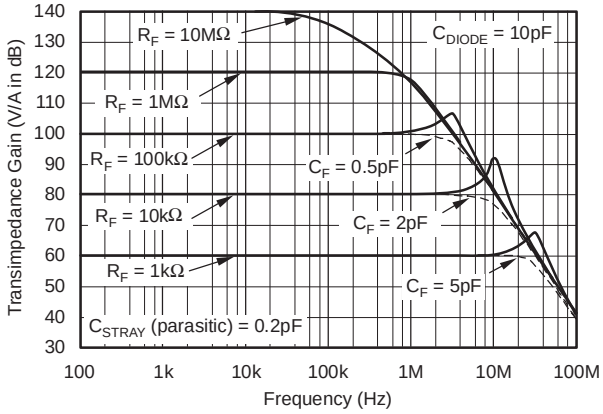
TRANSIMPEDANCE AMP CHARACTERISTIC



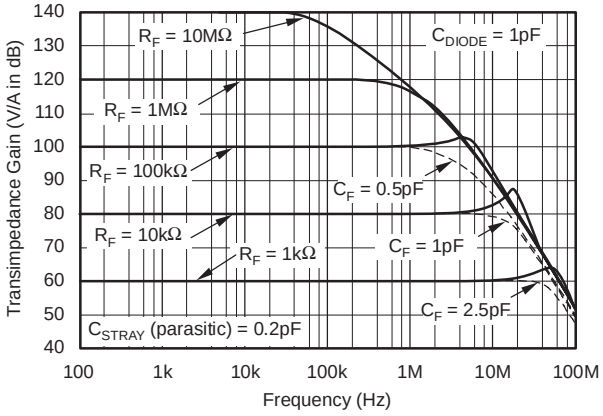
TRANSIMPEDANCE AMP CHARACTERISTIC



TRANSIMPEDANCE AMP CHARACTERISTIC



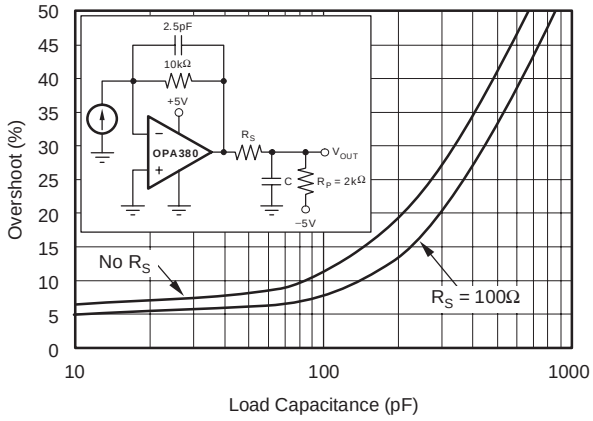
TRANSIMPEDANCE AMP CHARACTERISTIC



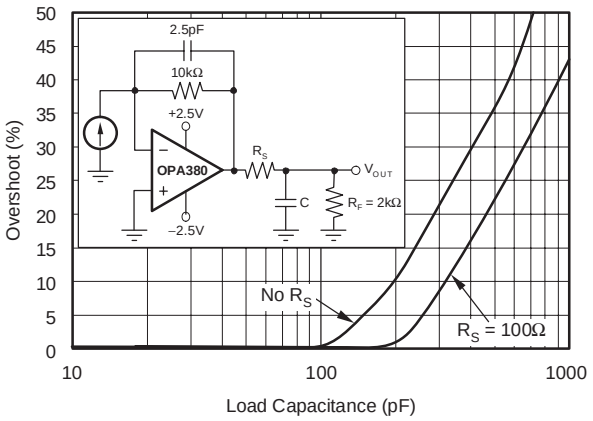
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (continued)

All specifications at T_A = +25°C, R_L = 2kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

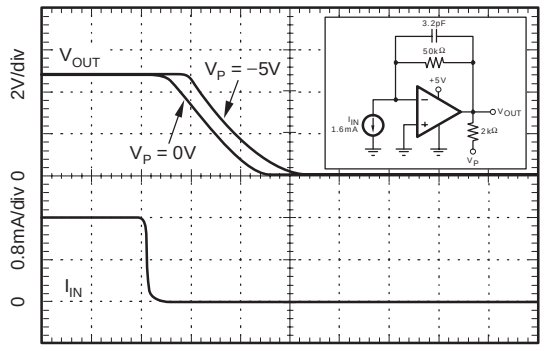
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



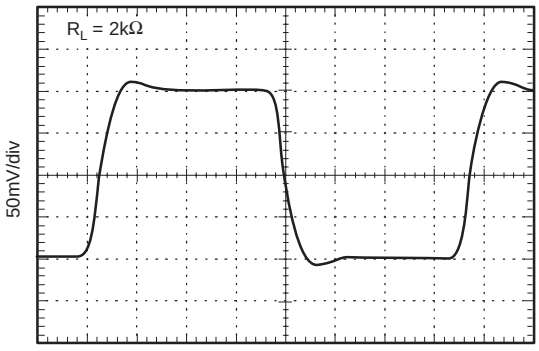
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



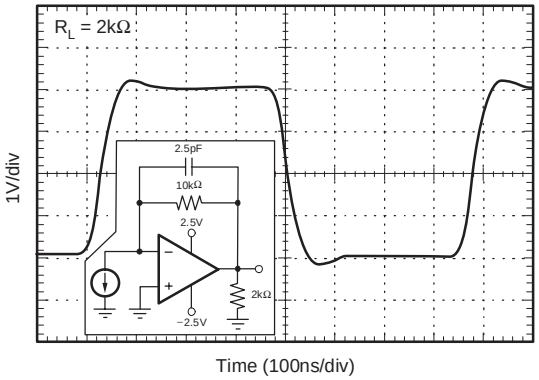
OVERLOAD RECOVERY



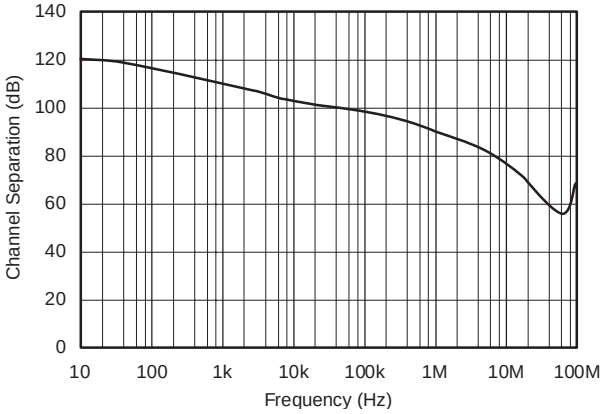
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



CHANNEL SEPARATION vs INPUT FREQUENCY



APPLICATIONS INFORMATION

BASIC OPERATION

The OPA380 is a high-performance transimpedance amplifier with very low 1/f noise. As a result of its unique architecture, the OPA380 has excellent long-term input voltage offset stability—a 300-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of 1μV.

The OPA380 performance results from an internal auto-zero amplifier combined with a high-speed amplifier. The OPA380 has been designed with circuitry to improve overload recovery and settling time over a traditional composite approach. It has been specifically designed and characterized to accommodate circuit options to allow 0V output operation (see Figure 3).

The OPA380 is used in inverting configurations, with the noninverting input used as a fixed biasing point. Figure 1 shows the OPA380 in a typical configuration. Power-supply pins should be bypassed with 1μF ceramic or tantalum capacitors. Electrolytic capacitors are not recommended.

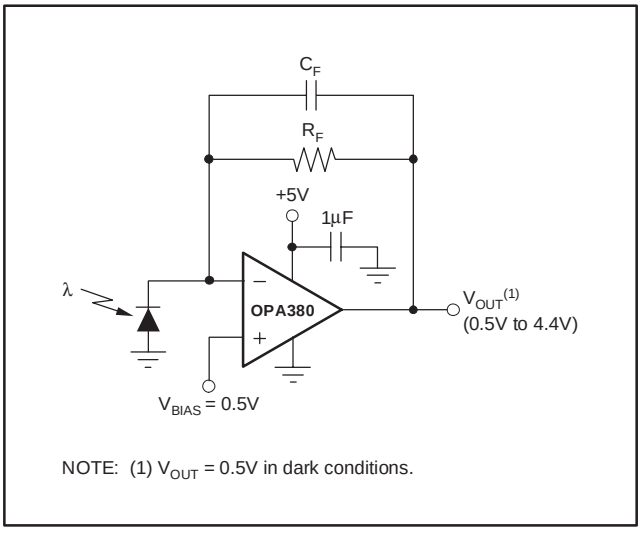


Figure 1. OPA380 Typical Configuration

OPERATING VOLTAGE

The OPA380 series op amps are fully specified from 2.7V to 5.5V over a temperature range of −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

INTERNAL OFFSET CORRECTION

The OPA380 series op amps use an auto-zero topology with a time-continuous 90MHz op amp in the signal path. This amplifier is zero-corrected every 100μs using a proprietary technique. Upon power-up, the amplifier requires approximately 400μs to achieve specified V_{OS} accuracy, which includes one full auto-zero cycle of approximately 100μs and the start-up time for the bias circuitry. Prior to this time, the amplifier will function properly but with unspecified offset voltage.

This design has virtually no aliasing and very low noise. Zero correction occurs at a 10kHz rate, but there is very little fundamental noise energy present at that frequency due to internal filtering. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

INPUT VOLTAGE

The input common-mode voltage range of the OPA380 series extends from V− to (V+) – 1.8V. With input signals above this common-mode range, the amplifier will no longer provide a valid output value, but it will not latch or invert.

INPUT OVERVOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current is limited to 10mA. The OPA380 series feature no phase inversion when the inputs extend beyond supplies if the input is current limited.

OUTPUT RANGE

The OPA380 is specified to swing within at least 600mV of the positive rail and 100mV of the negative rail with a 2kΩ load with excellent linearity. Swing to the negative rail while maintaining good linearity can be extended to 0V—see the section, *Achieving Output Swing to Ground*. See the Typical Characteristic curve, *Output Voltage Swing vs Output Current*.

The OPA380 can swing slightly closer than specified to the positive rail; however, linearity will decrease and a high-speed overload recovery clamp limits the amount of positive output voltage swing available, as shown in Figure 2.

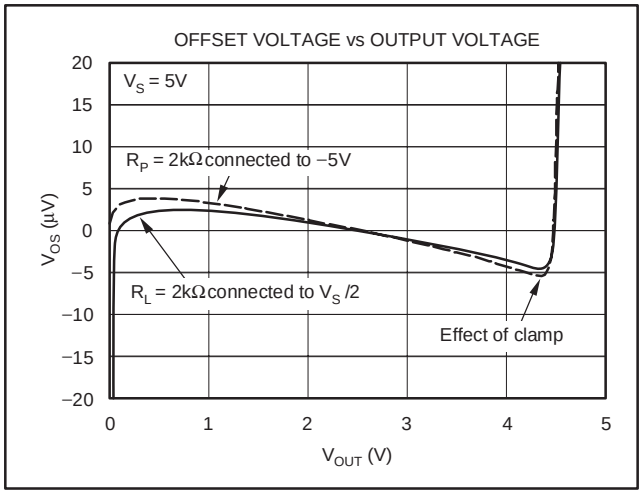


Figure 2. Effect of High-Speed Overload Recovery Clamp on Output Voltage

OVERLOAD RECOVERY

The OPA380 has been designed to prevent output saturation. After being overdriven to the positive rail, it will typically require only 100ns to return to linear operation. The time required for negative overload recovery is greater, *unless* a pull-down resistor connected to a more negative supply is used to extend the output swing all the way to the negative rail—see the following section, *Achieving Output Swing to Ground*.

ACHIEVING OUTPUT SWING TO GROUND

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +4.096V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach 0V.

The output of the OPA380 can be made to swing to ground, or slightly below, on a single-supply power source. This extended output swing requires the use of another resistor and an additional negative power supply. A pull-down resistor may be connected between the output and the negative supply to pull the output down to 0V. See Figure 3.

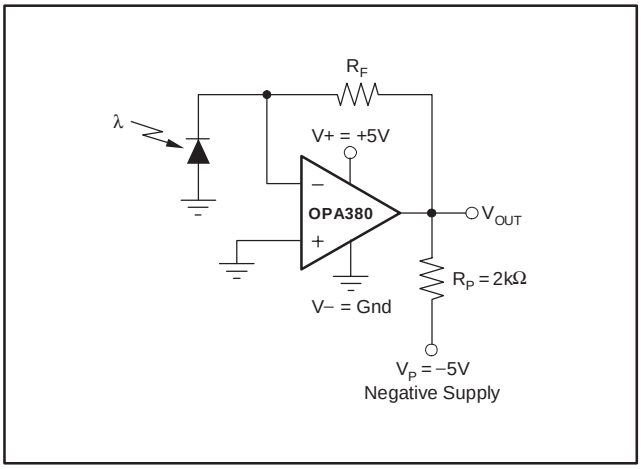


Figure 3. Amplifier with Optional Pull-Down Resistor to Achieve V_{OUT} = 0V

The OPA380 has an output stage that allows the output voltage to be pulled to its negative supply rail using this technique. However, this technique only works with some types of output stages. The OPA380 has been designed to perform well with this method. Accuracy is excellent down to 0V. Reliable operation is assured over the specified temperature range.

BIASING PHOTODIODES IN SINGLE-SUPPLY CIRCUITS

The +IN input can be biased with a positive DC voltage to offset the output voltage and allow the amplifier output to indicate a true *zero* photodiode measurement when the photodiode is not exposed to any light. It will also prevent the added delay that results from coming out of the negative rail. This bias voltage appears across the photodiode, providing a reverse bias for faster operation. An RC filter placed at this bias point will reduce noise, as shown in Figure 4. This bias voltage can also serve as an offset bias point for an ADC with range that does not include ground.

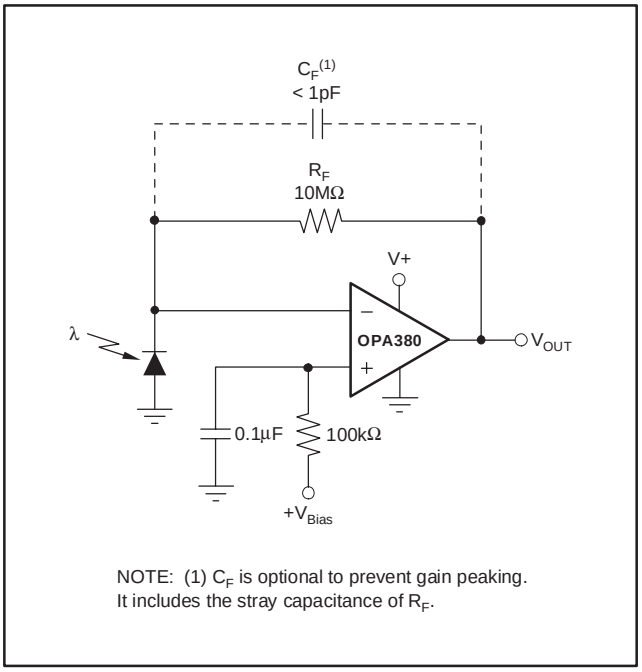


Figure 4. Filtered Reverse Bias Voltage

TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA380 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design are shown in Figure 5:

the total input capacitance (C_{TOT}), consisting of the photodiode capacitance (C_{DIODE}) plus the parasitic common-mode and differential-mode input capacitance (3pF + 1.1pF for the OPA380);

the desired transimpedance gain (R_F);

the Gain Bandwidth Product (GBW) for the OPA380 (90MHz).

With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_{STRAY} is the stray capacitance of R_F, which is 0.2pF for a typical surface-mount resistor.

To achieve a maximally flat, 2nd-order, Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F(C_F + C_{STRAY})} = \sqrt{\frac{GBW}{4\pi R_F C_{TOT}}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_{TOT}}} Hz \quad (2)$$

These equations will result in maximum transimpedance bandwidth. For even higher transimpedance bandwidth, the high-speed CMOS OPA300 (SBOS271 (180MHz GBW)), or the OPA656 (SBOS196 (230MHz GBW)) may be used.

For additional information, refer to Application Bulletin AB−050 (SBOA055), *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.

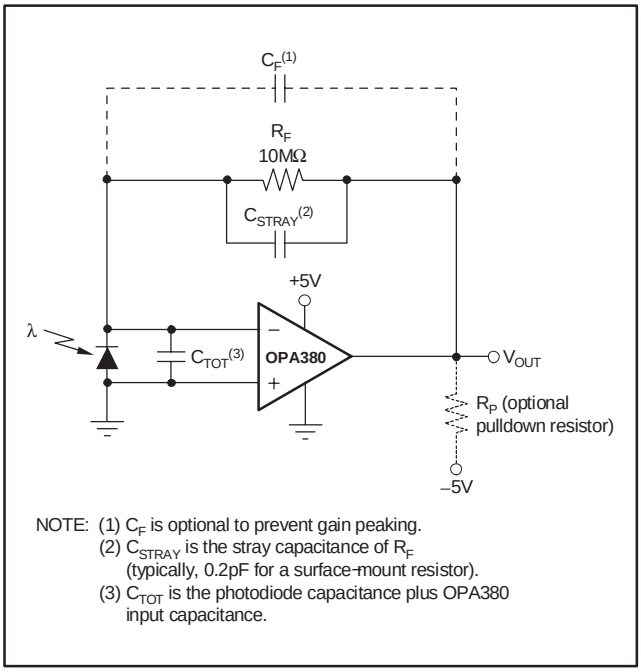


Figure 5. Transimpedance Amplifier

TRANSIMPEDANCE BANDWIDTH AND NOISE

Limiting the gain set by R_F can decrease the noise occurring at the output of the transimpedance circuit. However, all required gain should occur in the transimpedance stage, since adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise spectral density produced by R_F increases with the square-root of R_F, whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.

Total noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor, C_F, across the feedback resistor, R_F, to limit bandwidth, even if not required for stability if total output noise is a concern.

Figure 6a shows the transimpedance circuit without any feedback capacitor. The resulting transimpedance gain of this circuit is shown in Figure 7. The –3dB point is approximately 10MHz. Adding a 16pF feedback capacitor (Figure 6b) will limit the bandwidth and result in a –3dB point at approximately 1MHz (see Figure 7). Output noise will be further reduced by adding a filter (R_{FILTER} and C_{FILTER}) to create a second pole (Figure 6c). This second pole is placed within the feedback loop to maintain the amplifier's low output impedance. (If the pole was placed outside the feedback loop, an additional buffer would be required and would inadvertently increase noise and dc error).

Using R_{DIODE} to represent the equivalent diode resistance, and C_{TOT} for equivalent diode capacitance plus OPA380 input capacitance, the noise zero, f_Z, is calculated by:

$$f_Z = \frac{(R_{DIODE} + R_F)}{2\pi R_{DIODE} R_F (C_{TOT} + C_F)} \quad (3)$$

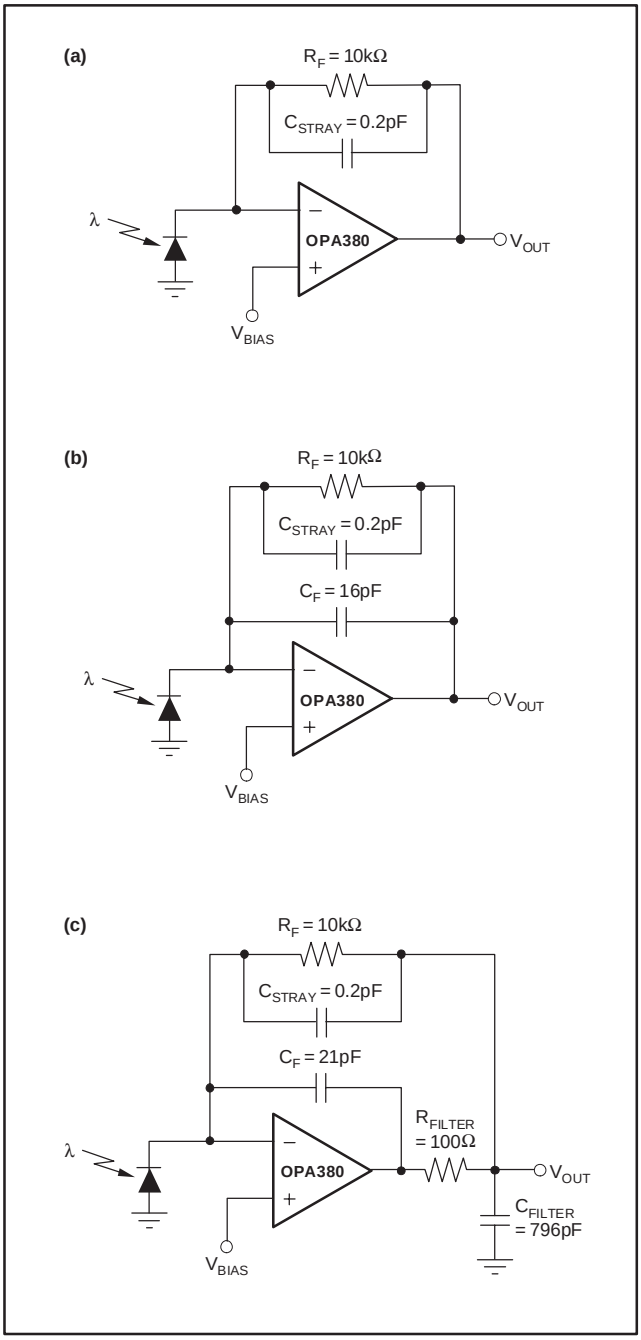


Figure 6. Transimpedance Circuit Configurations with Varying Total and Integrated Noise Gain

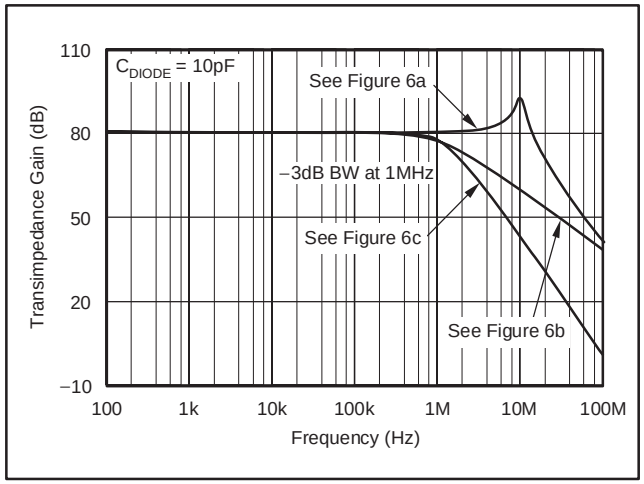


Figure 7. Transimpedance Gains for Circuits in Figure 6

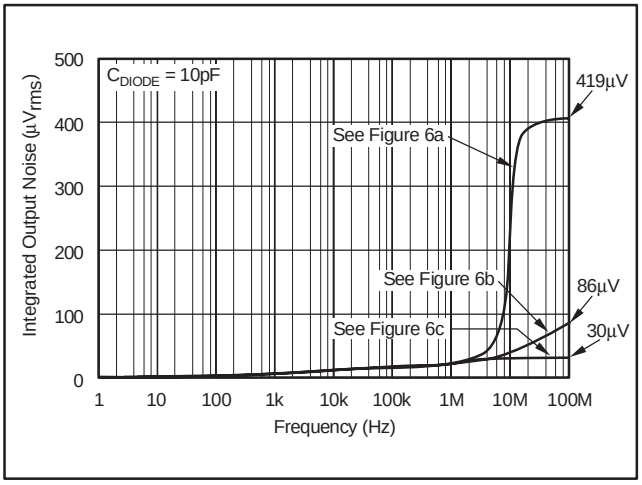


Figure 9. Integrated Output Noise for Circuits in Figure 6

The effect of these circuit configurations on output noise is shown in Figure 8 and on integrated output noise in Figure 9. A 2-pole Butterworth filter (maximally flat in passband) is created by selecting the filter values using the equation:

$$C_F R_F = 2C_{FILTER} R_{FILTER} \quad (4)$$

with:

$$f_{-3dB} = \frac{1}{2\pi\sqrt{R_F R_{FILTER} C_F C_{FILTER}}} \quad (5)$$

The circuit in Figure 6b rolls off at 20dB/decade. The circuit with the additional filter shown in Figure 6c rolls off at 40dB/decade, resulting in improved noise performance.

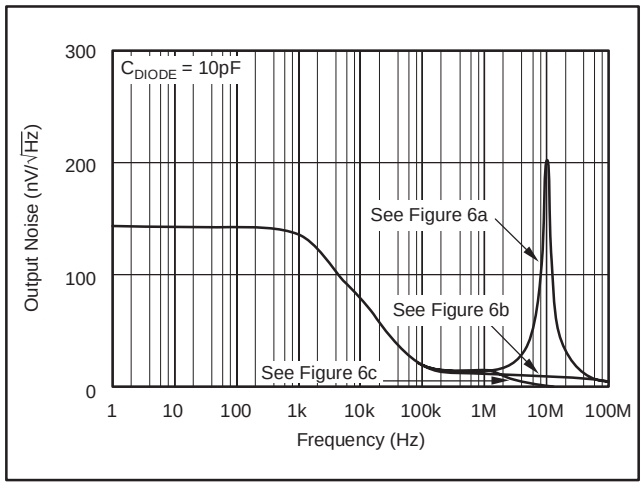


Figure 8. Output Noise for Circuits in Figure 6

Figure 10 shows the effect of diode capacitance on integrated output noise, using the circuit in Figure 6c.

For additional information, refer to *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download from the TI web site.

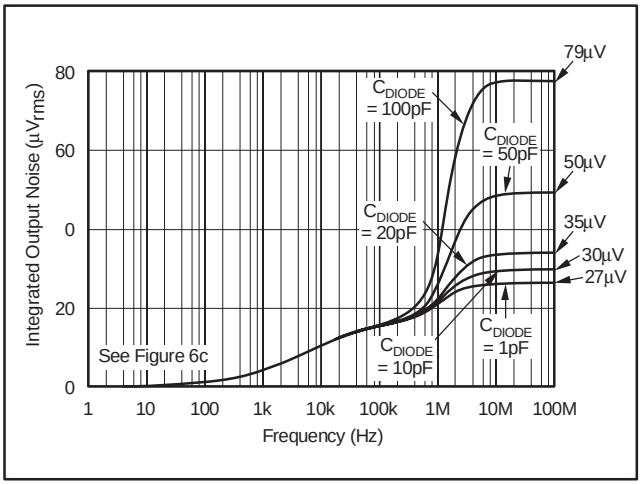


Figure 10. Integrated Output Noise for Various Values of C_{DIODE} for Circuit in Figure 6c

BOARD LAYOUT

Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage, as shown in Figure 11.

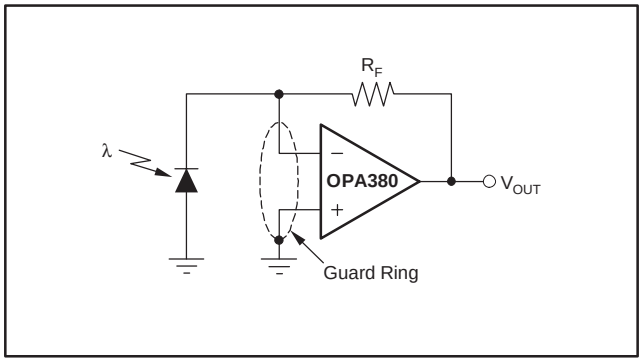


Figure 11. Connection of Input Guard

OTHER WAYS TO MEASURE SMALL CURRENTS

Logarithmic amplifiers are used to compress extremely wide dynamic range input currents to a much narrower range. Wide input dynamic ranges of 8 decades, or 100pA to 10mA, can be accommodated for input to a 12-bit ADC. (Suggested products: LOG101, LOG102, LOG104, and LOG112.)

Extremely small currents can be accurately measured by integrating currents on a capacitor. (Suggested product: IVC102.)

Low-level currents can be converted to high-resolution data words. (Suggested product: DDC112.)

For further information on the range of products available, search www.ti.com using the above specific model names or by using keywords *transimpedance* and *logarithmic*.

CAPACITIVE LOAD AND STABILITY

The OPA380 series op amps can drive up to 500pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads (see the Typical Characteristic curve, *Small-Signal Overshoot vs Capacitive Load*).

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor in series with the load. This reduces ringing with large capacitive loads while maintaining DC accuracy.

DRIVING FAST 16-BIT ANALOG-TO-DIGITAL CONVERTERS (ADC)

The OPA380 series is optimized for driving a fast 16-bit ADC such as the ADS8411. The OPA380 op amp buffers the converter's input capacitance and resulting charge injection while providing signal gain. Figure 12 shows the OPA380 in a single-ended method of interfacing the ADS8411 16-bit, 2MSPS ADC. For additional information, refer to the ADS8411 data sheet.

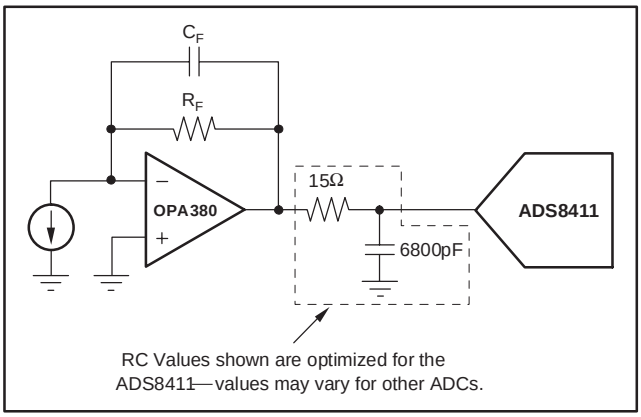


Figure 12. Driving 16-Bit ADCs

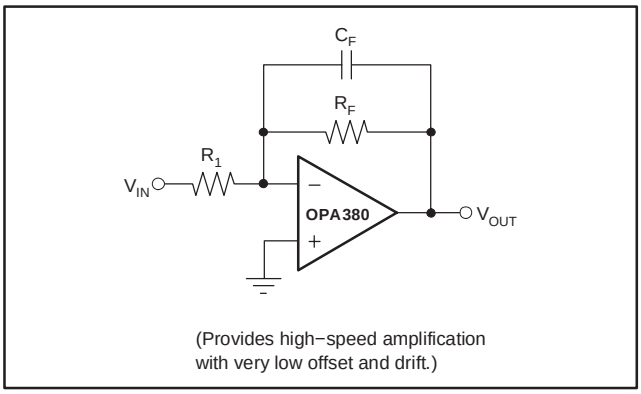


Figure 13. OPA380 Inverting Gain Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2380AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBX	Samples
OPA2380AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBX	Samples
OPA2380AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBX	Samples
OPA2380AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBX	Samples
OPA380AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 380A	Samples
OPA380AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 380A	Samples
OPA380AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	AUN	Samples
OPA380AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	AUN	Samples
OPA380AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	AUN	Samples
OPA380AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	AUN	Samples
OPA380AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 380A	Samples
OPA380AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 380A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

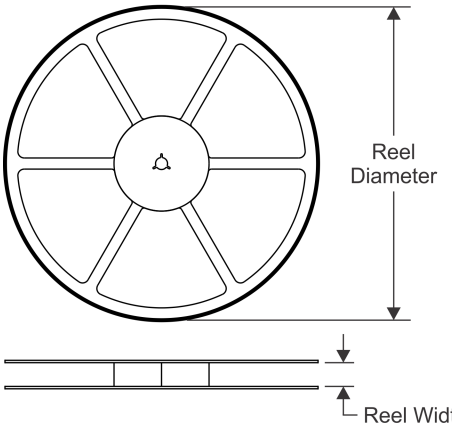
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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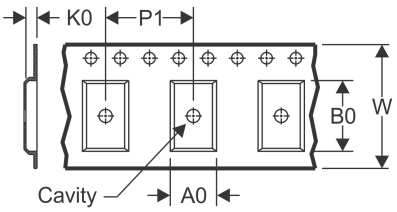
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

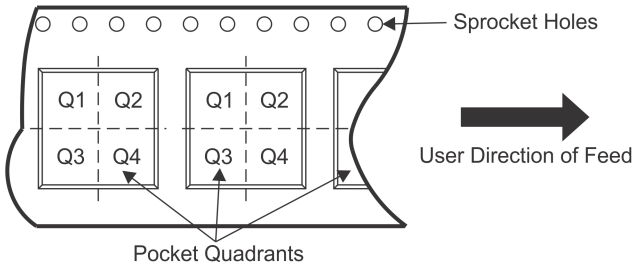


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

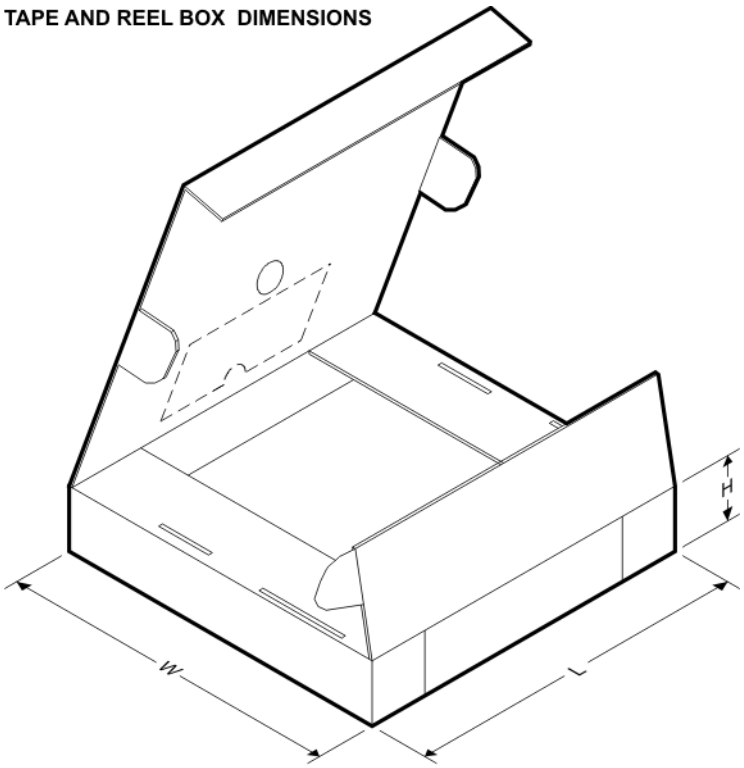
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

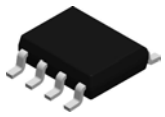
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2380AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2380AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA380AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA380AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA380AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2380AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2380AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA380AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA380AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA380AIDR	SOIC	D	8	2500	367.0	367.0	35.0

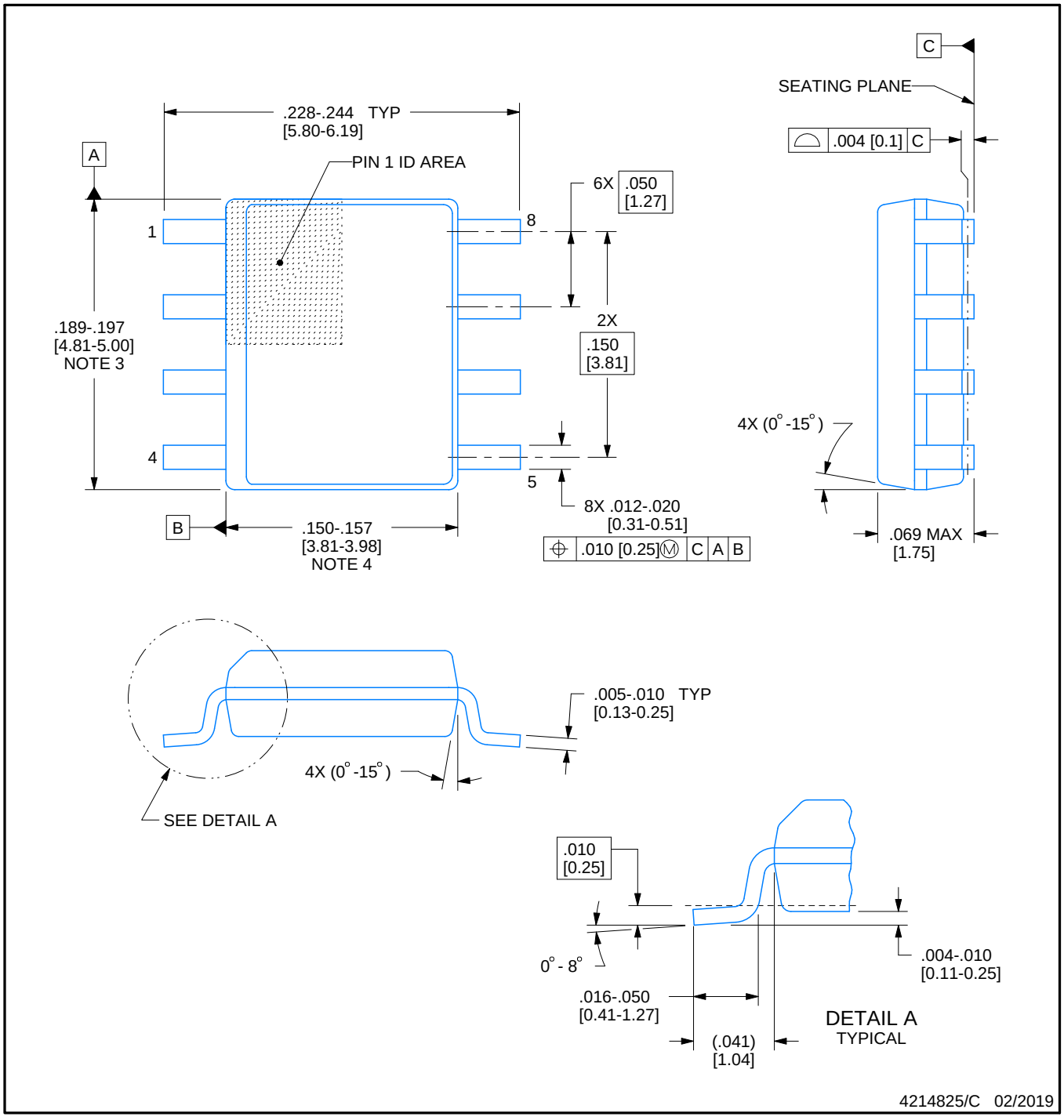


PACKAGE OUTLINE

D0008A

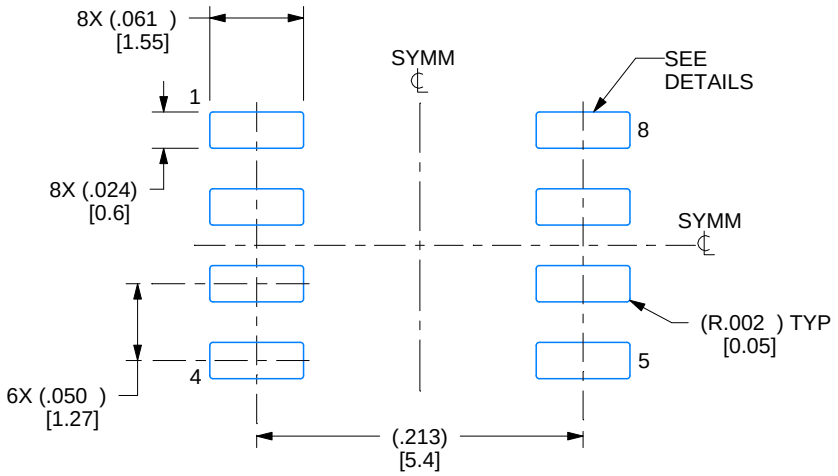
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

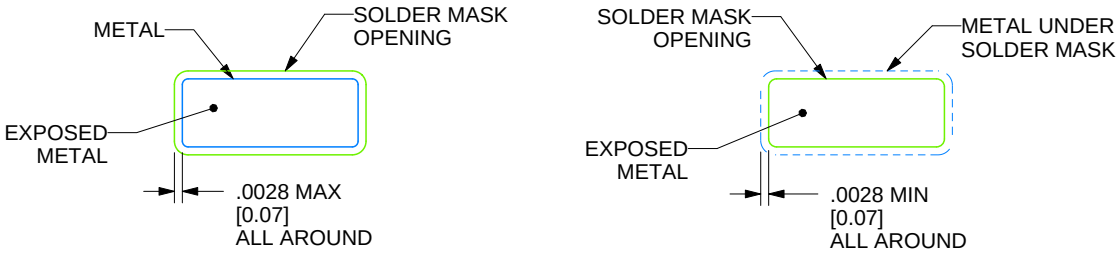


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

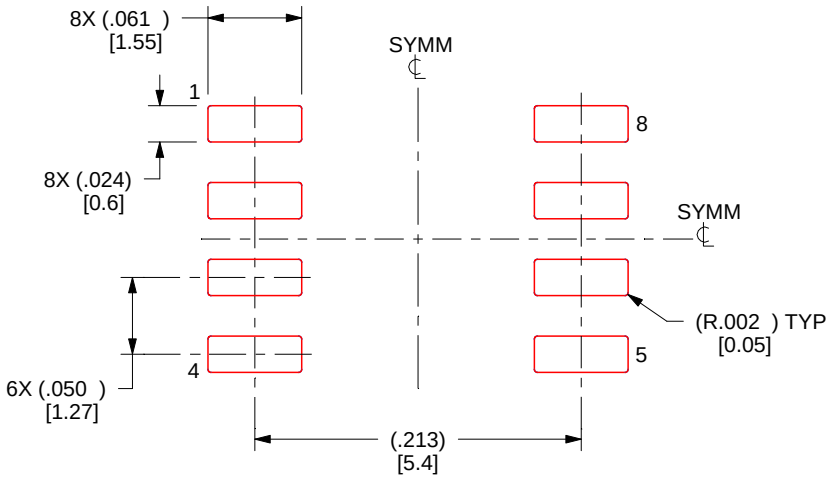
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



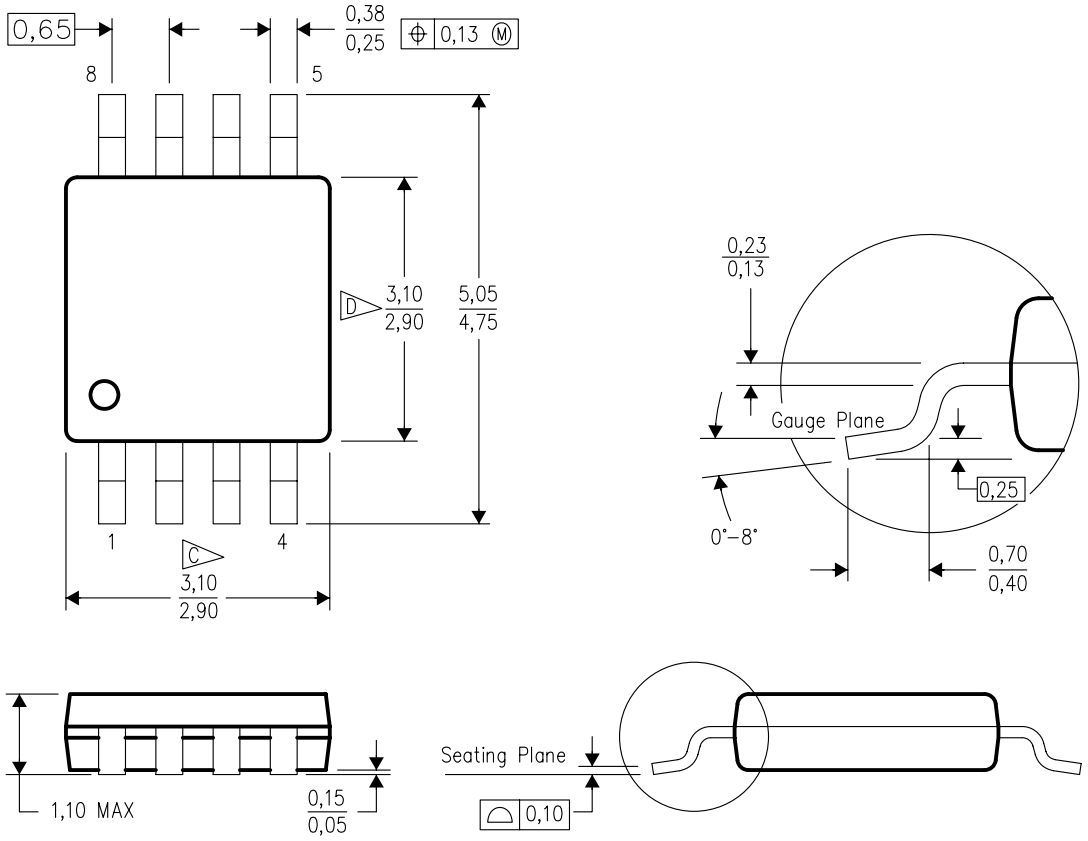
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

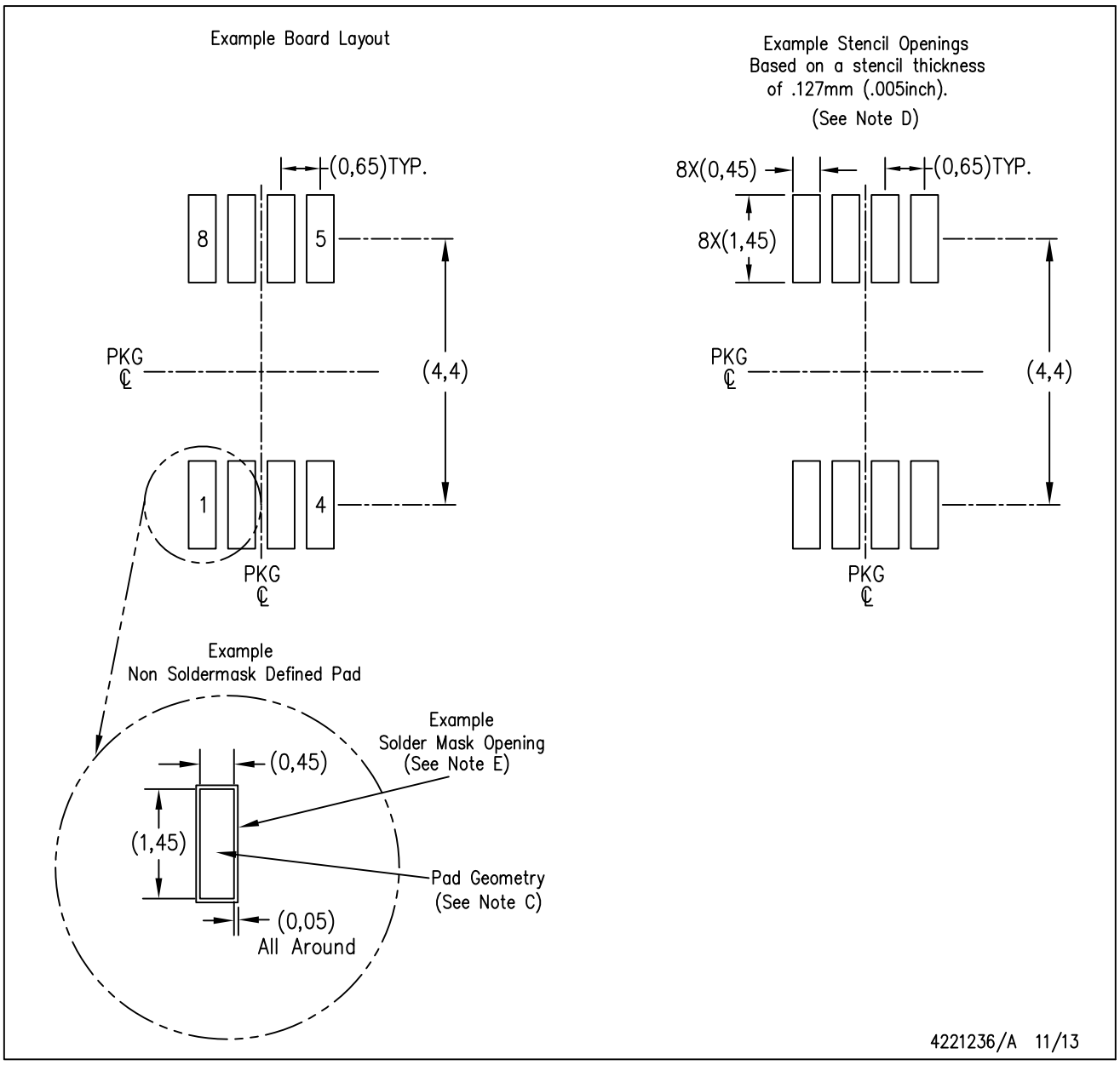
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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