THE DATASHEET OF

MAX16826ATJ+

MAX16826

Programmable, Four-String HB LED Driver with Output-Voltage Optimization and Fault Detection

General Description

The MAX16826 high-brightness LED (HB LED) driver is designed for backlighting automotive LCD displays and other display applications such as industrial or desktop monitors and LCD televisions. The MAX16826 integrates a switching regulator controller, a 4-channel linear current sink driver, an analog-to-digital converter (ADC), and an I²C interface. The IC is designed to withstand automotive load dump transients up to 40V and can operate under cold crank conditions.

The MAX16826 contains a current-mode PWM switching regulator controller that regulates the output voltage to the LED array. The switching regulator section is configurable as a boost or SEPIC converter and its switching frequency is programmable from 100kHz to 1MHz.

The MAX16826 includes 4 channels of programmable, fault-protected, constant-current sink driver controllers that are able to drive all white, RGB, or RGB plus amber LED configurations. LED dimming control for each channel is implemented by direct PWM signals for each of the four linear current sinks. An internal ADC measures the drain voltage of the external driver transistors and the output of the switching regulator. These measurements are then made available through the I²C interface to an external microcontroller (µC) to enable output voltage optimization and fault monitoring of the LEDs.

The amplitude of the LED current in each linear current-sink channel and the switch-mode regulator output voltage is programmed using the I²C interface. Additional features include: cycle-by-cycle current limit, shorted LED string protection, and overtemperature protection. The MAX16826 is available in a thermally enhanced, 5mm x 5mm, 32-pin thin QFN package and is specified over the automotive -40°C to +125°C temperature range.

Applications

LCD Backlighting:

- Automotive Infotainment Displays
- Automotive Cluster Displays
- Industrial and Desktop Monitors
- LCD TVs

Automotive Lighting:

- Adaptive Front Lighting
- Low- and High-Beam Assemblies

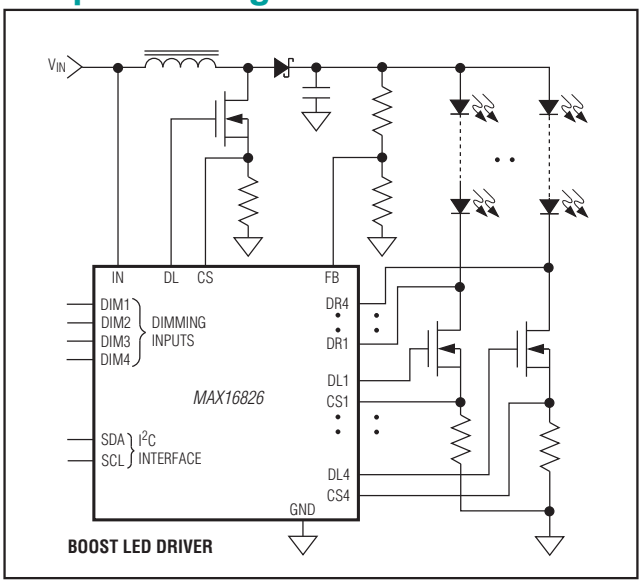
Typical Application Circuit and Pin Configuration appear at end of data sheet.

Benefits and Features

- 4 Channels of Programmable, Fault-Protected, Constant-Current Source-Driver Controllers for All White, RGB, or RGB Plus Amber LED Configurations
  - Drives One to Four LED Strings
  - Individual PWM Dimming Inputs per String
  - Very Wide Dimming Range
- Configurable as a boost or SEPIC Converter with Programmable 100kHz to 1MHz Switching Frequency for Design Flexibility
  - Integrated Boost/SEPIC Controller
  - External MOSFETs Allow Wide-Range LED Current with Multiple LEDs per String
  - 200kHz to 2MHz Programmable Switching Frequency for Optimizing Size vs. Efficiency
  - External Switching-Frequency Synchronization
- I²C Allows the Current-Sink Drain Voltages to be Read to Minimize Power Dissipation and Detect LED String Fault Conditions
  - 7-Bit Internal ADC for LED Voltage Monitoring and Optimization
  - Dynamic Adjustment of LED String Currents and Output Voltage
  - Standby Mode
- Protection Features Improve Reliability
  - LED Short and Open Detection
  - Overvoltage and Overtemperature Protection

Ordering Information appears at end of data sheet.

Simplified Diagram



Absolute Maximum Ratings

IN to GND (Continuous) .....-0.3V to +30V
IN Peak Current (≤ 400ms) 300mA
IN Continuous Current 50mA
PGND to GND .....-0.3V to +0.3V
All Other Pins to GND.....-0.3V to +6V
DL Peak Current (< 100ns).....±3A
DL Continuous Current.....±50mA
DL1, DL2, DL3, DL4 Peak Current .....±50mA
DL1, DL2, DL3, DL4 Continuous Current .....±20mA
V_{CC} Continuous Current 50mA
All Other Pins Current.....±20mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 34.5mW/°C above +70°C)
Multilayer Board 2759mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{IN}	V_{SYNC} = 3V	4.75		24	V
Quiescent Current	I_{IN}	DL_ = unconnected; R19, C33 = open		5	10	mA
Shutdown Current	$I_{IN,SD}$	V_{SYNC} = 0V		20	75	µA
Standby Current	$I_{IN,SB}$	I^2C standby activated		3		mA
I^2C-COMPATIBLE I/O (SCL, SDA)						
Input High Voltage	V_{IH}		1.5			V
Input Low Voltage	V_{IL}				0.5	V
Input Hysteresis	V_{HYS}			25		mV
Input High Leakage Current	I_{IH}	V_{LOGIC} = 5V	-1		+1	µA
Input Low Leakage Current	I_{IL}	V_{LOGIC} = 0V	-1		+1	µA
Input Capacitance	C_{IN}			10		pF
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Current	I_{OH}	V_{OH} = 5V			1	µA
I^2C-COMPATIBLE TIMING						
Serial Clock (SCL) Frequency	f_{SCL}				400	kHz
BUS Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		0.3			µs
Data In Hold Time	$t_{HD:DATIN}$		0.03		0.9	µs
Data Out Hold Time	$t_{HD:DATOUT}$		0.3			µs

Electrical Characteristics (continued)

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Receive SCL/SDA Rise Time	t_R	C_B = 400pF		300		ns
Minimum Receive SCL/SDA Rise Time	t_R	C_B = 400pF		60		ns
Maximum Receive SCL/SDA Fall Time	t_F	C_B = 400pF		300		ns
Minimum Receive SCL/SDA Fall Time	t_F	C_B = 400pF		60		ns
Transmit SDA Fall Time	t_F	C_B = 400pF, I_O = 3mA	60		250	ns
Pulse Width of Suppressed Spike	t_{SP}			50		ns
INTERNAL REGULATORS (IN, V_{CC})						
V_{CC} Output Voltage	V_{VCC}	0V < I_{VCC} < 30mA (Note 2), 4.75V < V_{IN} < 24V, DL, DL1 to DL4 unconnected	4.5	5.25	5.65	V
V_{CC} Undervoltage Lockout	V_{VCC_UVLO}	V_{CC} rising			4.5	V
V_{CC} Undervoltage Lockout Hysteresis	V_{VCC_HYS}		135	175	205	mV
IN Shunt Regulation Voltage		I_{IN} = 250mA	24.05	26.0	27.5	V
PWM GATE DRIVER (DL)						
Peak Source Current				2		A
Peak Sink Current				2		A
DL High-Side Driver Resistance		I_{DL} = -100mA		2.25		Ω
DL Low-Side Driver Resistance		I_{DL} = +100mA		1.30		Ω
Minimum DL Pulse Width				40		ns
PWM CONTROLLER, SOFT-START (FB, COMP, OVP)						
FB Voltage Maximum	$V_{FB,MAX}$	FB shorted to COMP; MAX16826 only	1.230	1.250	1.260	V
		FB shorted to COMP; MAX16826B only	1.23	1.25	1.27	
FB Voltage Minimum	$V_{FB,MIN}$	FB shorted to COMP; MAX16826 only	862	876	885	mV
		FB shorted to COMP; MAX16826B only	735	750	765	
FB Voltage LSB		FB shorted to COMP; MAX16826 only		2.94		mV
		FB shorted to COMP; MAX16826B only		3.9		
FB Input Bias Current	I_{FB}	0V < V_{FB} < 5.5V	-100	0	+100	nA
Feedback-Voltage Line Regulation		Level to produce V_{COMP} = 1.25V, 4.5V < V_{VCC} < 5.5V			±0.25	%/V
Soft-Start Current	I_{SS}	V_{CSS} = 0.5V_{VCC}	3.2	6.0	10.4	µA
OVP Input Bias Current	I_{OVP}	0V < V_{OVP} < 5.5V	-100	0	+100	nA
Slope Compensation	I_{SLOPE}		19	26	32	µA/µs

Electrical Characteristics (continued)

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER (FB, COMP)						
Open-Loop Gain	A_{OL}			80		dB
Unity-Gain Bandwidth	BW			2		MHz
Phase Margin	PM			65		Degrees
Error-Amplifier Output Current	I_{COMP}	Sourcing, V_{COMP} = 3V		1.9		mA
		Sinking, V_{COMP} = 2V		0.9		
COMP Clamp Voltage	V_{COMP}	V_{FB} = 0V	3.25		4.5	V
COMP Short-Circuit Current	I_{COMP_SC}			12		mA
PWM CURRENT LIMIT (CS)						
Cycle-by-Cycle Current-Limit Threshold	V_{CL}	V_{DL} = 0V	187	200	217	mV
Cycle-by-Cycle Current-Limit Propagation Time To DL	$t_{PROP, CL}$	10mV overdrive		80		ns
Gross Current-Limit Threshold	V_{GCL}	V_{CSS} = 0V	250	270	280	mV
Gross Current-Limit Propagation Time To DL	$t_{PROP,GCL}$	10mV overdrive		80		ns
Input Bias Current		0V < V_{CS} < 5.5V	-100	0	+100	nA
PWM OSCILLATOR (RTCT)						
RTCT Voltage Ramp (Peak to Peak)	V_{RAMP}	5.5V < V_{IN} < 24V	1.60	1.65	1.80	V
RTCT Voltage Ramp Valley	V_{RAMP_VALLEY}	5.5V < V_{IN} < 24V	1.11	1.20	1.27	V
Discharge Current	I_{DIS}	V_{RTCT} = 2V	7.8	8.4	9.1	mA
Frequency Range	f_{OSC}	5.5V < V_{IN} < 24V	100		1000	kHz
SYNCHRONIZATION (SYNC/ENABLE)						
Input Rise/Fall Time					200	ns
Input Frequency Range			100		1000	kHz
Input High Voltage			1.5			V
Input Low Voltage					0.5	V
Input Minimum Pulse Width			200			ns
Input Bias Current		0V < V_{SYNC} < 5.5V	-100	0	+100	nA
Delay to Shutdown		V_{SYNC} = 0V	13	32	65	µs
LED DIMMING (DIM1–DIM4)						
Input High Voltage	$V_{DIM,MAX}$		1.5			V
Input Low Voltage	$V_{DIM,MIN}$				0.5	V
Minimum Dimming Frequency	f_{DIM}	t_{ON} = 2µs (Note 3)	45			Hz
Input Bias Current	I_{DIM}	0V < $V_{DIM\_}$ < 5.5V	-100	0	+100	nA

Electrical Characteristics (continued)

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

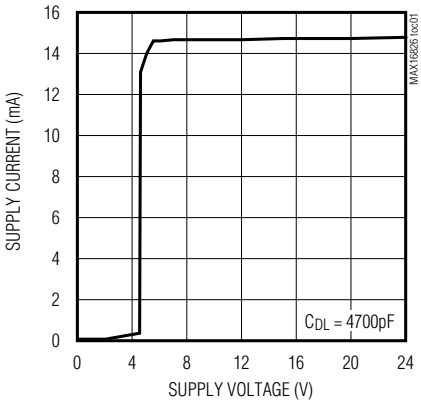
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC (DR1–DR4, OVP)						
Maximum Error	E_{MAX}				±50	mV
ADC Single Bit Acquisition Latency		(Note 4)		2		µs
DR Channel Sample Time	$t_{DR,SMPL}$			190		ms
OVP Channel Sample Time	$t_{OVP,SMPL}$			20		µs
Full-Scale Input Voltage	V_{FS}		1.215	1.24	1.2550	V
Least Significant Bit	V_{LSB}			9.76		mV
DR Input Bias Current	I_{DR}	0V < $V_{DR\_}$ < 5.5V	-100	0	+100	nA
DRAIN FAULT COMPARATORS (DR1–DR4) (Shorted LED String Comparator)						
Drain Fault Comparator Threshold	V_{DFTH}	Voltage to drive DL1–DL4 low	1.4	1.52	1.63	V
Drain Fault Comparator Delay	t_{DFD}	10mV overdrive		1		µs
LINEAR REGULATORS (DL1–DL4, CS1–CS4)						
Transconductance	Gm	ΔI = -500µA		75		mS
Maximum Output Current	I_{DL}	Sourcing or sinking		15		mA
CS1–CS4 Input Bias Current	I_{CS}	0V < V_{CS} < 5.5V	-100	0	+100	nA
CS1–CS4 Regulation Voltage Maximum	$V_{CS,MAX}$	CS_ = DL_, FB DAC full scale; MAX16826 only	306	316	324	mV
		CS_ = DL_, FB DAC full scale; MAX16826B only	308	318	328	
CS1–CS4 Regulation Voltage Minimum	$V_{CS,MIN}$	CS_ = DL_, FB DAC minus full scale; MAX16826 only	90	97	105	mV
		CS_ = DL_, FB DAC minus full scale; MAX16826B only	90	99	109	
CS1–CS4 Regulation Voltage LSB	$V_{CS,LSB}$	CS_ = DL_, FB DAC 1-bit transition		1.72		mV

Note 1: All devices are 100% production tested at T_J = +25°C and T_J = +125°C. Limits to -40°C are guaranteed by design.
Note 2: I_{CC} includes the internal bias currents and the current used by the gate drivers to drive DL, DL1, DL2, DL3, and DL4.
Note 3: Minimum frequency to allow the internal ADC to complete at least one measurement. t_{ON} is the on-time with the LED current in regulation.
Note 4: Minimum LED current pulse duration, which is required to correctly acquire 1 bit.

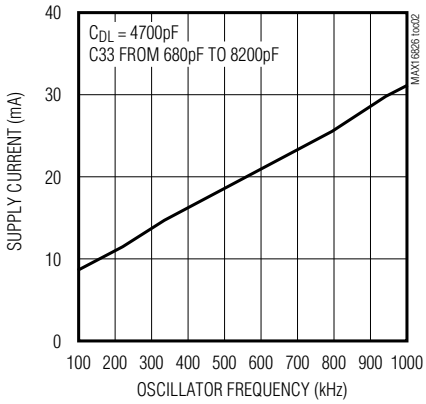
Typical Operating Characteristics

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF. T_A = +25°C, unless otherwise noted.)

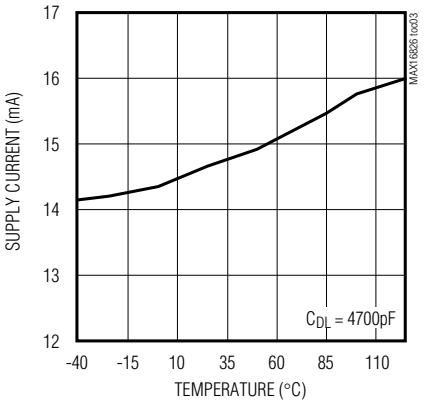
SUPPLY CURRENT vs. SUPPLY VOLTAGE



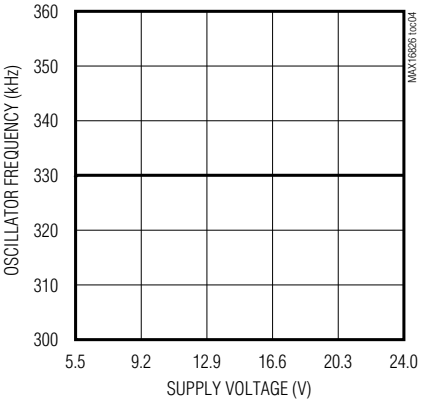
SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



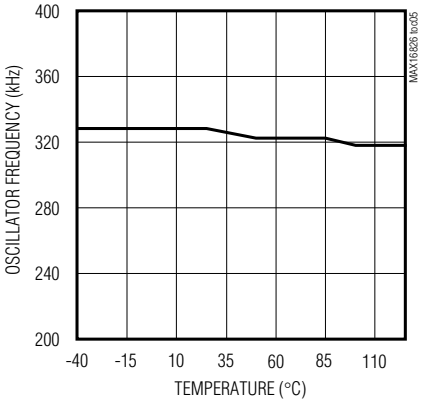
SUPPLY CURRENT vs. TEMPERATURE



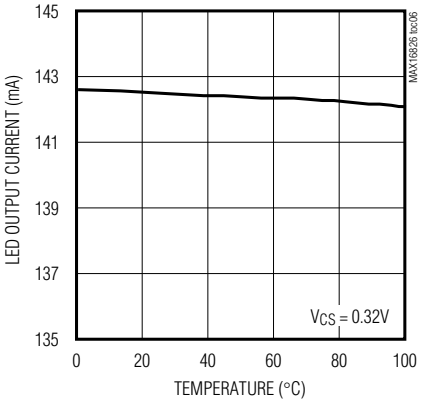
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



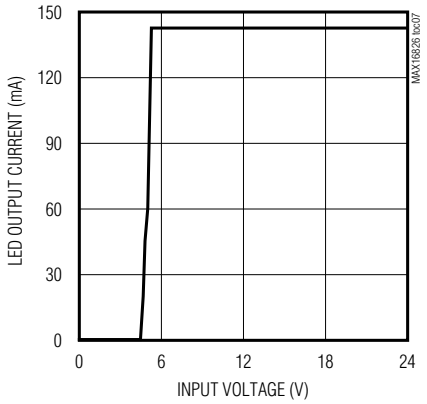
OSCILLATOR FREQUENCY vs. TEMPERATURE



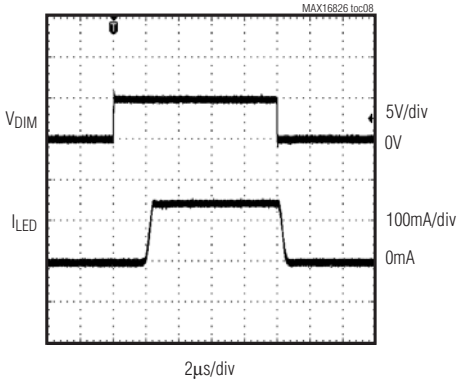
LED OUTPUT CURRENT vs. TEMPERATURE



LED OUTPUT CURRENT vs. INPUT VOLTAGE



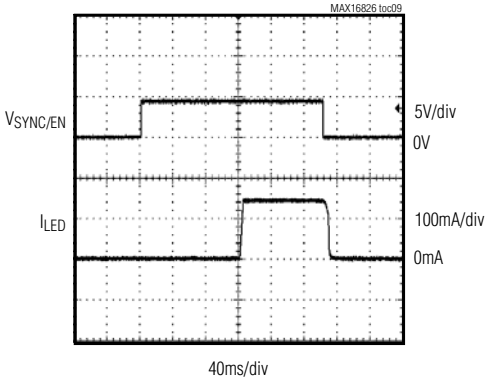
DIM INPUT TO ILED OUTPUT WAVEFORM



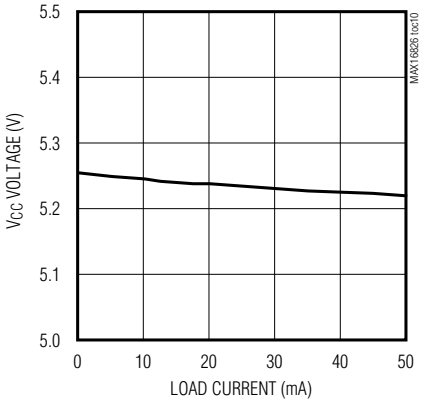
Typical Operating Characteristics (continued)

(V_{IN} = 12V, R19 = 2kΩ, C33 = 2200pF, R17 = 1.27kΩ, $C_{DL\_}$ = 0.01µF. T_A = +25°C, unless otherwise noted.)

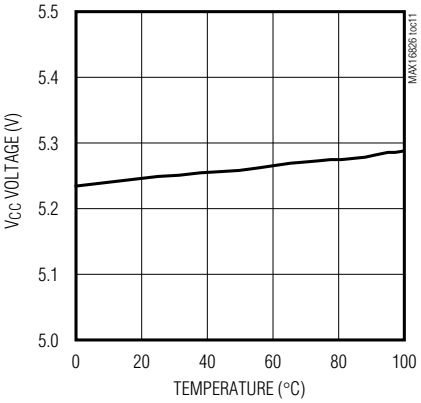
ENABLE AND DISABLE RESPONSE



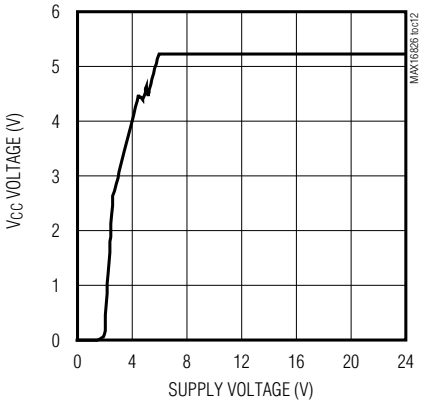
VCC VOLTAGE vs. LOAD CURRENT



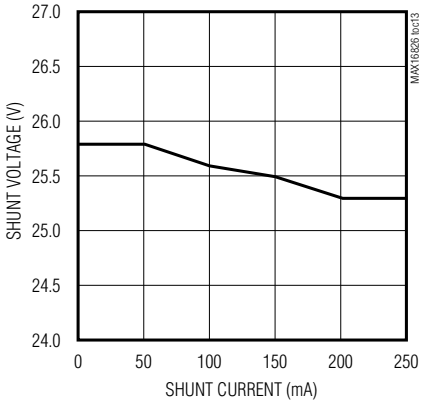
VCC VOLTAGE vs. TEMPERATURE



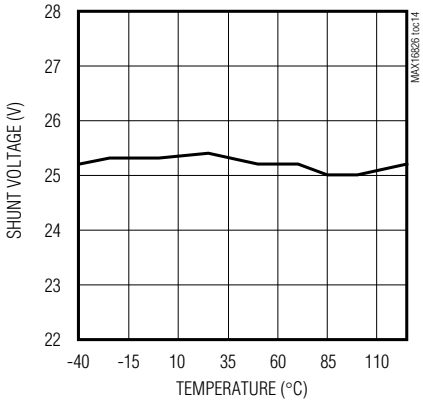
VCC VOLTAGE vs. SUPPLY VOLTAGE



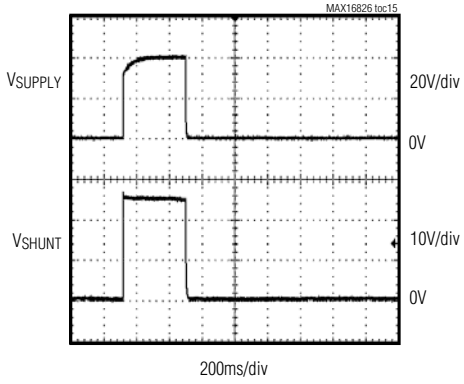
SHUNT VOLTAGE vs. SHUNT CURRENT



SHUNT VOLTAGE vs. TEMPERATURE



SHUNT REGULATOR LOAD DUMP RESPONSE



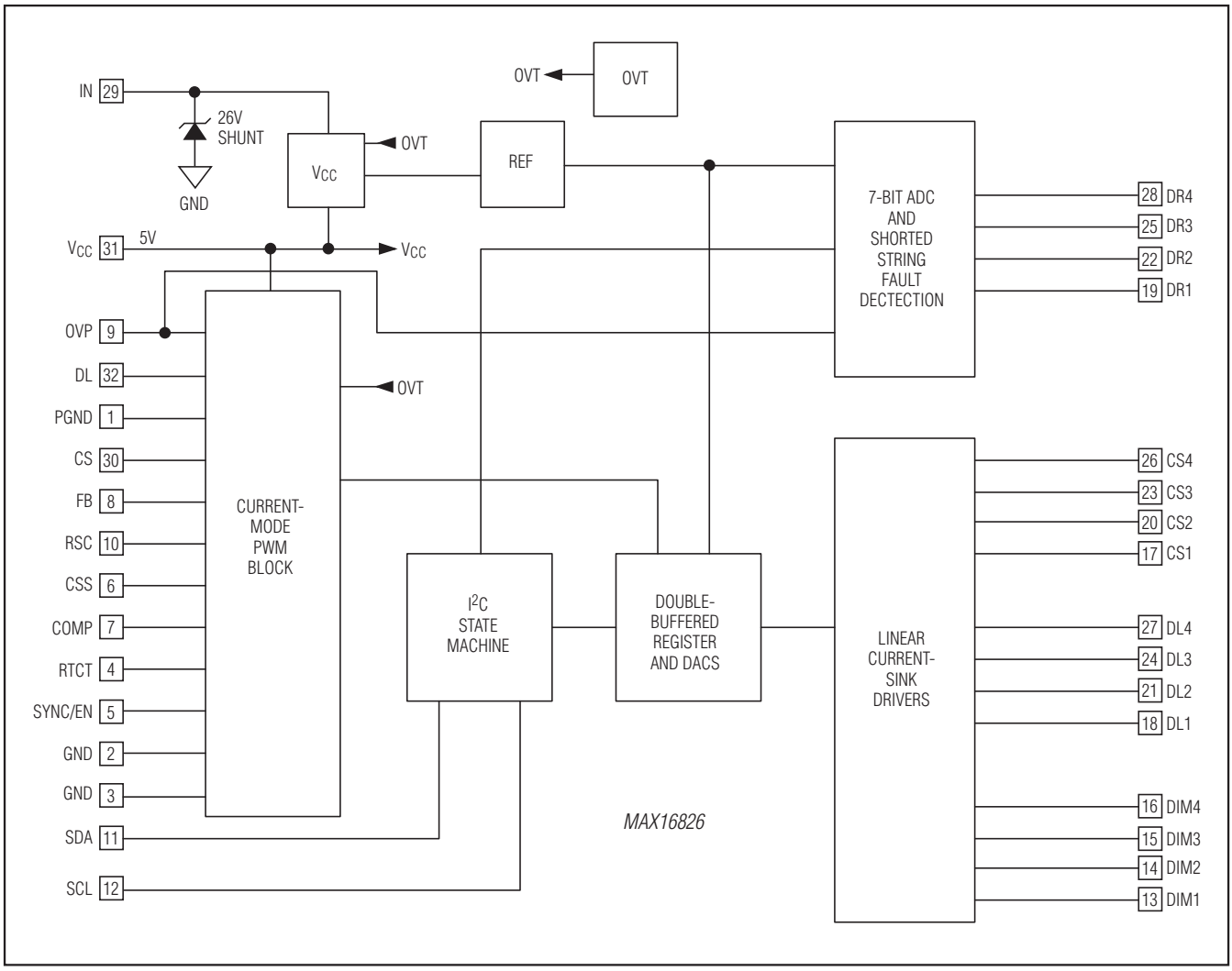
Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground
2, 3	GND	Analog Ground
4	RTCT	Timing Resistor and Capacitor Connection. A resistor, R19 (in the *Typical Application Circuit*), from V_{CC} to RTCT and a capacitor C33, from RTCT to GND set the oscillator frequency. See the *Oscillator* section to calculate RT and CT component values.
5	SYNC/EN	Synchronization and Enable Input. There are three operating modes: SYNC/EN = LOW: Low current shutdown mode with all circuits shut down except shunt regulator. SYNC/EN = HIGH: All circuits active with oscillator frequency set by RTCT network. SYNC/EN = CLOCKED: All circuits active with oscillator frequency set by SYNC clock input. Conversion cycles initiate on the rising edge of external clock input. The frequency programmed by R19/C33 must be 10% lower than the input SYNC/EN signal frequency.
6	CSS	Soft-Start Timing Capacitor Connection. Connect a capacitor from CSS to GND to program the required soft-start time for the switching regulator output voltage to reach regulation. See the *Soft-Start (CSS)* section to calculate C_{CSS}.
7	COMP	Switching Regulator Compensation Component Connection. Connect the compensation network between COMP and FB.
8	FB	Switching Regulator Feedback Input. Connect FB to the center of a resistor-divider connected between the switching regulator output and GND to set the output voltage. FB is regulated to a voltage set by an internal register. See the *Setting Output Voltage* section for calculating resistor values.
9	OVP	Switching Regulator Overvoltage Input. Connect OVP to the center of a resistor-divider connected between the switching regulator output and GND. For normal operation, configure the resistor-divider so that the voltage at this pin does not exceed 1.25V. If operation under load dump conditions is also required, configure the resistor-divider so that the voltage at OVP is less than 1.25V.
10	RSC	Slope Compensation Resistor and PWM Comparator Input Connection. Connect a resistor, R17, from RSC to the switching current-sense resistor to set the amount of the compensation ramp. See the *Slope Compensation (RSC)* section for calculating the value.
11	SDA	I^2C Serial Data Input/Output
12	SCL	I^2C Serial Clock Input
13	DIM1	LED String 1 Logic-Level PWM Dimming Input. A high logic level on DIM1 enables the current sink to operate at the maximum current as determined by its sense resistor and internal register value. A low logic level disables the current source.
14	DIM2	LED String 2 Logic-Level PWM Dimming Input. A high logic level on DIM2 enables the current sink to operate at the maximum current as determined by its sense resistor and internal register value. A low logic level disables the current source.
15	DIM3	LED String 3 Logic-Level PWM Dimming Input. A high logic level on DIM3 enables the current sink to operate at the maximum current as determined by its sense resistor and internal register value. A low logic level disables the current source.
16	DIM4	LED String 4 Logic-Level PWM Dimming Input. A high logic level on DIM4 enables the current sink to operate at the maximum current as determined by its sense resistor and internal register value. A low logic level disables the current source.
17	CS1	LED String 1 Current-Sense Input. CS1 is regulated to a value set by an internal register. The regulation voltage can be set between 97mV and 316mV.

Pin Description (continued)

PIN	NAME	FUNCTION
18	DL1	LED String 1 Linear Current Source Output. DL1 drives the gate of the external FET on LED String 1 and has approximately 15mA source/sink capability. Connect a minimum capacitor of 4700pF from DL1 to GND to compensate the internal transconductance amplifier as well as program the rise and fall times of the LED currents.
19	DR1	LED String 1 External FET Drain Voltage Sense. The internal ADC uses this input to measure the drain to GND voltage of the current sink FET. Drain voltage measurement information can be read back from the I^2C interface. Connect a voltage-divider to scale drain voltage as necessary.
20	CS2	LED String 2 Current-Sense Input. CS2 is regulated to a value set by an internal register. The regulation voltage can be set between 97mV and 316mV.
21	DL2	LED String 2 Linear Current Source Output. DL2 drives the gate of the external FET on LED String 2 and has approximately 15mA source/sink capability. Connect a minimum capacitor of 4700pF from DL2 to GND to compensate the internal transconductance amplifier, as well as program the rise and fall times of the LED currents.
22	DR2	LED String 2 External FET Drain Voltage Sense. The internal ADC uses this input to measure the drain to GND voltage of the current sink FET. Drain voltage measurement information can be read back from the I^2C interface. Connect a voltage-divider to scale drain voltage as necessary.
23	CS3	LED String 3 Current-Sense Input. CS3 is regulated to a value set by an internal register. The regulation voltage can be set between 97mV and 316mV.
24	DL3	LED String 3 Linear Current Source Output. DL3 drives the gate of the external FET on LED String 3 and has approximately 15mA source/sink capability. Connect a minimum capacitor of 4700pF from DL3 to GND to compensate the internal transconductance amplifier, as well as program the rise and fall times of the LED currents.
25	DR3	LED String 3 External FET Drain Voltage Sense. The internal ADC uses this input to measure the drain to GND voltage of the current sink FET. Drain voltage measurement information can be read back from the I^2C interface. Connect a voltage-divider to scale drain voltage as necessary.
26	CS4	LED String 4 Current-Sense Input. CS4 is regulated to a value set by an internal register. The regulation voltage can be set between 97mV and 316mV.
27	DL4	LED String 4 Linear Current Source Output. DL3 drives the gate of the external FET on LED String 4 and has approximately 15mA source/sink capability. Connect a minimum capacitor of 4700pF from DL4 to GND to compensate the internal transconductance amplifier, as well as program the rise and fall times of the LED currents.
28	DR4	LED String 4 External FET Drain Voltage Sense. The internal ADC uses this input to measure the drain to GND voltage of the current sink FET. Drain voltage measurement information can be read back from the I^2C interface. Connect a voltage-divider to scale drain voltage as necessary.
29	IN	Power Supply. IN is internally connected to a 26V shunt regulator that sinks current. In conjunction with an external resistor it allows time-limited load dump events as high as 40V to be safely handled by the IC. Bypass IN to GND with a minimum 10µF capacitor.
30	CS	Current-Sense Input
31	V_{CC}	Gate Driver Regulator Output. Bypass V_{CC} to GND with a minimum 4.7µF ceramic capacitor. Gate drive current pulses come from the capacitor connected to V_{CC}. Place the capacitor as close as possible to V_{CC}. If IN is powered by a voltage less than 5.5V, connect V_{CC} directly to IN.
32	DL	Switching Regulator Gate Driver Output
—	EP	Exposed Pad. Connect the exposed pad to the ground plane for heatsinking. Do not use this pad as the only ground connection to the IC.

Simplified Block Diagram



Detailed Description

The MAX16826 HB LED driver integrates a switching regulator controller, a 4-channel linear current sink driver, a 7-bit ADC, and an I²C interface. The IC is designed to operate from a 4.75V to 24V input voltage range and can withstand automotive load dump transients up to 40V.

The current-mode switching regulator controller is configurable as a boost or SEPIC converter to regulate the voltage to drive the four strings of HB LEDs. Its programmable switching frequency (100kHz to 1MHz) allows the use of a small inductor and filter capacitors. The four current sink regulators use independent external current-sense resistors to provide constant currents for each string of LEDs. Four DIM inputs allow a very wide range of independent pulsed dimming to each LED string. An internal 7-bit ADC measures the drain voltage of the external driver transistors to enable output voltage optimization and fault monitoring of the LEDs. The MAX16826 is capable of driving four strings of LEDs. The number of LEDs in each string is only limited by the topology of choice, the rating of the external components, and the resolution of the ADC and internal DAC.

The MAX16826 provides additional flexibility with an internal I²C serial interface to communicate with a microcontroller (µC). The interface can be used to dynamically adjust the amplitude of the LED current in each LED string and the switch-mode regulator output voltage. It can also be used to read the ADC drain voltage measurements for each string, allowing a µC to dynamically adjust the output voltage to minimize the power dissipation in the LED current sink FETs. The I²C interface can also be used to detect faults such as LED short or open.

Modes of Operation

The MAX16826 has six modes of operation: normal mode, undervoltage lockout (UVLO) mode, thermal shutdown (TSD) mode, shutdown (SHDN) mode, standby (STBY) mode, and overvoltage protection (OVP) mode.

The normal mode is the default state where each current sink regulator is maintaining a constant current through each of the LED strings. Digitized voltage feedback from the drains of the current sink FETs can be used to establish a secondary control loop by using an external µC to control the output of the switching stage for the purpose of achieving low-power dissipation across these FETs.

UVLO mode occurs when V_{VCC} goes below 4.3V. In UVLO mode, each of the linear current sinks and the switching regulator is shut down until the input voltage exceeds the rising UVLO threshold.

TSD mode occurs when the die temperature exceeds the internally set thermal limit (+160°C). In TSD mode, each of the linear regulators and the switching regulator is shut down until the die temperature cools by 20°C.

SHDN mode occurs when SYNC/EN is driven low. In SHDN mode, all internal circuitry with the exception of the shunt regulator is deactivated to limit current draw to less than 50µA. SHDN mode disengages when SYNC/EN is driven high or clocked.

STBY mode is initiated using the I²C interface. In STBY mode, each of the linear current sinks and the switching regulator is shut down. STBY mode is also deactivated using the I²C interface. In STBY mode, the internal V_{CC} regulator and the shunt regulator remain active. Whenever the MAX16826 enters a mode that deactivates the switching regulator, the soft-start capacitor is discharged so that soft-start occurs upon reactivation.

OVP mode occurs when the voltage at OVP is higher than the internal reference. In OVP mode, the switching regulator gate-drive output is latched off and can only be restored by cycling enable, power, or entering standby mode.

Switching Preregulator Stage

The MAX16826 features a current-mode controller that is capable of operating in the frequency range of 100kHz to 1MHz. Current-mode control provides fast response and simplifies loop compensation.

Output voltage regulation can be achieved in a two-loop configuration. A required conventional control loop can be set up by using the internal error amplifier with its inverting input connected to FB. The bandwidth of this loop is set to be as high as possible utilizing conventional compensation techniques. The noninverting input of this amplifier is connected to a reference voltage that is dynamically adjustable using the I²C interface. The optional slower secondary loop consists of the external µC using the I²C interface reading out the voltages at the drains of the current sink FETs and adjusting the reference voltage for the error amplifier.

To regulate the output voltage, the error amplifier compares the voltage at FB to the internal 1.25V (adjustable down by using the I²C interface) reference. The output of the error amplifier is compared to the sum of the current-sense signal and the slope compensation ramp at RSC to control the duty cycle at DL.

Two current-limit comparators also monitor the voltage across the sense resistor using CS. If the primary current-limit threshold is reached, the FET is turned off and remains off for the reminder of the switching cycle. If the current through the FET reaches the secondary current limit, the switching cycle is terminated and the soft-start capacitor is discharged. The converter then restarts in soft-start mode preventing inductor current runaway due to the delay of the primary cycle-by-cycle current limit. The switching regulator controller also features an overvoltage protection circuit that latches the gate driver off if the voltage at OVP exceeds the internal 1.25V reference voltage.

Shunt Regulator

The MAX16826 has an internal 26V (typ) shunt regulator to provide the primary protection against an automotive load dump. When the input voltage is below 26V, the shunt voltage at IN tracks the input voltage. When the input voltage exceeds 26V, the shunt regulator turns on to sink current, and the voltage at IN is clamped to 26V. During a load dump, the input voltage can reach 40V, and the shunt regulator through the resistor connected to IN is forced to sink large amounts of current for up to 400ms to limit the voltage that appears at IN to the shunt regulation voltage. The sinking current of the shunt regulator is limited by the value of resistor (R1 in Figure 1) in series with IN. There are two criteria that determine the value of R1: the maximum acceptable shunt current during load dump, and the voltage drop on R1 under normal operating conditions with low battery voltage. For example, with typical 20mA input current in normal operation, 250mA load dump current limit, 40V maximum load dump voltage, the R1 value is:

$$R1 = \frac{V_{INMIN} - V_{INREG}}{I_Q} = \frac{7.5 - 5.5}{20 \times 10^{-3}} = 100\Omega$$

where V_{INMIN} is the minimum operating voltage and V_{INREG} is the minimum acceptable voltage at IN.

Use the following equation to verify that the current through R1 is less than 250mA under a load-dump condition:

$$I_{LD} = \frac{V_{LD} - 26V}{R1} = \frac{40 - 26}{100} = 140mA$$

For stable operation, the shunt regulator requires a minimum 10µF of ceramic capacitance from IN to GND.

V_{CC} Regulator

The 5.25V V_{CC} regulator provides bias for the internal circuitry including the bandgap reference and gate drivers. Externally bypass V_{CC} with a minimum 4.7µF ceramic capacitor. V_{CC} has the ability to supply up to 50mA of current, but external loads should be minimized so as not to take away drive capability for internal circuitry. If IN is powered by a voltage less than 5.5V, connect V_{CC} directly to IN.

Switch-Mode Controller

The MAX16826 consists of a current-mode controller that is capable of operating in the 100kHz to 1MHz frequency range (Figure 2). Current-mode control provides fast response and simplifies loop compensation. The error amplifier compares the voltage at FB to 1.25V and varies the COMP output accordingly to regulate. The PWM comparator compares the voltage at COMP with the voltage at RSC to determine the switching duty cycle. The primary cycle-by-cycle current-limit comparator interrupts the on-time if the sense voltage is larger than 200mV. When the sense voltage is larger than 270mV, the secondary gross current-limit comparator is activated to discharge the soft-start capacitor. This forces the IC to re-soft-start preventing inductor current runaway due to the delay of the primary cycle-by-cycle current limit.

The switch-mode controller also features a low current shutdown mode, adjustable soft-start, and thermal shutdown protection.

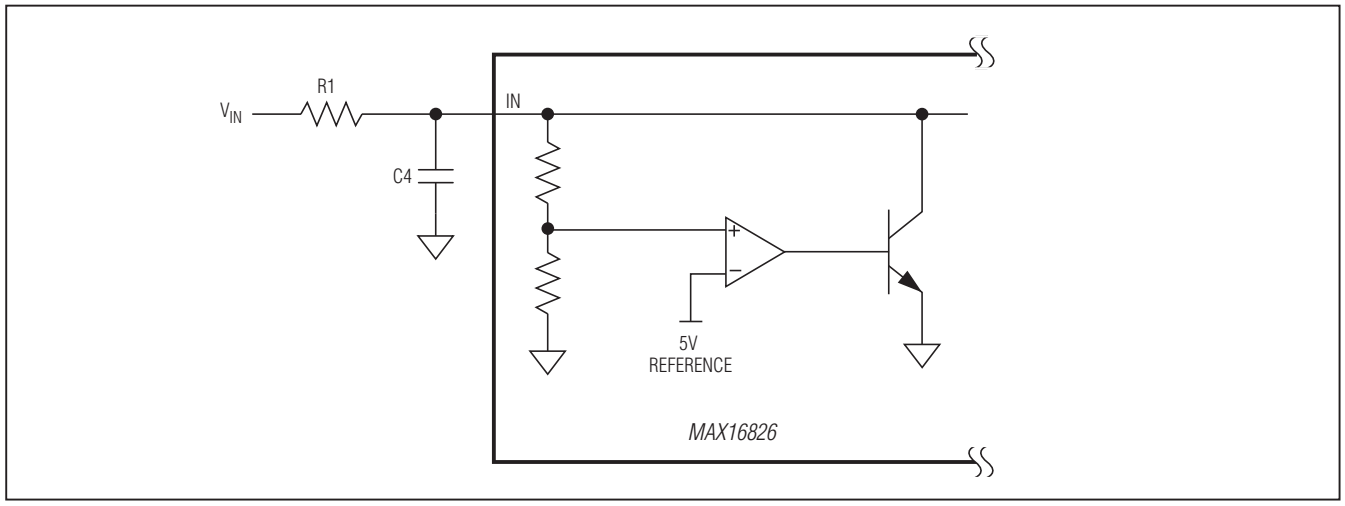


Figure 1. Shunt Regulator Block Diagram

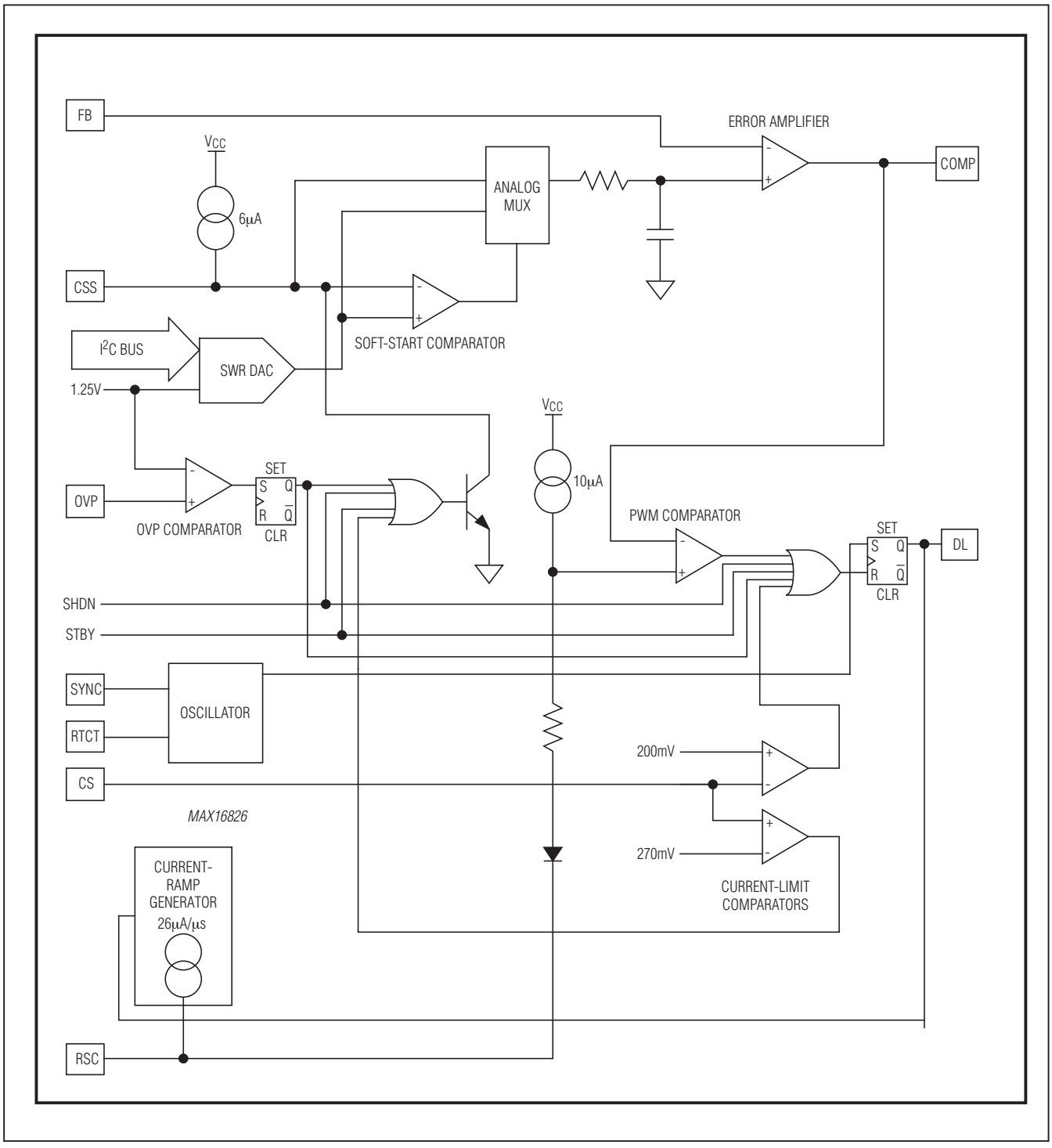


Figure 2. Switch Regulator Controller Block Diagram

Oscillator

The MAX16826 oscillator frequency is programmable using an external capacitor (C33 in the *Typical Application Circuit*) and a resistor (R19) at RTCT. R19 is connected from RTCT to V_{CC} and C33 is connected from RTCT to GND. C33 charges through RT until V_{RTCT} reaches 2.85V. CT then discharges through an 8.4mA internal current sink until V_{RTCT} drops to 1.2V. C33 is then allowed to charge through R19 again. The period of the oscillator is the sum of the charge and discharge times of C3. Calculate these times as follows:

The charge time is:

$$t_C = 0.55 \times R19 \times C33$$

The discharge time is:

$$t_D = R19 \times C33 \times \ln\left((R19 - 281.86)/(R19 - 487.45)\right)$$

where t_C and t_D is in seconds, R19 is in ohms (Ω), and C33 is in farads (F).

The oscillator frequency is then:

$$f_{OSC} = \frac{1}{t_C + t_D}$$

The charge time (t_C) in relation to the period (t_C + t_D) sets the maximum duty cycle of the switching regulator. Therefore, the charge time (t_C) is constrained by the desired maximum duty cycle. Typically, the duty cycle should be limited to 95%. The oscillator frequency is programmable from 100kHz to 1MHz. The MAX16826 can be synchronized to an external oscillator through SYNC/EN.

Slope Compensation (RSC)

The MAX16826 uses an internal ramp generator for slope compensation to stabilize the current loop when the duty cycle exceeds 50%. A slope compensation resistor (R17 in the *Typical Application Circuit*) is connected between RSC and the switching current-sense resistor at the source of the external switching FET. When the voltage at DL transitions from low to high, a ramped current with a slope of 26µA/µs is generated and flows through the slope compensation resistor. It is effectively summed with the current-sense signal. When the voltage at DL is low, the current ramp is reset to 0. Calculate R17 as follows:

$$R17 = \frac{(V_{OUT} - V_{INMIN}) \times R12}{34.28 \times L1}$$

where V_{OUT} is the switching regulator output and V_{INMIN} is the minimum operating input voltage.

Current Limit (CS)

The MAX16826 includes a primary cycle-by-cycle, current-limit comparator and a secondary gross current-limit comparator to terminate the on-time or switch cycle during an overload or fault condition. The current-sense resistor (R12 in the *Typical Application Circuit*) connected between the source of the switching FET and GND and the internal threshold, set the current limit. The current-sense input (CS) has a voltage trip level (V_{CS}) of 200mV. Use the following equation to calculate R39:

$$R12 = V_{CS}/I_{PK}$$

where I_{PK} is the peak current that flows through the switching FET. When the voltage across R12 exceeds the current-limit comparator threshold, the FET driver (DL) turns the switch off within 80ns. In some cases, a small RC filter may be required to filter out the leading-edge spike on the sensed waveform. Set the time constant of the RC filter at approximately 100ns and adjust as needed.

If, for any reason, the voltage at CS exceeds the 270mV trip level of the gross current limit as set by a second comparator, then the switching cycle is immediately terminated and the soft-start capacitor is discharged. This allows a new soft-start cycle and prevents inductor current buildup.

Soft-Start (CSS)

Soft-start is achieved by charging the external soft-start capacitor (C30 in the *Typical Application Circuit*) at startup. An internal fixed 6µA current source charges the soft-start capacitor until V_{CSS} reaches V_{CC}. To achieve the required soft-start timing for the switching regulator output voltage to reach regulation, the value of the soft-start capacitor at CSS is calculated as:

$$C30 = 6\mu A \times t_{SS}/V_{REF}$$

where t_{SS} is the required time to achieve the switching regulator output regulation and V_{REF} is the set FB regulation voltage. When the IC is disabled, the soft-start capacitor is discharged to GND.

Synchronization and Enable Input

The SYNC/EN input provides both external clock synchronization (if desired) and enable control. When SYNC/EN is held low, all circuits are disabled and the IC enters low-current shutdown mode. When SYNC/EN is high, the IC is enabled and the switching regulator clock uses the RTCT network to set the operating frequency. See the *Oscillator* section for details. The SYNC/EN can also be used for frequency synchronization by connecting it to an external clock signal from 100kHz to 1MHz. The switching cycle initiates on the

rising edge of the clock. When using external synchronization, the clock frequency set by RTCT must be 10% lower than the synchronization signal frequency.

Overvoltage Protection (OVP)

OVP limits the maximum voltage of the switching regulator output for protection against overvoltage due to circuit faults, for example a disconnected FB. Connect OVP to the center of a resistor-divider connected between the switching regulator output and GND to set the output-voltage OVP limit. Typically, the OVP output voltage limit is set higher than the load dump voltage.

Calculate the value of R15 and R16 as follows:

$$R15 = (V_{OVP}/1.25 - 1) \times R16$$

Or to calculate V_{OVP}:

$$V_{OVP} = 1.25 \times (1 + R15/R16)$$

where R15 and R16 are shown in the *Typical Application Circuit*. The internal OVP comparator compares the voltage at OVP with the internal reference (1.25V typ) to decide if an overvoltage error occurs. If an overvoltage error is detected, switching stops, the switching regulator gate-drive output is latched off, and the soft-start capacitor is discharged. The latch can only be reset by toggling SYNC/EN, activating the I^2C standby mode, or cycling power.

The internal ADC also uses OVP to sense the switching regulator output voltage. Output voltage measurement information can be read back from the I^2C interface. Voltage is digitized to 7-bit resolution.

Undervoltage Lockout (UVLO)

When the voltage at V_{CC} is below the V_{CC} undervoltage threshold (V_{VCC_UVLO}, typically 4.3V falling), the MAX16826 enters undervoltage lockout. V_{CC} UVLO forces the linear regulators and the switching regulator into shutdown mode until the V_{CC} voltage is high enough to allow the device to operate normally. In V_{CC} UVLO, the V_{CC} regulator remains active.

Thermal Shutdown

The MAX16826 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds +160°C. The outputs are enabled again when the die temperature drops below +140°C. In thermal shutdown, all internal circuitry is shut down with the exception of the shunt regulator.

Linear Current Sources (CS1–CS4, DL1–DL4)

The MAX16826 uses transconductance amplifiers to control each LED current sink. The amplifier outputs (DL1–DL4) drive the gates of the external current sink FETs (Q2 to Q5 in the *Typical Application Circuit*). The source of each MOSFET is connected to GND through a current-sense resistor. CS1–CS4 are connected to the respective inverting input of the amplifiers and also to the source of the external current sink FETs where the LED string current-sense resistors are connected. The noninverting input of each amplifier is connected to the output of an internal DAC. The DAC output is programmable using the I^2C interface to output between 97mV and 316mV. The regulated string currents are set by the value of the current-sense resistors (R28 to R31 in the *Typical Application Circuit*) and the corresponding DAC output voltages.

LED PWM Dimming (DIM1–DIM4)

The MAX16826 features a versatile dimming scheme for controlling the brightness of the four LED strings. Independent LED string dimming is accomplished by driving the appropriate DIM1–DIM4 inputs with a PWM signal with a frequency up to 100kHz. Although the brightness of the corresponding LED string is proportional to the duty cycle of its respective PWM dimming signal, finite LED current rise and fall times limit this linearity when the dim pulse width approaches 2µs. Each LED string can be independently controlled. Simultaneous control of the PWM dimming and the LED string currents in an analog way over a 3:1 range provides great flexibility allowing independent two-dimensional brightness control that can be used for color point setup and brightness control.

Analog-to-Digital Converter (ADC)

The MAX16826 has an internal ADC that measures the drain voltage of the external current sink driver FETs (Q2 to Q5 in the *Typical Application Circuit*) using DR1 - DR4 and the switching regulator output voltage using OVP. Fault monitoring and switching stage output-voltage optimization is possible by using an external microcontroller to read out these digitized voltages through the I^2C interface. The ADC is a 7-bit SAR (successive-approximation register) topology. It sequentially samples and converts the drain voltage of each channel and V_{OVP}. An internal 5-channel analog MUX is used to select the channel the ADC is sampling. Conversions are driven by an internally generated 1MHz clock and gated by the external dimming signals. After a conversion, each measurement is stored into its respective register and can be accessed through the I^2C interface. The digital circuitry that controls the analog MUX includes a 190ms timer. If the ADC does not complete a conversion within this 190ms measurement window then the analog MUX will sequence to the next channel. For the ADC to complete one full conversion, the cumulative PWM dimming on-time must be greater than 10µs within the 190ms measurement window. The minimum PWM dimming on-time

is 2µs, so the ADC requires at least 5 of these minimum pulses within the 190ms measurement window to complete a conversion. During PWM dimming, LED current pulse widths of less than 2µs are possible, but the ADC may not have enough sampling time to complete a conversion in this scenario and the corresponding data may be incomplete or inaccurate. Therefore, adaptive voltage optimization may not be possible when the LED current-pulse duration is less than 2µs. The LED current pulse duration is shorter than the pulse applied at the DIM_ inputs because of the LED turn-on delay.

Faults and Fault Detection

The MAX16826 features circuitry that automatically detects faults such as overvoltage or shorted LED string. An internal fault register at the address OAh is used to record these faults. For example, if a shorted LED string is detected, the corresponding fault register bit is set and the faulty output is shut down.

Shorted LED strings are detected with fast comparators connected to DR1–DR4. The trip threshold of these comparators is 1.52V (typ). When this threshold is exceeded, the shorted string is latched off and the corresponding bit of register OAh is set.

After the internal ADC completes a conversion, the result is stored in the corresponding register and can be read out by the external µC. The µC then compares the conversion data with the preset limit to determine if there is a fault.

When an LED string opens, the voltage at the corresponding current-sink FET drain node goes to 0V. However, the ADC can only complete a conversion if the LED current comes into regulation. If an LED string opens before the LED current can come into regulation, the ADC cannot complete a conversion and the MSB (eighth bit) is set to indicate an incomplete conversion or timeout condition. Thus, an examination of the MSB provides an indication that the LED string is open. If the LED string opens after the LED current is in regulation, the ADC can make conversions and reports that the drain voltage is 0V. Therefore, to detect an open condition, monitor the MSB and the ADC measurement. If the MSB is set and the CS_ on-time is greater than 2µs, or if the ADC measures 0 at the drain, then there is an open circuit.

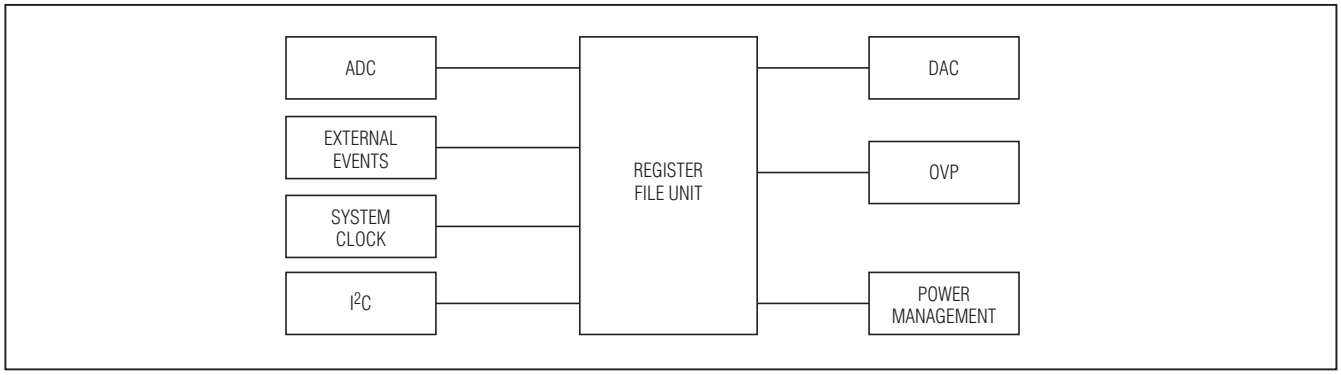


Figure 3. Digital Block Diagram

Table 1. ADC Response

CONDITION	ADC RESPONSE
Shorted string fault	Load full-scale code into register, no conversions on affected channel until power or enable is cycled.
Shorted string fault while converting	Immediately load full-scale code into register and cease conversion effort on this channel until power or enable is cycled.
ADC register read when it is being updated	Previous sample is shifted out through the I2C interface and then the register is updated with the new measurement.
UVLO	Immediately terminate conversions, do not update current register.
STBY	Immediately terminate conversions, do not update current register.
SHDN	Immediately terminate conversions, do not update current register.

Overview of the Digital Section

Figure 3 shows the block diagram of the digital section in the MAX16826. The I²C serial interface provides flexible control of the IC and is in charge of writing/reading to/from the register file unit. The ADC block is a 7-bit 5-channel SAR ADC. The eighth bit of the ADC data register indicates an incomplete conversion or timeout has occurred. This bit is set whenever the LED current fails to come into regulation during the DIM PWM on-time. This indicates there is either an LED open condition or the CS_ on-time is less than 2µs.

A reason for this among other possibilities is an open LED string condition. This eighth or MSB bit can be tested to determine open string faults.

I²C Interface

The MAX16826 internal I²C serial interface provides flexible control of the amplitude of the LED current in each string and the switch-mode regulator output voltage. It is also able to read the current sink FET drain voltages, as well as the switching regulator output voltage through OVP and thus enable some fault detection and power dissipation minimization. By using an external µC, the MAX16826 internal control and status registers are also accessed through the standard bidirectional, 2-wire, I²C serial interface.

The I²C interface provides the following I/O functions and programmability:

- Current sink FET drain and switching regulator output-voltage measurement. The measurement for each channel and the regulator output is stored in its respective register and can be accessed through the I²C interface. The SAR ADC measures the drain voltage of each current sink FET sequentially. This uses one 8-bit register for each channel to store the measurement made by the 7-bit SAR ADC and 1 bit to indicate a timeout during the ADC conversion cycle.
- Adjustment of the switching regulator output. This is used for adaptive voltage optimization to improve overall efficiency. The switching regulator output is downward adjustable by changing its reference voltage. This uses a 7-bit register.
- Adjustment of the reference voltage of the current-sink regulators. The reference voltage at the noninverting input of each of the linear regulator drive amplifiers can be changed to make adjustments in the current of each LED string for a given sense resistor. The output can be adjusted down from a maximum of 316mV to 97mV in 1.72mV increments.
- Fault reporting. When a shorted string fault or an overvoltage fault occurs, the fault is recorded.
- Standby mode. When a one is entered into the standby register the IC goes into standby mode.

The 7-bit I²C address is 58h and the 8-bit I²C address is B1h for a read operation and B0h for a write operation. Address the MAX16826 using the I²C interface to read the state of the registers or to write to the registers. Upon a read command, the MAX16826 transmits the data in the register that the address register is pointing to. This is done so that the user has the ability to confirm the data written to a register before the output is enabled. Use the fault register to diagnose any faults.

Serial Addressing

The I²C interface consists of a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between the master and the slave. The MAX16826 is a slave-only device, relying upon a master to generate a clock signal. The master initiates data transfer to and from the MAX16826 and generates SCL to synchronize the data transfer (Figure 4).

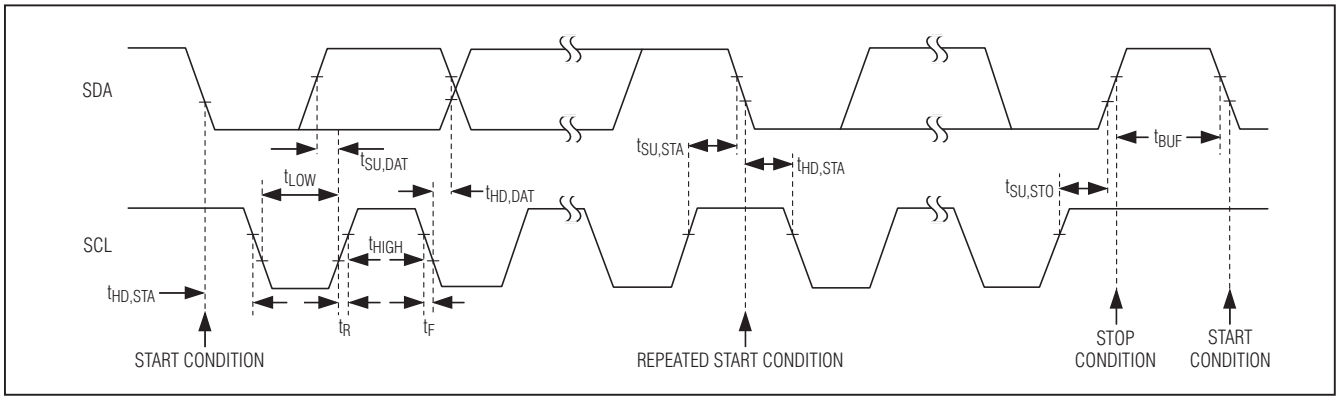


Figure 4. 2-Wire Serial Interface Timing Detail

I²C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage using a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to ensure proper device operation.

A bus master initiates communication with the MAX16826 as a slave device by issuing a START condition followed by the MAX16826 address. The MAX16826 address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). After receiving the proper address, the MAX16826 issues an acknowledge bit by pulling SDA low during the ninth clock cycle.

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the MAX16826, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 4). Both START and STOP conditions are generated by the bus master.

Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock (Figure 5).

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data (Figure 6). After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse, such that the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the MAX16826, it releases the SDA line and the MAX16826 takes the control of SDA line and generates the acknowledge bit. When SDA remains high during this 9th clock pulse, this is defined as the not acknowledge signal. The master then generates either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

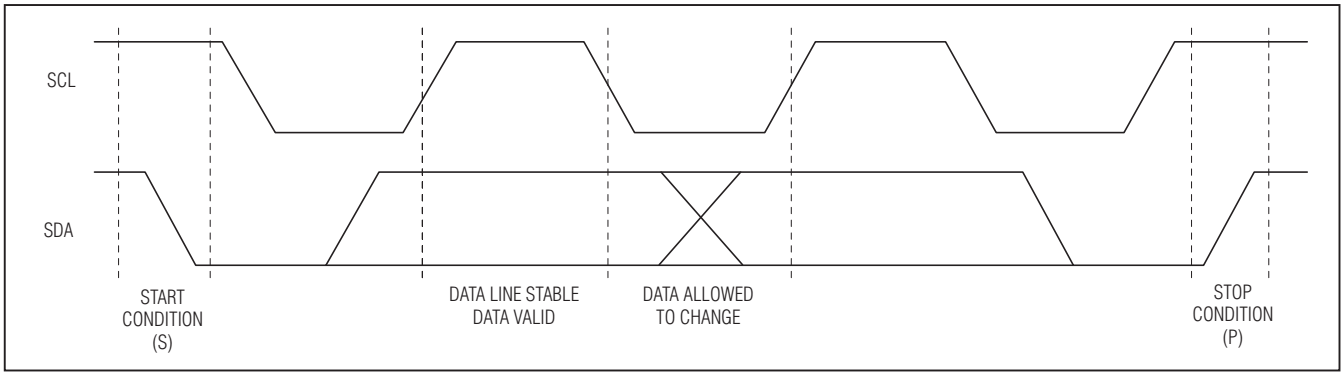


Figure 5. Bit Transfer

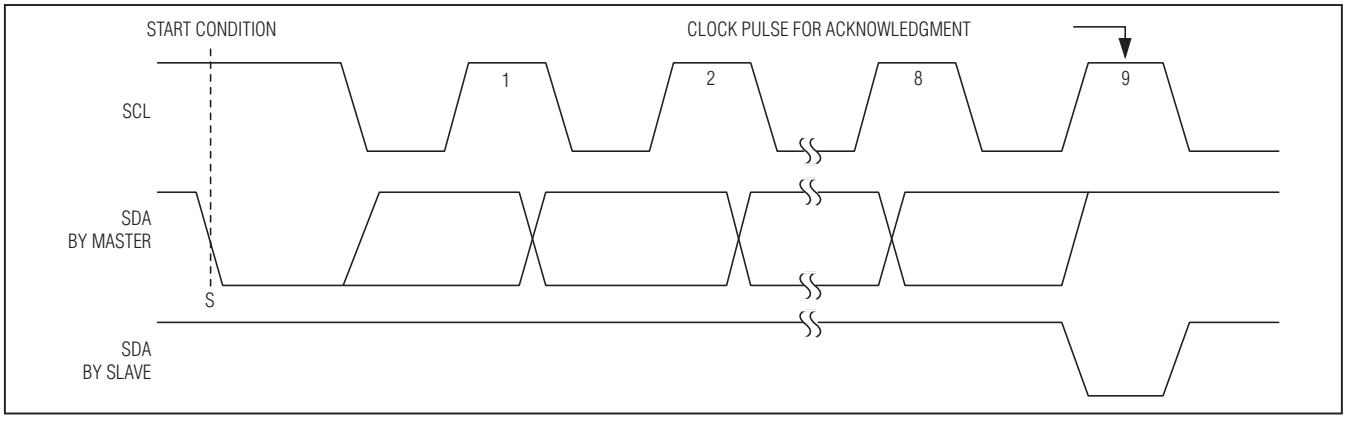


Figure 6. Acknowledge

Accessing the MAX16826

The communication between the µC and the MAX16826 is based on the usage of a set of protocols defined on top of the standard I²C protocol definition. They are exclusively write byte(s) and read byte(s).

Write Byte(s)

The write byte protocol is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address followed by a write bit (low).
3) The addressed slave asserts an ACK by pulling SDA low.
4) The master sends an 8-bit command code.
5) The slave asserts an ACK by pulling SDA low.
6) The master sends an 8-bit data byte.
7) The slave acknowledges the data byte.
8) The master generates a STOP condition or repeats 6 and 7 to write next byte(s).

The command is interpreted as the destination address (register file unit) and data is written in the addressed location. The slave asserts a NACK at step 5 if the command is not valid. The master then interrupts the communication by issuing a STOP condition. If the address is correct, the data byte is written to the addressed register. After the write, the internal address pointer is increased by one. When the last location is reached, it cycles to the first register.

Read Byte(s)

The read sequence is:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends an 8-bit command byte.
5) The active slave asserts an ACK on the data line.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends an 8-bit data byte.
10) The master asserts a NACK on the data line to complete operations or asserts an ACK and repeats 9 and 10.
11) The master generates a STOP condition.

The data byte read from the device is the content of the addressed location(s). Once the read is done, the internal pointer is increased by one. When the last location is reached, it cycles to the first one. If the device is busy or the address is not correct (out of memory map), the command code is not acknowledged and the internal address pointer is not altered. The master then interrupts the communication by issuing a STOP condition.

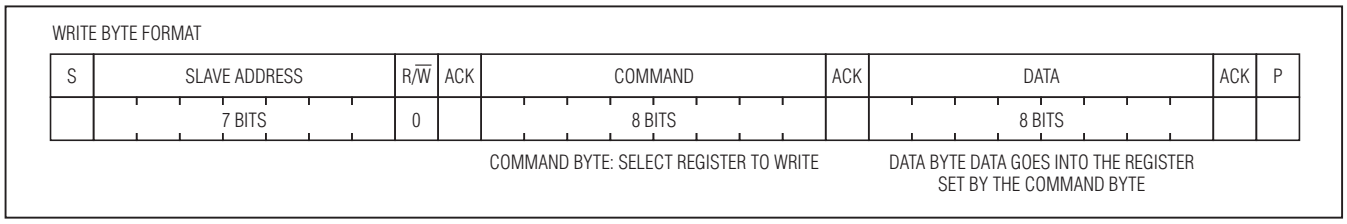


Figure 7. Write Byte Format

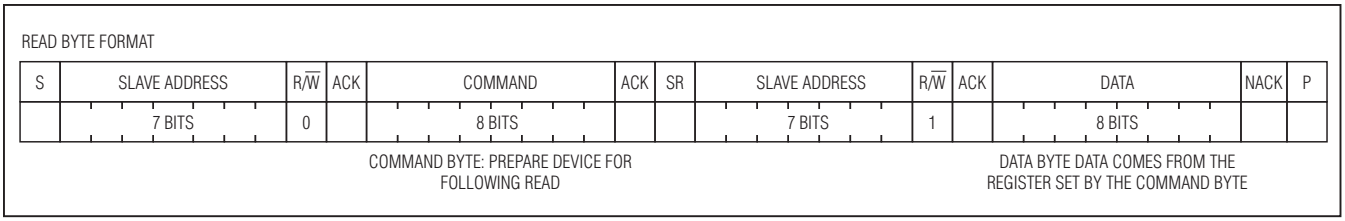


Figure 8. Read Byte Format

Register File Unit

The register file unit is used to store all the control information from the SDA line and configure the MAX16826 for different operating conditions. The register file assignments of the MAX16826 are in Table 2.

Registers 00h to 03h: String Current Programming

These registers are used to program LED string 1 to LED string 4 current sink values. For each LED string, CS1–CS4 inputs are connected to the source of the external current sink FET and internally are connected to the inverting input of the internal transconductance amplifier. The noninverting input of this amplifier is connected to the output of an internal DAC programmed by these registers. As the DAC is incremented, its output voltage decreases from 316mV to 97mV in 1.72mV steps by the data written in the register 00h to 03h; thus, the steady-state voltage at CS1–CS4 is given by the following formula:

$$V_{CS1,2,3,4} = 316mV - (1.72mV \times RegisterValue[6:0])$$

For example, if 00h is set to 20h, then the CS1 voltage is:

$$V_{CS1} = 316mV - 1.72mV \times 32 = 265.3mV$$

Register 04h: Switching Regulator Output Programming

Set the switching regulator output voltage by connecting FB to the center of a resistive voltage-divider between the switching regulator output and GND. V_{FB} is regulated to a voltage from 876mV to 1.25V (typ) set by the register 04h through the I^2C interface.

The FB reference voltage can be decreased from 1.25V, its maximum value, by approximately 2.9mV steps. The steady-state voltage at FB then is regulated to:

$$V_{FB} = 1.25V - (2.91mV \times 04h[6:0])$$

Registers 05h to 08h: External Current-Sink FET Drain Voltage ADC Readings

These registers store the drain voltages of the external current sink FETs. For each register, bits 6–0 are the conversion data of the ADC outputs. Bit 7 is used to show if the conversion is terminated by the ADC (indicated by 0) or if there is an internal timeout (indicated by 1). If the drain voltage exceeds the preset reference voltage, the corresponding LED string fault bit is asserted. See the *Faults and Fault Detection* section for more information on the internal timeout function.

Register 09h: Switching Regulator Voltage ADC Output

Bits 6-0 of this register store the voltage present at OVP. This voltage is a scaled down version of the switching regulator output voltage. Bit 7 is not used.

Register 0Ah: Fault Status Register

This register stores all the external events or fault information such as overvoltage and shorted LED string faults. The fault events are logged only if the system is not in standby mode and their active states are longer than one clock cycle. Cycle enable or power to clear the fault status register. Initiating standby mode using the I^2C interface can also be used to clear the fault status

Table 2. Register File Assignments

REGISTER ADDRESS	R/W	USED BIT RANGE	RESET VALUE	DESCRIPTION
00h	R/W	[6:0]	00h	LED String 1 current programming value.
01h	R/W	[6:0]	00h	LED String 2 current programming value.
02h	R/W	[6:0]	00h	LED String 3 current programming value.
03h	R/W	[6:0]	00h	LED String 4 current programming value.
04h	R/W	[6:0]	00h	Switching regulator output voltage programming value.
05h	R	[7:0]	00h	LED String 1 external FET drain voltage ADC output.
06h	R	[7:0]	00h	LED String 2 external FET drain voltage ADC output.
07h	R	[7:0]	00h	LED String 3 external FET drain voltage ADC output.
08h	R	[7:0]	00h	LED String 4 external FET drain voltage ADC output.
09h	R	[6:0]	00h	OVP voltage, ADC output.
0Ah	R	[5:0]	00h	Fault status register.
0Bh	R/W	[0]	00h	Device standby command.
0Ch	R	[2:0]	—	Device revision code.

register. First, activate standby mode and then deactivate this mode using the I²C interface. Next, perform a read operation on the fault status register. The old fault information is reported in this first read operation. The conclusion of the read operation clears the data contained in the register. Subsequent read o perations confirm that the fault status register has been cleared.

The description of this register is as follows:

Bit 0: Overvoltage sense flag. This flag is set if the voltage at OVP exceeds 1.25V; switching stops until power or the enable or standby is cycled.

- Bit 1: Not used.
- Bit 2: LED string 1 shorted flag. A diode short in LED string 1 has been detected if this bit is set.
- Bit 3: LED string 2 shorted flag. A diode short in LED string 2 has been detected if this bit is set.
- Bit 4: LED string 3 shorted flag. A diode short in LED string 3 has been detected if this bit is set.
- Bit 5: LED string 4 shorted flag. A diode short in LED string 4 has been detected if this bit is set.

Register 0Bh Bit 0: Device Standby Command

When register 0Bh bit 0 is set to 1, the IC enters a low-current standby mode. In this mode, the system clock is off and no operation is allowed. Set this bit to 0 to leave standby mode and back to normal operation mode.

Register 0Ch Bit 2-0: Device Revision Code

These 3 bits are a hardwired value that identifies the IC's revision.

Applications Information

Programming LED Currents

The MAX16826 uses sense resistors (R28, R29, R30, R31 in the *Typical Application Circuit*) to set the output current for each LED string. To set the LED current for a particular string, connect a sense resistor across the corresponding current-sense input (CS1–CS4) and GND. For optimal accuracy, connect the low-side of the current-sense resistors to GND with short traces. The value needed for the sense resistor for a given current is calculated with the equation below:

$$R31 = V_{CS1}/I_{OUT1}$$

where V_{CS1} can be set from 97mV to 316mV by the internal registers through the I²C interface and I_{OUT1} is the desired LED string 1 current.

Calculating the Value of Peak Current-Limit Resistor

The value of R12 sets the peak switching current that flows in the switching FET (Q1). Set the value of resistor R12 using the equation below:

$$R12 = 0.19/(1.2 \times I_{PK})$$

where I_{PK} is the peak inductor current at minimum input voltage and maximum load.

Boost Inductor Value

The value of the boost inductor is calculated using the following equation:

$$L1 = \frac{V_{INMIN} \times (V_{OUT} - V_{INMIN})}{V_{OUT} \times f_{SW} \times \Delta I_L}$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the desired output voltage, and f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak ripple in the boost inductor. Higher inductor values lead to lower ripple but at a higher cost and size. Choose an inductor value that gives peak-to-peak ripple current in the order of 30% to 40% of the average current in the inductor at low-line and full-rated load. This choice of inductor is a compromise between cost, size, and performance for the boost converter.

Setting Output Voltage

Set the switch regulator output voltage by connecting FB to the center of a resistive voltage-divider between the switching regulator output and GND. V_{FB} is regulated to a voltage from 0.88V to 1.25V (typ) set by an internal register through the I²C interface. Choose R13 and R14 in the *Typical Application Circuit* for a reasonable bias current in the resistive divider and use the following formula to set the output voltage:

$$V_{OUT} = (1 + R13/R14) \times V_{FB}$$

where V_{FB} is the regulated voltage set by the internal register.

Adaptive Voltage Optimization

The availability of the digitized switching regulator output voltage and current sink drain voltages and the ability to change the switching regulator output voltage provide the ability to do adaptive voltage optimization. A slow digital control loop is established with an external µC closing the loop. Firmware residing in the external µC is tasked to read each one of the current sink FET drain voltages and select the minimum value of the four LED strings. The minimum value is subtracted from the scaled output voltage reading, and then the switching regulator output is forced to maintain the difference required to provide current regulation in the current sink FETs.

Switching Noise Effects on ADC Readings

Excessive switching noise can corrupt the ADC readings on the current sink MOSFET drains. Proper PCB layout is critical to minimize this noise. The output diode should be selected appropriately. The capacitance and reverse recovery characteristics of the output diode contribute to ground noise. Diodes with lower capacitance and lower reverse recovery time will result in lower current spikes at the turn on edge of the boost switch. The lower current spike will result in lower ground noise. Another method to reduce the ground noise is to add a gate resistor in series with the gate of the switching MOSFET. For most applications the gate resistor should be in the range of 4.7 to 10ohms. Care must be taken in selecting the gate resistor value, due to power dissipation increase on the boost transistor. A higher resistor value reduces the switching noise, but power dissipation due to switching losses will increase. The ground noise should be measured by measuring the voltage between the ground of the input capacitor that is farthest from the IC on the PCB and the ground of the MAX16826. The pins 1,2 and 3 are the ground pins of the MAX16826. To prevent problems on the ADC readings of the MAX16826 the ground noise measured from the IC ground to the input capacitor ground should be less than 0.5V peak to peak on a wide bandwidth scope using a wide bandwidth probe. A wide bandwidth scope must have a bandwidth greater than 150MHz.

SEPIC Topology

The SEPIC power topology is very useful when the input voltage is expected to be higher or lower than the output voltage of the switching regulator stage as required by the number of LEDs used in a single string.

The SEPIC topology is more complex than the simple boost topology and it requires the use of two additional energy storage components, L2 and C25, in Figure 9.

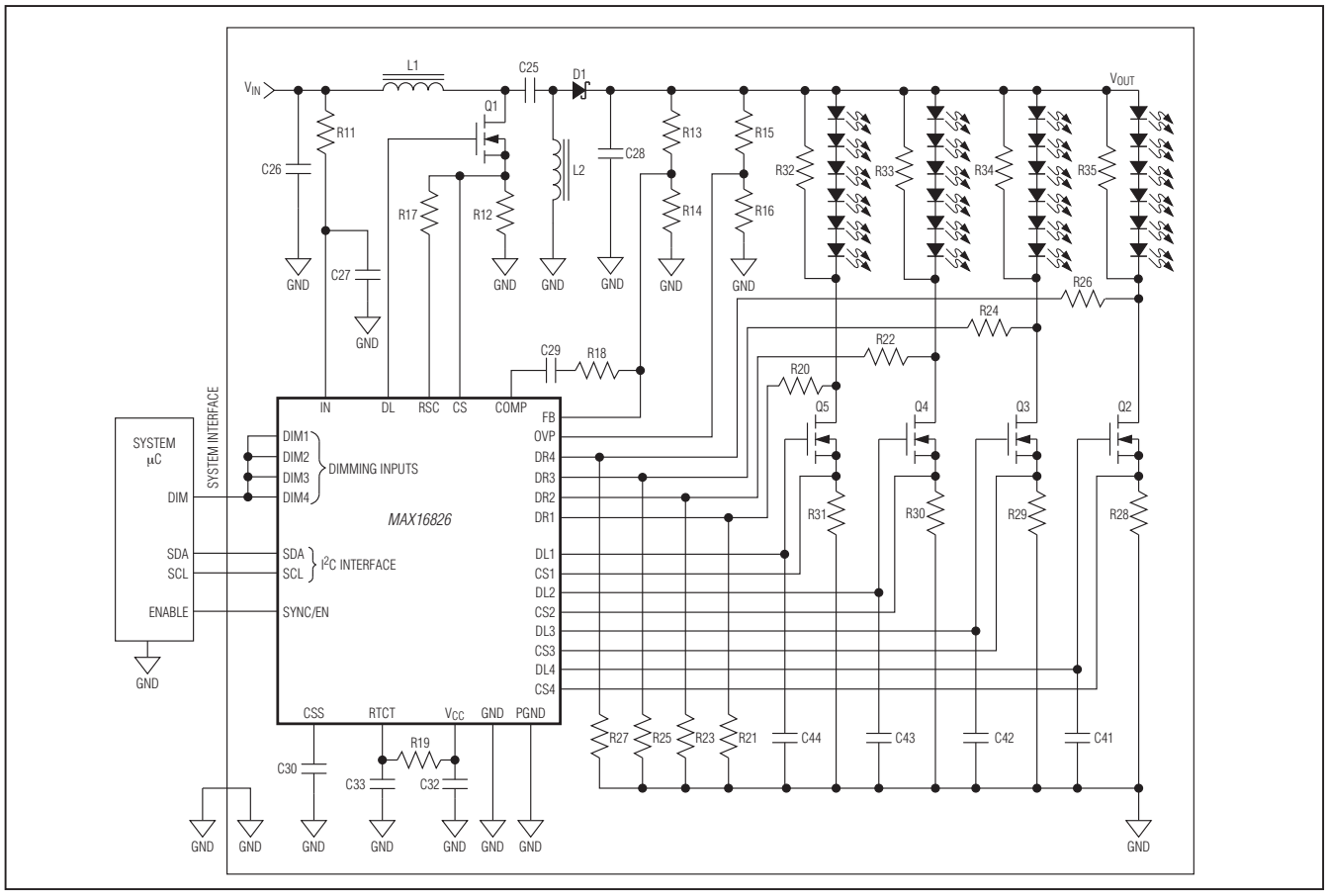


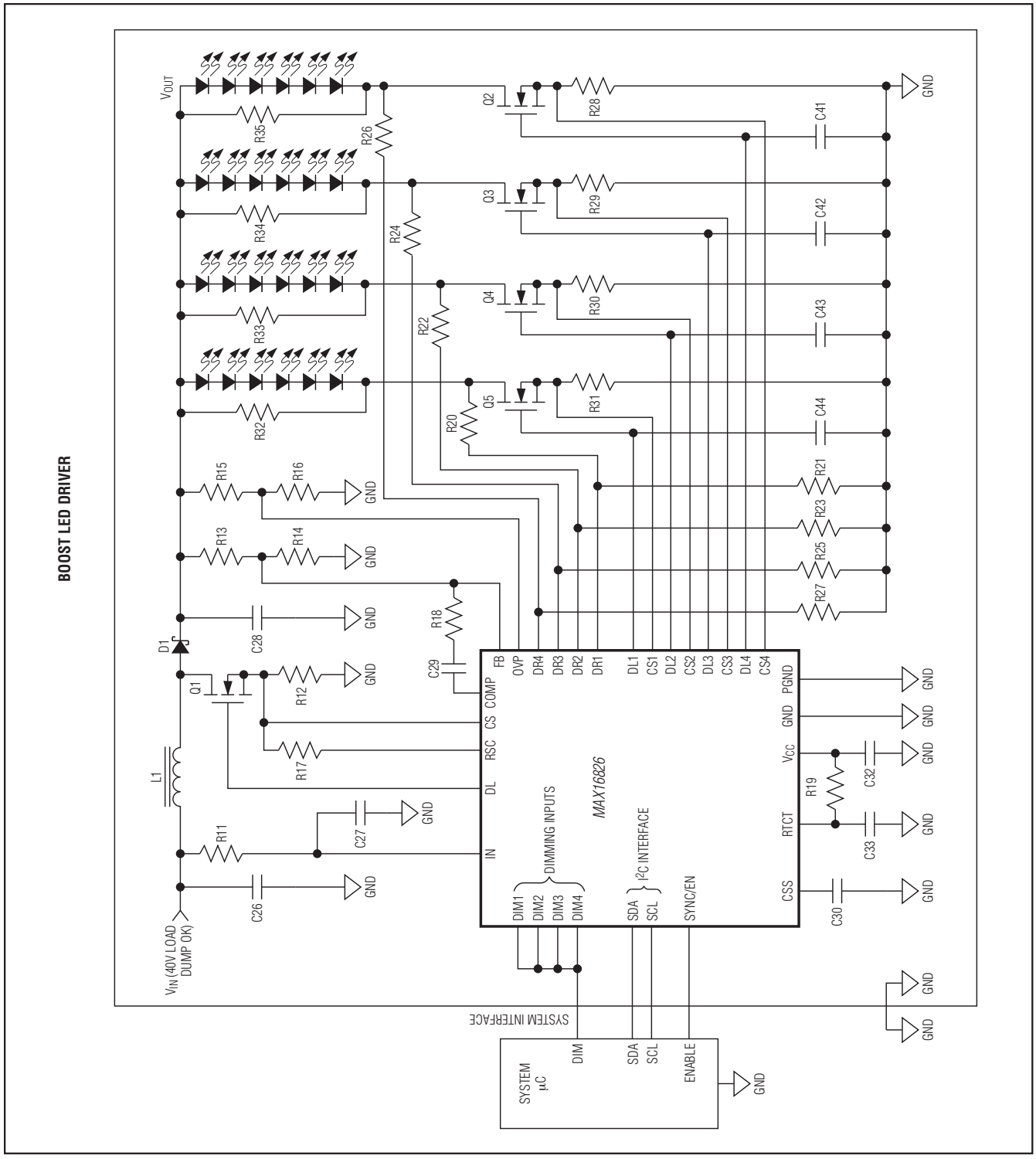
Figure 9. SEPIC-Based LED Driver

PCB Layout and Routing

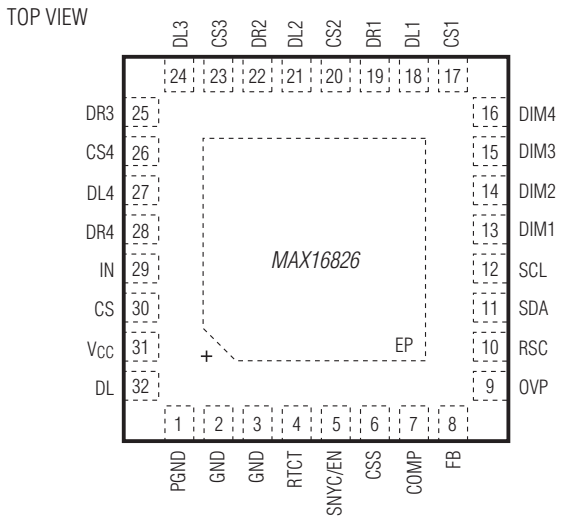
Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of the high current-switching loop of the rectifier diode, switching FET, sense resistor, and output capacitor to avoid excessive switching noise. Use wide and short traces for the gate-drive loop from DL, to the FET gate, and through the current-sense resistor, then returning to the IC PGND and GND.
- Connect high-current input and output components with short and wide connections. The high-current input loop is from the positive terminal of the input capacitor to the inductor, to the switching FET, to the current-sense resistor, and to the negative terminal of the input capacitor. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode, to the positive terminal of the output capacitor, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.
- Place the feedback and even voltage-divider resistors as close to FB and OVP as possible. The divider center trace should be kept short. Placing the resistors far away causes the sensing trace to become antennas that can pick up switching noise. Avoid running the sensing traces near drain connection of the switching FET.
- Place the input bypass capacitor as close to the device as possible. The ground connection of the bypass capacitor should be connected directly to GND with a wide trace.
- Minimize the size of the switching FET drain node while keeping it wide and short. Keep the drain node away from the feedback node and ground. If possible, avoid running this node from one side of the PCB to the other. Use DC traces as shields, if necessary.
- Provide large enough cooling copper traces for the external current sink FETs. Calculate the worst-case power dissipation and allocate sufficient area for cooling.
- Refer to the MAX16826 Evaluation Kit for an example of proper board layout.

Typical Application Circuit



Pin Configuration



TQFN
(5mm x 5mm)

EXPOSED PAD.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16826ATJ+	-40°C to +125°C	32 TQFN-EP*
MAX16826ATJ/V+	-40°C to +125°C	32 TQFN-EP*
MAX16826AGJ/VY+	-40°C to +125°C	32 QFN-EP*
MAX16826BATJ+	-40°C to +125°C	32 TQFN-EP*
MAX16826BATJ/V+	-40°C to +125°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255-4	**21-0140**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/08	Initial release	—
1	3/09	Added automotive version, updated *Features*, *EC table*, *Typical Operating Characteristics*, *Switching Preregulator Stage, Oscillator, Analog-to-Digital (ADC), Faults and Fault Detection* sections	1, 2, 5, 6, 11, 14–17, 20
2	12/09	Improve definition of minimum on-time for proper ADC operation	5, 10, 16
3	6/10	Added MAX16826B part	2–5, 25
4	12/11	Added MAX16826AGJ/VY+ to data sheet	25
5	10/13	Added *Switching Noise Effects on ADC Readings* section	22
6	2/15	Updated *Benefits and Features* section	1
7	2/16	Added missing lead(Pb)-Free designations in *Ordering Information* table	25
7.1		Corrected revision date	1, 26

