THE DATASHEET OF

NCX8193GUX

NCX8193

Audio jack detection and configuration with false detection prevention

Rev. 2 — 21 November 2014 **Product data sheet**

1. General description

The NCX8193 is an advanced audio jack accessory detector and controller.
It supports 3-pole and 4-pole connectors and detects the insertion of plugs into jacks using a fault detection technique. An internal microphone bias line switch allows a codec or application processor to control the audio jack configuration. The device supports a broad variety of after-market headphones.

2. Features and benefits

- Fail-safe headset and headphone detection
- Low-power standby mode
- Click free switching
- Low THD and noise microphone pass through channel
- Send/End button detection
- Low ON resistance: 0.9 Ω (typical) at a supply voltage of 2.8 V
- ESD protection:
  - HBM JEDEC JDS-001 Class 3B exceeds 8 kV
- Operating ambient temperature –40°C to +85°C

3. Applications

- Headphones with integrated microphone and remote control buttons

4. Ordering information

Table 1. Ordering information

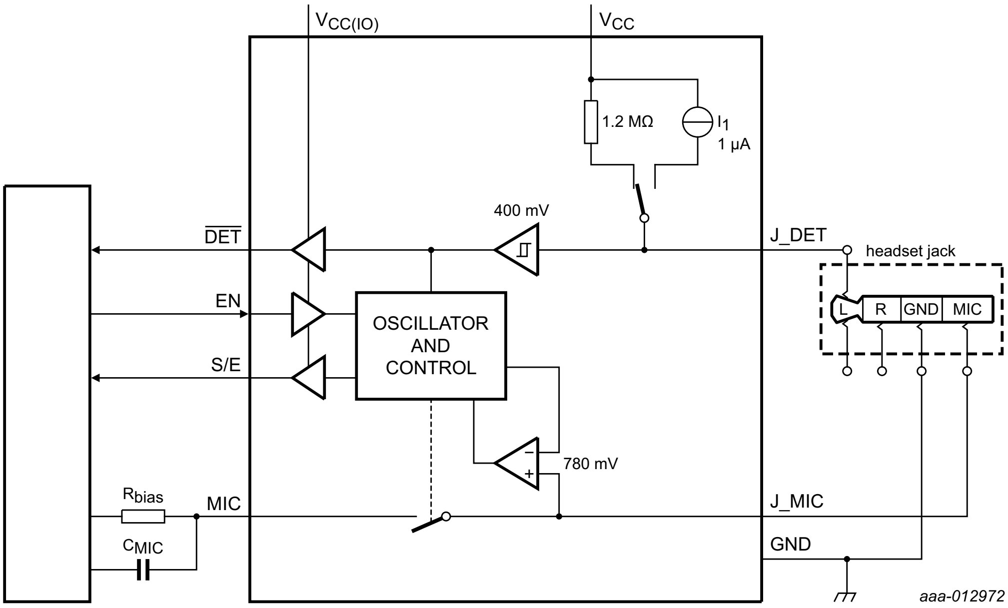
Type number	Package			
	Temperature range	Name	Description	Version
NCX8193GU	–40 °C to +85 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.8 × 1.4 × 0.5 mm	SOT1160-2

5. Marking

Table 2. Marking codes

Type number	Marking code
NCX8193GU	q8

6. Functional diagram

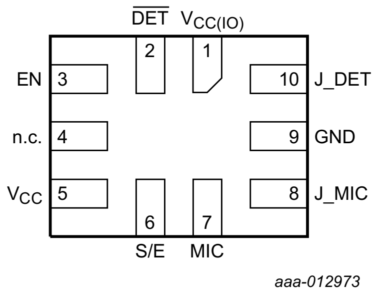


J_DET is pulled up to V_{CC} in Sleep mode; J_DET is connected to I_1 in Active mode.

Fig 1. Simplified schematic

7. Pinning information

7.1 Pinning



Transparent top view,
solder pads facing down

Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
$V_{CC(IO)}$	1	Power	digital interface input/output supply voltage; headphone mode bias supply
$\overline{DET}$	2	O	plug detect; Plug inserted: $\overline{DET}$ = LOW; unplugged: $\overline{DET}$ = HIGH
EN	3	I	microphone bias path switch SWM control. closed: EN = HIGH; open: EN = LOW
n.c.	4	n.c.	not connected (preferably connected GND)
V_{CC}	5	Power	core supply (e.g. battery)
S/E	6	O	keypress-detect; key press: S/E = HIGH; NO key press: S/E = LOW
MIC	7	I/O	microphone bias connection audio codec side
J_MIC	8	I/O	microphone bias connection audio headset side
GND	9	ground	ground
J_DET	10	I/O	plug detection bias and logic level input

8. Functional description

The simplified schematic of the NCX8193 is shown in Figure 1.

If no plug is inserted, J_DET is pulled-up to V_{CC} via a 1.2 MΩ resistor. Once J_DET is pulled below 400 mV, the pull-up resistor is switched out and J_DET is connected to a variable current source. The current source slowly increases its output current. If J_DET remains lower than 300 mV, $\overline{DET}$ is set LOW to indicate that a plug has been inserted.

In case $\overline{DET}$ is set LOW, when EN is HIGH, J_DET is connected to the current source and the integrated button press detection circuit on J_MIC is active. The button press detection uses a trigger level of 780 mV. It enables a 1.8 V bias voltage in combination with an R_{bias}, matching the series resistance of the microphone, to detect button presses. Not only call-end button press but also forward and reverse button press event levels can be passed from J_MIC to MIC. The codec or processor decodes according to the individual button pressed. Refer to Figure 3 and Figure 4 for details.

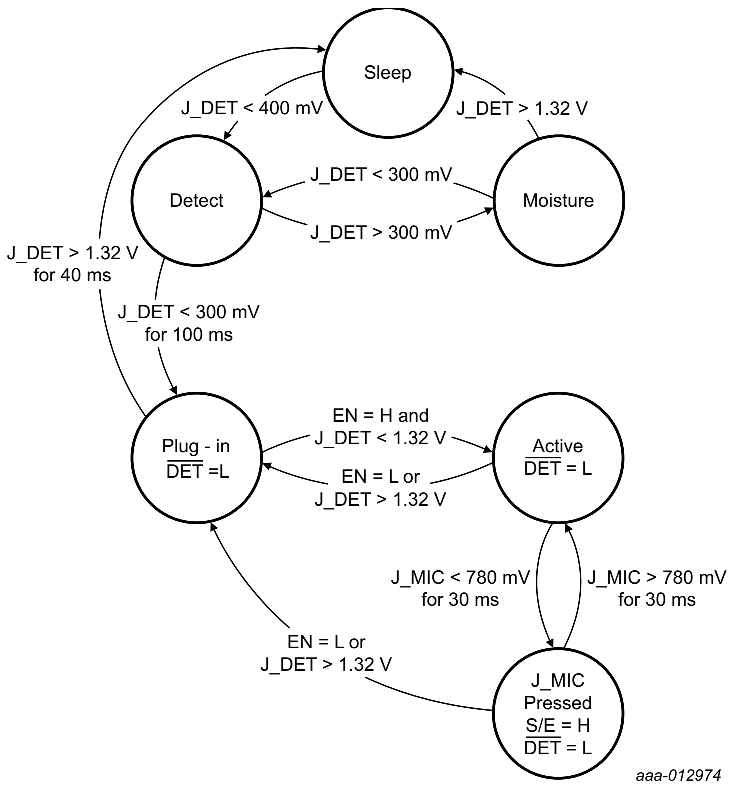
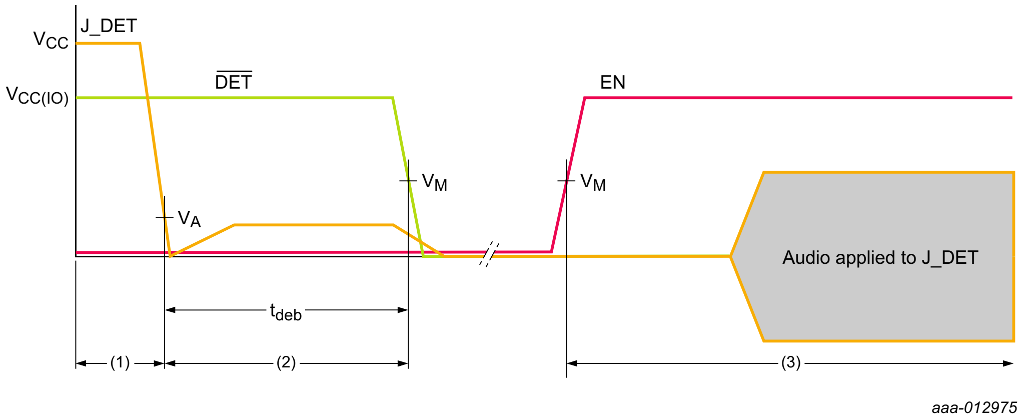


Fig 3. Simplified status diagram of NCX8193



(1) J_DET = V_{CC}; microphone path is open.
(2) J_DET = I_1; microphone path is open.
(3) J_DET = I_1; microphone path is closed.

Fig 4. Basic headset plug-in detection

Table 4. Simplified status diagram signal and functional conditions[1]

		States					
		Sleep	**Detect**	**Moisture**	**Plug-in**	**Active**	**J_MIC pressed**
I/O	J_DET	H	L	0.3 V	audio signal	audio signal	audio signal
Input	EN	X	X	X	L	H	H
I/O	J_MIC	L	L	L	L	> 780 mV	< 780 mV
I/O	MIC	Z	Z	Z	Z	J_MIC	J_MIC
Output	$\overline{\text{DET}}$	H [2]	H	H	L	L	L
Output	S/E	L	L	L	L	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] In case an unplug event is detected, $\overline{\text{DET}}$ remains LOW for 40 ms before returning to HIGH.'

9. Application diagram

For stable operation of the NCX8913, place a 4.7 μF capacitor between V_{CC} and GND and place a 1μF capacitor between $V_{CC(IO)}$ and GND. These bypass capacitors should be placed as close to the device as possible with low-ohmic connections from the power supplies and GND connections.

When the headset or accessory plug is inserted into audio jack, the J_DET pin is shorted to the left (L) audio channel. Audio performance, within the audio range of 20 – 20 kHz, may be affected when connecting external circuitry to the J_DET pin.

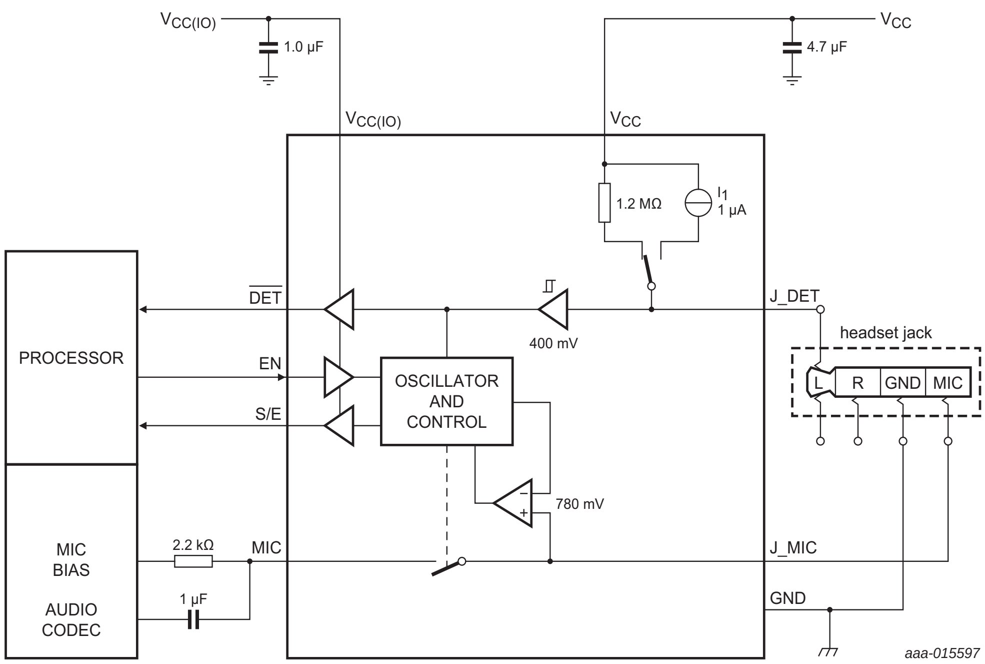


Fig 5. NCX8193 application diagram

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6.0	V
$V_{CC(IO)}$	input/output supply voltage		–0.5	+6.0	V
V_I	input voltage	J_MIC; MIC	–0.5	V_{CC}	V
		EN	–0.5	$V_{CC(IO)}$ + 0.1	V
		J_DET	–1.5	V_{CC}	V
V_O	output voltage	$\overline{DET}$; S/E	–0.5	$V_{CC(IO)}$ + 0.3	V
ΔV	voltage difference	V_{CC} to J_DET	-	6.0	V
I_{SW}	switch current	continuous current from MIC to J_MIC	-	50	mA

Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation		-	250	mW

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.4	5.25	V
$V_{CC(IO)}$	input/output supply voltage	$V_{CC(IO)} \leq V_{CC}$	1.6	V_{CC}	V
V_I	input voltage	MIC; J_MIC	0	V_{CC}	V
ΔV	voltage difference	V_{CC} to J_DET	-	5.5	V
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	148	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure that all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 8. Static characteristics

At recommended operating conditions, unless otherwise specified typical values are measured with V_{CC} = 3.6 V and $V_{CC(IO)}$ = 1.8 V. Voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
Digital control								
V_{IH}	HIGH-level input voltage	EN	-	-	-	$0.7V_{CC(IO)}$	-	V
V_{IL}	LOW-level input voltage	EN	-	-	-	-	$0.3V_{CC(IO)}$	V
V_{OH}	HIGH-level output voltage	$\overline{DET}$; S/E; I_O = 0.5 mA	-	-	-	$0.8V_{CC(IO)}$	-	V
V_{OL}	LOW-level output voltage	$\overline{DET}$; S/E; I_O = 0.5 mA	-	-	-	-	$0.2V_{CC(IO)}$	V
C_I	input capacitance	J_DET	-	5	-	-	-	pF
		EN	-	1	-	-	-	pF

Table 8. Static characteristics *...continued*

At recommended operating conditions, unless otherwise specified typical values are measured with V_{CC} = 3.6 V and $V_{CC(IO)}$ = 1.8 V. Voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
Microphone bias switch								
$I_{S(OFF)}$	OFF-state leakage current	MIC; $V_{I(MIC)}$ = 850 mV; see Figure 6	-	-	-	-	0.1	µA
R_{ON}	ON resistance	MIC; $I_{O(J\_MIC)}$ = 30 mA; $V_{I(MIC)}$ = 850 mV; see Figure 7 and Figure 8						
		V_{CC} = 2.8 V; see Figure 9	-	0.9	-	-	1.5	Ω
		V_{CC} = 3.0 V; see Figure 10	-	0.9	-	-	1.5	Ω
		V_{CC} = 3.3 V; see Figure 11	-	0.9	-	-	1.5	Ω
		V_{CC} = 3.8 V; see Figure 12	-	0.9	-	-	1.5	Ω
$R_{ON(flat)}$	ON resistance (flatness)	$I_{O(J\_MIC)}$ = 30 mA; 0.8 V < $V_{I(MIC)}$ < 1.2 V						
		V_{CC} = 2.8 V; see Figure 9	-	-	-	-	0.6	Ω
		V_{CC} = 3.0 V; see Figure 10	-	-	-	-	0.6	Ω
		V_{CC} = 3.3 V; see Figure 11	-	-	-	-	0.6	Ω
		V_{CC} = 3.8 V; see Figure 12	-	-	-	-	0.6	Ω
$C_{S(OFF)}$	OFF-state capacitance	J_MIC; MIC	-	20	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	J_MIC; MIC	-	60	-	-	-	pF
Audio/analog performance								
THD	total harmonic distortion	R_S = R_L = 600 Ω; V_{AC} = 0.5 V (p-p); V_{DC} = 1.7 V; f_i = 20 Hz to 20 kHz; V_{CC} = 3.8 V; $V_{CC(IO)}$ = 1.8 V; see Figure 13	-	0.01	-	-	-	%
α_{iso}	isolation (OFF-state)	R_S = R_L = 32 Ω; V_{AC} = 0.1 V (p-p); V_{DC} = 2.2 V; f_i = 20 kHz; V_{CC} = 3.8 V; $V_{CC(IO)}$ = 1.8 V; see Figure 14	-	–100	-	-	-	dB
PSRR	power supply rejection ratio	R_S = R_L = 600 Ω; V_{CC} = 3.8 V; $V_{CC(IO)}$ = 1.8 V; V_{DC} = 1.7 V; V_{AC} = 0.3 V (p-p); f_i = 217 Hz; see Figure 15	-	–110	-	-	-	dB

Table 8. Static characteristics *...continued*

At recommended operating conditions, unless otherwise specified typical values are measured with V_{CC} = 3.6 V and $V_{CC(IO)}$ = 1.8 V. Voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
Headset detection								
V_{T-}	negative-going threshold voltage	J_DET	-	-	-	-	400	mV
V_{ref}	reference voltage	J_DET; plug detect	-	300	-	270	330	mV
		J_DET; plug removed; 1.6 V < $V_{CC(IO)}$ < V_{CC}	-	1.32	-	1.2	1.44	V
f_{max}	maximum frequency	J_DET	-	-	-	20000	-	Hz
R_{pu}	pull-up resistance	J_DET	-	1.2	-	0.9	1.6	MΩ
I_{source}	source current	J_DET	-	1.0	-	-	-	μA
Button press; S/E detect								
V_{ref}	reference voltage	J_MIC	-	780	-	718	842	mV
Current consumption								
I_{CC}	supply current	power down; $V_{CC(IO)}$ = 0 V; V_{CC} = 3.6 V; J_DET = open	-	0.1	-	-	1	μA
$I_{CC(tot)}$	total supply current	$I_{CC(IO)}$ + I_{CC}; 1.6 V < $V_{CC(IO)}$ < 2.0 V; V_{CC} = 3.6 V;						
		Sleep mode; J_DET = open	-	0.1	-	-	1	μA
		Plug-in mode	-	15	-	-	25	μA
		Active mode	-	15	-	-	25	μA

13.1 Test circuits and graphs

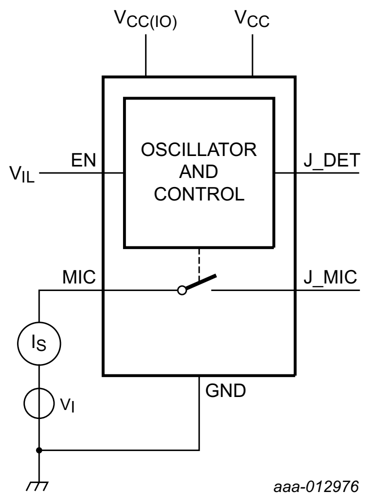
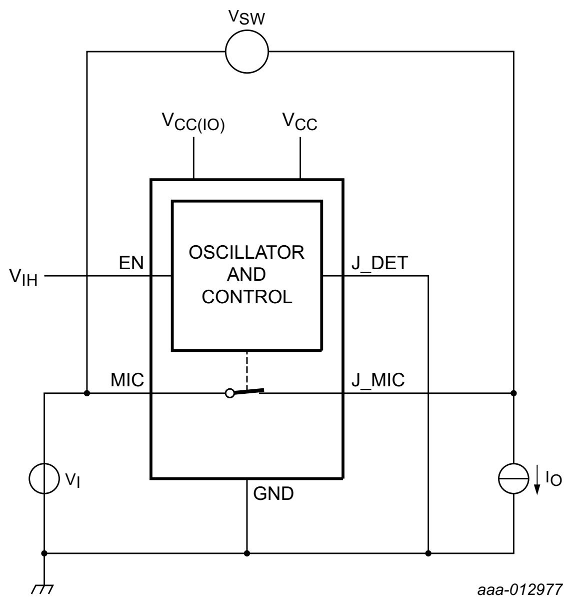
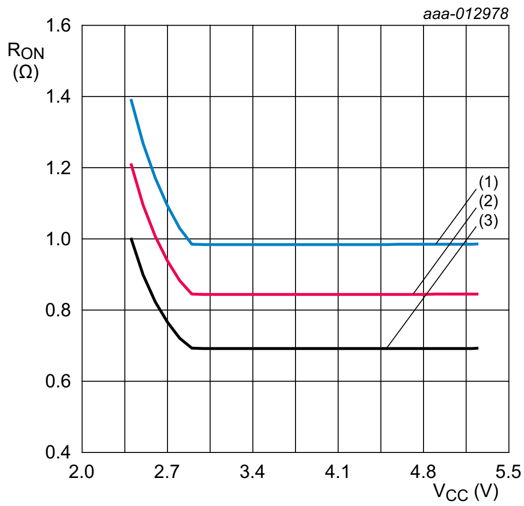


Fig 6. Test circuit for measuring OFF-state leakage current



$R_{ON} = V_{SW} / I_O$

Fig 7. Test circuit for measuring ON resistance

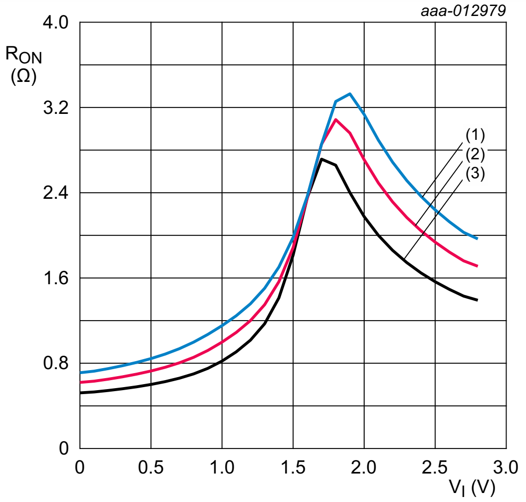


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 8. ON resistance versus V_{CC}

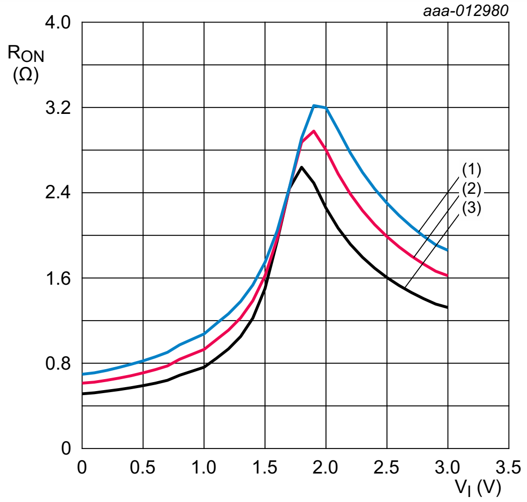


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 9. ON resistance as a function of $V_{I(MIC)}$; V_{CC} = 2.8 V

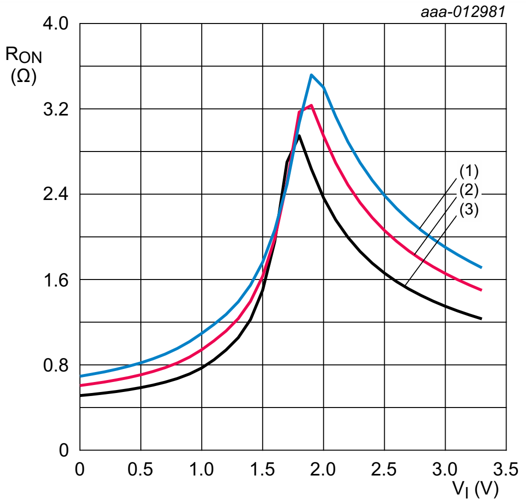


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. ON resistance as a function of $V_{I(MIC)}$; V_{CC} = 3.0 V

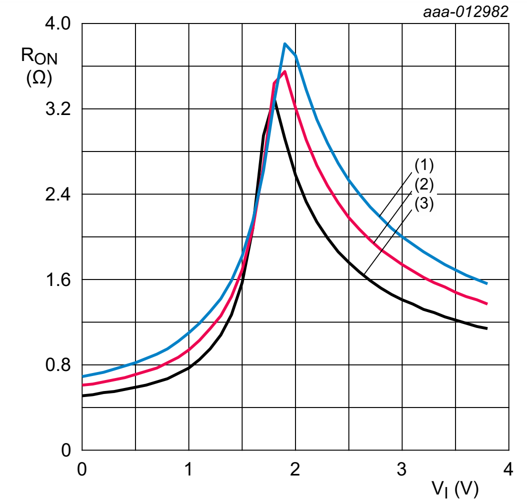


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 11. ON resistance as a function of $V_{I(MIC)}$; V_{CC} = 3.3 V



(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 12. ON resistance as a function of $V_{I(MIC)}$; V_{CC} = 3.8 V

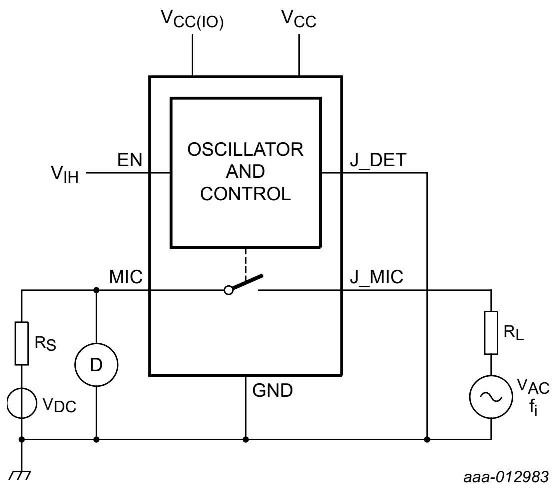


Fig 13. Test circuit for measuring total harmonic distortion

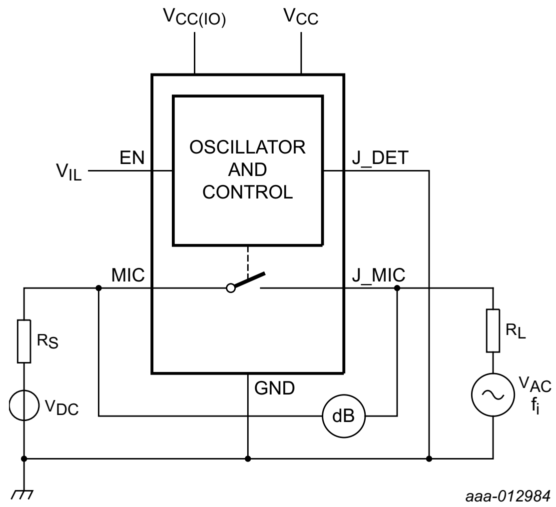


Fig 14. Test circuit for measuring isolation (OFF-state)

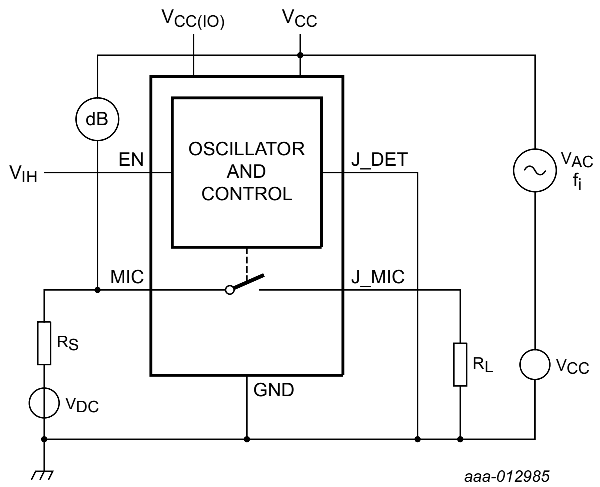


Fig 15. Test circuit for measuring the power supply rejection ratio

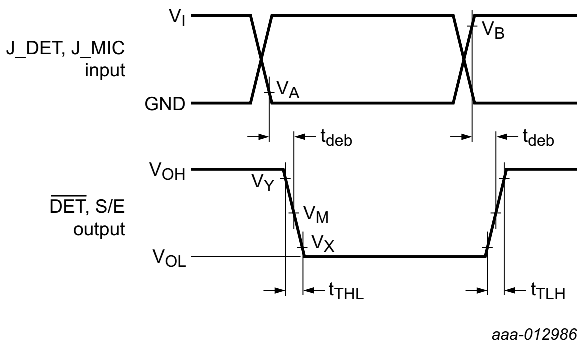
14. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; unless otherwise specified typical values are measured with V_{CC} = 3.6 V and $V_{CC(IO)}$ = 1.8 V; voltages are referenced to GND (ground = 0 V); see Figure 19.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{TLH}	LOW to HIGH output transition time	$\overline{DET}$; S/E; C_L = 5 pF; see Figure 16 and Figure 19	-	5	-	-	-	ns
t_{THL}	HIGH to LOW output transition time	$\overline{DET}$; S/E; C_L = 5 pF; see Figure 16 and Figure 19	-	2	-	-	-	ns
t_{deb}	debounce time	see Figure 16 and Figure 19						
		Detect to Plug-in	-	80	-	-	100	ms
		Plug-in to Sleep	-	40	-	-	-	ms
		Active to or from J_MIC Pressed	-	30	-	-	-	ms
t_{en}	enable time	EN to J_MIC; $V_{I(MIC)}$ = V_{CC}; see Figure 17 and Figure 20	-	15	-	-	-	µs
t_{dis}	disable time	$V_{I(MIC)}$ = V_{CC};						
		EN to J_MIC; see Figure 17 and Figure 20	-	15	-	-	-	µs
		J_DET to J_MIC; see Figure 18	-	15	-	-	-	µs

14.1 Waveform and test circuits



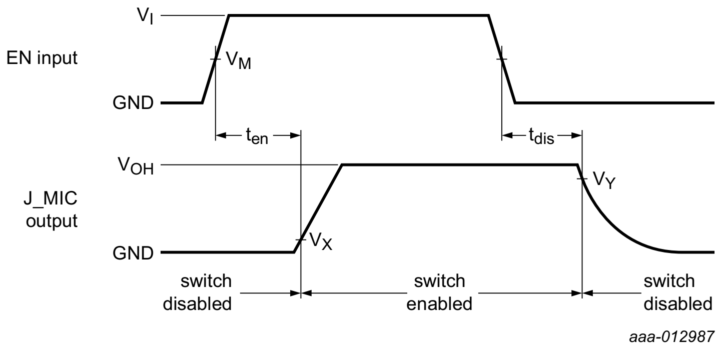
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 16. Input to output propagation delays

Table 10. Measurement points

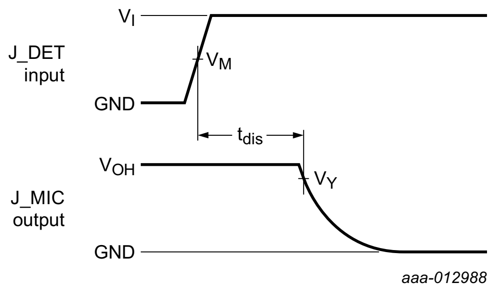
Supply voltage		Input J_DET		Input J_MIC		Output $\overline{DET}$, S/E		
V_{CC}	$V_{CC(IO)}$	V_A	V_B	V_A	V_B	V_M	V_X	V_Y
3.6 V	1.8 V	0.05 V	1.44 V	0.7 V	0.85 V	$0.5V_{CC(IO)}$	$0.2V_{CC(IO)}$	$0.8V_{CC(IO)}$



Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 17. Enable and disable times (EN to J_MIC)



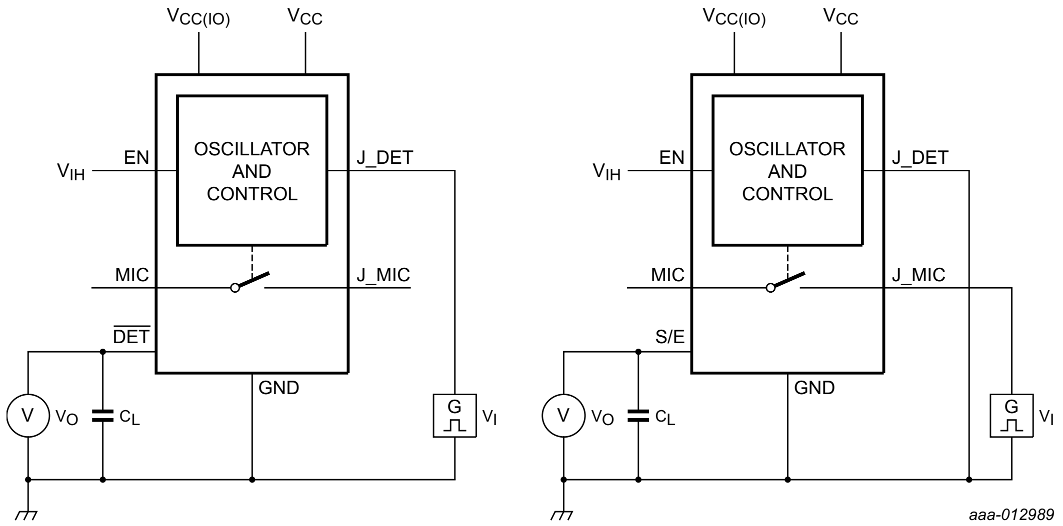
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 18. Enable and disable times (J_DET to J_MIC)

Table 11. Measurement points

Supply Voltage		Input J_DET	Input EN	Output J_MIC	
V_{CC}	$V_{CC(IO)}$	V_M	V_M	V_X	V_Y
3.6 V	1.8 V	1.44 V	$0.5V_{CC(IO)}$	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 12.

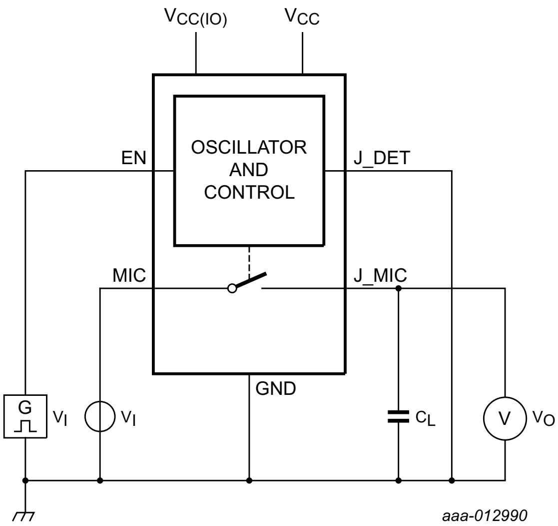
Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance.

Fig 19. Test circuit for measuring switching times

Table 12. Test data

Supply voltage		Input		Load
V_{CC}	$V_{CC(IO)}$	V_I	t_r, t_f	C_L
2.4 V to 5.25 V	1.6 V to V_{CC}	V_{CC}	≤ 2.5 ns	5 pF



Test data is given in Table 13.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance.

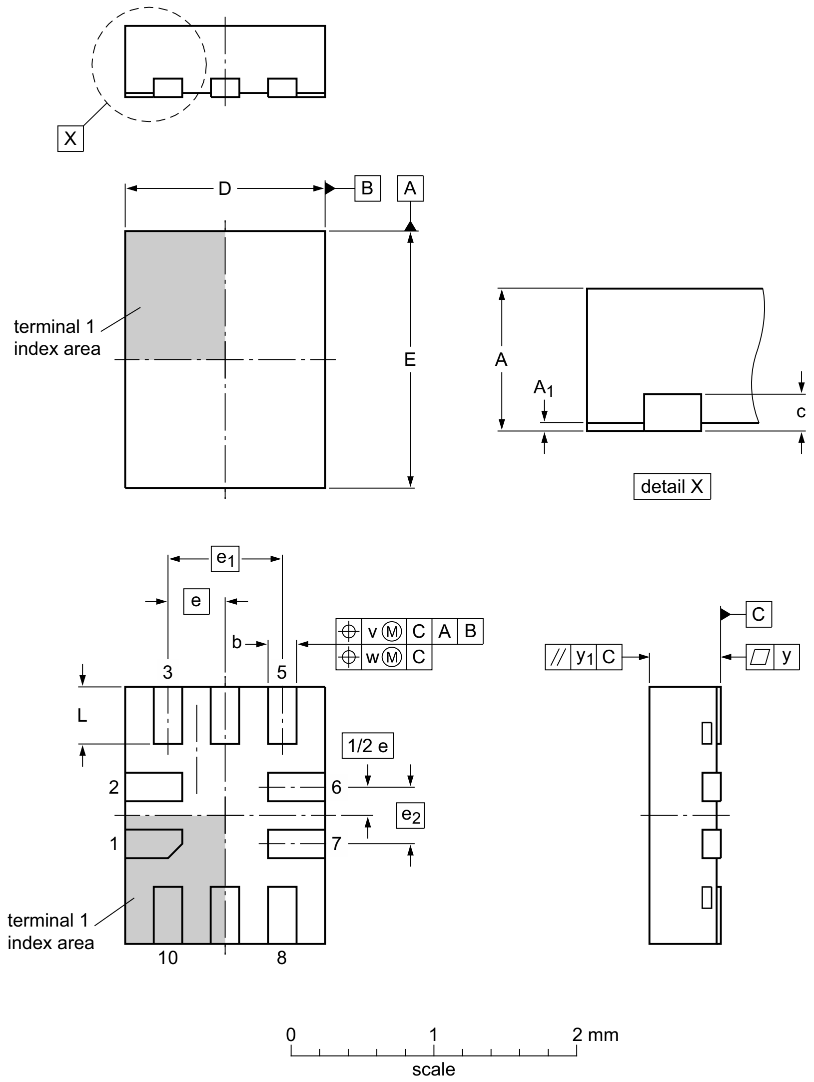
Fig 20. Test circuit for measuring switching times

Table 13. Test data

Supply voltage		Input			Load
V_{CC}	$V_{CC(IO)}$	$V_{I(EN)}$	$V_{I(J\_MIC)}$	t_r, t_f	C_L
2.4 V to 5.25 V	1.6 V to V_{CC}	$V_{CC(IO)}$	V_{CC}	≤ 2.5 ns	5 pF

15. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.8 x 1.4 x 0.5 mm **SOT1160-2**



Dimensions

Unit		A	A_1	b	c	D	E	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.5	0.05	0.25		1.5	1.9				0.45				
	nom			0.20	0.127	1.4	1.8	0.4	0.8	0.4	0.40	0.1	0.05	0.05	0.05
	min		0.00	0.15		1.3	1.7				0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-2_po

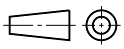
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1160-2	- - -	MO-255	- - -			~~14-01-07~~ 14-03-10

Fig 21. Package outline XQFN10 (SOT1160-2) package

16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
THD	Total Harmonic Distortion

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCX8193 v.2	20141121	Product data sheet	-	NCX8193 v.1
Modifications:	• Added application			
NCX8193 v.1	20140709	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

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