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# Arria® 10 Device Datasheet

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# Intel® Arria® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Arria® 10 devices.

Intel Arria 10 devices are offered in extended and industrial grades. Extended devices are offered in –E1 (fastest), –E2, and –E3 speed grades. Industrial grade devices are offered in the –I1, –I2, and –I3 speed grades.

The suffix after the speed grade denotes the power options offered in Intel Arria 10 devices.

- L—enables the device to operate at low static power while maintaining excellent performance.
- S—standard power specification.
- V—enables the device to run at lower than default $V_{CC}$, reducing static and dynamic power while retaining equivalent performance.
- H—small device with high performance at the fastest speed grade (–1).

**Related Information**

Intel Arria 10 Device Overview
Provides more information about the densities and packages of devices in the Intel Arria 10 family.

## Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Arria 10 devices.

## Operating Conditions

Intel Arria 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Arria 10 devices, you must consider the operating requirements described in this section.

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*Other names and brands may be claimed as the property of others.

## Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Arria 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

***Caution:*** Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 1. Absolute Maximum Ratings for Intel Arria 10 Devices**

| Symbol | Description | Condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage power supply | — | –0.50 | 1.21 | V |
| $V_{CCP}$ | Periphery circuitry and transceiver fabric interface power supply | — | –0.50 | 1.21 | V |
| $V_{CCERAM}$ | Embedded memory power supply | — | –0.50 | 1.36 | V |
| $V_{CCPT}$ | Power supply for programmable power technology and I/O pre-driver | — | –0.50 | 2.46 | V |
| $V_{CCBAT}$ | Battery back-up power supply for design security volatile key register | — | –0.50 | 2.46 | V |
| $V_{CCPGM}$ | Configuration pins power supply | (1) | –0.50 | 2.46 | V |
| $V_{CCIO}$ | I/O buffers power supply | 3 V I/O | –0.50 | 4.10 | V |
| | | LVDS I/O | –0.50 | 2.46 | V |
| $V_{CCA_PLL}$ | Phase-locked loop (PLL) analog power supply | — | –0.50 | 2.46 | V |
| $V_{CCT_GXB}$ | Transmitter power supply | — | –0.50 | 1.34 | V |
| $V_{CCR_GXB}$ | Receiver power supply | — | –0.50 | 1.34 | V |
| $V_{CCH_GXB}$ | Transceiver output buffer power supply | — | –0.50 | 2.46 | V |
| $V_{CCL_HPS}$ | HPS core voltage and periphery circuitry power supply | — | –0.50 | 1.27 | V |
| $V_{CCIO_HPS}$ | HPS I/O buffers power supply | 3 V I/O | –0.50 | 4.10 | V |
| | | LVDS I/O | –0.50 | 2.46 | V |

*continued...*

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

| Symbol | Description | Condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIOREF_HPS}$ | HPS I/O pre-driver power supply | — | –0.50 | 2.46 | V |
| $V_{CCPLL_HPS}$ | HPS PLL power supply | — | –0.50 | 2.46 | V |
| $I_{OUT}$ | DC output current per pin | — | –25 (2)(3)(4)(5)(6) | 25 | mA |
| $T_J$ | Operating junction temperature | — | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | — | –65 | 150 | °C |

### Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Arria 10 devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Arria 10 Devices chapter
  Provides the power sequencing requirements for Intel Arria 10 devices.

## Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Arria 10 Devices chapter*.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

**Table 2. Maximum Allowed Overshoot During Transitions for Intel Arria 10 Devices**

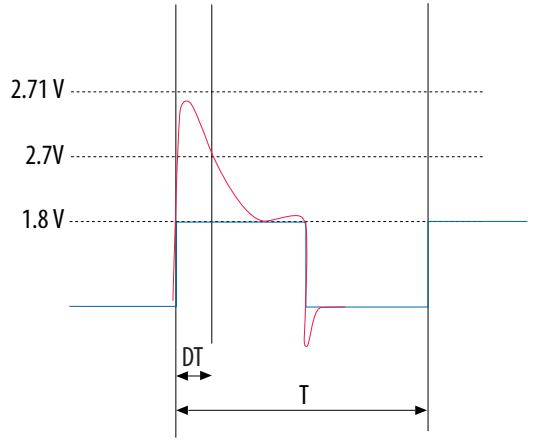
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

| Symbol | Description | Condition (V) | | Overshoot Duration as % at $T_J$ = 100°C | Unit |
|---|---|---|---|---|---|
| | | LVDS I/O (7) | 3 V I/O | | |
| Vi (AC) | AC input voltage | 2.50 | 3.80 | 100 | % |
| | | 2.55 | 3.85 | 42 | % |
| | | 2.60 | 3.90 | 18 | % |
| | | 2.65 | 3.95 | 9 | % |
| | | 2.70 | 4.00 | 4 | % |
| | | > 2.70 | > 4.00 | No overshoot allowed | % |

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

**Figure 1. Intel Arria 10 Devices Overshoot Duration**




## Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Arria 10 devices.

## Recommended Operating Conditions

### Table 3. Recommended Operating Conditions for Intel Arria 10 Devices

This table lists the steady-state voltage values expected from Intel Arria 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum (8) | Typical | Maximum (8) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage power supply | Standard and low power (9) | 0.87 | 0.9 | 0.93 | V |
| | | | 0.92 | 0.95 | 0.98 | V |
| | | SmartVID (10) | 0.82 | — | 0.93 | V |
| $V_{CCP}$ | Periphery circuitry and transceiver fabric interface power supply | Standard and low power (9) | 0.87 | 0.9 | 0.93 | V |
| | | | 0.92 | 0.95 | 0.98 | V |
| | | SmartVID (10) | 0.82 | — | 0.93 | V |
| $V_{CCPGM}$ | Configuration pins power supply | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| $V_{CCERAM}$ | Embedded memory power supply | 0.9 V (9) | 0.87 | 0.9 | 0.93 | V |
| | | 0.95 V (9) | 0.92 | 0.95 | 0.98 | V |
| $V_{CCBAT}$ (11) | Battery back-up power supply (For design security volatile key register) | — | 1.14 | — | 1.89 | V |

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) You can operate –1 and –2 speed grade devices at 0.9 V or 0.95 V typical value. You can operate –3 speed grade device only at 0.9 V typical value. Operating at 0.95 V results in higher core performance and higher power consumption. Refer to core performance in this datasheet for different typical values. For more information about the power consumption of different typical values, refer to the Intel Quartus® Prime software, Power Analyzer report, and Early Power Estimator (EPE).

(10) SmartVID is supported in devices with –3V speed grades only.

(11) If you do not use the design security feature in Intel Arria 10 devices, connect $V_{CCBAT}$ to a 1.5-V to 1.8-V power supply. Intel Arria 10 power-on reset (POR) circuitry monitors $V_{CCBAT}$. Intel Arria 10 devices do not exit POR if $V_{CCBAT}$ is not powered up.

| Symbol | Description | Condition | Minimum [8] | Typical | Maximum [8] | Unit |
|---|---|---|---|---|---|---|
| $V_{CCPT}$ | Power supply for programmable power technology and I/O pre-driver | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| $V_{CCIO}$ | I/O buffers power supply | 3.0 V (for 3 V I/O only) | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V (for 3 V I/O only) | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | (12) | 1.35 | (12) | V |
| | | 1.25 V | 1.19 | 1.25 | 1.31 | V |
| | | 1.2 V | (12) | 1.2 | (12) | V |
| $V_{CCA_PLL}$ | PLL analog voltage regulator power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{REFP_ADC}$ | Precision voltage reference for voltage sensor | — | 1.2475 | 1.25 | 1.2525 | V |
| $V_I$ [13][14] | DC input voltage | 3 V I/O | –0.3 | — | 3.3 | V |
| | | LVDS I/O | –0.3 | — | 2.19 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Extended | 0 | — | 100 | °C |
| | | Industrial | –40 | — | 100 | °C |

***continued...***

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(12) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

(13) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(14) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

| Symbol | Description | Condition | Minimum [8] | Typical | Maximum [8] | Unit |
|---|---|---|---|---|---|---|
| | | Military | [15] | — | [15] | °C |
| $t_{RAMP}$ [16] | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

### Related Information

- I/O Standard Specifications on page 19
- Intel Arria 10 Military Temperature Range Support Technical Brief
  Provides more details on the military requirement.

## Transceiver Power Supply Operating Conditions

### Table 4. Transceiver Power Supply Operating Conditions for Intel Arria 10 GX/SX Devices

| Symbol | Description | Condition [17] | Minimum [18] | Typical | Maximum [18] | Unit |
|---|---|---|---|---|---|---|
| $V_{CCT_GXB\ [L1,R4]\ [C, D, E, F, G, H, I, J]}$ [19] | Transmitter power supply | Chip-to-Chip ≤ 17.4 Gbps<br>Or<br>Backplane [20] ≤ 12.5 Gbps | 1.0 | 1.03 | 1.06 | V |
| | | Chip-to-Chip ≤ 11.3 Gbps | 0.92 | 0.95 | 0.98 | V |

*continued...*

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(15) For more details on the military requirement, refer to the *Intel Arria 10 Military Temperature Range Support Technical Brief*.

(16) $t_{ramp}$ is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(17) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Intel Arria 10 GX/SX Devices for exact data rate ranges.

(18) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(19) To support PCIe* Gen3, this pin must be 1.03 V (± 30 mV) or higher.

| Symbol | Description | Condition (17) | Minimum (18) | Typical | Maximum (18) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCR_GXB[L1,R4]}$ [C, D, E, F, G, H, I, J] (19) | Receiver power supply | Chip-to-Chip ≤ 17.4 Gbps Or Backplane (20) ≤ 12.5 Gbps | 1.0 | 1.03 | 1.06 | V |
| | | Chip-to-Chip ≤ 11.3 Gbps | 0.92 | 0.95 | 0.98 | V |
| $V_{CCH_GXB[L,R]}$ | Transceiver output buffer power supply | — | 1.710 | 1.8 | 1.890 | V |

*Note:* Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-side basis to minimize power consumption. Refer to the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines* and the Intel Quartus Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

## Table 5. Transceiver Power Supply Operating Conditions for Intel Arria 10 GT Devices

| Symbol | Description | Condition (21) | Minimum (18) | Typical | Maximum (18) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCT_GXB[L,R]}$ | Transmitter power supply | Chip-to-Chip ≤ 25.8 Gbps (22) Or Backplane (20) ≤ 12.5 Gbps | 1.10 | 1.12 | 1.14 | V |
| | | Chip-to-Chip ≤ 15 Gbps | 1.0 | 1.03 | 1.06 | V |

***continued...***

(17) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Intel Arria 10 GX/SX Devices for exact data rate ranges.

(18) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(20) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(21) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Intel Arria 10 GT Devices table for exact data rate ranges.

(22) 25.8 Gbps is the maximum data rate for GT channels. 17.4 Gbps is the maximum data rate for GX channels.

| Symbol | Description | Condition (21) | Minimum (18) | Typical | Maximum (18) | Unit |
|---|---|---|---|---|---|---|
| | | Or<br>Backplane (20) ≤ 12.5 Gbps | | | | |
| | | Chip-to-Chip ≤ 11.3 Gbps | 0.92 | 0.95 | 0.98 | V |
| $V_{CCR_GXB[L,R]}$ | Receiver power supply | Chip-to-Chip ≤ 25.8 Gbps<br>Or<br>Backplane (20) ≤ 12.5 Gbps | 1.10 | 1.12 | 1.14 | V |
| | | Chip-to-Chip ≤ 15 Gbps<br>Or<br>Backplane (20) ≤ 12.5 Gbps | 1.0 | 1.03 | 1.06 | V |
| | | Chip-to-Chip ≤ 11.3 Gbps | 0.92 | 0.95 | 0.98 | V |
| $V_{CCH_GXB[L,R]}$ | Transceiver output buffer power supply | — | 1.710 | 1.8 | 1.890 | V |

### Related Information

- Transceiver Performance for Intel Arria 10 GT Devices on page 27
  Provides the data rate ranges for different transceiver speed grades.
- Transceiver Performance for Intel Arria 10 GX/SX Devices on page 25
  Provides the data rate ranges for different transceiver speed grades.
- Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines

(21) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Intel Arria 10 GT Devices table for exact data rate ranges.

## HPS Power Supply Operating Conditions

### Table 6. HPS Power Supply Operating Conditions for Intel Arria 10 SX Devices

This table lists the steady-state voltage and current values expected from Intel Arria 10 system-on-a-chip (SoC) devices with ARM*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Intel Arria 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Intel Arria 10 SoC devices.

| Symbol | Description | Condition | Minimum (23) | Typical | Maximum (23) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCL_HPS}$ | HPS core voltage and periphery circuitry power supply | 0.9 V (24) | 0.87 | 0.9 | 0.93 | V |
| | | 0.95 V (24) | 0.92 | 0.95 | 0.98 | V |
| $V_{CCIO_HPS}$ | HPS I/O buffers power supply | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| $V_{CCIOREF_HPS}$ | HPS I/O pre-driver power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCPLL_HPS}$ | HPS PLL analog voltage regulator power supply | — | 1.71 | 1.8 | 1.89 | V |

#### Related Information

- Recommended Operating Conditions on page 8
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 56
  Provides the maximum HPS clock frequencies.

## DC Characteristics

### Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

(23) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(24) $V_{CCL_HPS}$ options are valid under the operating conditions specified in the Maximum HPS Clock Frequencies table.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

### Related Information

- Early Power Estimator for Intel Arria 10 User Guide
  Provides more information about power estimation tools.
- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  Provides more information about power estimation tools.

## I/O Pin Leakage Current

**Table 7. I/O Pin Leakage Current for Intel Arria 10 Devices**

| Symbol | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –80 | 80 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –80 | 80 | µA |

## Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC* standard.

### Table 8. Bus Hold Parameters for Intel Arria 10 Devices

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 (25), 26 (26) | — | 12 (25), 32 (26) | — | 30 (25), 55 (26) | — | 60 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 (25), –26 (26) | — | –12 (25), –32 (26) | — | –30 (25), –55 (26) | — | –60 | — | –70 | — | µA |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.3 | 0.9 | 0.38 | 1.13 | 0.68 | 1.07 | 0.70 | 1.7 | 0.8 | 2 | V |

## OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

(25) This value is only applicable for LVDS I/O bank.

(26) This value is only applicable for 3 V I/O bank.

## Table 9. OCT Calibration Accuracy Specifications for Intel Arria 10 Devices

Calibration accuracy for the calibrated on-chip series termination ($R_S$ OCT) and on-chip parallel termination ($R_T$ OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

| Symbol | Description | Condition (V) | Resistance Tolerance | | | Unit |
|---|---|---|---|---|---|---|
| | | | –E1, –I1 | –E2, –I2 | –E3, –I3 | |
| 25-Ω and 50-Ω $R_S$ | Internal series termination with calibration (25-Ω and 50-Ω setting) | $V_{CCIO}$ = 1.8, 1.5, 1.2 | ± 15 | ± 15 | ± 15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.25, 1.2 | ± 15 | ± 15 | ± 15 | % |
| | | $V_{CCIO}$ = 1.35 | ± 20 | ± 20 | ± 20 | % |
| 48-Ω, 60-Ω, 80-Ω, and 120-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.2 | ± 15 | ± 15 | ± 15 | % |
| 240-Ω $R_S$ | Internal series termination with calibration (240-Ω setting) | $V_{CCIO}$ = 1.2 | ± 20 | ± 20 | ± 20 | % |
| 30-Ω $R_T$ | Internal parallel termination with calibration (30-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 34-Ω, 48-Ω, 80-Ω, and 240-Ω $R_T$ | Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 | ± 15 | ± 15 | ± 15 | % |
| 40-Ω, 60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| | | $V_{CCIO}$ = 1.2 (27) | ± 15 | ± 15 | ± 15 | % |
| 80-Ω $R_T$ | Internal parallel termination with calibration (80-Ω setting) | $V_{CCIO}$ = 1.2 | ± 15 | ± 15 | ± 15 | % |

(27) Only applicable to POD12 I/O standard.

## OCT Without Calibration Resistance Tolerance Specifications

### Table 10. OCT Without Calibration Resistance Tolerance Specifications for Intel Arria 10 Devices

This table lists the Intel Arria 10 OCT without calibration resistance tolerance to PVT changes.

| Symbol | Description | Condition (V) | Resistance Tolerance | | | Unit |
|---|---|---|---|---|---|---|
| | | | –E1, –I1 | –E2, –I2 | –E3, –I3 | |
| 25-Ω and 50-Ω $R_S$ | Internal series termination without calibration (25-Ω and 50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5 | –40 to +30 | ± 40 | ± 40 | % |
| | | $V_{CCIO}$ = 1.8, 1.5, 1.2 | –50 to +30 | ± 50 | ± 50 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination without calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 | –50 to +30 | ± 50 | ± 50 | % |
| 48-Ω and 60-Ω $R_S$ | Internal series termination without calibration (48-Ω and 60-Ω setting) | $V_{CCIO}$ = 1.2 | –50 to +30 | ± 50 | ± 50 | % |
| 120-Ω $R_s$ | Internal series termination without calibration (120-Ω setting) | $V_{CCIO}$ = 1.2 | –50 to +30 | ± 50 | ± 50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 1.8 | ± 25 | ± 35 | ± 40 | % |

## Pin Capacitance

### Table 11. Pin Capacitance for Intel Arria 10 Devices

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $C_{IO_COLUMN}$ | Input capacitance on column I/O pins | 2.5 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output/feedback pins | 2.5 | pF |

## Internal Weak Pull-Up and Weak Pull-Down Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. The weak pull-down feature is only available for the pins as described in the Internal Weak Pull-Down Resistor Values for Intel Arria 10 Devices table.

### Table 12. Internal Weak Pull-Up Resistor Values for Intel Arria 10 Devices

| Symbol | Description | Condition (V) [28] | Value [29] | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option. | $V_{CCIO}$ = 3.0 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 2.5 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.8 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.35 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.25 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.2 ±5% | 25 | kΩ |

### Table 13. Internal Weak Pull-Down Resistor Values for Intel Arria 10 Devices

| Pin Name | Description | Condition (V) | Value [29] | Unit |
|---|---|---|---|---|
| nIO_PULLUP | Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins. | $V_{CC}$ = 0.9 ±3.33% | 25 | kΩ |
| TCK | Dedicated JTAG test clock input pin. | $V_{CCPGM}$ = 1.8 ±5 % | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.2 ±5% | 25 | kΩ |
| MSEL[0:2] | Configuration input pins that set the configuration scheme for the FPGA device. | $V_{CCPGM}$ = 1.8 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.2 ±5% | 25 | kΩ |

#### Related Information

Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

[28] Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

[29] Valid with ±25% tolerances to cover changes over PVT.

## I/O Standard Specifications

Tables in this section list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Intel Arria 10 devices.

For minimum voltage values, use the minimum $V_{CCIO}$ values. For maximum voltage values, use the maximum $V_{CCIO}$ values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

### Related Information

- Recommended Operating Conditions on page 8
- Intel Arria 10 Military Temperature Range Support Technical Brief
  Provides more details on the military requirement.

### Single-Ended I/O Standards Specifications

**Table 14. Single-Ended I/O Standards Specifications for Intel Arria 10 Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ [30] (mA) | $I_{OH}$ [30] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.3 | 0.4 | 2.4 | 2 | –2 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.3 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.3 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

(30) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

## Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

### Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Arria 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-135/ SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125/ SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-12/ SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |
| POD12 | 1.16 | 1.2 | 1.24 | 0.69 × $V_{CCIO}$ | 0.7 × $V_{CCIO}$ | 0.71 × $V_{CCIO}$ | — | $V_{CCIO}$ | — |

## Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

### Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Arria 10 Devices

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (31) (mA) | $I_{OH}$ (31) (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-18 Class I | –0.3 | $V_{REF}$ –0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ –0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ –0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| SSTL-135/ SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| SSTL-125/ SSTL-125 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| SSTL-12/ SSTL-12 Class I, II | — | $V_{REF}$ – 0.10 | $V_{REF}$ + 0.10 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ –0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ –0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |

*continued...*

(31) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (31) (mA) | $I_{OH}$ (31) (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |
| POD12 | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | (0.7 – 0.15) × $V_{CCIO}$ | (0.7 + 0.15) × $V_{CCIO}$ | — | — |

## Differential SSTL I/O Standards Specifications

### Table 17. Differential SSTL I/O Standards Specifications for Intel Arria 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{SWING(AC)}$ (V) | | $V_{IX(AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Min | Typ | Max |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | 0.5 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (32) | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{REF} – V_{IL(AC)})$ | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 |
| SSTL-135/ SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.18 | (32) | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 |

*continued...*

(31) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

(32) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{SWING(AC)}$ (V) | | $V_{IX(AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Min | Typ | Max |
| SSTL-125/ SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (32) | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ |
| SSTL-12/ SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | (32) | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ | $V_{REF} - 0.15$ | $V_{CCIO}/2$ | $V_{REF} + 0.15$ |
| POD12 | 1.16 | 1.2 | 1.24 | 0.16 | — | 0.3 | — | $V_{REF} - 0.08$ | — | $V_{REF} + 0.08$ |

## Differential HSTL and HSUL I/O Standards Specifications

### Table 18. Differential HSTL and HSUL I/O Standards Specifications for Intel Arria 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{DIF(AC)}$ (V) | | $V_{IX(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.4 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.4 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO} + 0.3$ | 0.3 | $V_{CCIO} + 0.48$ | — | $0.5 \times V_{CCIO}$ | — | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ |
| HSUL-12 | 1.14 | 1.2 | 1.3 | $2(V_{IH(DC)} - V_{REF})$ | $2(V_{REF} - V_{IH(DC)})$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{REF} - V_{IH(AC)})$ | $0.5 \times V_{CCIO} - 0.12$ | $0.5 \times V_{CCIO}$ | $0.5 \times V_{CCIO} + 0.12$ | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ |

## Differential I/O Standards Specifications

### Table 19. Differential I/O Standards Specifications for Intel Arria 10 Devices

Differential inputs are powered by $V_{CCPT}$ which requires 1.8 V.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) (33) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (34) | | | $V_{OCM}$ (V) (34) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVDS (35) | 1.71 | 1.8 | 1.89 | 100 | $V_{CM}$ = 1.25 V | — | 0 | $D_{MAX}$ ≤700 Mbps | 1.85 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | | 1 | $D_{MAX}$ >700 Mbps | 1.6 | | | | | | |
| RSDS (36) | 1.71 | 1.8 | 1.89 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (37) | 1.71 | 1.8 | 1.89 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (38) | 1.71 | 1.8 | 1.89 | 300 | — | — | 0.6 | $D_{MAX}$ ≤700 Mbps | 1.7 | — | — | — | — | — | — |
| | | | | | | | 1 | $D_{MAX}$ >700 Mbps | 1.6 | | | | | | |

### Related Information

Transceiver Specifications for Intel Arria 10 GX, SX, and GT Devices on page 29
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

(33) The minimum $V_{ID}$ value is applicable over the entire common mode range, $V_{CM}$.

(34) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.

(35) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.

(36) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(37) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.1 V to 1.625 V.

(38) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

# Switching Characteristics

This section provides the performance characteristics of Intel Arria 10 core and periphery blocks for extended grade devices.

## Transceiver Performance Specifications

### Transceiver Performance for Intel Arria 10 GX/SX Devices

#### Table 20. Transmitter and Receiver Data Rate Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Transceiver Speed Grade 3 | Transceiver Speed Grade 4 | Unit |
|---|---|---|---|---|---|---|
| Chip-to-Chip (39) | Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 1.03$ V | 17.4 | 15 | 14.2 | 12.5 | Gbps |
| | Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 0.95$ V | 11.3 | 11.3 | 11.3 | 11.3 | Gbps |
| | Minimum Data Rate | 1.0 (40) | | | | Gbps |
| Backplane (39) | Maximum data rate $V_{CCR_GXB} = V_{CCT_GXB} = 1.03$ V | 12.5 | 12.5 | 12.5 | 10.3125 | Gbps |
| | Minimum Data Rate | 1.0 (40) | | | | Gbps |

#### Table 21. ATX PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Transceiver Speed Grade 3 | Transceiver Speed Grade 4 | Unit |
|---|---|---|---|---|---|---|
| Supported Output Frequency | Maximum Frequency | 8.7 | 7.5 | 7.1 | 6.25 | GHz |
| | Minimum Frequency | 500 | | | | MHz |

(39) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(40) Intel Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

### Table 22. Fractional PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Transceiver Speed Grade 3 | Transceiver Speed Grade 4 | Unit |
|---|---|---|---|---|---|---|
| Supported Output Frequency | Maximum Frequency | 6.25 | 6.25 | 6.25 | 6.25 | GHz |
| | Minimum Frequency | 500 | | | | MHz |

### Table 23. CMU PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Transceiver Speed Grade 3 | Transceiver Speed Grade 4 | Unit |
|---|---|---|---|---|---|---|
| Supported Output Frequency | Maximum Frequency | 5.15625 | 5.15625 | 5.15625 | 5.15625 | GHz |
| | Minimum Frequency | 2450 | | | | MHz |

#### Related Information

Transceiver Power Supply Operating Conditions on page 10

## High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GX/SX Devices

### Table 24. High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GX/SX Devices

The frequencies listed are the maximum frequencies.

| Symbol/Description | Condition (V) | Core Speed Grade with Power Options | | | Unit |
|---|---|---|---|---|---|
| | | -E1H | -E2 / -I2 | -E3 / -I3 | |
| 20-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 516 | 400 | 400 | MHz |
| 20-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 491 | 400 | 400 | MHz |
| 32-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 441 | 404 | 335 | MHz |
| 32-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 441 | 404 | 335 | MHz |
| 64-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 272 | 234 | 222 | MHz |
| 64-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 272 | 234 | 222 | MHz |
| PCIe Gen3 HIP-Fabric interface | $V_{CC}$ = 0.9/0.95 | 300 | 250 | 125 | MHz |

## Transceiver Performance for Intel Arria 10 GT Devices

### Table 25. Transmitter and Receiver Data Rate Performance

| Symbol/Description | Condition | | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Unit |
|---|---|---|---|---|---|
| Chip-to-chip (41) | Maximum data rate $V_{CCR_GXB}$ = $V_{CCT_GXB}$ = 1.12 V | GT Channel (42) | 25.8 | 25.8 | Gbps |
| | | GX Channel | 17.4 | 15 | Gbps |
| | Maximum data rate $V_{CCR_GXB}$ = $V_{CCT_GXB}$ = 1.03 V | GX Channel | 16 | 14.2 | Gbps |
| | Maximum data rate $V_{CCR_GXB}$ = $V_{CCT_GXB}$ = 0.95 V | GX Channel | 11.3 | 11.3 | Gbps |
| | Minimum data rate | GT Channel | 1.0 (43) | | Gbps |
| | | GX Channel | | | |
| Backplane (41) | Maximum data rate $V_{CCR_GXB}$ = $V_{CCT_GXB}$ = 1.12 V | GX Channel | 12.5 | 12.5 | Gbps |
| | Maximum data rate $V_{CCR_GXB}$ = $V_{CCT_GXB}$ = 1.03 V | GX Channel | 12.5 | 12.5 | Gbps |
| | Minimum data rate | GX Channel | 1.0 (43) | | Gbps |

### Table 26. ATX PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Unit |
|---|---|---|---|---|
| Supported Output Frequency | Maximum frequency | 12.9 | | GHz |
| | Minimum frequency | 500 | | MHz |

(41) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(42) GT channels can only achieve 25.8 Gbps when $V_{CCT_GXB}$ = 1.12 V and $V_{CCR_GXB}$ = 1.12 V.

(43) Intel Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

### Table 27. Fractional PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Unit |
|---|---|---|---|---|
| Supported Output Frequency | Maximum frequency | 6.25 | | GHz |
| | Minimum frequency | 500 | | MHz |

### Table 28. CMU PLL Performance

| Symbol/Description | Condition | Transceiver Speed Grade 1 | Transceiver Speed Grade 2 | Unit |
|---|---|---|---|---|
| Supported Output Frequency | Maximum frequency | 5.15625 | | GHz |
| | Minimum frequency | 2450 | | MHz |

#### Related Information

Transceiver Power Supply Operating Conditions on page 10

## High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GT Devices

### Table 29. High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GT Devices

The frequencies listed are the maximum frequencies.

| Symbol/Description | Condition (V) | Core Speed Grade with Power Options | | Unit |
|---|---|---|---|---|
| | | -1 | -2 | |
| 20-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 400 | | MHz |
| 20-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 400 | | MHz |
| 32-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 404 | | MHz |
| 32-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 404 | | MHz |
| 64-bit interface - FIFO | $V_{CC}$ = 0.9/0.95 | 407 | | MHz |
| 64-bit interface - Registered | $V_{CC}$ = 0.9/0.95 | 407 | | MHz |
| PCIe Gen3 HIP-Fabric interface | $V_{CC}$ = 0.9/0.95 | 250 | | MHz |

## Transceiver Specifications for Intel Arria 10 GX, SX, and GT Devices

### Table 30. Reference Clock Specifications

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O Standards | Dedicated reference clock pin | CML, Differential LVPECL, LVDS, and HCSL | | | |
| | RX reference clock pin | CML, Differential LVPECL, and LVDS | | | |
| Input Reference Clock Frequency (CMU PLL) | | 61 | — | 800 | MHz |
| Input Reference Clock Frequency (ATX PLL) | | 100 | — | 800 | MHz |
| Input Reference Clock Frequency (fPLL PLL) | | 25 (44) / 50 (45) | — | 800 | MHz |
| Rise time | 20% to 80% | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | % |
| On-chip termination resistors | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ | Dedicated reference clock pin | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | V |
| Absolute $V_{MIN}$ | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | $V_{CCR_GXB}$ = 0.95 V | — | 0.95 | — | V |

*continued...*

(44) This specification is for HDMI mode only.

(45) This specification is for other non-HDMI modes.

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| | $V_{CCR_GXB}$ = 1.03 V | — | 1.03 | — | V |
| | $V_{CCR_GXB}$ = 1.12 V | — | 1.12 | — | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) (46) | 100 Hz | — | — | –70 | dBc/Hz |
| | 1 kHz | — | — | –90 | dBc/Hz |
| | 10 kHz | — | — | –100 | dBc/Hz |
| | 100 kHz | — | — | –110 | dBc/Hz |
| | ≥ 1 MHz | — | — | –120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) | 1.5 MHz to 100 MHz (PCIe) | — | — | 4.2 | ps (rms) |
| $R_{REF}$ | — | — | 2.0 k ±1% | — | Ω |
| $T_{SSC-MAX-PERIOD-SLEW}$ | Max SSC df/dt | | | 0.75 | |

## Table 31. Transceiver Clocks Specifications

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| CLKUSR pin for transceiver calibration | Transceiver Calibration | 100 | — | 125 | MHz |
| reconfig_clk | Reconfiguration interface | 100 | — | 125 | MHz |

(46) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

## Table 32. Transceiver Clock Network Maximum Data Rate Specifications

| Clock Network | Maximum Performance (47) | | | Channel Span | Unit |
|---|---|---|---|---|---|
| | ATX | fPLL | CMU | | |
| x1 | 17.4 | 12.5 | 10.3125 | 6 channels in a single bank | Gbps |
| x6 | 17.4 | 12.5 | N/A | 6 channels in a single bank | Gbps |
| PLL feedback compensation mode | 17.4 | 12.5 | N/A | Side-wide | Gbps |
| xN at 0.95 V $V_{CCR_GXB}$/ $V_{CCT_GXB}$ | 10.5 | 10.5 | N/A | Up two banks and down two banks (47) (48) | Gbps |
| xN at 1.03 V $V_{CCR_GXB}$/ $V_{CCT_GXB}$ | 15.0 | 12.5 | N/A | Up two banks and down two banks(47) (48) | Gbps |
| xN at 1.12 V $V_{CCR_GXB}$/ $V_{CCT_GXB}$ | 16.0 | 12.5 | N/A | Up two banks and down two banks(47) (48) | Gbps |

## Table 33. Receiver Specifications

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O Standards | — | High Speed Differential I/O, CML , Differential LVPECL , and LVDS(49) | | | |
| Absolute $V_{MAX}$ for a receiver pin (50) | — | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin (50) | — | -0.4 | — | — | V |

***continued...***

(47) The maximum data rate depends on speed grade.

(48) For more information, refer to the PLLs and Clock Networks chapter of the *Intel Arria 10 Transceiver PHY User Guide*.

(49) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(50) The device cannot tolerate prolonged operation at this absolute maximum.

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration | $V_{CCR_GXB}$ = 1.12 V | — | — | 2.0 | V |
| | $V_{CCR_GXB}$ = 1.03 V | — | — | 2.0 | V |
| | $V_{CCR_GXB}$ = 0.95 V | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (51) | — | 50 | — | — | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 30% | — | Ω |
| | 100-Ω setting | — | 100 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) (52) | $V_{CCR_GXB}$ = 0.95 V | — | 600 | — | mV |
| | $V_{CCR_GXB}$ = 1.03 V | — | 700 | — | mV |
| | $V_{CCR_GXB}$ = 1.12 V | — | 700 | — | mV |
| $t_{LTR}$ (53) | — | — | — | 10 | µs |
| $t_{LTD}$ (54) | — | 4 | — | — | µs |
| $t_{LTD_manual}$ (55) | — | 4 | — | — | µs |

*continued...*

(51) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(52) Intel Arria 10 devices only support DC coupling when using the Hybrid Memory Cube (HMC) or the Intel QuickPath Interconnect (QPI) specifications.

(53) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(54) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{LTR_LTD_manual}$(56) | — | 15 | — | — | µs |
| Run Length | — | — | — | 200 | UI |
| CDR PPM tolerance | PCIe-only | -300 | — | 300 | PPM |
| | All other protocols | -1000 | — | 1000 | PPM |
| Programmable DC Gain | Setting = 0-4 | 0 | — | 10 | dB |
| Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gbps with 0.95 V $V_{CCR}$ | Setting = 0-28 | 0 | — | 19 | dB |
| Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gpbs with 1.03 V $V_{CCR}$ | Setting = 0-28 | 0 | — | 21 | dB |
| Programmable AC Gain at High Gain mode and Data Rate ≤ 17.4 Gpbs with 1.03 V $V_{CCR}$ | Setting = 0-28 | 0 | — | 17 | dB |
| Programmable AC Gain at High Data Rate mode | Setting = 0-15 | 0 | — | 8 | dB |

(55) $t_{LTD_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(56) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

## Table 34. Transmitter Specifications

| Symbol/Description | Condition | All Transceiver Speed Grades | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O Standards | — | High Speed Differential I/O [57] | | | — |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | $V_{CCT}$ = 0.95 V | — | 450 | — | mV |
| | $V_{CCT}$ = 1.03 V | — | 500 | — | mV |
| | $V_{CCT}$ = 1.12 V | — | 550 | — | mV |
| $V_{OCM}$ (DC coupled) | $V_{CCT}$ = 0.95 V | — | 450 | — | mV |
| | $V_{CCT}$ = 1.03 V | — | 500 | — | mV |
| | $V_{CCT}$ = 1.12 V | — | 550 | — | mV |
| Rise time [58] | 20% to 80% | 20 | — | 130 | ps |
| Fall time [58] | 80% to 20% | 20 | — | 130 | ps |
| Intra-differential pair skew [59] | TX $V_{CM}$ = 0.5 V and slew rate setting of SLEW_R5 [60] | — | — | 15 | ps |

(57) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Arria 10 transceivers.

(58) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(59) In QPI mode, if $V_{CM}$ < 0.17 V, the input Vid must be greater than 100 mV. If $V_{CM}$ > 0.17 V, the input Vid must be greater than 70 mV.

(60) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

### Table 35. Typical Transmitter $V_{OD}$ Settings

| Symbol | $V_{OD}$ Setting | $V_{OD}$-to-$V_{CCT}$ Ratio |
|---|---|---|
| $V_{OD}$ differential value = $V_{OD}$-to-$V_{CCT}$ ratio x $V_{CCT}$ | 31 | 1.00 |
| | 30 | 0.97 |
| | 29 | 0.93 |
| | 28 | 0.90 |
| | 27 | 0.87 |
| | 26 | 0.83 |
| | 25 | 0.80 |
| | 24 | 0.77 |
| | 23 | 0.73 |
| | 22 | 0.70 |
| | 21 | 0.67 |
| | 20 | 0.63 |
| | 19 | 0.60 |
| | 18 | 0.57 |
| | 17 | 0.53 |
| | 16 | 0.50 |
| | 15 | 0.47 |
| | 14 | 0.43 |
| | 13 | 0.40 |
| | 12 | 0.37 |

### Table 36. Transmitter Channel-to-channel Skew Specifications

| Mode | Channel Span | Maximum Skew | Unit |
|---|---|---|---|
| x6 Clock | Up to 6 channels in one bank | 61 | ps |
| xN Clock | Within 2 banks | 230 | ps |
| | Up 2 banks and down 2 banks | 500 | |
| PLL Feedback Compensation (61), (62), (63) | Side-wide | 1600 | ps |

**Related Information**

PLLs and Clock Networks

## Core Performance Specifications

### Clock Tree Specifications

### Table 37. Clock Tree Performance for Intel Arria 10 Devices

| Parameter | Performance (All Speed Grades) | Unit |
|---|---|---|
| Global clock, regional clock, and small periphery clock | 644 | MHz |
| Large periphery clock | 525 | MHz |

(61) `refclk` is set to 125 MHz during the test.

(62) You can reduce the lane-to-lane skew by increasing the reference clock frequency.

(63) The middle `refclk` location provides the lowest lane-to-lane skew.

# PLL Specifications

## Fractional PLL Specifications

### Table 38. Fractional PLL Specifications for Intel Arria 10 Devices

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | — | 30 | — | 800 (64) | MHz |
| $f_{INPFD}$ | Input clock frequency to the phase frequency detector (PFD) | — | 30 | — | 700 | MHz |
| $f_{CASC_INPFD}$ | Input clock frequency to the PFD of destination cascade PLL | — | 30 | — | 60 | MHz |
| $f_{VCO}$ | PLL voltage-controlled oscillator (VCO) operating range | — | 6 | — | 14.025 | GHz |
| $t_{EINDUTY}$ | Input clock duty cycle | — | 45 | — | 55 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock | — | — | — | 644 | MHz |
| $f_{DYCONFIGCLK}$ | Dynamic configuration clock for `reconfig_clk` | — | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or deassertion of `pll_powerdown` | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop bandwidth | — | 0.3 | — | 4 | MHz |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | Non-SmartVID | — | — | 50 | ps |
| | | SmartVID | — | — | 75 | ps |

*continued...*

(64) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{ARESET}$ | Minimum pulse width on the `pll_powerdown` signal | — | 10 | — | — | ns |
| $t_{INCCJ}$ (65)(66) | Input clock cycle-to-cycle jitter | $F_{REF} \geq 100$ MHz | — | — | 0.13 | UI (p-p) |
| | | $F_{REF} < 100$ MHz | — | — | 650 | ps (p-p) |
| $t_{OUTPJ}$ (67) | Period jitter for clock output | $F_{OUT} \geq 100$ MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT} < 100$ MHz | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ}$ (67) | Cycle-to-cycle jitter for clock output | $F_{OUT} \geq 100$ MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT} < 100$ MHz | — | — | 60 | mUI (p-p) |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | — | — | 32 | — | bit |

### Related Information

- Memory Output Clock Jitter Specifications on page 53
  Provides more information about the external memory interface clock output jitter specifications.
- KDB link: How do I compensate for the jitter of PLL cascading or non-dedicated clock path for Intel Arria 10 PLL reference clock?
  For the Intel Quartus Prime software version prior to 17.1, the fPLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.

(65) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(66) $F_{REF}$ is $f_{IN}/N$, specification applies when $N = 1$.

(67) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Arria 10 Devices table.

## I/O PLL Specifications

### Table 39. I/O PLL Specifications for Intel Arria 10 Devices

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | –1 speed grade | 10 | — | 800 (68) | MHz |
| | | –2 speed grade | 10 | — | 700 (68) | MHz |
| | | –3 speed grade | 10 | — | 650 (68) | MHz |
| $f_{INPFD}$ | Input clock frequency to the PFD | — | 10 | — | 325 | MHz |
| $f_{CASC_INPFD}$ | Input clock frequency to the PFD of destination cascade PLL | — | 10 | — | 60 | MHz |
| $f_{VCO}$ | PLL VCO operating range | –1 speed grade | 600 | — | 1600 | MHz |
| | | –2 speed grade | 600 | — | 1434 | MHz |
| | | –3 speed grade | 600 | — | 1250 | MHz |
| $f_{CLBW}$ | PLL closed-loop bandwidth | — | 0.1 | — | 8 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | — | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock (C counter) | –1, –2, –3 speed grade | — | — | 644 | MHz |
| $f_{OUT_EXT}$ | Output frequency for external clock output | –1 speed grade | — | — | 800 | MHz |
| | | –2 speed grade | — | — | 720 | MHz |
| | | –3 speed grade | — | — | 650 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for dedicated external clock output (when set to 50%) | Non-SmartVID | 45 | 50 | 55 | % |
| | | SmartVID | 42 | 50 | 58 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | — | 10 | ns |

*continued...*

(68) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DYCONFIGCLK}$ | Dynamic configuration clock for `mgmt_clk` and `scanclk` | — | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or deassertion of `areset` | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | — | 10 | — | — | ns |
| $t_{INCCJ}$ (69)(70) | Input clock cycle-to-cycle jitter | $F_{REF}$ ≥ 100 MHz | — | — | 0.15 | UI (p-p) |
| | | $F_{REF}$ < 100 MHz | — | — | 750 | ps (p-p) |
| $t_{OUTPJ_DC}$ | Period jitter for dedicated clock output | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{OUTCCJ_DC}$ | Cycle-to-cycle jitter for dedicated clock output | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{OUTPJ_IO}$ (71) | Period jitter for clock output on the regular I/O | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ_IO}$ (71) | Cycle-to-cycle jitter for clock output on the regular I/O | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{CASC_OUTPJ_DC}$ | Period jitter for dedicated clock output in cascaded PLLs | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |

(69) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(70) $F_{REF}$ is $f_{IN}/N$, specification applies when $N$ = 1.

(71) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Arria 10 Devices table.

### Related Information

- Memory Output Clock Jitter Specifications on page 53
  Provides more information about the external memory interface clock output jitter specifications.
- KDB link: How do I compensate for the jitter of PLL cascading or non-dedicated clock path for Intel Arria 10 PLL reference clock?
  For the Intel Quartus Prime software version prior to 17.1, the I/O PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.

## DSP Block Specifications

**Table 40. DSP Block Performance Specifications for Intel Arria 10 Devices ($V_{CC}$ and $V_{CCP}$ at 0.9 V Typical Value)**

| Mode | Performance | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | –E1S, –E1H | –I1S, –I1H | –E2L, –E2S | –I2L, –I2S | –E3S, –E3V | –I3S, –I3V | |
| Fixed-point 18 × 19 multiplication mode | 548 | 528 | 456 | 438 | 364 | 346 | MHz |
| Fixed-point 27 × 27 multiplication mode | 541 | 522 | 450 | 434 | 358 | 344 | MHz |
| Fixed-point 18 × 18 multiplier adder mode | 548 | 529 | 459 | 440 | 370 | 351 | MHz |
| Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode | 539 | 517 | 444 | 422 | 349 | 326 | MHz |
| Fixed-point 18 × 19 systolic mode | 548 | 529 | 459 | 440 | 370 | 351 | MHz |
| Complex 18 × 19 multiplication mode | 548 | 528 | 456 | 438 | 364 | 346 | MHz |
| Floating point multiplication mode | 548 | 527 | 447 | 427 | 347 | 326 | MHz |
| Floating point adder or subtract mode | 488 | 471 | 388 | 369 | 288 | 266 | MHz |
| Floating point multiplier adder or subtract mode | 483 | 465 | 386 | 368 | 290 | 270 | MHz |
| Floating point multiplier accumulate mode | 510 | 490 | 418 | 393 | 326 | 294 | MHz |
| Floating point vector one mode | 502 | 482 | 404 | 382 | 306 | 282 | MHz |
| Floating point vector two mode | 474 | 455 | 383 | 367 | 293 | 278 | MHz |

**Table 41. DSP Block Performance Specifications for Intel Arria 10 Devices ($V_{CC}$ and $V_{CCP}$ at 0.95 V Typical Value)**

| Mode | Performance | | Unit |
|---|---|---|---|
| | –I1S, –I1H | –I2L, –I2S | |
| Fixed-point 18 × 19 multiplication mode | 635 | 517 | MHz |
| Fixed-point 27 × 27 multiplication mode | 633 | 517 | MHz |
| Fixed-point 18 × 18 multiplier adder mode | 635 | 516 | MHz |
| Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode | 631 | 509 | MHz |
| Fixed-point 18 × 19 systolic mode | 635 | 516 | MHz |
| Complex 18 × 19 multiplication mode | 635 | 517 | MHz |
| Floating point multiplication mode | 635 | 501 | MHz |
| Floating point adder or subtract mode | 564 | 468 | MHz |
| Floating point multiplier adder or subtract mode | 564 | 475 | MHz |
| Floating point multiplier accumulate mode | 581 | 482 | MHz |
| Floating point vector one mode | 574 | 471 | MHz |
| Floating point vector two mode | 550 | 450 | MHz |

## Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $f_{MAX}$.

## Table 42. Memory Block Performance Specifications for Intel Arria 10 Devices ($V_{CC}$ and $V_{CCP}$ at 0.9 V Typical Value)

| Memory | Mode | Performance | | | | | |
|---|---|---|---|---|---|---|---|
| | | –E1S, –E1H | –I1S, –I1H | –E2L, –E2S, –I2L, –I2S | –E3S, –E3V | –I3S, –I3V | Unit |
| MLAB | Single port, all supported widths (×16/×32) | 700 | 660 | 570 | 490 | 490 | MHz |
| | Simple dual-port, all supported widths (×16/×32) | 700 | 660 | 570 | 490 | 490 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 460 | 450 | 400 | 330 | 330 | MHz |
| | ROM, all supported width (×16/×32) | 700 | 660 | 570 | 490 | 490 | MHz |
| M20K Block | Single-port, all supported widths | 730 | 690 | 625 | 530 | 510 | MHz |
| | Simple dual-port, all supported widths | 730 | 690 | 625 | 530 | 510 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 550 | 520 | 470 | 410 | 410 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 470 | 450 | 410 | 360 | 360 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 620 | 590 | 520 | 470 | 470 | MHz |
| | True dual port, all supported widths | 730 | 690 | 600 | 480 | 480 | MHz |
| | ROM, all supported widths | 730 | 690 | 625 | 530 | 510 | MHz |

## Table 43. Memory Block Performance Specifications for Intel Arria 10 Devices ($V_{CC}$ and $V_{CCP}$ at 0.95 V Typical Value)

| Memory | Mode | Performance | | |
|---|---|---|---|---|
| | | –I1S, –I1H | –I2L, –I2S | Unit |
| MLAB | Single port, all supported widths (×16/×32) | 706 | 610 | MHz |
| | Simple dual-port, all supported widths (×16/×32) | 706 | 610 | MHz |
| | Simple dual-port with read and write at the same address | 482 | 428 | MHz |
| | ROM, all supported width (×16/×32) | 706 | 610 | MHz |
| M20K Block | Single-port, all supported widths | 735 | 670 | MHz |

*continued...*

| Memory | Mode | Performance | | |
|---|---|---|---|---|
| | | –I1S, –I1H | –I2L, –I2S | Unit |
| | Simple dual-port, all supported widths | 735 | 670 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 555 | 500 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 480 | 440 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 630 | 555 | MHz |
| | True dual port, all supported widths | 735 | 640 | MHz |
| | ROM, all supported widths | 735 | 670 | MHz |

## Temperature Sensing Diode Specifications

### Internal Temperature Sensing Diode Specifications

**Table 44. Internal Temperature Sensing Diode Specifications for Intel Arria 10 Devices**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution |
|---|---|---|---|---|---|
| –40 to 125°C | ±5°C | No | 1 MHz | < 5 ms | 10 bits |

#### Related Information

Transfer Function for Internal TSD
Provides the transfer function for the internal TSD.

## External Temperature Sensing Diode Specifications

### Table 45. External Temperature Sensing Diode Specifications for Intel Arria 10 Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $I_{bias}$, diode source current | 10 | — | 100 | µA |
| $V_{bias}$, voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | — | 1.03 | — | — |

## Internal Voltage Sensor Specifications

### Table 46. Internal Voltage Sensor Specifications for Intel Arria 10 Devices

| Parameter | | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Resolution | | — | — | 6 | Bit |
| Sampling rate | | — | — | 500 | Ksps |
| Differential non-linearity (DNL) | | — | — | ±1 | LSB |
| Integral non-linearity (INL) | | — | — | ±1 | LSB |
| Gain error | | — | — | ±1 | % |
| Offset error | | — | — | ±1 | LSB |
| Input capacitance | | — | 20 | — | pF |
| Clock frequency | | 0.1 | — | 11 | MHz |
| Unipolar Input Mode | Input signal range for Vsigp | 0 | — | 1.5 | V |
| | Common mode voltage on Vsign | 0 | — | 0.25 | V |
| | Input signal range for Vsigp – Vsign | 0 | — | 1.25 | V |

# Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

### Table 47. High-Speed I/O Specifications for Intel Arria 10 Devices

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

The Intel Arria 10 devices support the following output standards using true LVDS output buffer types on all I/O banks:

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

| Symbol | Condition | –E1S(72), –E1H, –I1S(72), –I1H | | | –E2L, –E2S(72), –I2L, –I2S(72) | | | –E3L, –E3S(72), –E3V, –I3L, –I3S(72), –I3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK_in}$ (input clock frequency) True Differential I/O Standards | Clock boost factor W = 1 to 40 (73) | 10 | — | 800 | 10 | — | 700 | 10 | — | 625 | MHz |
| $f_{HSCLK_in}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor W = 1 to 40 (73) | 10 | — | 625 | 10 | — | 625 | 10 | — | 525 | MHz |
| $f_{HSCLK_OUT}$ (output clock frequency) | — | — | — | 800 (74) | — | — | 700 (74) | — | — | 625 (74) | MHz |

*continued...*

(72) –E1S and –E2S speed grades are applicable to both $V_{CC}$ = 0.9 V and 0.95 V. –E3S speed grade is only applicable to $V_{CC}$ = 0.9 V.

(73) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(74) This is achieved by using the PHY clock network.

| Symbol | | Condition | –E1S(72), –E1H, –I1S(72), –I1H | | | –E2L, –E2S(72), –I2L, –I2S(72) | | | –E3L, –E3S(72), –E3V, –I3L, –I3S(72), –I3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | True Differential I/O Standards - $f_{HSDR}$ (data rate) (75) | SERDES factor J = 4 to 10 (76)(77)(78) | (78) | — | 1600 | (78) | — | 1434 | (78) | — | 1250 | Mbps |
| | | SERDES factor J = 3 (76)(77)(78) | (78) | — | 1200 | (78) | — | 1076 | (78) | — | 938 | Mbps |
| | | SERDES factor J = 2, uses DDR registers | (78) | — | 333 (79) | (78) | — | 275 (79) | (78) | — | 250 (79) | Mbps |
| | | SERDES factor J = 1, uses DDR registers | (78) | — | 333 (79) | (78) | — | 275 (79) | (78) | — | 250 (79) | Mbps |
| | $t_{x\ Jitter}$ - True Differential I/O Standards | Total jitter for data rate, 600 Mbps – 1.6 Gbps | — | — | 160 | — | — | 200 | — | — | 250 | ps |
| | | Total jitter for data rate, < 600 Mbps | — | — | 0.1 | — | — | 0.12 | — | — | 0.15 | UI |

*continued...*

(72) –E1S and –E2S speed grades are applicable to both $V_{CC}$ = 0.9 V and 0.95 V. –E3S speed grade is only applicable to $V_{CC}$ = 0.9 V.

(75) Requires package skew compensation with PCB trace length.

(76) The $F_{max}$ specification is based on the fast clock used for serial data. The interface $F_{max}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(77) The $V_{CC}$ and $V_{CCP}$ must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(78) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency ($f_{OUT}$) provided you can close the design timing and the signal integrity meets the interface requirements.

| Symbol | | Condition | –E1S(72), –E1H, –I1S(72), –I1H | | | –E2L, –E2S(72), –I2L, –I2S(72) | | | –E3L, –E3S(72), –E3V, –I3L, –I3S(72), –I3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | $t_{DUTY}$ (80) | TX output clock duty cycle for Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| | $t_{RISE\ \&}$ & $t_{FALL}$ (77)(81) | True Differential I/O Standards | — | — | 160 | — | — | 180 | — | — | 200 | ps |
| | TCCS (80)(75) | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| Receiver | True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 4 to 10 (76)(77)(78) | 150 | — | 1600 | 150 | — | 1434 | 150 | — | 1250 | Mbps |
| | | SERDES factor J = 3 (76)(77)(78) | 150 | — | 1200 | 150 | — | 1076 | 150 | — | 938 | Mbps |
| | $f_{HSDR}$ (data rate) (without DPA) (75) | SERDES factor J = 3 to 10 | (78) | — | (82) | (78) | — | (82) | (78) | — | (82) | Mbps |
| | | SERDES factor J = 2, uses DDR registers | (78) | — | (79) | (78) | — | (79) | (78) | — | (79) | Mbps |
| | | SERDES factor J = 1, uses DDR registers | (78) | — | (79) | (78) | — | (79) | (78) | — | (79) | Mbps |
| DPA (FIFO mode) | DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| DPA (soft CDR mode) | DPA run length | SGMII/GbE protocol | — | — | 5 | — | — | 5 | — | — | 5 | UI |

continued...

(72) –E1S and –E2S speed grades are applicable to both $V_{CC}$ = 0.9 V and 0.95 V. –E3S speed grade is only applicable to $V_{CC}$ = 0.9 V.

(80) Not applicable for `DIVCLK` = 1.

(81) This applies to default pre-emphasis and $V_{OD}$ settings only.

(82) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

| Symbol | | Condition | –E1S(72), –E1H, –I1S(72), –I1H | | | –E2L, –E2S(72), –I2L, –I2S(72) | | | –E3L, –E3S(72), –E3V, –I3L, –I3S(72), –I3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | All other protocols | — | — | 50 data transition per 208 UI | — | — | 50 data transition per 208 UI | — | — | 50 data transition per 208 UI | — |
| Soft CDR mode | Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | ± ppm |
| Non DPA mode | Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |

## DPA Lock Time Specifications

### Table 48. DPA Lock Time Specifications for Intel Arria 10 Devices

The specifications are applicable to both extended and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions (83) | Maximum Data Transition (84) |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 |
| | 10010000 | 4 | 64 | 640 |
| Miscellaneous | 10101010 | 8 | 32 | 640 |
| | 01010101 | 8 | 32 | 640 |

(72) –E1S and –E2S speed grades are applicable to both $V_{CC}$ = 0.9 V and 0.95 V. –E3S speed grade is only applicable to $V_{CC}$ = 0.9 V.

(83) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

(84) This is the maximum data transition consumed by DPA to lock.

## LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

**Figure 2. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps**

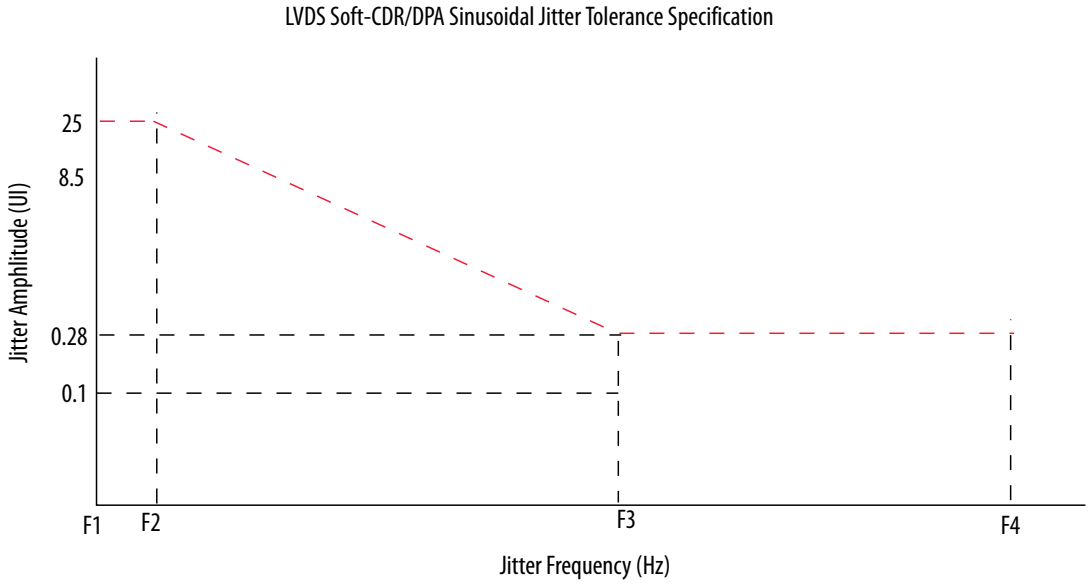
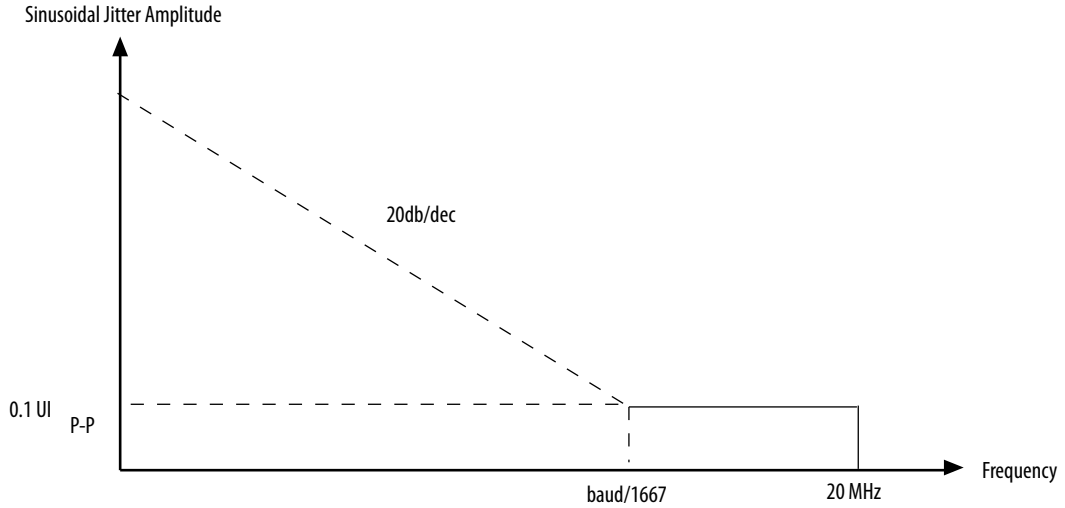



**Table 49. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.00 |
| F2 | 17,565 | 25.00 |
| F3 | 1,493,000 | 0.28 |
| F4 | 50,000,000 | 0.28 |

**Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps**




## Memory Standards Supported by the Hard Memory Controller

**Table 50. Memory Standards Supported by the Hard Memory Controller for Intel Arria 10 Devices**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|---|---|---|---|
| DDR4 SDRAM | Quarter rate | Yes | 1,200 |
| DDR3 SDRAM | Quarter rate | Yes | 1,066 |
| DDR3L SDRAM | Quarter rate | Yes | 933 |
| LPDDR3 SDRAM | Quarter rate | — | 800 |

### Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

## Memory Standards Supported by the Soft Memory Controller

### Table 51. Memory Standards Supported by the Soft Memory Controller for Intel Arria 10 Devices

This table lists the overall capability of the soft memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| RLDRAM 3(85) | Quarter rate | 1,200 |
| QDR IV SRAM(85) | Quarter rate | 1,066 |
| QDR II SRAM | Half rate | 633 |
| QDR II+ SRAM | Half rate | 633 |
| QDR II+ Xtreme SRAM | Half rate | 633 |

#### Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

## Memory Standards Supported by the HPS Hard Memory Controller

### Table 52. Memory Standards Supported by the HPS Hard Memory Controller for Intel Arria 10 Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,066 |
| DDR3L SDRAM | Half rate | 933 |

#### Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(85) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

## DLL Range Specifications

### Table 53. DLL Frequency Range Specifications for Intel Arria 10 Devices

Intel Arria 10 devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

| Parameter | Performance (for All Speed Grades) | Unit |
|---|---|---|
| DLL operating frequency range | 600 – 1333 | MHz |

## DQS Logic Block Specifications

### Table 54. DQS Phase Shift Error Specifications for DLL-Delayed Clock ($t_{DQS_PSERR}$) for Intel Arria 10 Devices

This error specification is the absolute maximum and minimum error.

| Symbol | Performance (for All Speed Grades) | Unit |
|---|---|---|
| $t_{DQS_PSERR}$ | 5 | ps |

## Memory Output Clock Jitter Specifications

### Table 55. Memory Output Clock Jitter Specifications for Intel Arria 10 Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) $10^{-12}$, equivalent to 14 sigma.

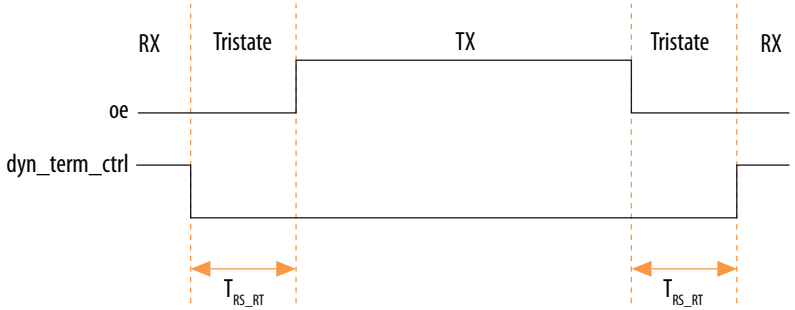
| Protocol | Parameter | Symbol | Non-SmartVID | | | SmartVID (–3V Speed Grade) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Data Rate (Mbps) | Min | Max | Data Rate (Mbps) | Min | Max | |
| DDR3 | Clock period jitter | $t_{JIT(per)}$ | 2,133 | –40 | 40 | 1,600 | –70 | 70 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | 2,133 | –40 | 40 | 1,600 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | 2,133 | –40 | 40 | 1,600 | –100 | 100 | ps |
| DDR4 | Clock period jitter | $t_{JIT(per)}$ | 2,400 | –40 | 40 | 1,600 | –63 | 63 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | 2,400 | –40 | 40 | 1,600 | –63 | 63 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | 2,400 | –40 | 40 | 1,600 | –100 | 100 | ps |

## OCT Calibration Block Specifications

### Table 56. OCT Calibration Block Specifications for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for $R_S$ OCT /$R_T$ OCT calibration | > 2000 | — | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS_RT}$ | Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT | — | 2.5 | — | ns |

### Figure 4. Timing Diagram for on oe and dyn_term_ctrl Signals




## HPS Specifications

This section provides HPS specifications and timing for Intel Arria 10 devices.

If you are using the early I/O release configuration flow, you cannot initially use SmartVID to power your device. Instead, you can use a fixed power supply until after the FPGA is configured. When the FPGA is configured, you can then enable SmartVID.

## HPS Reset Input Requirements

### Table 57. HPS Reset Input Requirements for Intel Arria 10 Devices

| Description | Min | Max | Unit |
|---|---|---|---|
| HPS cold reset pulse width | 600 | — | ns |
| HPS warm reset pulse width | 600 | — | ns |
| Cold reset deassertion to BSEL sampling, using `osc1_clk` (86) | — | 1000 | `osc1_clk` cycles |
| Cold reset deassertion to BSEL sampling, using secure clock, without RAM clearing | — | 100 | µs |
| Cold reset deassertion to BSEL sampling, using secure clock, with RAM clearing | — | 50 | ms |

(86) `osc1_clk` is supplied from the `HPS_CLK1` pin.

## HPS Clock Performance

### Table 58. Maximum HPS Clock Frequencies Across Device Speed Grades for Intel Arria 10 Devices

| HPS Clock | Temperature Grade | $V_{CCL_HPS}$ = 0.9 V (typical) | | | $V_{CCL_HPS}$ = 0.95 V (typical) (87) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | –1 Speed Grade | –2 Speed Grade | –3 Speed Grade | –1 Speed Grade | –2 Speed Grade | –3 Speed Grade | |
| mpu_base_clk | All | 1,200 | 1,000 | 800 | 1,500 | 1,200 | 1,000 | MHz |
| noc_base_clk | All | 400 | 400 | 300 | 500 | 400 | 300 | MHz |
| hmc_free_clk (88) | All | 600 | 533 | 467 | 600 | 533 | 467 | MHz |

#### Related Information

- Clock Select, Intel Arria 10 Hard Processor System Technical Reference Manual
  Provides information on the Clock Select (CSEL) values that require higher voltage operation.
- SoC Security chapter, Intel Arria 10 Hard Processor System Technical Reference Manual
  Provides information about programming fuses.
- External Memory Interface Spec Estimator
  Provides the specific details of the maximum allowed SDRAM operating frequency, which is twice the frequency of `hmc_free_clk`.

## HPS PLL Specifications

### HPS PLL Input Requirements

The HPS main PLL receives the clock signal from the `HPS_CLK1` pin. For details on this pin, refer to the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*.

(87) You must use 0.95 V $V_{CCL_HPS}$ for CSEL values of 0x7 – 0xE.

(88) The hmc_free_clk is 1/2 of the SDRAM interface clock. For the external memory interface clock specifications, refer to the External Memory Interface Spec Estimator.

### Table 59. HPS PLL Input Requirements for Intel Arria 10 Devices

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Clock input range | 10 | — | 50 | MHz |
| Clock input jitter tolerance | — | — | 2 | % |
| Clock input duty cycle | 45 | 50 | 55 | % |

#### Related Information

Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines
Provides more information about the `HPS_CLK1` pin.

## HPS PLL Performance

### Table 60. HPS PLL Performance for Intel Arria 10 Devices

| Description | $V_{CCL_HPS}$ | –1 Speed Grade | | –2 Speed Grade | | –3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| HPS PLL VCO output | 0.95 V | 320 | 3,000 | 320 | 2,400 | 320 | 2,000 | MHz |
| | 0.90 V | 320 | 2,400 | 320 | 2,000 | 320 | 1,600 | MHz |
| h2f_user0_clk | — | — | 400 | — | 400 | — | 400 | MHz |
| h2f_user1_clk | — | — | 400 | — | 400 | — | 400 | MHz |

## HPS PLL Output Specifications

### Table 61. HPS PLL Output Specifications for Intel Arria 10 Devices

| Description | Min | Max | Max | Unit |
|---|---|---|---|---|
| Clock jitter tolerance | –2.5 | — | 2.5 | % |
| Clock duty cycle | 45 | 50 | 55 | % |
| Clock rise time | 350 | — | 1075 | ps |
| Clock fall time | 200 | — | 450 | ps |
| HPS PLL lock time | — | — | 3.6 | ms |

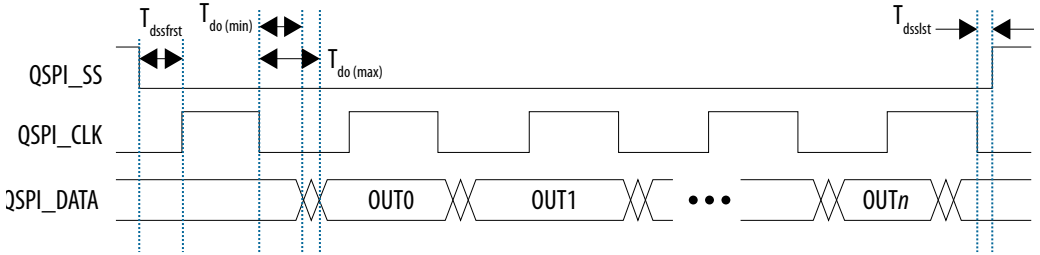
## Quad SPI Flash Timing Characteristics

### Table 62. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Intel Arria 10 Devices

Note that the Intel Arria 10 HPS boot loader calibrates the input timing automatically.

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{qspi_ref_clk}$ | QSPI_REF_CLK clock period | 2.5 | — | — | ns |
| $T_{clk}$ | QSPI_CLK clock period | 9.25 | — | — | ns |
| $T_{dutycycle}$ | QSPI_CLK duty cycle | 45 | 50 | 55 | % |
| $T_{dssfrst}$ (89) | QSPI_SS asserted to first QSPI_CLK edge | 3.6 | — | 5.25 | ns |
| $T_{dsslst}$ (89) | Last QSPI_CLK edge to QSPI_SS deasserted | –1 | — | 1 | ns |
| $T_{do}$ | QSPI_DATA output delay | 0 | — | 2.6 | ns |
| $T_{su}$ | Input setup with respect to QSPI_CLK capture edge | $6.5 - (R_{delay} \times T_{qspi_ref_clk})$ (90) | — | — | ns |
| $T_{h}$ | Input hold with respect to QSPI_CLK capture edge | $(R_{delay} + 1) \times T_{qspi_ref_clk}$ (90) | — | — | ns |
| $T_{dssb2b}$ (89) | Minimum delay of slave select deassertion between two back-to-back transfer | 1 | — | — | QSPI_CLK |

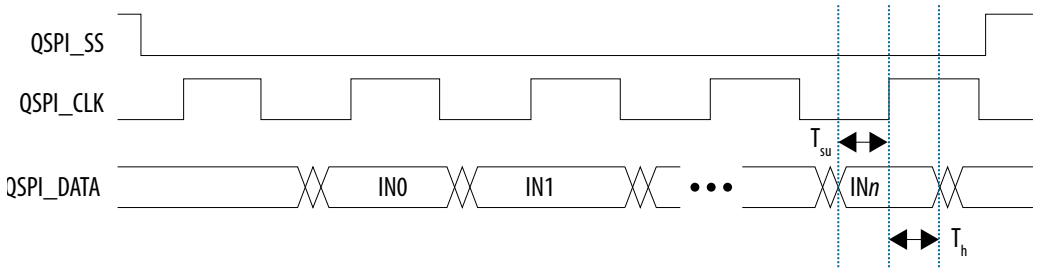
### Figure 5. Quad SPI Flash Serial Output Timing Diagram




(89) This delay is programmable in whole QSPI_REF_CLK increments using the `delay` register in the Quad SPI module.

(90) $R_{delay}$ is programmable in whole QSPI_REF_CLK increments using the delay field in the `rddatacap` register in the Quad SPI module.

**Figure 6. Quad SPI Flash Serial Input Timing Diagram**




## SPI Timing Characteristics

**Table 63. SPI Master Timing Requirements for Intel Arria 10 Devices**

You can adjust the input delay timing by programming the `rx_sample_dly` register.

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | SPI_CLK clock period | 16.67 | — | — | ns |
| $T_{dutycycle}$ | SPI_CLK duty cycle | 45 | 50 | 55 | % |
| $T_{dssfrst}$ (91) | SPI_SS asserted to first SPI_CLK edge | 1.5 × $T_{SPI_CLK}$ – 2 | — | — | ns |
| $T_{dsslst}$ (91) | Last SPI_CLK edge to SPI_SS deasserted | $T_{SPI_CLK}$ – 2 | — | — | ns |
| $T_{dio}$ | Master-out slave-in (MOSI) output delay | –1 | — | 1 | ns |

***continued...***

(91) SPI_SS behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{su}$ (92) | Input setup in respect to SPI_CLK capture edge | 16 – (rx_sample_dly × $T_{spi_ref_clk}$) (93) (94) | — | — | ns |
| $T_h$ (92) | Input hold in respect to SPI_CLK capture edge | 0 | — | — | ns |
| $T_{dssb2b}$ | Minimum delay of slave select deassertion between two back-to-back transfers (frames) | 1 | — | — | SPI_CLK |

(92) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the scpol register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

(93) A rx_sample_dly value of 0 is an invalid setting.

(94) SPI_REF_CLK is the internal reference clock of the SPI Slave, which is l4_main_clk.

**Figure 7. SPI Master Output Timing Diagram**

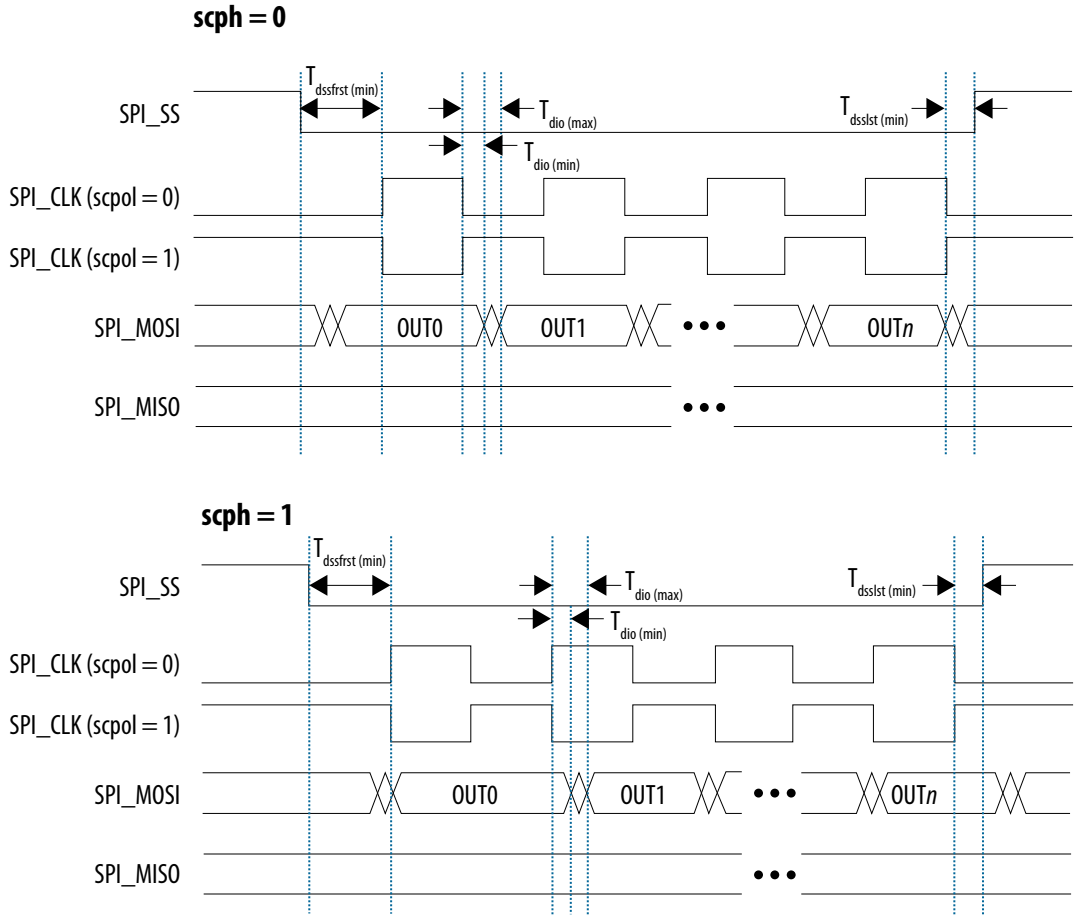
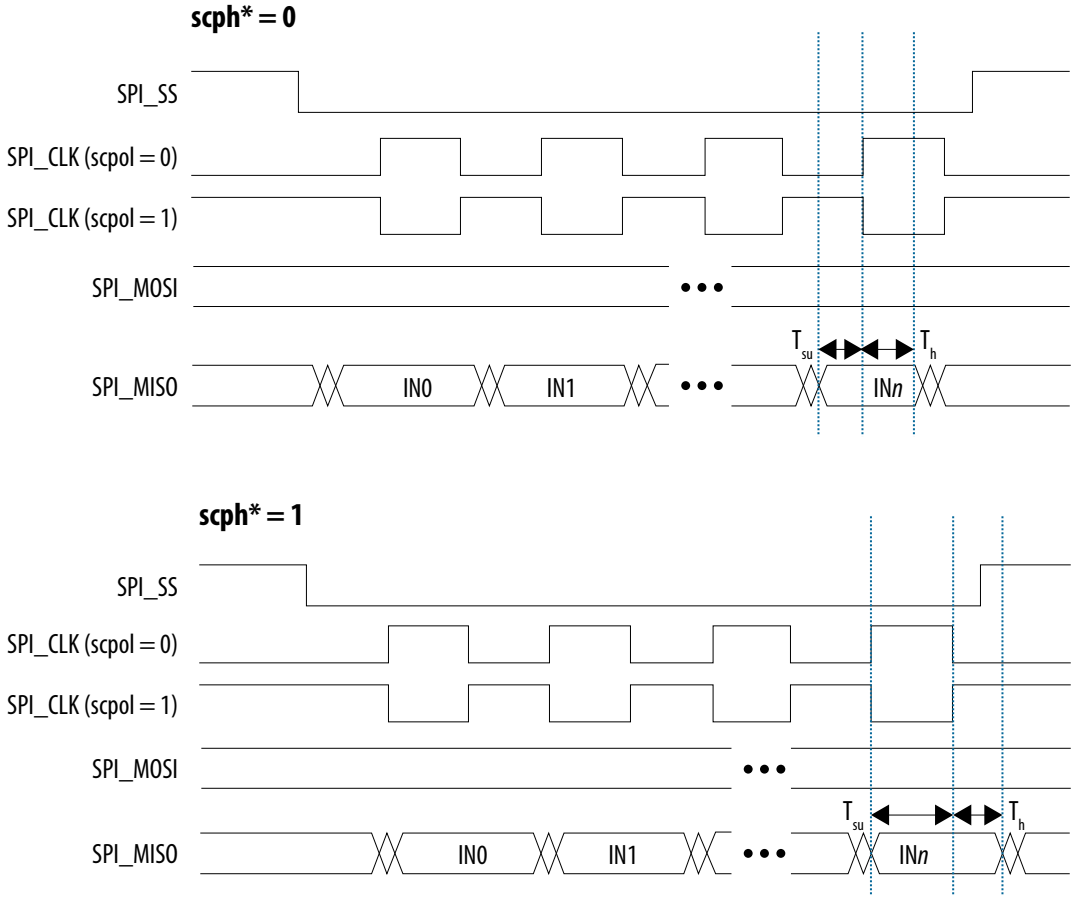


**Figure 8. SPI Master Input Timing Diagram**



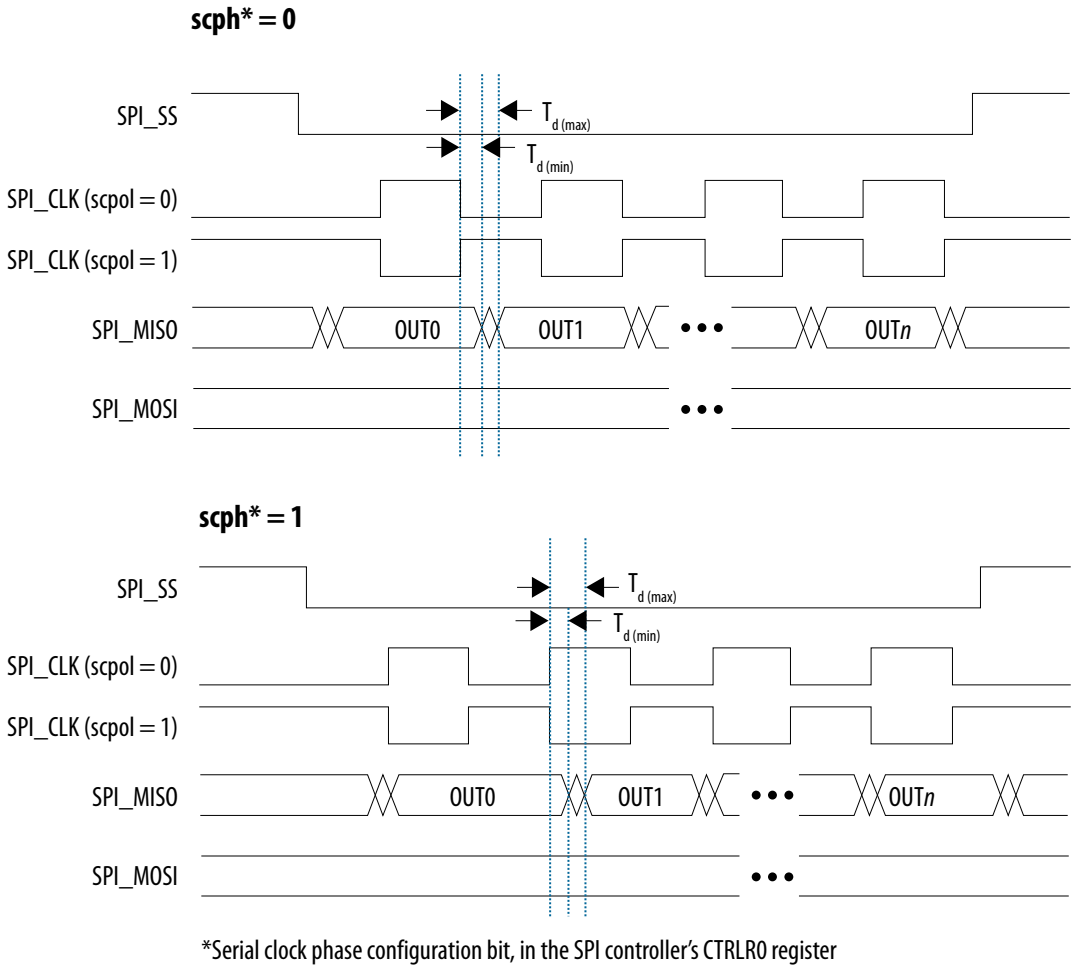

*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

### Table 64. SPI Slave Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | SPI_CLK clock period | 20 | — | — | ns |
| $T_{dutycycle}$ | SPI_CLK duty cycle | 45 | 50 | 55 | % |
| $T_s$ | SPI slave input setup time | 5 | — | — | ns |
| $T_h$ | SPI slave input hold time | 8 | — | — | ns |
| $T_{suss}$ | SPI_SS asserted to first SCLK_IN edge | 5 | — | — | ns |
| $T_{hss}$ | Last SCLK_IN edge to SPI_SS deasserted | 5 | — | — | ns |
| $T_d$ | Master-in slave-out (MISO) output delay | $2 \times T_{spi_ref_clk} + 5.3$ (95) | — | $3 \times T_{spi_ref_clk} + 11.8$ (95) | ns |

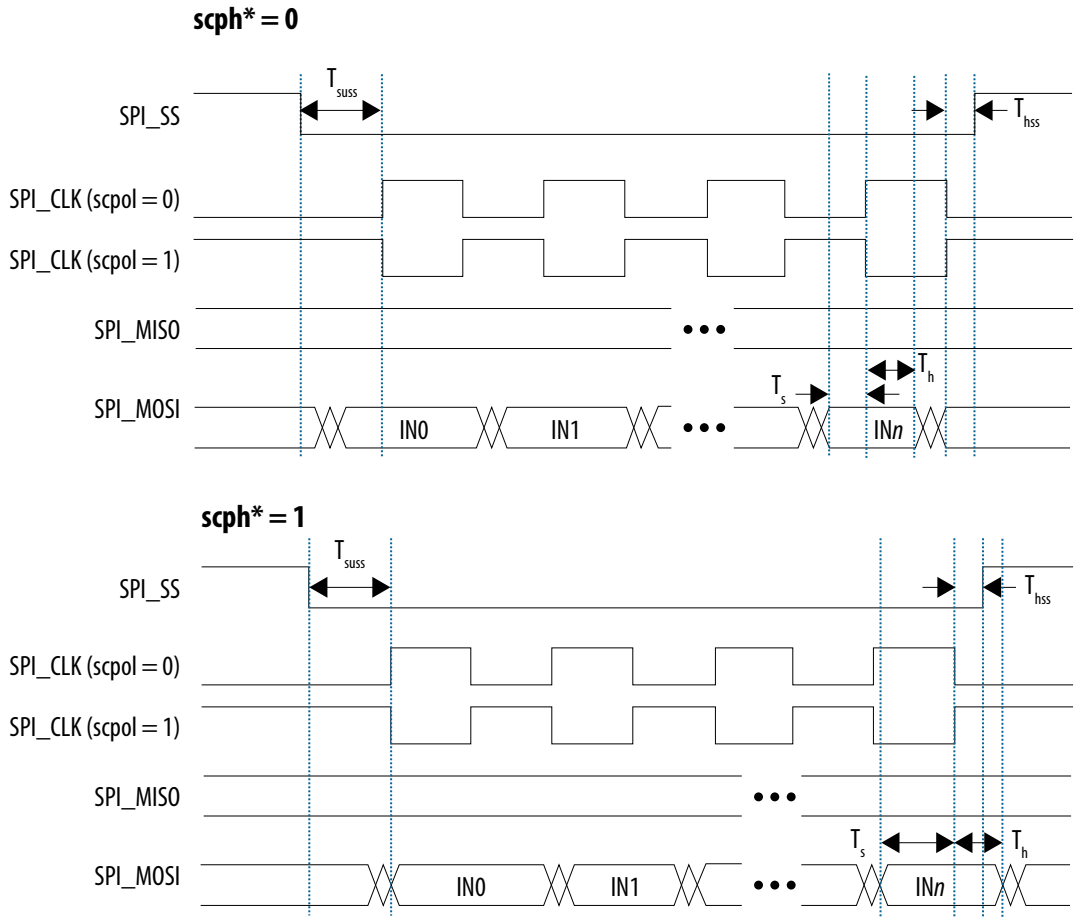
(95) `SPI_REF_CLK` is the internal reference clock of the SPI Slave, which is `l4_main_clk`.

**Figure 9. SPI Slave Output Timing Diagram**




*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

**Figure 10. SPI Slave Input Timing Diagram**




*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

## SD/MMC Timing Characteristics

### Table 65. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Arria 10 Devices

These timings apply to SD, MMC, and embedded MMC cards operating at 1.8 V and 3.0 V.

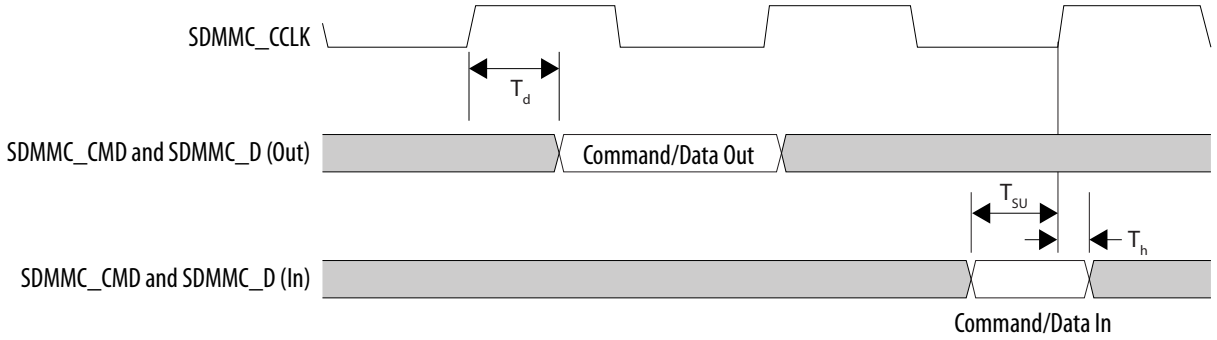
| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{sdmmc_cclk}$ | SDMMC_CCLK clock period (Identification mode) | — | 2500 | — | ns |
| | SDMMC_CCLK clock period (Standard SD mode) | — | 40 | — | ns |
| | SDMMC_CCLK clock period (High speed SD mode) | — | 20 | — | ns |
| $T_{dutycycle}$ | SDMMC_CCLK duty cycle | 45 | 50 | 55 | % |
| $T_{su}$ | SDMMC_CMD/SDMMC_D[7:0] input setup (96) | 7 – (l4_mp_clk × smplsel/2) | — | — | ns |
| $T_h$ | SDMMC_CMD/SDMMC_D[7:0] input hold (96) | –2.5 + (l4_mp_clk × smplsel/2) | — | — | ns |
| $T_d$ | SDMMC_CMD/SDMMC_D[7:0] output delay (97) | –1 + (l4_mp_clk × drvsel/2) (98) | — | 4 + (l4_mp_clk × drvsel/2) (98) | ns |

(96) When smplsel is set to 2 (in the system manager) and the reference clock (l4_mp_clk) is 200 MHz for example, the setup time is 2 ns and the hold time is 2.5 ns. The Boot ROM uses a smplsel setting of 0 and U-Boot can adjust this setting later in the boot process.

(97) When drvsel is set to 3 (in the system manager) and the reference clock (l4_mp_clk) is 200 MHz for example, the output delay time is 6.5 to 11.5 ns. The Boot ROM uses a drvsel setting of 3 and the Intel Quartus Prime software can adjust this setting later in the boot process. drvsel set to 0 is not a valid setting.

(98) l4_mp_clk is the SD/MMC controller reference clock.

**Figure 11. SD/MMC Timing Diagram**



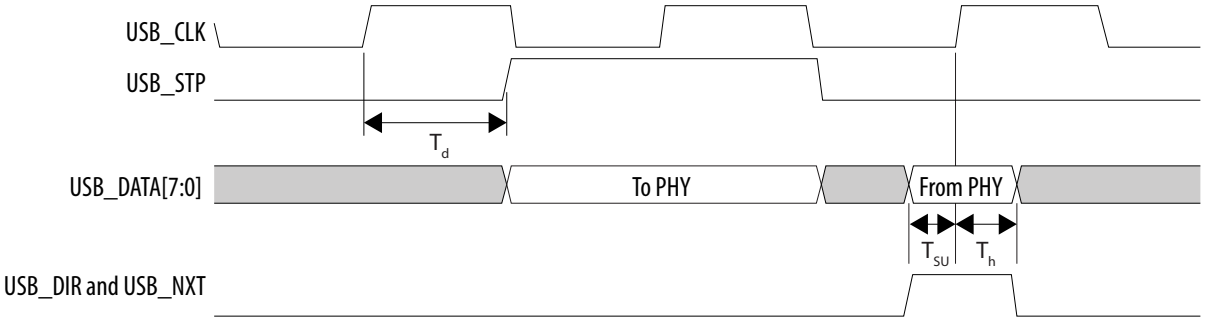

## USB ULPI Timing Characteristics

**Table 66. USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Arria 10 Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | USB_CLK clock period | — | 16.667 | — | ns |
| $T_d$(99) | Clock to USB_STP/USB_DATA[7:0] output delay | 1.5 | — | 8 | ns |
| $T_{su}$ | Setup time for USB_DIR/USB_NXT/USB_DATA[7:0] | 2 | — | — | ns |
| $T_h$ | Hold time for USB_DIR/USB_NXT/USB_DATA[7:0] | 1 | — | — | ns |

(99) For the maximum trace length, refer to the Intel Arria 10 SoC Device Design Guidelines.

**Figure 12. USB ULPI Timing Diagram**




**Related Information**

USB Interface Design Guidelines, Intel Arria 10 SoC Device Design Guidelines

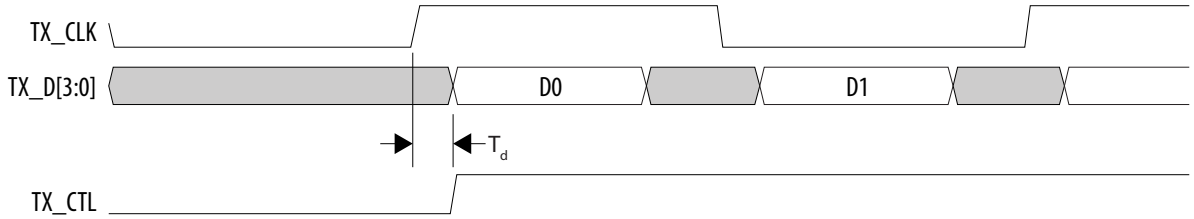
## Ethernet Media Access Controller (EMAC) Timing Characteristics

**Table 67. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Arria 10 Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | TX_CLK clock period | — | 8 | — | ns |
| $T_{clk}$ (100Base-T) | TX_CLK clock period | — | 40 | — | ns |
| $T_{clk}$ (10Base-T) | TX_CLK clock period | — | 400 | — | ns |
| $T_{dutycycle}$ | TX_CLK duty cycle | 45 | 50 | 55 | % |
| $T_d$ (100) | TX_CLK to TXD/TX_CTL output data delay | –0.5 | — | 0.5 | ns |

(100) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

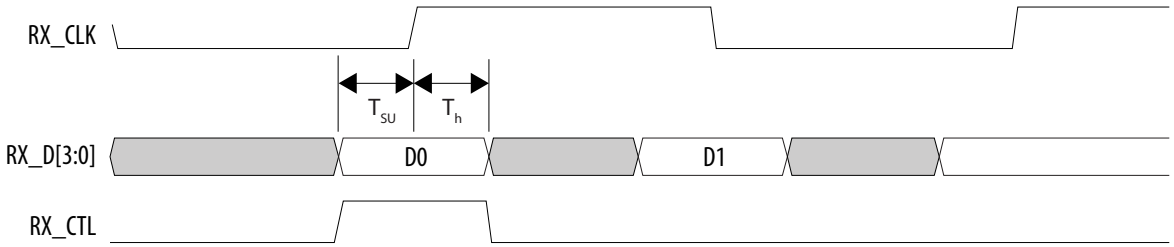
### Figure 13. RGMII TX Timing Diagram




### Table 68. RGMII RX Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | RX_CLK clock period | — | 8 | — | ns |
| $T_{clk}$ (100Base-T) | RX_CLK clock period | — | 40 | — | ns |
| $T_{clk}$ (10Base-T) | RX_CLK clock period | — | 400 | — | ns |
| $T_{su}$ | RX_D/RX_CTL setup time | 1 | — | — | ns |
| $T_h$ (101) | RX_D/RX_CTL hold time | 1 | — | — | ns |

### Figure 14. RGMII RX Timing Diagram




(101) For more information, refer to the Intel Arria 10 SoC Device Design Guidelines.

### Table 69. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (100Base-T) | TX_CLK clock period | — | 20 | — | ns |
| $T_{clk}$ (10Base-T) | TX_CLK clock period | — | 20 | — | ns |
| $T_{dutycycle}$ | Clock duty cycle, internal clock source | 35 | 50 | 65 | % |
| $T_{dutycycle}$ | Clock duty cycle, external clock source | 35 | 50 | 65 | % |

### Table 70. RMII TX Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_d$ | TX_CLK to TXD/TX_CTL output data delay | 7 | — | 10 | ns |

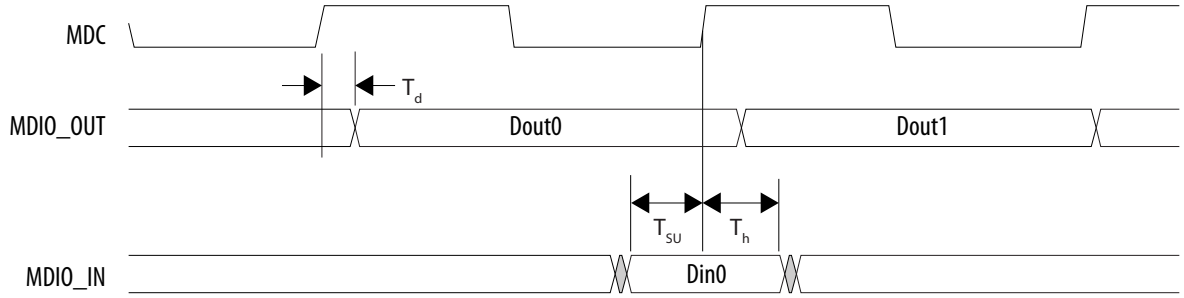
### Table 71. RMII RX Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{su}$ | RX_D/RX_CTL setup time | 1 | — | — | ns |
| $T_h$ | RX_D/RX_CTL hold time | 0.4 | — | — | ns |

### Table 72. Management Data Input/Output (MDIO) Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | MDC clock period | — | 400 | — | ns |
| $T_d$ | MDC to MDIO output data delay | 10.2 | — | 20 | ns |
| $T_{su}$ | Setup time for MDIO data | 10 | — | — | ns |
| $T_h$ | Hold time for MDIO data | 0 | — | — | ns |

**Figure 15. MDIO Timing Diagram**




**Related Information**

I/O Pin Timing, Intel Arria 10 SoC Device Design Guidelines

## I²C Timing Characteristics

**Table 73. I²C Timing Requirements for Intel Arria 10 Devices**

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{clk}$ | Serial clock (SCL) clock period | 10 | — | 2.5 | — | µs |
| $t_{HIGH}$ (102) | SCL high period | 4 (103) | — | 0.6 (104) | — | µs |
| $t_{LOW}$ (105) | SCL low period | 4.7 (106) | — | 1.3 (107) | — | µs |

*continued...*

(102) You can adjust $T_{clkhigh}$ using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(103) The recommended minimum setting for `ic_ss_scl_hcnt` is 440.

(104) The recommended minimum setting for `ic_fs_scl_hcnt` is 71.

(105) You can adjust $T_{clklow}$ using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(106) The recommended minimum setting for `ic_ss_scl_lcnt` is 500.

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{SU;DAT}$ | Setup time for serial data line (SDA) data to SCL | 0.25 | — | 0.1 | — | µs |
| $t_{HD;DAT}$ (108) | Hold time for SCL to SDA data | 0 | 3.15 | 0 | 0.6 | µs |
| $t_{VD;DAT}$ and $t_{VD;ACK}$ (109) | SCL to SDA output data delay | — | 3.45 (110) | — | 0.9 (111) | µs |
| $t_{SU;STA}$ | Setup time for a repeated start condition | 4.7 | — | 0.6 | — | µs |
| $t_{HD;STA}$ | Hold time for a repeated start condition | 4 | — | 0.6 | — | µs |
| $t_{SU;STO}$ | Setup time for a stop condition | 4 | — | 0.6 | — | µs |
| $t_{BUF}$ | SDA high pulse duration between STOP and START | 4.7 | — | 1.3 | — | µs |
| $t_r$ (112) | SCL rise time | — | 1000 | 20 | 300 | ns |
| $t_f$ (112) | SCL fall time | — | 300 | 20 × ($V_{dd}$ / 5.5) (113) | 300 | ns |
| $t_r$ (112) | SDA rise time | — | 1000 | 20 | 300 | ns |
| $t_f$ (112) | SDA fall time | — | 300 | 20 × ($V_{dd}$ / 5.5) (113) | 300 | ns |

(107) The recommended minimum setting for `ic_fs_scl_lcnt` is 141.

(108) $T_{HD;DAT}$ is affected by the rise and fall time.

(109) $t_{VD;DAT}$ and $t_{VD;ACK}$ is affected by the rise and fall time, in addition to the SDA hold time that is set by adjusting the `ic_sda_hold` register.

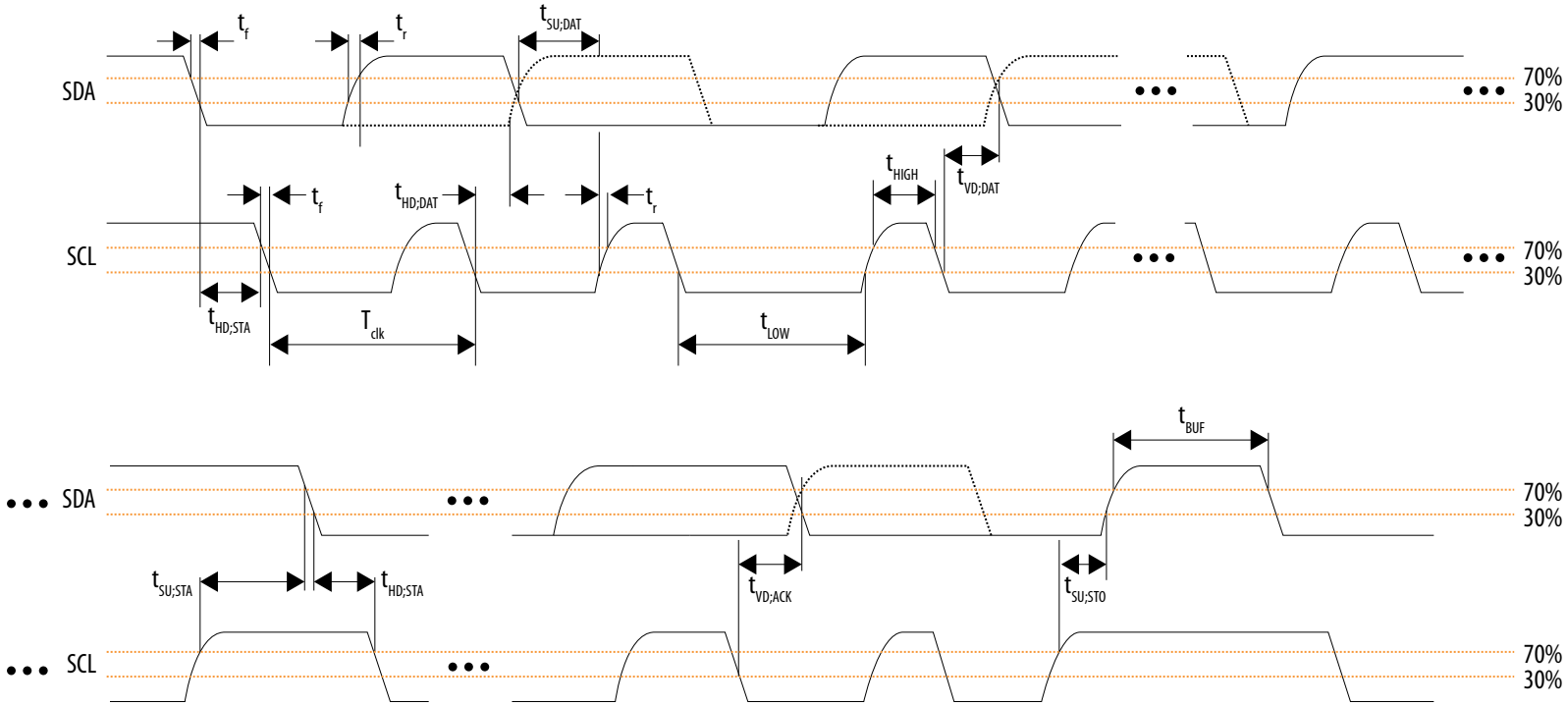
(110) Use maximum `SDA_HOLD` = 240 to be within the specification.

(111) Use maximum `SDA_HOLD` = 60 to be within the specification.

(112) Rise and fall time parameters vary depending on the external factors such as: characteristics of IO driver, pull-out resistor value, and total capacitance on the transmission line.

(113) $V_{dd}$ is the $I^2C$ bus voltage.

## Figure 16. I²C Timing Diagram



## NAND Timing Characteristics

### Table 74. NAND ONFI 1.0 Timing Requirements for Intel Arria 10 Devices

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{WP}$[114] | Write enable pulse width | 10 | — | ns |
| $t_{WH}$[114] | Write enable hold time | 7 | — | ns |
| $t_{RP}$[114] | Read enable pulse width | 10 | — | ns |
| $t_{REH}$[114] | Read enable hold time | 7 | — | ns |
| $t_{CLS}$[114] | Command latch enable to write enable setup time | 10 | — | ns |
| $t_{CLH}$[114] | Command latch enable to write enable hold time | 5 | — | ns |
| $t_{CS}$[114] | Chip enable to write enable setup time | 15 | — | ns |
| $t_{CH}$[114] | Chip enable to write enable hold time | 5 | — | ns |
| $t_{ALS}$[114] | Address latch enable to write enable setup time | 10 | — | ns |
| $t_{ALH}$[114] | Address latch enable to write enable hold time | 5 | — | ns |
| $t_{DS}$[114] | Data to write enable setup time | 7 | — | ns |
| $t_{DH}$[114] | Data to write enable hold time | 5 | — | ns |
| $t_{CEA}$ | Chip enable to data access time | — | 100 | ns |
| $t_{REA}$ | Read enable to data access time | — | 40 | ns |
| $t_{RHZ}$ | Read enable to data high impedance | — | 200 | ns |
| $t_{RR}$ | Ready to read enable low | 20 | — | ns |
| $t_{WB}$[114] | Write enable high to R/B low | — | 200 | ns |

(114) This timing is software programmable.

### Figure 17. NAND Command Latch Timing Diagram

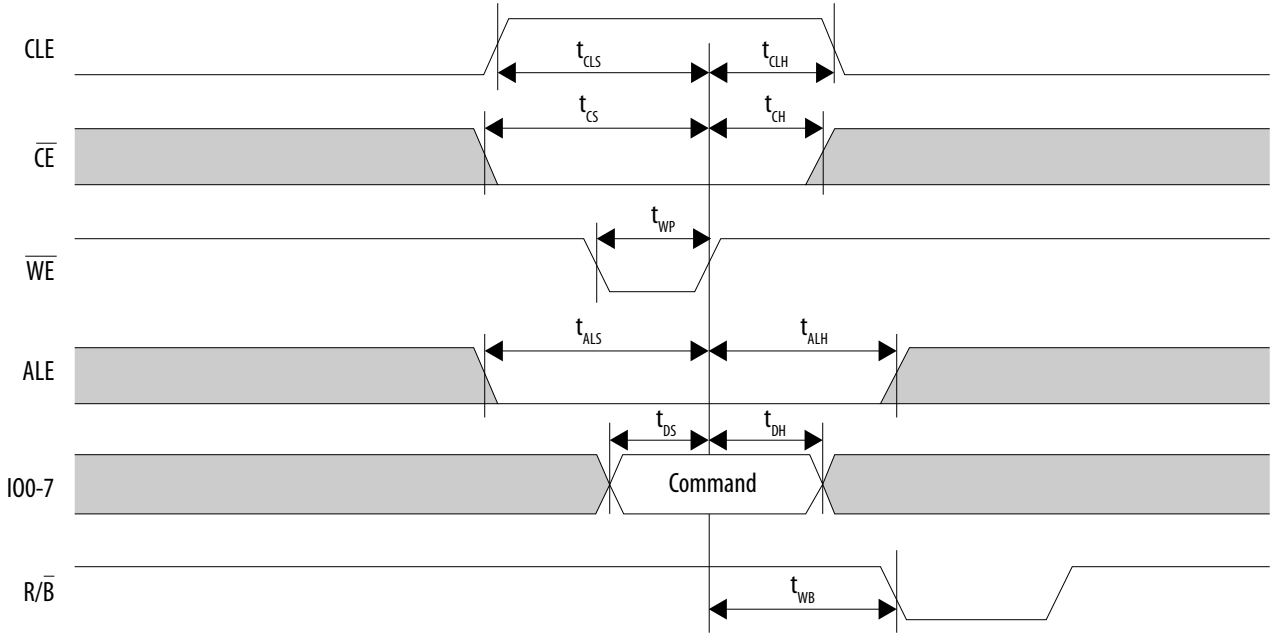


**Figure 18. NAND Address Latch Timing Diagram**

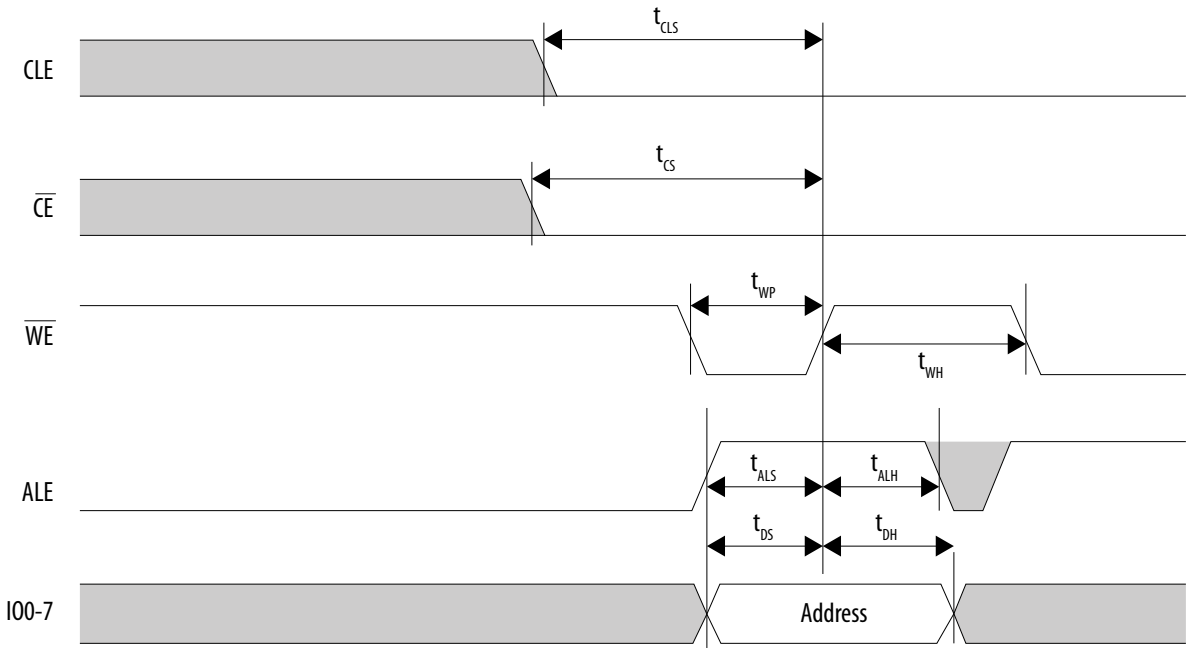


**Figure 19. NAND Data Output Cycle Timing Diagram**

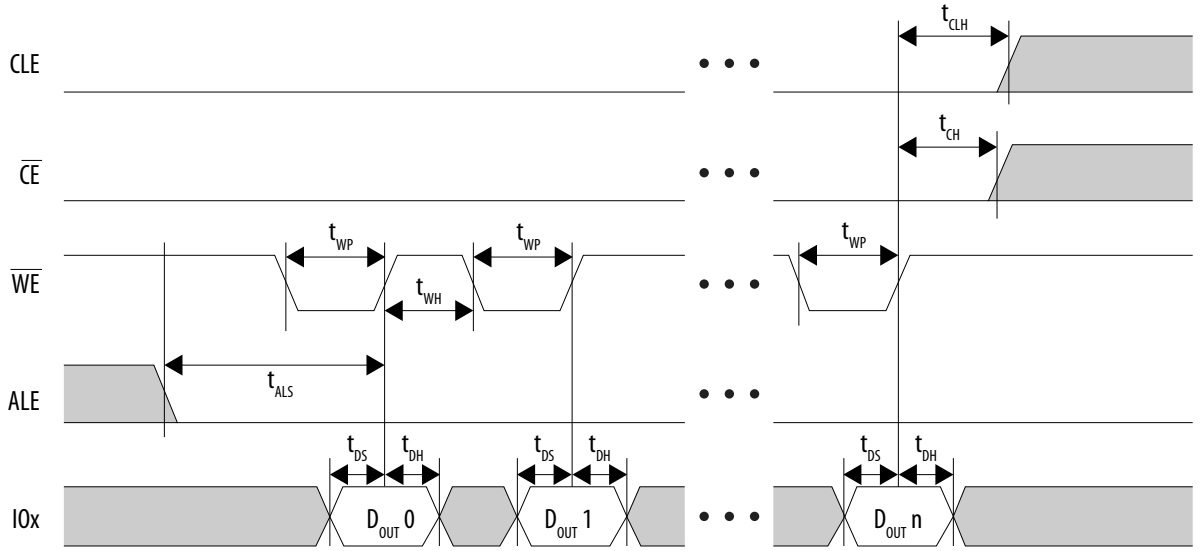



**Figure 20. NAND Data Input Cycle Timing Diagram**

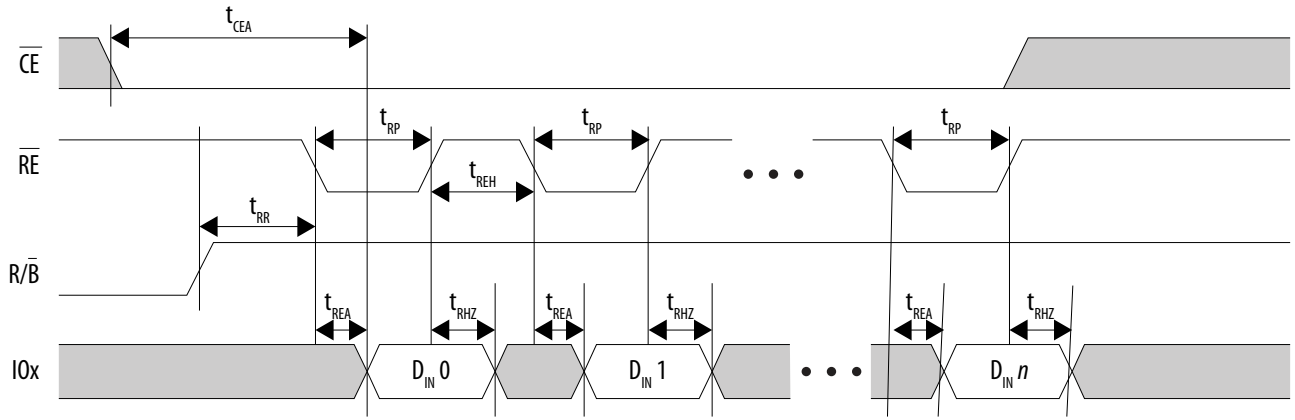
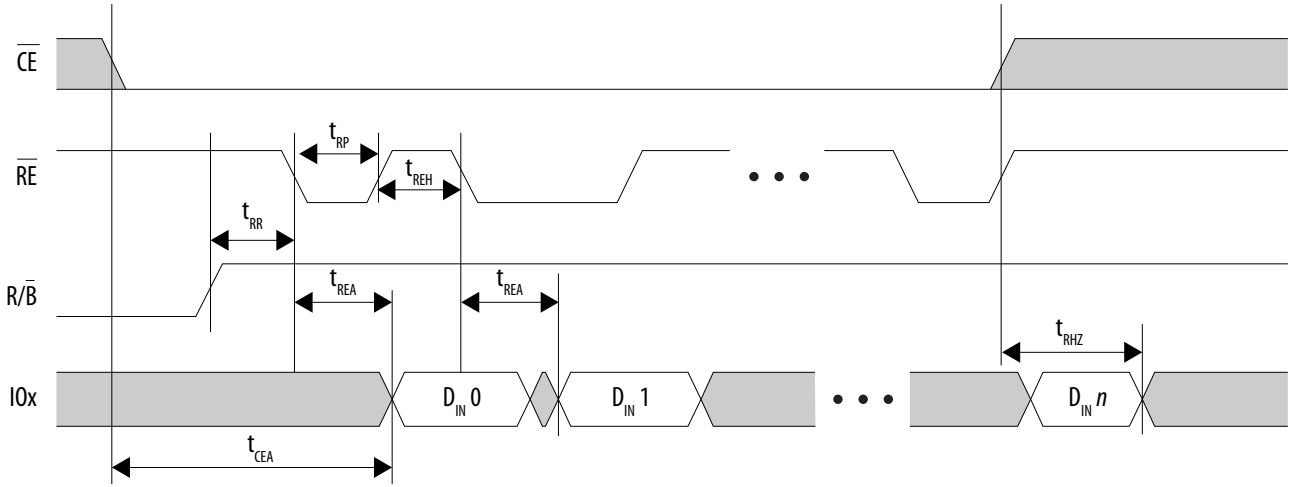


**Figure 21. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle**



## Figure 22. NAND Read Status Timing Diagram

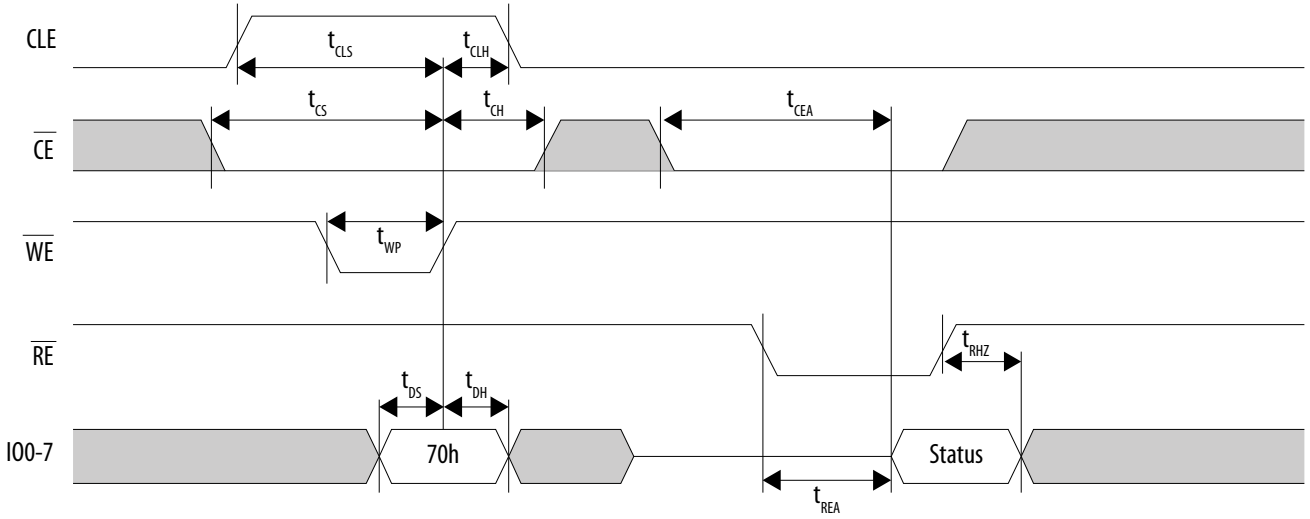
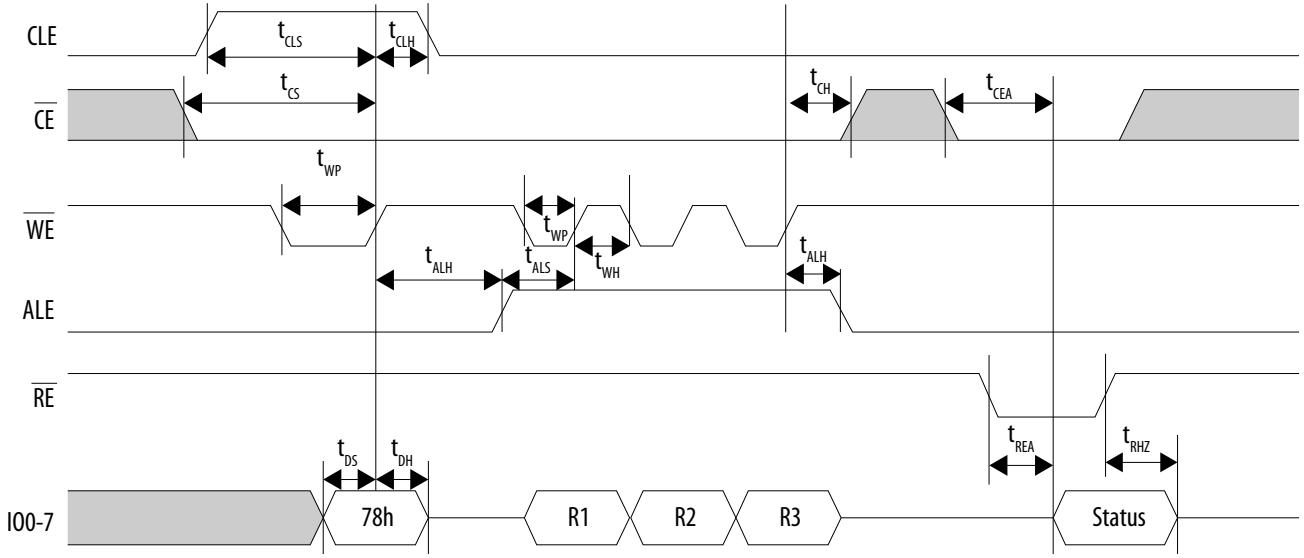


**Figure 23. NAND Read Status Enhanced Timing Diagram**




## Trace Timing Characteristics

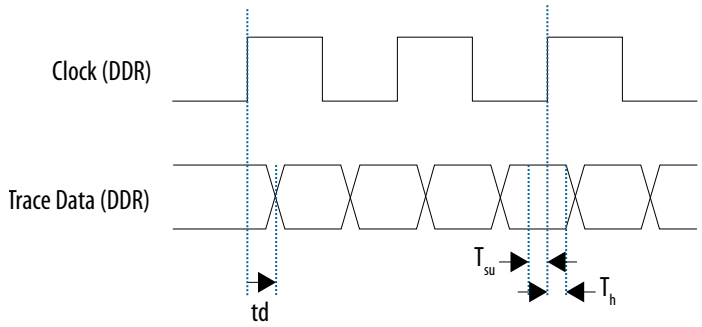
### Table 75. Trace Timing Requirements for Intel Arria 10 Devices

To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer (Standard) component. The FPGA trace interface offers a 32-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module datasheet for termination recommendations.

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | CLK clock period | 10 | — | — | ns |
| $T_{dutycycle}$ | CLK maximum duty cycle | 45 | 50 | 55 | % |
| $T_d$ | CLK to D0–D3 output data delay | –0.5 | — | 1 | ns |

**Figure 24. Trace Timing Diagram**




## GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is one debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz). Any pulses shorter than two debounce clock cycles are filtered by the GPIO peripheral.

If the external signal is less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal will not be filtered.

To ensure that the external signal is correctly debounced, set the debounce clock low enough so that by the time two debounce clock periods have passed, the signal has settled.

# Configuration Specifications

This section provides configuration specifications and timing for Intel Arria 10 devices.

## POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the `nSTATUS` is released high and your device is ready to begin configuration.

**Table 76. Fast and Standard POR Delay Specification for Intel Arria 10 Devices**

| POR Delay | Minimum | Maximum | Unit |
|---|---|---|---|
| Fast | 4 | 12 (115) | ms |
| Standard | 100 | 300 | ms |

### Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

## JTAG Configuration Timing

**Table 77. JTAG Timing Parameters and Values for Intel Arria 10 Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30, 167 (116) | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 | ns |

(115) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

(116) The minimum TCK clock period is 167 ns if $V_{CCBAT}$ is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

### Related Information

Glossary on page 96
Provides the JTAG configuration timing waveforms in the JTAG Timing Specifications term.

## FPP Configuration Timing

### DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

**Table 78. DCLK-to-DATA[] Ratio for Intel Arria 10 Devices**

You cannot turn on encryption and compression at the same time for Intel Arria 10 devices.

| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|---|---|---|---|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| FPP (32-bit wide) | Off | Off | 1 |
| | On | Off | 4 |
| | Off | On | 8 |

## FPP Configuration Timing when DCLK-to-DATA[] = 1

*Note:* When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Arria 10 Devices table.

### Table 79. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Arria 10 Devices

Use these timing parameters when the decompression and design security features are disabled.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 1,440 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 960 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 3,000 (117) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 3,000 (118) | µs |
| $t_{CF2CK}$ (119) | nCONFIG high to first rising edge on DCLK | 3,010 | — | µs |
| $t_{ST2CK}$ (119) | nSTATUS high to first rising edge of DCLK | 10 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × $1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × $1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16/×32) | — | 100 | MHz |

*continued...*

(117) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(118) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(119) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode (120) | 175 | 830 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (600 × CLKUSR period) | — | — |

### Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

## FPP Configuration Timing when DCLK-to-DATA[] >1

### Table 80. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Arria 10 Devices

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 1,440 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 960 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 3,000 (121) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 3,000 (121) | µs |
| $t_{CF2CK}$ (122) | nCONFIG high to first rising edge on DCLK | 3,010 | — | µs |
| $t_{ST2CK}$ (122) | nSTATUS high to first rising edge of DCLK | 10 | — | µs |

*continued...*

(120) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(121) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(122) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | $N$–1/$f_{DCLK}$ (123) | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16/×32) | — | 100 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (124) | 175 | 830 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (600 × CLKUSR period) | — | — |

## Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(123) $N$ is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(124) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

# AS Configuration Timing

## Table 81. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Arria 10 Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

The $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Intel Arria 10 Devices table.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CO}$ | DCLK falling edge to AS_DATA0/ASDO output | — | 2 | ns |
| $t_{SU}$ | Data setup time before falling edge on DCLK | 1 | — | ns |
| $t_{DH}$ | Data hold time after falling edge on DCLK | 1.5 | — | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode | 175 | 830 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (600 × CLKUSR period) | — | — |

### Related Information

- PS Configuration Timing on page 88
- AS Configuration Timing
  Provides the AS configuration timing waveform.

## DCLK Frequency Specification in the AS Configuration Scheme

### Table 82. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

You can only set 12.5, 25, 50, and 100 MHz in the Intel Quartus Prime software.

| Parameter | Minimum | Typical | Maximum | Intel Quartus Prime Software Settings | Unit |
|---|---|---|---|---|---|
| DCLK frequency in AS configuration scheme | 5.3 | 7.5 | 9.7 | 12.5 | MHz |
| | 10.5 | 15.0 | 19.3 | 25.0 | MHz |
| | 21.0 | 30.0 | 38.5 | 50.0 | MHz |
| | 42.0 | 60.0 | 77.0 | 100.0 | MHz |

## PS Configuration Timing

### Table 83. PS Timing Parameters for Intel Arria 10 Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 1,440 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 960 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 3,000 (125) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 3,000 (126) | µs |

*continued...*

(125) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(126) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CK}$ (127) | nCONFIG high to first rising edge on DCLK | 3,010 | — | µs |
| $t_{ST2CK}$ (127) | nSTATUS high to first rising edge of DCLK | 10 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (128) | 175 | 830 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (600 × CLKUSR period) | — | — |

## Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

(127) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(128) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

## Initialization

### Table 84. Initialization Clock Source Option and the Maximum Frequency for Intel Arria 10 Devices

| Initialization Clock Source | Configuration Scheme | Maximum Frequency (MHz) | Number of Clock Cycles for Initialization |
|---|---|---|---|
| Internal Oscillator | AS, PS, and FPP | 12.5 | 600 |
| CLKUSR (129)(130) | AS, PS, and FPP | 100 | |

## Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (`.rbf`)
- AS—Raw Programming Data File (`.rpd`)

The `.rpd` file size follows the Intel configuration devices capacity. However, the actual configuration bit stream size for `.rpd` file is the same as `.rbf` file.

(129) To enable CLKUSR as the initialization clock source, in the Intel Quartus Prime software, select **Device and Pin Options ➤ General ➤ Device initialization clock source ➤ CLKUSR pin**.

(130) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

## Table 85. Configuration Bit Stream Sizes for Intel Arria 10 Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

I/O configuration shift register (IOCSR) is a long shift register that facilitates the device I/O peripheral settings. The IOCSR bit stream is part of the uncompressed configuration bit stream, and it is specifically for the Configuration via Protocol (CvP) feature.

Uncompressed configuration bit stream sizes are subject to change for improvements and optimizations in the configuration algorithm. This table shows the estimated configuration bit stream sizes. Refer to the `.rbf` file generated in the Intel Quartus Prime software for the actual bit stream size.

| Variant | Product Line | Uncompressed Configuration Bit Stream Size (bits) | IOCSR Bit Stream Size (bits) | Recommended EPCQ-L Serial Configuration Device |
|---|---|---|---|---|
| Intel Arria 10 GX | GX 160 | 91,729,632 | 2,523,136 | EPCQ-L256 or higher density |
| | GX 220 | 91,729,632 | 2,523,136 | EPCQ-L256 or higher density |
| | GX 270 | 130,638,432 | 2,523,136 | EPCQ-L256 or higher density |
| | GX 320 | 130,638,432 | 2,523,136 | EPCQ-L256 or higher density |
| | GX 480 | 189,710,176 | 2,719,744 | EPCQ-L256 or higher density |
| | GX 570 | 252,959,072 | 2,916,352 | EPCQ-L256 or higher density |
| | GX 660 | 252,959,072 | 2,916,352 | EPCQ-L256 or higher density |
| | GX 900 | 351,292,512 | 2,785,280 | EPCQ-L512 or higher density |
| | GX 1150 | 351,292,512 | 2,785,280 | EPCQ-L512 or higher density |
| Intel Arria 10 GT | GT 900 | 351,292,512 | 2,785,280 | EPCQ-L512 or higher density |
| | GT 1150 | 351,292,512 | 2,785,280 | EPCQ-L512 or higher density |
| Intel Arria 10 SX | SX 160 | 91,729,632 | 2,523,136 | EPCQ-L256 or higher density |
| | SX 220 | 91,729,632 | 2,523,136 | EPCQ-L256 or higher density |
| | SX 270 | 130,638,432 | 2,523,136 | EPCQ-L256 or higher density |
| | SX 320 | 130,638,432 | 2,523,136 | EPCQ-L256 or higher density |

***continued...***

| Variant | Product Line | Uncompressed Configuration Bit Stream Size (bits) | IOCSR Bit Stream Size (bits) | Recommended EPCQ-L Serial Configuration Device |
|---|---|---|---|---|
| | SX 480 | 189,710,176 | 2,719,744 | EPCQ-L256 or higher density |
| | SX 570 | 252,959,072 | 2,916,352 | EPCQ-L256 or higher density |
| | SX 660 | 252,959,072 | 2,916,352 | EPCQ-L256 or higher density |

## Minimum Configuration Time Estimation

### Table 86. Minimum Configuration Time Estimation for Intel Arria 10 Devices

The estimated values are based on the uncompressed configuration bit stream sizes in the Configuration Bit Stream Sizes for Intel Arria 10 Devices table

| Variant | Product Line | Active Serial (131) | | | Fast Passive Parallel (132) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Intel Arria 10 GX | GX 160 | 4 | 100 | 229.32 | 32 | 100 | 28.67 |
| | GX 220 | 4 | 100 | 229.32 | 32 | 100 | 28.67 |
| | GX 270 | 4 | 100 | 326.6 | 32 | 100 | 40.82 |
| | GX 320 | 4 | 100 | 326.6 | 32 | 100 | 40.82 |
| | GX 480 | 4 | 100 | 474.28 | 32 | 100 | 59.28 |
| | GX 570 | 4 | 100 | 632.4 | 32 | 100 | 79.05 |
| | GX 660 | 4 | 100 | 632.4 | 32 | 100 | 79.05 |
| | GX 900 | 4 | 100 | 878.23 | 32 | 100 | 109.78 |
| | GX 1150 | 4 | 100 | 878.23 | 32 | 100 | 109.78 |

*continued...*

(131) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external `CLKUSR` may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(132) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

| Variant | Product Line | Active Serial (131) | | | Fast Passive Parallel (132) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Intel Arria 10 GT | GT 900 | 4 | 100 | 878.23 | 32 | 100 | 109.78 |
| | GT 1150 | 4 | 100 | 878.23 | 32 | 100 | 109.78 |
| Intel Arria 10 SX | SX 160 | 4 | 100 | 229.32 | 32 | 100 | 28.67 |
| | SX 220 | 4 | 100 | 229.32 | 32 | 100 | 28.67 |
| | SX 270 | 4 | 100 | 326.6 | 32 | 100 | 40.82 |
| | SX 320 | 4 | 100 | 326.6 | 32 | 100 | 40.82 |
| | SX 480 | 4 | 100 | 474.28 | 32 | 100 | 59.28 |
| | SX 570 | 4 | 100 | 632.4 | 32 | 100 | 79.05 |
| | SX 660 | 4 | 100 | 632.4 | 32 | 100 | 79.05 |

### Related Information

- Configuration Files on page 90
- DCLK Frequency Specification in the AS Configuration Scheme on page 88
  Provides the DCLK frequency using internal oscillator.

(131) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external `CLKUSR` may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(132) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

## Remote System Upgrades

### Table 87. Remote System Upgrade Circuitry Timing Specifications for Intel Arria 10 Devices

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $f_{MAX_RU_CLK}$ (133) | — | 40 | MHz |
| $t_{RU_nCONFIG}$ (134) | 250 | — | ns |
| $t_{RU_nRSTIMER}$ (135) | 250 | — | ns |

#### Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (`RU_CONFIG`) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (`RU_nRSTIMER`) signal.

## User Watchdog Internal Circuitry Timing Specifications

### Table 88. User Watchdog Internal Oscillator Frequency Specifications for Intel Arria 10 Devices

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

(133) This clock is user-supplied to the remote system upgrade circuitry. If you are using the Remote Update Intel FPGA IP core, the clock user-supplied to the Remote Update Intel FPGA IP core must meet this specification.

(134) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(135) This is equivalent to strobing the reset_timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

# I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

### Related Information

AN 775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

# Programmable IOE Delay

### Table 89. IOE Programmable Delay for Intel Arria 10 Devices

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the PHYLite for Parallel Interfaces Intel Arria 10 FPGA IP core.

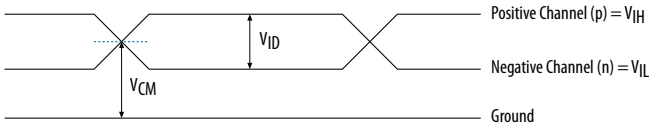
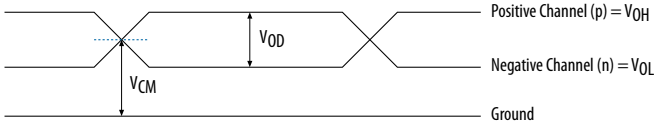
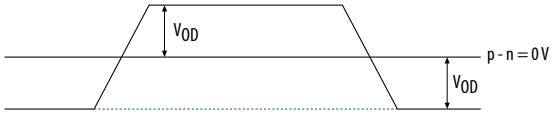
| Parameter (136) | Maximum Offset | Minimum Offset (137) | Fast Model | | Slow Model | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Extended | Industrial | –E1S, –E1H, –I1S, –I1H | –E2L, –E2S, –I2L, –I2S | –E3L, –E3S, –I3L, –I3S | |
| Input Delay Chain Setting (IO_IN_DLY_CHN) | 63 | 0 | 2.012 | 2.003 | 4.541 | 5.241 | 6.035 | ns |
| Output Delay Chain Setting (IO_OUT_DLY_CHN) | 15 | 0 | 0.478 | 0.475 | 1.088 | 1.263 | 1.462 | ns |

(136) You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

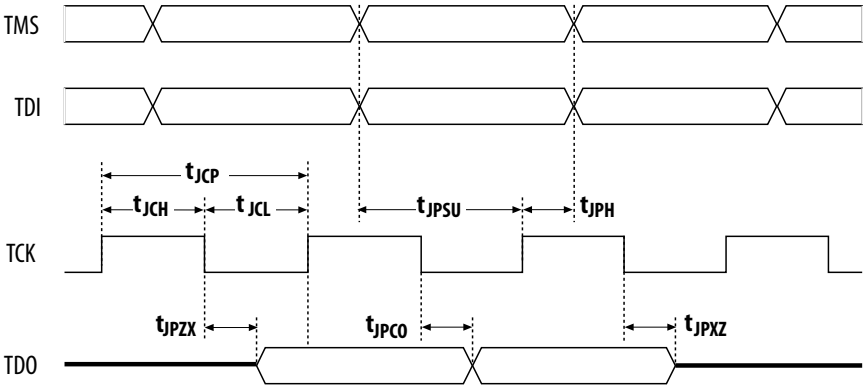
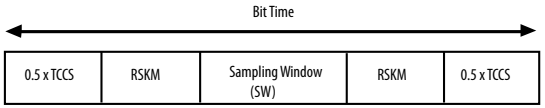
(137) Minimum offset does not include the intrinsic delay.

# Glossary

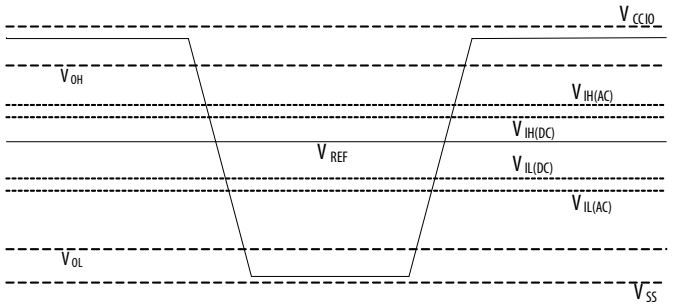
## Table 90. Glossary

| Term | Definition |
|---|---|
| Differential I/O Standards | Receiver Input Waveforms<br>**Single-Ended Waveform**<br><br><br>**Differential Waveform**<br><br><br>Transmitter Output Waveforms<br>**Single-Ended Waveform**<br><br><br>**Differential Waveform**<br><br> |
| $f_{HSCLK}$ | I/O PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |

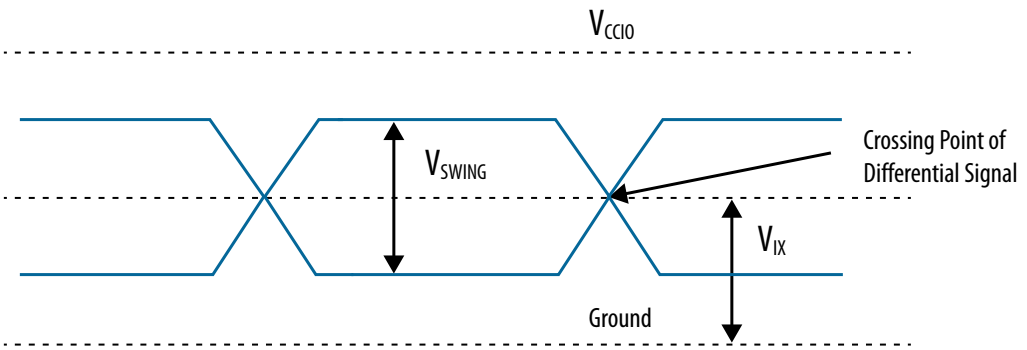
*continued...*

| Term | Definition |
|---|---|
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| JTAG Timing Specifications | JTAG Timing Specifications:<br> |
| $R_L$ | Receiver differential input discrete resistor (external to the Intel Arria 10 device). |
| Sampling window (SW) | Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:<br> |
| Single-ended voltage referenced I/O standard | The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.<br>Single-Ended Voltage Referenced I/O Standard |

***continued...***

| Term | Definition |
|---|---|
| |  |
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80–20%) |
| $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input |
| $t_{OUTPJ_IO}$ | Period jitter on the GPIO driven by a PLL |
| $t_{OUTPJ_DC}$ | Period jitter on the dedicated clock output driven by a PLL |
| $t_{RISE}$ | Signal low-to-high transition time (20–80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C$/w). |
| $V_{CM(DC)}$ | DC Common mode input voltage. |
| $V_{ICM}$ | Input Common mode voltage—The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |

*continued...*

| Term | Definition |
|---|---|
| $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |
| $V_{OCM}$ | Output Common mode voltage—The common mode of the differential signal at the transmitter. |
| $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. |
| $V_{SWING}$ | Differential input voltage |
| $V_{IX}$ | Crossing point of differential signal   |
| $V_{OX}$ | Output differential cross point voltage |
| W | High-speed I/O block—Clock Boost Factor |

# Document Revision History for the Intel Arria 10 Device Datasheet

| Document Version | Changes |
|---|---|
| 2022.02.14 | • Added $T_J$ specifications for Military devices in the *Recommended Operating Conditions for Intel Arria 10 Devices* table.<br>• Removed table description from the *I/O Pin Leakage Current for Intel Arria 10 Devices* table.<br>• Changed I/O standards from RSDS (HIO) to RSDS and Mini-LVDS (HIO) to Mini-LVDS in the *Differential I/O Standards Specifications for Intel Arria 10 Devices* table.<br>• Updated the conditions for $V_{ICM}$ (AC and DC coupled) in the *Transceiver Specifications for Intel Arria 10 GX, SX, and GT Devices — Receiver Specifications* table.<br>• Removed diagram: *DPA Lock Time Specifications with DPA PLL Calibration Enabled*.<br>• Added footnote to Maximum Data Transition in the *DPA Lock Time Specifications for Intel Arria 10 Devices* table.<br>• Updated the *Configuration Bit Stream Sizes for Intel Arria 10 Devices* table.<br>☐ Updated table description.<br>☐ Updated Uncompressed Configuration Bit Stream Size and IOCSR Bit Stream Size.<br>• Updated Minimum Configuration Time in the *Minimum Configuration Time Estimation for Intel Arria 10 Devices* table. |
| 2020.06.26 | Removed the note on HPS_PORSEL from $t_{RAMP}$ in the *Recommended Operating Conditions for Intel Arria 10 Devices* table. `HPS_PORSEL` pin is not available for Intel Arria 10 devices. |
| 2020.03.20 | Corrected $T_h$ from 10 ns to 0 ns in the *Management Data Input/Output (MDIO) Timing Requirements for Intel Arria 10 Devices* table. |
| 2019.06.24 | • Updated the definitions for the power options.<br>• Updated the note to the speed grades in the *High-Speed I/O Specifications for Intel Arria 10 Devices* table.<br>• Updated the definition and added a waveform for $V_{IX}$ in the *Glossary*. |
| 2018.11.29 | Removed $t_R$ and $t_F$ specifications in the *FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Arria 10 Devices* table. |
| 2018.09.24 | Removed specifications for automotive-grade devices (–A3 speed grade). |
| 2018.06.15 | • Added *Intel Arria 10 Devices Overshoot Duration* figure and description.<br>• Removed *Equation for OCT Variation Without Recalibration*.<br>• Updated the descriptions for $T_{dssfrst}$, $T_{dsslst}$, $T_{su}$, and $T_h$ in the *Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Intel Arria 10 Devices* table.<br>• Updated the column header from "Minimum Number of Clock Cycles" to "Number of Clock Cycles for Initialization" in the *Initialization Clock Source Option and the Maximum Frequency for Intel Arria 10 Devices* table. |
| 2018.04.06 | • Added notes to $I_{OUT}$ specification in the *Absolute Maximum Ratings for Intel Arria 10 Devices* table.<br>• Updated the maximum frequency for DDR3L SDRAM in the *Memory Standards Supported by the HPS Hard Memory Controller for Intel Arria 10 Devices* table. |

| Date | Version | Changes |
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| January 2018 | 2018.01.09 | • Added –E1H and –I1H speed grades.<br>• Removed –E2V and –I2V speed grades.<br>• Added a note to the –A3 speed grade to state that the specifications for automotive-grade devices are preliminary, pending characterization.<br>• Updated the *Recommended Operating Conditions for Intel Arria 10 Devices* table.<br>☐ Added a note to $V_I$<br>☐ Removed the note to $T_J$ for Industrial and Automotive devices. Note removed: –40°C is only applicable to Start of Test, when the device is powered-on. The device does not stay at the minimum junction temperature for a long time.<br>• Updated the note to RSDS (HIO) and Mini-LVDS (HIO) in the *Differential I/O Standards Specifications for Intel Arria 10 Devices* table.<br>• Added KDB link on PLL jitter compensation in the following tables:<br>☐ *Fractional PLL Specifications for Intel Arria 10 Devices*<br>☐ *I/O PLL Specifications for Intel Arria 10 Devices*<br>• Corrected the clock name from "osc1 clock" to `osc1_clk` and added a note in the *HPS Reset Input Requirements for Intel Arria 10 Devices* table.<br>• Added description about the `HPS_CLK1` pin in the *HPS PLL Input Requirements* section.<br>• Updated the note for $T_{su}$ and $T_h$ in the *Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Arria 10 Devices* table.<br>• Updated the note to `CLKUSR` in the *Initialization Clock Source Option and the Maximum Frequency for Intel Arria 10 Devices* table.<br>• Updated the *I/O Timing* section on the I/O timing information generation guidelines.<br>• Updated the description and maximum offset values in the *IOE Programmable Delay for Intel Arria 10 Devices* table. |
| June 2017 | 2017.06.16 | • Added specifications for automotive-grade devices.<br>• Removed –E1L and –I1L speed grades.<br>• Clarified the voltage requirement footnote for PCIe Gen3 support in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GX/SX Devices" table.<br>• Added notes for $T_J$ for Industrial and Automotive devices in Recommended Operating Conditions for Intel Arria 10 Devices table.<br>• Updated the description for $V_{CCH_GXB}$ in the following tables:<br>☐ Absolute Maximum Ratings for Intel Arria 10 Devices<br>☐ Transceiver Power Supply Operating Conditions for Intel Arria 10 GX/SX Devices<br>☐ Transceiver Power Supply Operating Conditions for Intel Arria 10 GT Devices<br>• Added full pin names in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GX/SX Devices" table.<br>• Clarified that the channel span for the x1 and x6 clock networks is six channels in a single bank in the "Transceiver Clock Network Maximum Data Rate Specifications" table.<br>• Updated $f_{VCO}$ specifications in Fractional PLL Specifications for Intel Arria 10 Devices table. |

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| Date | Version | Changes |
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| | | • Updated the following tables to keep only the maximum frequencies:<br>☐ Memory Standards Supported by the Hard Memory Controller for Intel Arria 10 Devices<br>☐ Memory Standards Supported by the Soft Memory Controller for Intel Arria 10 Devices<br>☐ Memory Standards Supported by the HPS Hard Memory Controller for Intel Arria 10 Devices<br>• Updated the description for Memory Output Clock Jitter Specifications for Intel Arria 10 Devices table.<br>• Updated the unit for "Cold reset deassertion to BSEL sampling, using osc1 clock" in HPS Reset Input Requirements for Intel Arria 10 Devices table.<br>• Updated the name of the internal reference clock to `SPI_REF_CLK` in the footnote in the following tables:<br>☐ SPI Master Timing Requirements for Intel Arria 10 Devices<br>☐ SPI Slave Timing Requirements for Intel Arria 10 Devices<br>• Updated maximum values for $t_{CF2CD}$ from 600 ns to 1,440 ns and $t_{CF2ST0}$ from 600 ns to 960 ns in the following tables:<br>☐ FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Arria 10 Devices<br>☐ FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Arria 10 Devices<br>☐ PS Timing Parameters for Intel Arria 10 Devices |
| May 2017 | 2017.05.08 | • Updated $V_{CCBAT}$ specifications in Recommended Operating Conditions for Intel Arria 10 Devices table.<br>• Changed the maximum skew specification for the xN clock line in the "Transmitter Channel-to-channel Skew Specifications" table.<br>• Changed the PCIe Gen3 HIP-Fabric interface spec for E3S and I3S devices in the "High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GX/SX Devices" table.<br>• Changed the conditions for $V_{ICM}$ in the "Receiver Specifications" table.<br>• Removed the DC Coupling specifications footnote from the "Receiver Specifications" table.<br>• Changed the conditions for the differential on-chip termination resistors parameter in the "Transmitter Specifications" table.<br>• Updated the footnote for $V_{ICM}$ (AC and DC coupled) parameter in the "Receiver Specifications" table.<br>• Added footnotes to the minimum specifications for the fPLL input reference clock frequency in the "Reference Clock Specifications" table depending on the selected mode.<br>• Changed the Core Speed Grade options in the "High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GX/SX Devices" table.<br>• Added information on power supply using early I/O release configuration flow in HPS Specifications section.<br>• Added description in the Configuration Bit Stream Sizes for Intel Arria 10 Devices table. |
| March 2017 | 2017.03.15 | • Changed the minimum value for the fPLL input reference clock frequency in the "Reference Clock Specifications" table.<br>• Added a footnote to the Supported I/O Standards parameter in the "Receiver Specifications" table.<br>• Added a footnote to $V_{CCR_GXB[L,\ R]}$ and $V_{CCT_GXB[L,\ R]}$ in the "Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices" table. |

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| Date | Version | Changes |
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| | | • Added $f_{CASC_INPFD}$ specification in the following tables:<br>☐ Fractional PLL Specifications for Intel Arria 10 Devices<br>☐ I/O PLL Specifications for Intel Arria 10 Devices<br>• Updated links to the External Memory Interface Spec Estimator in the following sections:<br>☐ Memory Standards Supported by the Hard Memory Controller<br>☐ Memory Standards Supported by the Soft Memory Controller<br>☐ Memory Standards Supported by the HPS Hard Memory Controller<br>• Updated Maximum HPS Clock Frequencies Across Device Speed Grades for Intel Arria 10 Devices table.<br>☐ Removed temperature ranges.<br>☐ Updated mpu_base_clk specification from 1,000 MHz to 1,200 MHz in –1 speed grade for $V_{CCL_HPS}$ = 0.9 V (typical).<br>• Updated HPS PLL VCO output maximum specification from 2,000 MHz to 2,400 MHz in -1 speed grade for $V_{CCL_HPS}$ = 0.9 V in HPS PLL Performance for Intel Arria 10 Devices table.<br>• Updated links to the Intel Arria 10 SoC Device Design Guidelines in the following sections:<br>☐ USB ULPI Timing Characteristics<br>☐ Ethernet Media Access Controller (EMAC) Timing Characteristics<br>• Updated uncompressed configuration bit stream size (bits) in Configuration Bit Stream Sizes for Intel Arria 10 Devices table.<br>• Added descriptions for Programmable IOE Delay.<br>• Removed PowerPlay text from tool name.<br>• Rebranded as Intel. |
| October 2016 | 2016.10.31 | • Added reference to the Intel Arria 10 SoC Device Design Guidelines for the USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Arria 10 Devices table.<br>• Added reference to the Intel Arria 10 SoC Device Design Guidelines for the RGMII RX Timing Requirements for Intel Arria 10 Devices table.<br>• Updated the $f_{VCO}$ values in the Fractional PLL Specifications for Intel Arria 10 Devices table.<br>• Updated the $t_{OUTPJ_DC}$ and $t_{OUTCCJ_DC}$ values in the I/O PLL Specifications for Intel Arria 10 Devices table.<br>• Updated the description to the DPA Lock Time Specifications for Intel Arria 10 Devices table as the specifications are applicable to both extended and industrial grades.<br>• Updated the description to the Maximum HPS Clock Frequencies Across Device Speed Grades for Intel Arria 10 Devices table as the specifications are applicable to both extended and industrial temperatures.<br>• Removed Preliminary tag for the Trace Timing Requirements for Intel Arria 10 Devices table.<br>• Changed the condition for the slew rate setting in the "Transmitter Specifications" table. |
| June 2016 | 2016.06.24 | • Updated $V_{CCL_HPS}$ specifications in HPS Power Supply Operating Conditions for Intel Arria 10 SX Devices table.<br>• Restructured the following tables:<br>☐ OCT Calibration Accuracy Specifications for Intel Arria 10 Devices<br>☐ OCT Without Calibration Resistance Tolerance Specifications for Intel Arria 10 Devices<br>• Removed PCML information in Differential I/O Standards Specifications for Intel Arria 10 Devices table. |

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| Date | Version | Changes |
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| | | • Changed values in the "Transmitter and Receiver Data Rate Performance" table.<br>• Updated specifications for memory standards supported by the hard memory controller, soft memory controller, and HPS hard memory controller.<br>• Updated DLL operating frequency range in DLL Frequency Range Specifications for Intel Arria 10 Devices table.<br>• Updated Memory Output Clock Jitter Specifications for Intel Arria 10 Devices table.<br>• Updated HPS Clock Performance specifications.<br>• Updated HPS PLL Performance for Intel Arria 10 Devices table.<br>☐ Updated HPS PLL VCO output –3 speed grade maximum specification for 0.95 V $V_{CCL_HPS}$.<br>☐ Added HPS PLL VCO output specifications for 0.90 V $V_{CCL_HPS}$.<br>☐ Added h2f_user0_clk and h2f_user1_clk specifications.<br>• Added a new table for HPS PLL Output Specifications.<br>• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Intel Arria 10 Devices table.<br>☐ Updated QSPI_CLK clock name.<br>☐ Updated $T_{clk}$, $T_{dssfrst}$, $T_{dsslst}$, and $T_{do}$ specifications.<br>☐ Added $T_{su}$ and $T_h$ specifications.<br>☐ Removed $T_{din_start}$ and $T_{din_end}$ specifications.<br>• Updated $T_{dssfrst}$, $T_{dsslst}$, $T_{dio}$, and $T_{su}$ specifications in SPI Master Timing Requirements for Intel Arria 10 Devices table.<br>• Updated $T_h$ and $T_d$ specifications in SPI Slave Timing Requirements for Intel Arria 10 Devices table.<br>• Updated $T_{su}$, $T_h$, and $T_d$ specifications in Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Arria 10 Devices table.<br>• Added a note to $T_d$ in Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Arria 10 Devices table.<br>• Updated $T_h$ specifications in RGMII RX Timing Requirements for Intel Arria 10 Devices table.<br>• Updated $T_d$ specifications in RMII TX Timing Requirements for Intel Arria 10 Devices table.<br>• Added notes in $I^2C$ Timing Requirements for Intel Arria 10 Devices table.<br>• Updated Trace Timing Requirements for Intel Arria 10 Devices table.<br>☐ Added description about increasing trace bandwidth.<br>☐ Updated $T_{clk}$ minimum specification from 5 ns to 10 ns.<br>• Updated the information on GPIO interface. |

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| Date | Version | Changes |
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| | | • Updated the following timing diagrams:<br>☐ Quad SPI Flash Serial Output Timing Diagram<br>☐ Quad SPI Flash Serial Input Timing Diagram<br>☐ SPI Master Output Timing Diagram<br>☐ SPI Master Input Timing Diagram<br>☐ SPI Slave Output Timing Diagram<br>☐ SPI Slave Input Timing Diagram<br>☐ $I^2C$ Timing Diagram<br>☐ NAND Address Latch Timing Diagram<br>☐ NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle<br>☐ NAND Read Status Timing Diagram<br>☐ Trace Timing Diagram<br>• Updated DCLK Frequency Specification in the AS Configuration Scheme table.<br>• Updated IOCSR bit stream sizes in Configuration Bit Stream Sizes for Intel Arria 10 Devices table.<br>• Corrected product line naming in the following tables:<br>☐ Configuration Bit Stream Sizes for Intel Arria 10 Devices<br>☐ Minimum Configuration Time Estimation for Intel Arria 10 Devices<br>• Updated IOE Programmable Delay for Intel Arria 10 Devices table.<br>• Removed Preliminary tags for all tables, except Trace Timing Requirements for Intel Arria 10 Devices table. |
| May 2016 | 2016.05.02 | • Updated Recommended Operating Conditions for Intel Arria 10 Devices table.<br>☐ Added specifications for 0.95 V typical value for $V_{CC}$, $V_{CCP}$, and $V_{CCERAM}$.<br>☐ Updated SmartVID specifications for $V_{CC}$ and $V_{CCP}$.<br>☐ Updated notes to $V_{CC}$, $V_{CCP}$, $V_{CCERAM}$, and $V_{CCBAT}$.<br>• Updated specifications for SSTL-12 240-Ω $R_S$, SSTL-135 34-Ω $R_S$, and SSTL-135 40-Ω $R_S$ in OCT Calibration Accuracy Specifications for Intel Arria 10 Devices table.<br>• Removed the condition $V_{CCIO}$ = 1.5 for 100-Ω $R_D$ in OCT Without Calibration Resistance Tolerance Specifications for Intel Arria 10 Devices table.<br>• Changed pin capacitance to maximum values.<br>• Added SSTL-135 Class I, II, SSTL-125 Class I, II, and SSTL-12 Class I, II I/O standards in the following tables:<br>☐ Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Arria 10 Devices<br>☐ Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Arria 10 Devices<br>☐ Differential SSTL I/O Standards Specifications for Intel Arria 10 Devices<br>• Corrected $V_{OD}$ specifications for Mini-LVDS (HIO) to 0.6 V in Differential I/O Standards Specifications for Intel Arria 10 Devices table.<br>• Changed the backplane data rates in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GX/SX Devices" table. |

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| | | • Changed the conditions and backplane data rates in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GT Devices" table.<br>• Changed the backplane data rates in the "Transceiver Performance for Intel Arria 10 GX/SX Devices" section.<br>• Changed the backplane data rates in the "Transceiver Performance for Intel Arria 10 GT Devices" section.<br>• Changed the minimum frequency in the "CMU PLL Performance" table.<br>• Changed the conditions and added a description to the "High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GX/SX Devices" table.<br>• Removed transceiver speed grade 5 from all tables in the "Transceiver Performance for Intel Arria 10 GX/SX Devices" section.<br>• Changed the notes in the "Transmitter and Receiver Data Rate Performance" table.<br>• Added a description to the "High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GT Devices" table.<br>• Changed the clock network names in the "Transceiver Clock Network Maximum Data Rate Specifications" table.<br>• Changed the conditions in the "High-Speed Serial Transceiver-Fabric Interface Performance for Intel Arria 10 GT Devices" table.<br>• Changed the channel span specifications in the "Transmitter Channel-to-channel Skew Specifications" table.<br>• Updated $f_{VCO}$, $f_{CLBW}$, $t_{PLL_PSERR}$, and jitter specifications in Fractional PLL Specifications for Intel Arria 10 Devices table.<br>• Updated $t_{OUTDUTY}$ and jitter specifications in I/O PLL Specifications for Intel Arria 10 Devices table.<br>• Updated the note to $f_{IN}$ specifications for fPLL and IOPLL.<br>• Updated High-Speed I/O Specifications for Intel Arria 10 Devices table.<br>☐ Added true RSDS and true mini-LVDS output standards data rates.<br>☐ Updated speed grades to reflect SmartVID specifications.<br>☐ Updated Transmitter $f_{HSDR}$ and Receiver $f_{HSDRDPA}$ specifications.<br>☐ Added minimum data rate for Receiver $f_{HSDRDPA}$ specifications.<br>• Updated LVDS I/O bank and 3 V I/O bank specifications, and added SmartVID specifications in Memory Standards Supported by the Hard Memory Controller for Intel Arria 10 Devices and Memory Standards Supported by the Soft Memory Controller for Intel Arria 10 Devices tables.<br>• Added new table: Memory Standards Supported by the HPS Hard Memory Controller for Intel Arria 10 Devices.<br>• Updated $t_{CO}$ from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Arria 10 Devices table.<br>• Added IOCSR definition and updated column heading from "IOCSR .rbf Size (bits)" to "IOCSR Bit Stream Size (bits)" in Configuration Bit Stream Sizes for Intel Arria 10 Devices table.<br>• Removed M suffix and $V_{CC}$ PowerManager feature. |
| February 2016 | 2016.02.11 | • Changed the datarates in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GT Devices" table.<br>• Changed the available speed grades and datarates in the "Transceiver Performance for Intel Arria 10 GT Devices" table.<br>• Changed the available speed grades and datarates in the "ATX PLL Performance" table. |

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| | | • Changed the available speed grades and datarates in the "Fractional PLL Performance" table.<br>• Changed the available speed grades in the "CMU PLL Performance" table.<br>• Changed the available speed grades and frequencies in the "High-Speed Serial Transceiver-Fabric Interface Performance for Arria 10 GT Devices" table. |
| December 2015 | 2015.12.31 | • Updated M20K block specifications for "True dual port, all supported widths" and "ROM, all supported widths" in the Memory Clock Performance Specifications ($V_{CC}$ and $V_{CCP}$ at 0.9 V Typical Value) table.<br>• Updated maximum resolution from 8 bit 6 bit and added minimum clock frequency of 0.1 MHz in Internal Voltage Sensor Specifications for Intel Arria 10 Devices table.<br>• Updated the sinusoidal jitter from 0.35 UI to 0.28 UI in LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications. |
| December 2015 | 2015.12.18 | • Changed the minimum specifications in the "Transceiver Power Supply Operating Conditions for Arria 10 GT Devices" table.<br>• Changed conditions in the "Transmitter and Receiver Data Rate Performance" table. |
| November 2015 | 2015.11.02 | • Added power option V which is supported with the SmartVID feature (lowest static power).<br>• Added note for SmartVID in Recommended Operating Conditions for Intel Arria 10 Devices table. Note: SmartVID is supported in devices with –2V and –3V speed grades only.<br>• Removed 20-Ω $R_T$ in OCT Calibration Accuracy Specifications for Intel Arria 10 Devices table.<br>• Updated specifications in OCT Without Calibration Resistance Tolerance Specifications for Intel Arria 10 Devices table.<br>• Updated the note for Value column in the Internal Weak Pull-Up Resistor Values for Intel Arria 10 Devices table. Added Internal Weak Pull-Down Resistor Values for Intel Arria 10 Devices table.<br>• Updated fractional PLL specifications:<br>☐ Updated $f_{IN}$ minimum from 50 MHz to 30 MHz and maximum from 1000 MHz to 800 MHz for all speed grades.<br>☐ Updated $f_{INPFD}$ minimum from 50 MHz to 30 MHz and maximum from 325 MHz to 700 MHz.<br>☐ Updated $f_{VCO}$ minimum from 3.125 GHz to 3.5 GHz and maximum from 6.25 GHz to 7.05 GHz.<br>☐ Updated $t_{EINDUTY}$ minimum from 40% to 45% and maximum from 60% to 55%.<br>☐ Removed the conditions for $f_{OUT}$ and $f_{CLBW}$.<br>☐ Updated the descriptions for $f_{DYCONFIGCLK}$, $t_{LOCK}$, and $t_{ARESET}$.<br>• Added –E2V, –I2V, –E3V, and –I3V speed grades in DSP Block Performance Specifications for Intel Arria 10 Devices ($V_{CC}$ and $V_{CCP}$ at 0.9 V Typical Value) table.<br>• Updated Memory Block Performance Specifications for Intel Arria 10 Devices table for $V_{CC}$ and $V_{CCP}$ at 0.9 V typical value. Added memory block performance specifications for $V_{CC}$ and $V_{CCP}$ at 0.95 V typical value.<br>• Removed the "Minimum Resolution with no Missing Codes" column in Internal Temperature Sensing Diode Specifications for Intel Arria 10 Devices table.<br>• Added a link in the Internal Temperature Sensing Diode Specifications section: *Transfer Function for Internal TSD* topic in the *Power Management in Intel Arria 10 Devices* chapter, *Intel Arria 10 Core Fabric and General Purpose I/Os Handbook*.<br>• Added descriptions to External Temperature Sensing Diode Specifications for Intel Arria 10 Devices table. |

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| | | • Updated Internal Voltage Sensor Specifications for Intel Arria 10 Devices table.<br>☐ Updated maximum resolution from 12 bits to 8 bits. Removed minimum resolution value.<br>☐ Updated maximum integral non-linearity (INL) from ±3 LSB to ±1 LSB.<br>☐ Updated maximum clock frequency from 20 MHz to 11 MHz.<br>☐ Added gain error and offset error specifications.<br>☐ Removed signal to noise and distortion ratio (SNR) specifications.<br>☐ Removed Bipolar input mode specifications.<br>• Updated "slow clock" to "core clock" in DPA Lock Time Specifications with DPA PLL Calibration Enabled diagram.<br>• Updated the maximum values of the following conditions for Transmitter True Differential I/O Standards - $f_{HSDR}$ (data rate) parameter in High-Speed I/O Specifications for Intel Arria 10 Devices table.<br>☐ SERDES factor J = 2, uses DDR registers<br>☐ SERDES factor J = 1, uses DDR registers<br>• Added the following tables:<br>☐ Memory Standards Supported by the Hard Memory Controller for Intel Arria 10 Devices<br>☐ Memory Standards Supported by the Soft Memory Controller for Intel Arria 10 Devices<br>• Updated minimum $T_{OCTCAL}$ value from 1000 cycles to 2000 cycles in OCT Calibration Block Specifications for Intel Arria 10 Devices table.<br>• Updated the hmc_free_clk specifications for the following speed grades in HPS Clock Performance for Intel Arria 10 Devices table:<br>☐ –1 speed grade: Updated from 667 MHz to 533 MHz.<br>☐ –2 speed grade: Updated from 544 MHz to 533 MHz.<br>• Changed from $T_{sclk}$ to $T_{clk}$ and added the following specifications in the Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Intel Arria 10 Devices table.<br>☐ $T_{qspi_clk}$<br>☐ $T_{din_start}$<br>☐ $T_{din_end}$<br>• Updated SPI Master Timing Requirements for Intel Arria 10 Devices table.<br>☐ Changed the symbol from $T_{spi_clk}$ to $T_{clk}$.<br>☐ Added note to $T_{dssfrst}$, $T_{dsslst}$, and $T_h$.<br>☐ Updated note to $T_{su}$.<br>☐ Updated the description for $T_{su}$ and $T_h$.<br>• Updated the note to $T_{ssfsu}$, $T_{ssfh}$, $T_{sslsu}$, and $T_{sslh}$ in the SPI Slave Timing Requirements for Intel Arria 10 Devices table.<br>• Updated the following timing diagrams:<br>☐ Quad SPI Flash Serial Output Timing Diagram<br>☐ SPI Master Output Timing Diagram<br>☐ SPI Slave Output Timing Diagram |

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| | | • Added the following timing diagrams:<br>☐ Quad SPI Flash Serial Input Timing Diagram<br>☐ SPI Master Input Timing Diagram<br>☐ SPI Slave Input Timing Diagram<br>• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Arria 10 Devices table.<br>☐ Changed $T_{clk}$ to $T_{sdmmc_clk_out}$ and `TMMC_CLK` to `TSDMMC_CLK_OUT`.<br>☐ Updated $T_d$ min from 5.5 ns to 8.5 ns and max from 12.5 ns to 11.5 ns.<br>☐ Updated note to $T_d$.<br>• Changed the title and symbols in the following timing diagrams:<br>☐ Changed from "NAND Data Input Cycle Timing Diagram" to "NAND Data Output Cycle Timing Diagram". Changed from $D_{IN}$ to $D_{OUT}$.<br>☐ Changed from "NAND Data Output Cycle Timing Diagram" to "NAND Data Input Cycle Timing Diagram". Changed from $D_{OUT}$ to $D_{IN}$.<br>☐ Changed from "NAND Extended Data Output (EDO) Cycle Timing Diagram" to "NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle". Changed from $D_{OUT}$ to $D_{IN}$.<br>• Changed from "ARM Trace Timing Characteristics" to "Trace Timing Characteristics".<br>• Updated the description in the GPIO Interface topic.<br>• Updated FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Arria 10 Devices table.<br>☐ Updated the maximum value for $t_{STATUS}$ and $t_{CF2ST1}$ from 1,506 µs to 3,000 µs.<br>☐ Updated $f_{MAX}$ for FPP ×8/×16 from 125 MHz to 100 MHz.<br>☐ Updated the minimum value for $t_{CF2CK}$ from 1,506 µs to 3,010 µs.<br>☐ Updated the minimum value for $t_{ST2CK}$ from 2 µs to 10 µs.<br>☐ Updated the maximum value for $t_{CD2UM}$ from 437 µs to 830 µs.<br>• Updated FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Arria 10 Devices table.<br>☐ Updated the maximum value for $t_{STATUS}$ and $t_{CF2ST1}$ from 1,506 µs to 3,000 µs.<br>☐ Updated $f_{MAX}$ for FPP ×8/×16 from 125 MHz to 100 MHz.<br>☐ Updated the minimum value for $t_{CF2CK}$ from 1,506 µs to 3,010 µs.<br>☐ Updated the minimum value for $t_{ST2CK}$ from 2 µs to 10 µs.<br>☐ Updated the maximum value for $t_{CD2UM}$ from 437 µs to 830 µs.<br>• Updated maximum value for $t_{CD2UM}$ from 437 µs to 830 µs in AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Arria 10 Devices table.<br>• Updated PS Timing Parameters for Intel Arria 10 Devices table.<br>☐ Updated the maximum value for $t_{STATUS}$ and $t_{CF2ST1}$ from 1,506 µs to 3,000 µs<br>☐ Updated the minimum value for $t_{CF2CK}$ from 1,506 µs to 3,010 µs.<br>☐ Updated the minimum value for $t_{ST2CK}$ from 2 µs to 10 µs.<br>☐ Updated the maximum value for $t_{CD2UM}$ from 437 µs to 830 µs. |

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| | | • Added description about `.rbf` and `.rpd` files in the Configuration Files section. Changed the table title from "Uncompressed Uncompressed .rbf Sizes Sizes for Intel Arria 10 Devices" to "Configuration Bit Stream Sizes for Intel Arria 10 Devices".<br>• Updated the note to Active Serial in Minimum Configuration Time Estimation for Intel Arria 10 Devices table. Note: The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external `CLKUSR` may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.<br>• Changed instances of *Quartus II* to *Quartus Prime*.<br>• Changed voltages and conditions in the "Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices" table.<br>• Changed maximum data rate conditions in the "Transmitter and Receiver Data Rate Performance" table.<br>• Changed conditions in the "Transmitter and Receiver Data Rate Performance" table in the *Transceiver Performance for Arria 10 GT Devices* section.<br>• Changed conditions in the "Reference Clock Specifications" table.<br>• Changed the clock networks in the "Transceiver Clock Network Maximum Data Rate Specifications" table.<br>• Changed conditions in the "Receiver Specifications" table.<br>• Changed conditions in the "Transmitter Specifications" table.<br>• Changed the minimum frequency in the "ATX PLL Performance," "Fractional PLL Performance," and "CMU PLL Performance" tables in the *Transceiver Performance for Intel Arria 10 GX/SX Devices* section.<br>• Changed the minimum frequeny in the "ATX PLL Performance," "Fractional PLL Performance," and "CMU PLL Performance" tables in the *Transceiver Performance for Intel Arria 10 GT Devices* section.<br>• Added a parameter to the "Reference Clock Specifications" table.<br>• Added footnote to the "Transmitter Specifications" table. |
| June 2015 | 2015.06.12 | • Changed the specifications for the backplane maximum data rate condition in the "Transmitter and Receiver Data Rate Performance" table for Intel Arria 10 GX/SX devices.<br>• Changed the specifications for transmitter `REFCLK` phase noise in the "Reference Clock Specifications" table.<br>• Added note in the following tables:<br>☐ Absolute Maximum Ratings for Intel Arria 10 Devices: $V_{CCPGM}$<br>☐ Maximum Allowed Overshoot During Transitions for Intel Arria 10 Devices: LVDS I/O<br>☐ Recommended Operating Conditions for Intel Arria 10 Devices: $V_I$<br>• Added HPS Specifications.<br>• Updated recommended EPCQ-L serial configuration devices in the Uncompressed .rbf Sizes table. |
| May 2015 | 2015.05.08 | Made the following changes:<br>• Changed the specifications for the $V_{ICM}$ (AC coupled) parameter in the "Reference Clock Specifications" table.<br>• Changed the maximum frequency in the "CMU PLL Performance" table in the *Transceiver Performance for GT Devices* section.<br>• Added a footnote to the transceiver speed grade 5 column in the "Transmitter and Receiver Data Rate Performance" table. |

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| Date | Version | Changes |
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| May 2015 | 2015.05.04 | • Updated the Maximum Allowed Overshoot During Transitions for Intel Arria 10 Devices table.<br>• Added a note to $t_{ramp}$ in the Recommended Operating Conditions for Intel Arria 10 Devices table. Note: $t_{ramp}$ is the ramp time of each individual power supply, not the ramp time of all combined power supplies.<br>• Changed the minimum, typical, and maximum values for the transmitter and receiver power supply in the "Transceiver Power Supply Operating Conditions for Intel Arria 10 GT Devices" table.<br>• Added –1 speed grade in the condition column for $V_{CCL_HPS}$ at 0.95 V in HPS Power Supply Operating Conditions for Intel Arria 10 SX Devices table.<br>• Added –I1S, –I2S, and –E2S speed grades to the following tables:<br>☐ Clock Tree Performance for Intel Arria 10 Devices<br>☐ DSP Block Performance Specifications for Intel Arria 10 Devices<br>☐ Memory Block Performance Specifications for Intel Arria 10 Devices<br>☐ High-Speed I/O Specifications for Intel Arria 10 Devices<br>☐ Memory Output Clock Jitter Specifications for Intel Arria 10 Devices<br>• Updated $f_{IN}$ minimum value from 27 MHz to 50 MHz for all speed grades in the Fractional PLL Specifications for Intel Arria 10 Devices table.<br>• Changed the description for $f_{INPFD}$ to "Input clock frequency to the PFD" in the I/O PLL Specifications for Intel Arria 10 Devices table.<br>• Updated DSP Block Performance Specifications for Intel Arria 10 Devices table for $V_{CC}$ and $V_{CCP}$ at 0.9 V typical value. Added DSP specifications for $V_{CC}$ and $V_{CCP}$ at 0.95 V typical value.<br>• Updated $I_{bias}$ minimum value from 8 µA to 10 µA and maximum value from 200 µA to 100 µA in the External Temperature Sensing Diode Specifications for Intel Arria 10 Devices table.<br>• Added DPA (soft CDR mode) specifications in High-Speed I/O Specifications for Intel Arria 10 Devices table.<br>• Added description in POR Specifications section: Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the `nSTATUS` is released high and your device is ready to begin configuration.<br>• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria 10 Devices chapter.<br>☐ FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1<br>☐ FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1<br>☐ AS Configuration Timing Waveform<br>☐ PS Configuration Timing Waveform<br>• Removed the DCLK-to-DATA[] ratio when both encryption and compression are turned on. Added description to the table: You cannot turn on encryption and compression at the same time for Intel Arria 10 devices.<br>• Updated the AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Arria 10 Devices table as follows:<br>☐ Changed the symbol for data hold time from $t_H$ to $t_{DH}$.<br>☐ Updated the minimum value for $t_{SU}$ from 0 ns to 1 ns.<br>☐ Updated the minimum value for $t_{DH}$ from 2.5 ns to 1.5 ns.<br>• Added a note to the DCLK Frequency Specification in the AS Configuration Scheme table. Note: You can only set 12.5, 25, 50, and 100 MHz in the Intel Quartus Prime software. |

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| Date | Version | Changes |
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| | | • Added a note to the Initialization Clock Source Option and the Maximum Frequency for Intel Arria 10 Devices. Note: If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.<br>• Changed Intel Arria 10 GS to Intel Arria 10 SX in Uncompressed .rbf Sizes and Minimum Configuration Time Estimation tables.<br>• Added IO_IN_DLY_CHN and IO_OUT_DLY_CHN in the IOE Programmable Delay table.<br>• Changed the Min/Typ/Max description for the $V_{ICM}$ (AC coupled) parameter in the "Reference Clock Specifications" table.<br>• Changed the Min/Typ/Max values in the "Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices" table.<br>• Changed the Min/Typ/Max values in the "Transceiver Power Supply Operating Conditions for Arria 10 GT Devices" table.<br>• Added a footnote to the maximum data rate for GT channels in the "Transceiver Performance for GT Devices" section.<br>• Made the following changes to the "Transceiver Performance for Arria 10 GX/SX Devices" section.<br>☐ Changed the maximum data rate condition for chip-to-chip and backplane in the "Transmitter and Receiver Data Rate Performance" table.<br>☐ Added TX minimum data rate to the "Transmitter and Receiver Data Rate Performance" table.<br>☐ Changed the minimum frequency in the "ATX PLL Performance" table.<br>☐ Changed the minimum frequency in the "Fractional PLL Performance" table.<br>☐ Changed the minimum and maximum frequency in the "CMU PLL Performance" table.<br>• Made the following changes to the "Transceiver Performance for Arria 10 GT Devices" section.<br>☐ Added TX minimum data rate to the "Transmitter and Receiver Data Rate Performance" table.<br>☐ Changed the maximum data rate condition for chip-to-chip and backplane in the "Transmitter and Receiver Data Rate Performance" table.<br>☐ Changed the minimum frequency in the "ATX PLL Performance" table.<br>☐ Changed the minimum frequency in the "Fractional PLL Performance" table.<br>☐ Changed the minimum frequency in the "CMU PLL Performance" table.<br>• Added voltage condition to the maximum peak-to-peak diff p-p after configuration and to the $V_{ICM}$ specifications in the "Receiver Specifications" table.<br>• Changed the voltage conditions for $V_{OCM}$ in the "Transmitter Specifications" table.<br>• Changed the $V_{OD}/V_{CCT}$ Ratios in the "Typical Transmitter $V_{OD}$ Settings" table.<br>• Added the "Transceiver Clock Network Maximum Data Rate Specifications" table. |
| January 2015 | 2015.01.23 | • Added a note in the "Transceiver Power Supply Operating Conditions" section.<br>• Made the following changes to the "Reference Clock Specifications" table:<br>☐ Added the input reference clock frequency parameters for the CMU PLL, ATX PLL, and fPLL PLL.<br>☐ Changed the maximum specification for rise time and fall time.<br>☐ Added the $V_{ICM}$ (AC and DC coupled) parameters.<br>☐ Changed the maximum value for Transmitter REFCLK Phase Noise (622 MHz) when ≥ 1 MHz.<br>• Changed the Min, Typ, and Max values for the reconfig_clk signal in the "Transceiver Clocks Specifications" table. |

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| Date | Version | Changes |
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| | | • Made the following changes to the "Receiver Specifications" table:<br>☐ Added the maximum peak-to-peak differential input voltage after device configuration specifications.<br>☐ Changed the minimum specification for the minimum differential eye opening at receiver serial input pins parameter.<br>☐ Removed the 120-ohm and 150-ohm conditions for the differential on-chip termination resistors parameter.<br>☐ Added the $V_{ICM}$ (AC and DC coupled) parameter.<br>☐ Added the Programmable DC Gain parameter.<br>• Made the following changes to the "Transmitter Specifications" table:<br>☐ Added the $V_{OCM}$ (AC coupled) parameter.<br>☐ Added the $V_{OCM}$ (DC coupled) parameter.<br>☐ Changed the rise and fall time minimum and maximum specifications.<br>• Added the "Typical Transmitter $V_{OD}$ Settings" table.<br>• Added a note to $V_{CC}$, $V_{CCP}$, and $V_{CCERAM}$ typical values in Recommended Operating Conditions table. Note: You can operate –1 and –2 speed grade devices at 0.9 V or 0.95 V typical value. You can operate -3 speed grade device at only 0.9 V typical value. Core performance shown in this datasheet is applicable for the operation at 0.9 V. Operating at 0.95 V results in higher core performance and higher power consumption. For more information about the performance and power consumption of 0.95 V operation, refer to the Intel Quartus Prime software timing reports and Early Power Estimator (EPE).<br>• Removed military grade operating junction temperature specifications ($T_J$) in Recommended Operating Conditions table.<br>• Updated the $V_{CCIO}$ range for HSTL-18 I/O standard in Differential HSTL and HSUL I/O Standards for Arria 10 Devices table as follows:<br>☐ Min: Updated from 1.425 V to 1.71 V<br>☐ Typ: Updated from 1.5 V to 1.8 V<br>☐ Max: Updated from 1.575 V to 1.89 V<br>• Added a statement to Differential I/O Standards Specifications for Intel Arria 10 Devices table: Differential inputs are powered by $V_{CCPT}$ which requires 1.8 V.<br>• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.<br>• Updated fractional PLL specifications.<br>☐ Updated $f_{OUT_C}$ to $f_{OUT}$ and updated the maximum value to 644 MHz for all speed grades.<br>☐ Updated $f_{VCO}$ minimum value from 2.4 GHz to 3.125 GHz.<br>☐ Removed $f_{OUT_L}$, $k_{VALUE}$, and $f_{RES}$ parameters.<br>• Updated I/O PLL specifications.<br>☐ Updated $f_{OUT_C}$ to $f_{OUT}$ and updated the maximum value to 644 MHz for all speed grades.<br>☐ Updated $f_{OUT_EXT}$ maximum value to 800 MHz (–1 speed grade), 720 MHz (–2 speed grade), and 650 MHz (–3 speed grade).<br>☐ Removed $f_{RES}$ parameter.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. |

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| Date | Version | Changes |
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| | | • Updated AS Timing Parameters for AS x1 and AS x4 Configurations in Intel Arria 10 Devices.<br>☐ Updated $t_{SU}$ minimum value from 1.5 ns to 0 ns.<br>☐ Updated $t_H$ minimum value from 0 ns to 2.5 ns.<br>• Updated `CLKUSR` initialization clock source maximum frequency from 125 MHz to 100 MHz for passive configuration schemes (PS and FPP).<br>• Added uncompressed `.rbf` sizes and minimum configuration time estimation for Intel Arria 10 GX and GS devices.<br>• Updated uncompressed `.rbf` sizes for Intel Arria 10 GX 900 and 1150 devices, and Intel Arria 10 GT 900 and 1150 devices.<br>☐ Updated configuration `.rbf` size from 335,106,890 bits to 351,292,512 bits.<br>☐ Updated IOCSR `.rbf` size from 6,702,138 bits to 1,885,396 bits.<br>• Updated minimum configuration time estimation for Intel Arria 10 GX 900 and 1150 devices, and Intel Arria 10 GT 900 and 1150 devices for the following configuration modes:<br>☐ Active serial: Updated from 837.77 ms to 883.20 ms.<br>☐ Fast Passive Parallel: Updated from 104.72 ms to 110.40 ms. |
| August 2014 | 2014.08.18 | • Changed the 3 V I/O conditions in Table 2.<br>• Table 3:<br>☐ Added a note to the Minimum and Maximum operating conditions.<br>☐ Changed $V_{CCERAM}$ values.<br>☐ Changed the Maximum recommended operating conditions for 3 V I/O $V_I$.<br>• Added a note to the I/O pin pull-up tolerance in Table 12.<br>• Changed the $V_{IH}$ values for LVTTL, LVCMOS and 2.5 I/O standards in Table 13.<br>• Table 14, Table 15, and Table 16:<br>☐ Added SSTL-12 I/O standard.<br>☐ Removed Class I, II for SSTL-135 and SSTL-125 I/O standards.<br>• Table 19:<br>☐ Changed the minimum data rate specification for transmitter and receiver data rates.<br>☐ Changed the minimum frequency specification for the fractional PLL.<br>☐ Changed the minimum frequency specification for the CMU PLL.<br>• Changed the Core Speed Grade with Power Options section in Table 20.<br>• Table 21:<br>☐ Changed the minimum data rate specification for transmitter and receiver data rates.<br>☐ Changed the minimum frequency specification for the Fractional PLL.<br>☐ Changed the minimum frequency specification for the CMU PLL.<br>☐ Changed the minimum frequency of the ATX PLL. |

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| | | • Table 23:<br>☐ Added a note to the High Speed Differential I/O standard.<br>☐ Changed the specifications for CLKUSR pin.<br>• Added columns in Table 29.<br>• Changed the maximum $f_{HSCLK_in}$ and $t_{xJitter}$ in Table 32.<br>• Changed the minimum formula for $t_{CD2UMC}$ in Table 42, Table 43, Table 44, and Table 46.<br>• Changed the CLKUSR maximum frequency and minimum number of cycles in Table 47.<br>• Table 48:<br>☐ Changed the IOCSR `.rbf` size.<br>☐ Added Recommended EPCQ-L Serial Configuration Device.<br>• Changed the DCLK frequency and minimum configuration time for FPP in Table 49.<br>• Added the following tables:<br>☐ External Temperature Sensing Diode Specifications for Intel Arria 10 Devices<br>☐ IOE Programmable Delay for Intel Arria 10 Devices<br>• Removed the following figures:<br>☐ CTLE Response in High Gain Mode for Intel Arria 10 Devices with Data Rates ≥ 8 Gbps<br>☐ Removed the CTLE Response in High Gain Mode for Intel Arria 10 Devices with Data Rates < 8 Gbps |
| March 2014 | 2014.03.14 | Updated Table 3, Table 5, Table 21, Table 23, Table 24, Table 32, and Table 41. |
| December 2013 | 2013.12.06 | Updated Figure 1 and Figure 2. |
| December 2013 | 2013.12.02 | Initial release. |

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