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THE DATASHEET OF

XA7Z020-1CLG484I

XA Zynq-7000 SoC Data Sheet: Overview

DS188 (v1.3.2) July 2, 2018 **Product Specification**

XA Zynq-7000 SoC First Generation Architecture

The XA Zynq™-7000 Automotive family is based on the Xilinx® SoC architecture. These products integrate a feature-rich dual-core ARM® Cortex™-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the heart of the PS and also include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. This highly integrated, flexible, and power-optimized solution is ideal for high computationally intensive and performance demanding applications. The automotive family focuses on automotive applications and consists of the Z-7010, Z-7020, and Z-7030 devices.

Processing System (PS)

Dual-Core ARM Cortex-A9 Based Application Processor Unit (APU)

- 2.5 DMIPS/MHz per CPU
- CPU frequency: Up to 667 MHz
- Coherent multiprocessor support
- ARMv7-A architecture
  - TrustZone security
  - Thumb-2 instruction set
- Jazelle RCT execution Environment Architecture
- NEON media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ technology and Program Trace Macrocell (PTM)
- Timer and Interrupts
  - Three watchdog timers
  - One global timer
  - Two triple-timer counters

Caches

- 32 KB Level 1 4-way set-associative instruction and data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache (shared between the CPUs)
- Byte-parity support

On-Chip Memory

- On-chip boot ROM
- 256 KB on-chip RAM (OCM)
- Byte-parity support

External Memory Interfaces

- Multiprotocol dynamic memory controller
- 16-bit or 32-bit interfaces to DDR3L, DDR3, DDR2, or LPDDR2 memories
- ECC support in 16-bit mode
- 1 GB of address space using single rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces

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- 8-bit SRAM data bus with up to 64 MB support
- Parallel NOR flash support
- ONFI1.0 NAND flash support (1-bit ECC)
- 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

I/O Peripherals and Interfaces

- Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - GMII and RGMII interfaces
- Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
  - USB 2.0 compliant device IP core
  - On-the-go, high-speed, full-speed, and low-speed modes support
  - Intel EHCI compliant USB host
  - 8-bit ULPI external PHY interface
- Two full CAN 2.0B compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
  - External PHY interface
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the programmable logic (PL)
- Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA AXI based
- QoS support on critical masters for latency and bandwidth control

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadeable adders

36 Kb Block RAM

- True Dual-Port
- Up to 72 bits wide
- Configurable as dual 18 Kb

DSP Blocks

- 18 x 25 signed multiply
- 48-bit adder/accumulator
- 25-bit pre-adder

Programmable I/O Blocks

- Supports LVCMOS, LVDS, and SSTL
- 1.2V to 3.3V I/O
- Programmable I/O delay and SerDes

JTAG Boundary-Scan

- IEEE Std 1149.1 Compatible Test Interface

Two 12-Bit Analog-to-Digital Converters

- On-chip voltage and temperature sensing
- Up to 17 external differential input channels
- One million samples per second maximum conversion rate

Automotive Temperature Range

- I-Grade: Tj = –40°C to +100°C
- Q-Grade: Tj = –40°C to +125°C

Automotive Standards

- AEC-Q100 qualification
  (Beyond AEC-Q100 Qualification is available upon request)
- Production Part Approval Process (PPAP) Documentation

Serial Transceivers

- Up to 4 receivers and transmitters
- Supports up to 6.6 Gb/s data rates

PCI Express® Block

- Root Complex and Endpoint configurations
- Supports up to Gen2 speeds
- Supports up to 4 lanes

Feature Summary

Table 1: **XA Zynq-7000 SoC**

	Device Name	Z-7010	Z-7020	Z-7030
	Part Number	**XA7Z010**	**XA7Z020**	**XA7Z030**
Processing System	Processor Core	Dual ARM Cortex-A9 MPCore with CoreSight technology		
	Processor Extensions	NEON & Single/Double Precision Floating Point for each processor		
	Maximum Frequency	667 MHz (-1)		
	L1 Cache	32 KB Instruction, 32 KB Data per processor		
	L2 Cache	512 KB		
	On-Chip Memory	256 KB		
	External Memory Support(1)	DDR3L, DDR3, DDR2, LPDDR2		
	External Static Memory Support(1)	2x Quad-SPI, NAND, NOR		
	DMA Channels	8 (4 dedicated to Programmable Logic)		
	Peripherals(1)	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO		
	Security(2)	AES and SHA 256b for device security		
Processing System to Programmable Logic Interface Ports (Primary Interfaces and Interrupts Only)		2x AXI 32b Master 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts		
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Kintex® FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600
	Flip-Flops	35,200	106,400	157,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)
	Programmable DSP Slices (18x25 MACCs)	80	220	400
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs
	PCI Express (Root Complex and Endpoint)	–	–	Gen2 x4
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs		
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication		

Notes:

1. Restrictions apply for CLG225 package. Refer to UG585, *Zynq-7000 SoC Technical Reference Manual* (TRM) for details.
2. Security is shared by the processing system and the programmable logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Device-Package Combinations

XA Zynq-7000 SoCs device-package combinations are listed in Table 1.

Table 2: **Device-Package Combinations**

Package(1)	CLG225		CLG400		CLG484		FBG484 / FBV484			
Size	13 x 13 mm		17 x 17 mm		19 x 19 mm		23 x 23 mm			
Ball Pitch	0.8 mm		0.8 mm		0.8 mm		1.0 mm			
Device	PS I/O(2)	SelectIO™ HR	PS I/O(2)	SelectIO HR(3)	PS I/O(2)	SelectIO HR(3)	PS I/O(2)	GTX	SelectIO HR	SelectIO HP(4)
XA7Z010	86	54	130	100						
XA7Z020			130	125	130	200				
XA7Z030							130	4	100	63

Notes:
1. All packages listed are Pb-free.
2. PS I/O includes user I/O and DDR I/O.
3. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
4. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

XA Zynq-7000 Family Description

The XA Zynq-7000 family offers the flexibility and scalability of an FPGA, while providing the performance, power, and ease of use typically associated with ASICs and ASSPs. The range of devices in the XA Zynq-7000 SoC family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each device in the XA Zynq-7000 family contains the same PS, the PL and I/O resources vary between the devices.

The XA Zynq-7000 architecture enables implementation of custom logic in the PL and custom software in the PS. It allows for the realization of unique and differentiated system functions. The integration of the PS with the PL allows levels of performance that two-chip solutions (e.g., an ASSP with an FPGA) cannot match due to their limited I/O bandwidth, latency, and power budgets.

Xilinx offers a large number of soft IP for the XA Zynq-7000 family. Stand-alone and Linux device drivers are available for the peripherals in the PS and the PL. The award-winning ISE® Design Suite: System Edition development environment enables a rapid product development for software, hardware, and systems engineers. Adoption of the ARM-based PS also brings a broad range of third-party tools and IP providers in combination with Xilinx's existing PL ecosystem.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A9 processor are also available for the XA Zynq-7000 family.

The PS and the PL are on separate power domains, enabling the user of these devices to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.

Figure 1 illustrates the functional blocks of the XA Zynq-7000 SoC. For more information on the functional blocks, see UG585, *Zynq-7000 SoC Technical Reference Manual*.

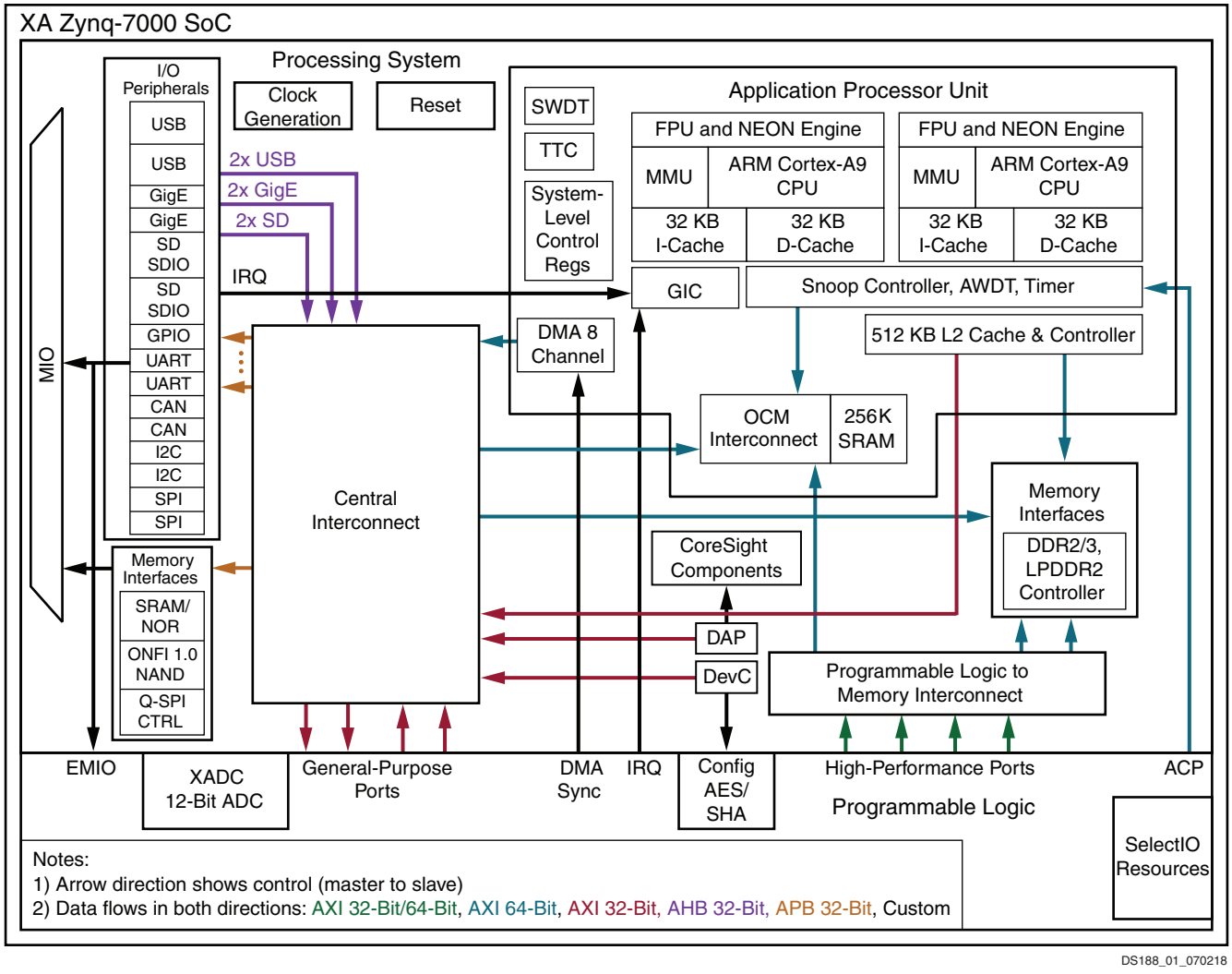


Figure 1: **XA Zynq-7000 SoC Overview**

Processor System Description

As shown in Figure 1, the PS comprises four major blocks:

- Application processor unit (APU)
- Memory interfaces
- I/O peripherals (IOP)
- Interconnect

Application Processor Unit (APU)

The key features of the APU include:

- Dual core ARM Cortex-A9 MPCores. Features associated with each core include:
  - 2.5 DMIPS/MHz
  - Operating frequency range:
    - Z-7010/Z-7020 (wire bond), Z-7030 (flip-chip): Up to 667 MHz (-1)
  - Ability to operate in single processor, symmetric dual processor, and asymmetric dual processor modes
  - Single and double precision floating point: up to 2.0 MFLOPS/MHz each
  - NEON media processing engine for SIMD support
  - Thumb-2 support for code compression
  - Level 1 caches (separate instruction and data, 32 KB each)
    - 4-way set-associative
    - Non-blocking data cache with support for up to four outstanding read and write misses each
  - Integrated memory management unit (MMU)
  - TrustZone for secure mode operation
- Accelerator coherency port (ACP) interface enabling coherent accesses from PL to CPU memory space
- Unified Level 2 cache (512 KB)
  - 8-way set-associative
  - TrustZone enabled for secure operation
- Dual-ported, on-chip RAM (256 KB)
  - Accessible by CPU and PL
  - Designed for low latency access from the CPU
- 8-channel DMA
  - Supports multiple transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather
  - 64-bit AXI interface, enabling high throughput DMA transfers
  - 4 channels dedicated to PL
  - TrustZone enabled for secure operation
  - Dual register access interfaces enforce separation between secure and non-secure accesses
- Interrupts and Timers
  - General interrupt controller (GIC)
  - Three watch dog timers (WDT) (one per CPU and one system WDT)
  - Two triple timers/counters (TTC)

- CoreSight debug and trace support for Cortex-A9
  - Program trace Macrocell (PTM) for instruction and trace
  - Cross trigger interface (CTI) enabling hardware breakpoints and triggers

Memory Interfaces

The memory interface unit includes a dynamic memory controller and static memory interface modules. The dynamic memory controller supports DDR3L, DDR3, DDR2, and LPDDR2 memories. The static memory controllers support a NAND flash interface, a Quad-SPI flash interface, a parallel data bus, and a parallel NOR flash interface.

Dynamic Memory Interfaces

The multi-protocol DDR memory controller can be configured to provide 16-bit or 32-bit-wide accesses to a 1 GB address space using a single rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. ECC is supported in 16-bit bus access mode. The PS incorporates both the DDR controller and the associated PHY, including its own set of dedicated I/Os. Speed of up to 1066 Mb/s for DDR3L and DDR3 is supported.

The DDR memory controller is multi-ported and enables the processing system and the programmable logic to have shared access to a common memory. The DDR controller features four AXI slave ports for this purpose:

- One 64-bit port is dedicated for the ARM CPU(s) via the L2 cache controller and can be configured for low latency.
- Two 64-bit ports are dedicated for PL access.
- One 64-bit AXI port is shared by all other AXI masters via the central interconnect.

Static Memory Interfaces

The static memory interfaces support external static memories:

- 8-bit SRAM data bus supporting up to 64 MB
- 8-bit parallel NOR flash supporting up to 64 MB
- ONFi 1.0 NAND flash support with 1-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

I/O Peripherals (IOP)

The IOP unit contains the data communication peripherals. Key features of the IOP include:

- Two 10/100/1000 tri-mode Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - Supports an external PHY interface
- Two USB 2.0 OTG peripherals, each supporting up to 12 endpoints
  - Supports high-speed and full-speed modes in Host, Device, and On-The-Go configurations
  - Fully USB 2.0 compliant, Host, and Device IP core
  - Uses 32-bit AHB DMA master and AHB slave interfaces
  - Provides an 8-bit ULPI external PHY interface
  - Intel EHCI compliant USB host controller registers and data structures
- Two full CAN 2.0B compliant CAN bus interface controllers
  - CAN 2.0-B standard as defined by BOSCH Gmbh
  - ISO 118981-1
  - An external PHY interface
- Two SD/SDIO 2.0 compliant SD/SDIO controllers with built-in DMA
- Two full-duplex SPI ports with three peripheral chip selects
- Two UARTs
- Two master and slave I2C interfaces
- Up to 118 GPIO bits

Using the TrustZone system, the two Ethernet, two SDIO, and two USB ports (all master devices) can be configured to be secure or non-secure.

The IOP peripherals communicate to external devices through a shared pool of up to 54 dedicated multiuse I/O (MIO) pins. Each peripheral can be assigned one of several pre-defined groups of pins, enabling a flexible assignment of multiple devices simultaneously. Although 54 pins are not enough for simultaneous use of all the I/O peripherals, most IOP interface signals are available to the PL, allowing use of standard PL I/O pins when powered up and properly configured. All MIO pins support 1.8V HSTL and LVCMOS standards as well as 2.5V/3.3V standards.

Interconnect

The APU, memory interface unit, and the IOP are all connected to each other and to the PL through a multilayered ARM AMBA AXI interconnect.The interconnect is non-blocking and supports multiple simultaneous master-slave transactions.

The interconnect is designed with latency sensitive masters, such as the ARM CPU, having the shortest paths to memory, and bandwidth critical masters, such as the potential PL masters, having high throughput connections to the slaves with which they need to communicate.

Traffic through the interconnect can be regulated through the Quality of Service (QoS) block in the interconnect. The QoS feature is used to regulate traffic generated by the CPU, DMA controller, and a combined entity representing the masters in the IOP.

PS Interfaces

PS External Interfaces

The XA Zynq-7000 SoCs' PS external interfaces use dedicated pins that cannot be assigned as PL pins. These include:

- Clock, reset, boot mode, and voltage reference
- Up to 54 dedicated multiuse I/O (MIO) pins, software-configurable to connect to any of the internal I/O peripherals and static memory controllers
- 32-bit or 16-bit DDR2/DDR3L/DDR3/LPDDR2 memories

MIO Overview

The function of the MIO is to multiplex access from the PS peripheral and static memory interfaces to the PS pins as defined in the configuration registers. There are up to 54 pins available for use by the IOP and static memory interfaces in the PS. Table 3 shows where the different peripherals pins can be mapped. A block diagram of the MIO module is shown in Figure 2.

If additional I/O pins beyond the 54 are required, it is possible to route these through the PL to the I/O associated with the PL. This feature is referred to as extendable multiplexed I/O (EMIO).

Port mappings can appear in multiple locations. For example, there are up to 12 possible port mappings for CAN pins. The XPS Zynq-7000 SoC's PS MIO Configuration tool should be used for peripheral and static memory pin mapping.

Table 3: **MIO Peripheral Interface Mapping**

Peripheral Interface	MIO	EMIO
Quad-SPI NOR/SRAM NAND	Yes	No
USB 0,1	Yes — External PHY	No
SDIO 0,1	Yes — 50 MHz	Yes — 25 MHz
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 54 bits	Yes CAN: External PHY GPIO: Up to 64 bits
GigE: 0,1	RGMII v2.0 External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, and MII in Programmable Logic
UART: 0,1	Simple UART: Only two pins (Tx and Rx)	Full UART (Tx, Rx, DTR, DCD, DSR, RI, RTS and CTS): Requires either: • Two Processing System pins (Rx and Tx) through MIO and six additional Programmable Logic pins, *or* • Eight Programmable Logic pins
Debug Trace Ports	Yes — Up to 16 trace bits	Yes — Up to 32 trace bits
Processor JTAG	Yes	Yes

Notes:
1. Restrictions apply for CLG225 package. Refer to UG585, *Zynq-7000 SoC Technical Reference Manual* (TRM) for details.

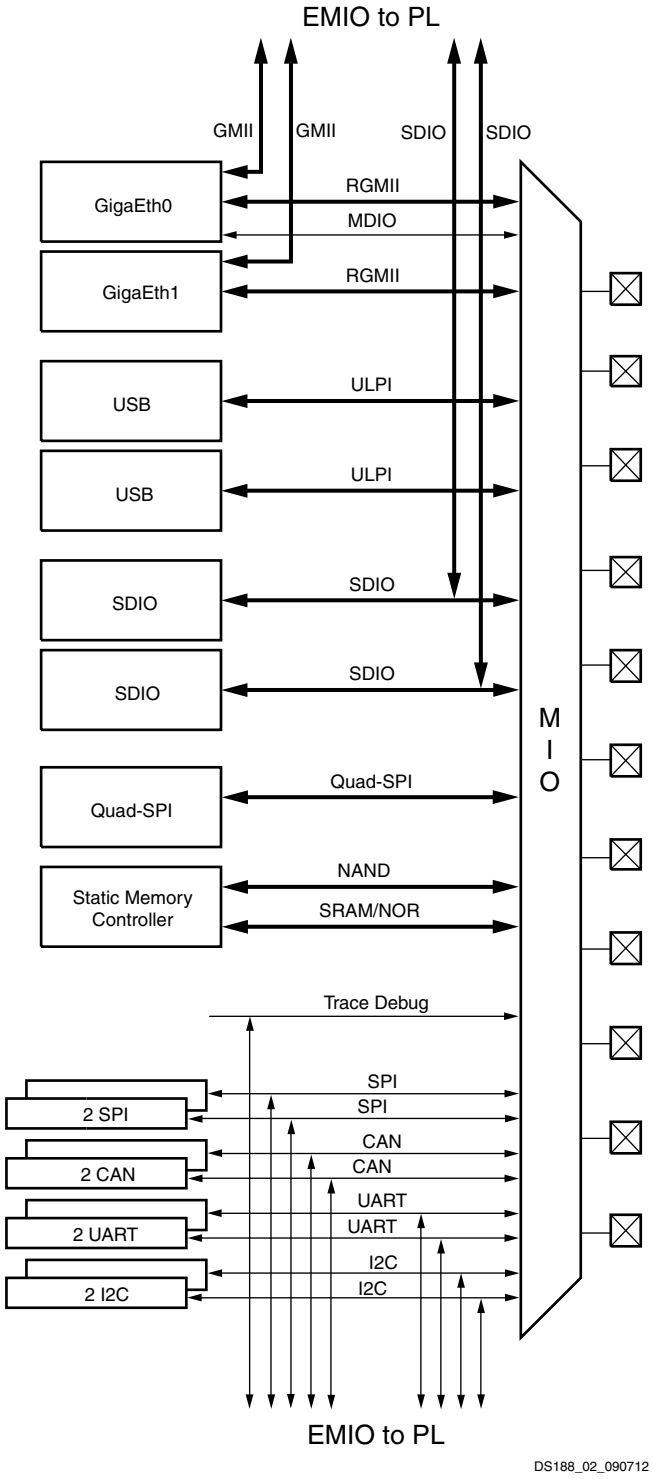


Figure 2: **MIO Module Block Diagram**

PS-PL Interface

The PS-PL interface includes:

- AMBA AXI interfaces for primary data communication
  - Two 32-bit AXI master interfaces
  - Two 32-bit AXI slave interfaces
  - Four 64-bit/32-bit configurable, buffered AXI slave interfaces with direct access to DDR memory and OCM, referred to as high-performance AXI ports
  - One 64-bit AXI slave interface (ACP port) for coherent access to CPU memory
- DMA, interrupts, events signals
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS GIC
  - Four DMA channel signals for the PL
  - Asynchronous triggering signals
- Extendable multiplexed I/O (EMIO) allows unmapped PS peripherals to access PL I/O
- Clocks and resets
  - Four PS clock outputs to the PL with start/stop control
  - Four PS reset outputs to the PL
- Configuration and miscellaneous
  - Processor configuration access port (PCAP) to support full and partial PL configuration, and secured PS boot image decryption and authentication
  - JTAG interface

The two highest performance interfaces between the PS and the PL for data transfer are the high-performance AXI ports and ACP interfaces. The high performance AXI ports are used for high throughput data transfer between the PS and the PL. Coherency, if required, is managed under software control. When hardware coherent access to the CPU memory is required, the ACP port is to be used.

High-Performance AXI Ports

The high-performance AXI ports provide access from the PL to DDR and OCM in the PS. The four dedicated AXI memory ports from the PL to the PS are configurable as either 32-bit or 64-bit interfaces. As shown in Figure 3, these interfaces connect the PL to the memory interconnect via a FIFO controller. Two of the three output ports go to the DDR memory controller and the third goes to the dual-ported on-chip memory (OCM).

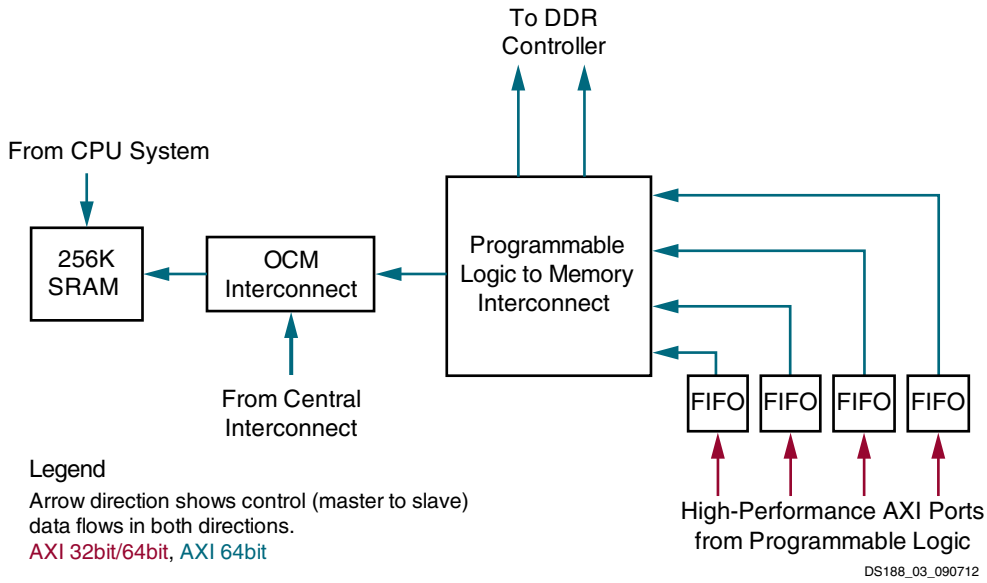


Figure 3: **PL Interface to PS Memory Subsystem**

Each high-performance AXI port has these characteristics:

- Reduced latency between PL and processing system memory
- 1 KB deep FIFO
- Configurable either as 32- or 64-bit AXI interfaces
- Supports up to a 32 word buffer for read acceptance
- Supports data release control for write accesses to use AXI interconnect bandwidth more efficiently
- Supports multiple AXI commands issuing to DDR and OCM

Accelerator Coherency Port (ACP)

The Zynq-7000 SoC accelerator coherency port (ACP) is a 64-bit AXI slave interface that provides connectivity between the APU and a potential accelerator function in the PL. The ACP directly connects the PL to the snoop control unit (SCU) of the ARM Cortex-A9 processors, enabling cache-coherent access to CPU data in the L1 and L2 caches. The ACP provides a low latency path between the PS and a PL-based accelerator when compared with a legacy cache flushing and loading scheme.

Programmable Logic (PL) Description

Key PL features include:

- CLB
  - Eight LUTs per CLB for random logic implementation or distributed memory
  - Memory LUTs are configurable as 64x1 or 32x2 bit RAM or shift register (SRL)
  - 16 flip-flops per CLB
  - 2 x 4-bit cascadeable adders for arithmetic functions
- 36 Kb block RAM
  - True dual-port
  - Up to 36 bits wide
  - Configurable as dual 18 Kb block RAMs
- DSP slices
  - 18 x 25 signed multiply
  - 48-bit adder/accumulator
- Programmable I/O blocks
  - Support for common I/O standards including LVCMOS, LVDS, and SSTL
  - 1.2V to 3.3V I/O
  - Built-in programmable I/O delay
- Two 12-bit analog to digital converters (XADC)
  - On-chip voltage and temperature
  - Up to 17 external differential input channels
- PL configuration module
- Low-power serial transceivers in selected Zynq-7000 SoCs
- An integrated Endpoint/Root Port (can be Root Complex when connected to the PS) block for PCI Express in selected Zynq-7000 SoCs

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- True 6-input LUTs
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in the XA Zynq-7000 SoC can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well

as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one flip-flop per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Each XA Zynq-7000 SoC has up to five clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL).

Table 4: **MMCM and PLL Count**

Device	MMCMs	PLLs
XA7Z010	2	2
XA7Z020	4	4
XA7Z030	5	5

Mixed-Mode Clock Manager and Phase-Locked Loop

The MMCM and PLL share many characteristics. Both can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of both components is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers: D, M, and O. The pre-divider D (programmable by configuration and afterwards via DRP) reduces the input frequency and feeds one input of the traditional PLL phase/frequency comparator. The feedback divider M (programmable by configuration and afterwards via DRP) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases: 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. Each can be selected to drive one of the output dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by configuration to divide by any integer from 1 to 128.

The MMCM and PLL have three input-jitter filter options: Low-bandwidth mode, which has the best jitter attenuation; high-bandwidth mode, which has the best phase offset; and optimized mode, which allows the tools to find the best setting.

MMCM Additional Programmable Features

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of $^{1}/_{8}$ and can thus increase frequency synthesis capabilities by a factor of 8.

The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,200 MHz, the phase-shift timing increment is 15 ps.

Clock Distribution

Each XA Zynq-7000 SoC provides six different types of clock lines (BUFG, BUFR, BUFIO, BUFH, BUFMR, and the high-performance clock) to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew.

Global Clock Lines

In each XA Zynq-7000 SoC, 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset as well as many logic inputs. There are 12 global clock lines within any clock region driven by the horizontal clock buffers (BUFH). Each BUFH can be independently enabled/disabled, allowing for clocks to be turned off within a region, thereby offering fine-grain control over which clock regions consume power. Global clock lines can be driven by global clock buffers, which can also perform glitchless clock multiplexing and clock enable functions. Global clocks are often driven from the CMT, which can completely eliminate the basic clock distribution delay.

Regional Clocks

Regional clocks can drive all clock destinations in their region. A region is defined as any area that is 50 I/O and 50 CLB high and half the device wide. XA Zynq-7000 SoCs have between eight and twenty-four regions. There are four regional clock tracks in every region. Each regional clock buffer can be driven from either of four clock-capable input pins, and its frequency can optionally be divided by any integer from 1 to 8.

I/O Clocks

I/O clocks are especially fast and serve only I/O logic, as described in the I/O Logic section. XA Zynq-7000 SoCs have a direct connection from the MMCM to the I/O for low-jitter, high-performance interfaces.

Block RAM

Some of the key features of the block RAM include:

- Dual-port 36 Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every XA Zynq-7000 SoC has between 60 and 265 dual-port block RAMs, each storing 36 Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

Synchronous Operation

Each memory access, read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged.

Programmable Data Width

Each port can be configured as 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8), 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64). The two ports can have different aspect ratios without any constraints.

Each block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36 Kb block RAM also applies to each of the smaller 18 Kb block RAMs.

Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18 Kb RAM) or 36 bits (36 Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72.

Both sides of the dual-port 36 Kb RAM can be of variable width.

Two adjacent 36 Kb block RAMs can be configured as one cascaded 64K × 1 dual-port RAM without any additional logic.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable. Similar to the block RAM, the FIFO width and depth are programmable, but the write and read ports always have identical width.

First word fall-through mode presents the first-written word on the data output even before the first read operation. After the first word has been read, there is no difference between this mode and the standard mode.

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 × 18 twos complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All XA Zynq-7000 SoCs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 464 MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Input/Output

Some highlights of the PL input/output functionality include:

- High-performance SelectIO technology with support for 800 Mb/s DDR3
- High-frequency decoupling capacitors within the package for enhanced signal integrity
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation

The number of I/O pins varies depending on device and package size. Each I/O is configurable and can comply with a large number of I/O standards. With the exception of the supply pins and a few dedicated configuration pins, all other PL pins have the same I/O capabilities, constrained only by certain banking rules. The SelectIO resources in XA Zynq-7000 SoCs are classed as High Range (HR). The HR I/Os offer voltage support that ranges from 1.2V to 3.3V.

All I/O pins are organized in banks, with 50 pins per bank. Each bank has one common V_{CCO} output supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). There are two V_{REF} pins per bank (except configuration bank 0). A single bank can have only one V_{REF} voltage value.

XA Zynq-7000 SoCs use small form factor wire-bond and flip-chip packages for lowest cost.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All XA Zynq-7000 SoCs support differential standards beyond LVDS: HT, RSDS, BLVDS, differential SSTL, and differential HSTL.

Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended SSTL and differential SSTL. The SSTL I/O standard can support data rates of up to 667 Mb/s for DDR3 (-1Q grade) interfacing applications.

3-State Digitally Controlled Impedance and Low-Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low-power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input and some outputs can be individually delayed by up to 32 increments of 78 ps or 52 ps each. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each I/O pin possesses an 8-bit IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 3, 4, 5, 6, 7, or 8 bits. By cascading two IOSERDES from two adjacent pins (default from differential I/O), wider width conversions of 10 and 14 bits can also be supported. The ISERDES has a special oversampling mode capable of asynchronous data recovery for applications like a 1.25 Gb/s LVDS I/O-based SGMII interface.

Low-Power Serial Transceivers

Some highlights of the low-power serial transceivers include:

- High-performance GTX transceivers capable of up to 6.6 Gb/s with lidless flip-chip packages.
- Low-power mode optimized for chip-to-chip interfaces.
- Advanced Transmit pre and post emphasis, and receiver linear (CTLE) and decision feedback equalization (DFE), including adaptive equalization for additional margin.

Ultra-fast serial data transmission to optical modules, between ICs on the same PCB, over the backplane, or over longer distances is becoming increasingly popular and important to enable customer line cards to scale to 200 Gb/s. It requires specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues at these high data rates.

The Zynq-7000 SoCs transceiver counts range from 0 to 4 transceiver circuits. Each serial transceiver is a combined transmitter and receiver. The various Zynq-7000 serial transceivers can use a combination of ring oscillators and LC tank architecture to allow the ideal blend of flexibility and performance while enabling IP portability across the family members. Lower data rates can be achieved using Zynq-7000 logic-based oversampling. The serial transmitter and receiver are independent circuits that use an advanced PLL architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80. This allows the designer to trade-off datapath width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits. This allows the designer to trade-off internal datapath width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the PL using the RXUSRCLK clock. For short channels, the transceivers offers a special low power mode (LPM) for additional power reduction.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCI Express and SATA/SAS applications.

Integrated Block for PCI Express Designs

Highlights of the integrated block for PCI Express include:

- Compliant to the PCI Express Base Specification 2.1 with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s) and Gen2 (5 Gb/s)
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error Reporting and ECRC features

All Zynq-7000 SoCs with transceivers include an integrated block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom communication between the Zynq-7000 SoC and other devices via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the Zynq-7000 SoC.

This block is highly configurable to system design requirements and can operate 1, 2, or 4 lanes at the 2.5 Gb/s and 5.0 Gb/s data rates. For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCI Express, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: lane width, maximum payload size, PL interface speeds, reference clock frequency, and base address register decoding and filtering.

Xilinx offers a wrapper for the integrated block: AXI4 (memory mapped). AXI4 (memory mapped) is designed for Xilinx Platform Studio/EDK design flow and MicroBlaze™ processor based designs.

More information and documentation on solutions for PCI Express designs can be found at: http://www.xilinx.com/technology/protocols/pciexpress.htm.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture at I-grade temperature specs include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All XA Zynq-7000 SoCs integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the XA Zynq-7000 SoCs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer mode with the dedicated analog input (see UG480, *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the JTAG interface. User-defined alarm thresholds can automatically indicate over-temperature events and unacceptable power supply variation. A user-specified limit (for example, 100°C) can be used to initiate an automatic power-down.

System-Level Functions

Several functions span both the PS and PL and include:

- Reset management
- Clock management
- Device configuration
- Hardware and software debug support
- Power management

Reset Management

The reset management function provides the ability to reset the entire device or individual units within it. The PS supports these reset functions and signals:

- External and internal power-on reset signal
- Warm reset
- Watchdog timer reset
- User resets to PL
- Software, watchdog timer, or JTAG provided resets
- Security violation reset (locked down reset)

Clock Management

The PS in the Zynq-7000 product family is equipped with three phase-locked loops (PLLs), providing flexibility in configuring the clock domains within the PS. There are three primary clock domains of interest within the PS. These include the APU, the DDR controller, and the I/O peripherals (IOP). The frequencies of all of these domains can be configured independently under software control.

PS Boot and Device Configuration

XA Zynq-7000 SoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the PL must be powered on to enable the use of the security block located within the PL, which provides 256-bit AES and SHA decryption/authentication.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NOR, NAND, Quad-SPI, SD, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the ARM Cortex-A9 CPUs executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the OCM.

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain the SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, NOR, or Quad-SPI) and SDIO are configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or callable after boot.

Hardware and Software Debug Support

The debug system used in the XA Zynq-7000 SoC is based on ARM's CoreSight architecture. It uses ARM CoreSight components including an embedded trace buffer (ETB), a program trace Macrocell (PTM), and an instrument trace Macrocell (ITM). This enables instruction trace features as well as hardware breakpoints and triggers. The programmable logic can be debugged with the Xilinx ChipScope™ Pro embedded logic analyzer.

Debug Ports

There are two JTAG ports available that can be chained together or used separately. When chained together, a single port is used for ARM processor code downloads and run-time control operations, PL configuration, and PL debug with the ChipScope Pro embedded logic analyzer. This enables tools such as the Xilinx Software Development Kit (SDK) and ChipScope Pro analyzer to share a single download cable from Xilinx.

When the JTAG chain is split, one port is used for PS support, including direct access to the ARM DAP interface. This CoreSight interface enables the use of ARM-compliant debug and software development tools such as Development Studio 5 (DS-5). The other JTAG port can then be used by the Xilinx FPGA tools for access to the PL, including configuration bitstream downloads and PL debug with the ChipScope Pro analyzer. In this mode, users can download to, and debug the PL in the same manner as a stand-alone FPGA.

Power Management

The PS and PL reside on different power planes. This enables the PS and PL to be connected to independent power rails, each with its own dedicated power supply pins. If PL power-off mode is not needed, the user can tie the PS and PL power rails together. When the PS is in power-off mode, it holds the PL in a permanent reset condition. The power control for the PL is accomplished through external pins to the PL. External power management circuitry can be used to control power. The external power management circuitry could be controlled by software and the PS GPIO.

Power Modes

These are a few of the power savings modes offered by the XA Zynq-7000 SoC:

- Programmable Logic Power Off (Sleep)
  - The PS and PL reside on different power planes and the PS can run with the PL powered off. For security reasons, the PL cannot be powered on before the PS. The PL requires reconfiguration after each power-on. The user should take PL configuration time into consideration when using this power savings mode.
- PS Clock Control
  - The PS can be run at a reduced clock rate down to 30 MHz using the internal PLLs. The clock rate can be changed dynamically. To change the clock dynamically, the user must unlock the system control register to access the PS clock control register or the clock generation control register.
- Single Processor Mode
  - In this mode, the second Cortex-A9 CPU is switched off using clock gating and the first CPU is kept fully operational.

Power Examples

Power for the XA Zynq-7000 SoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use Xilinx Power Estimator (XPE) at http://www.xilinx.com/products/design_tools/logic_design/xpe.htm.

Memory Map

XA Zynq-7000 SoCs support a 4 GB address space, organized as described in Table 5.

Table 5: **Memory Map**

Start Address	Size (MB)	Description
0x0000_0000	1,024	DDR DRAM and on-chip memory (OCM)
0x4000_0000	1,024	PL AXI slave port #0
0x8000_0000	1,024	PL AXI slave port #1
0xE000_0000	256	IOP devices
0xF000_0000	128	Reserved
0xF800_0000	32	Programmable registers access via AMBA APB bus
0xFA00_0000	32	Reserved
0xFC00_0000	64 MB - 256 KB	Quad-SPI linear address base address (except top 256 KB which is in OCM), 64 MB reserved, only 32 MB is currently supported
0xFFFC_0000	256 KB	OCM when mapped to high address space

Ordering Information

Table 6 shows the speed and temperature grades available in the different device families. Some devices might not be available in every speed and temperature grade.

Table 6: **Speed Grade and Junction Temperature Ranges**

Device	Speed Grade and Junction Temperature Range	
	Industrial (I) –40°C to +100°C	Automotive (Q) –40°C to +125°C
XA Zynq-7000	-1	-1

The ordering information, shown in Figure 4, applies to all packages including Pb-Free.

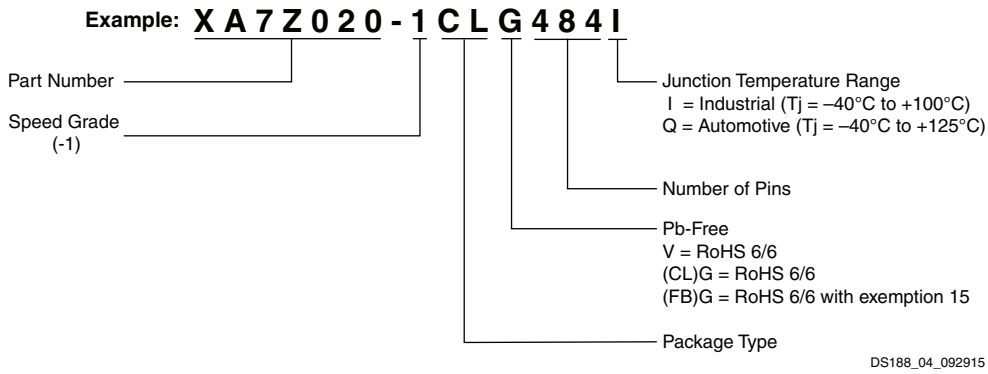


Figure 4: **Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/02/2018	1.3.2	Typographical updates.
07/08/2016	1.3.1	Typographical updates.
10/15/2015	1.3	Changed document classification to Product Specification from Advance Product Specification. Updated Table 2. Updated Ordering Information.
10/10/2014	1.2	Added DDR3L to: External Memory Interfaces; Table 1; Memory Interfaces; Dynamic Memory Interfaces; and PS External Interfaces. Updated I/O Peripherals (IOP) and Clock Management.
06/04/2014	1.1	Added Z-7030 device; Serial Transceivers; PCI Express® Block; Table 4; Low-Power Serial Transceivers; Integrated Block for PCI Express Designs Updated Table 1; Table 2; Application Processor Unit (APU); Programmable Logic (PL) Description; Clock Management; Block RAM; Input/Output; Power Examples (including the removal of Table 4), and XADC (Analog-to-Digital Converter).
10/15/2012	1.0	Initial Xilinx release.

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