THE DATASHEET OF

PI6C41202LE

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PI6C41202
PI6C41204
PI6C41204A

LVCMOS to LVPECL Driver

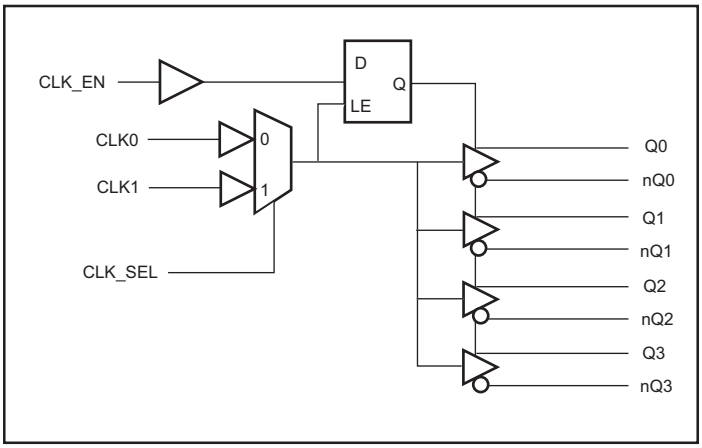
Features

- Up to Four LVPECL outputs
- Selectable CLK0 or CLK1 inputs
- LVCMOS or LVTTL input level
- 30ps max output skew
- 150ps max part-to-part skew
- 1.9ns max propagation delay
- 266 MHz output frequency
- Packaging (Pb-free & Green available):
  -14-pin TSSOP
  - 20-pin TSSOP

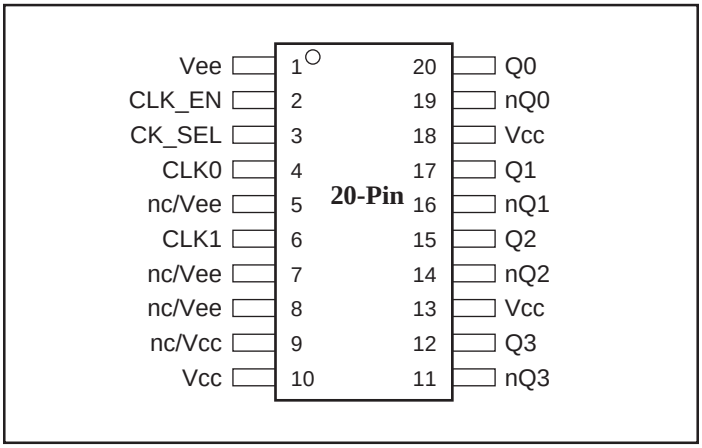
Description

PI6C4120x is a high-performance LVCMOS or LVTTL to LVPECL clock buffer. The PI6C41204 is a 4 output version with 2 selectable inputs, pin compatible with ICS8535-01. PI6C41204A is the enhanced version with extra power and ground pins to minimize noise and jitter. The PI6C41202 is similar to the PI6C41204 except it has two outputs.

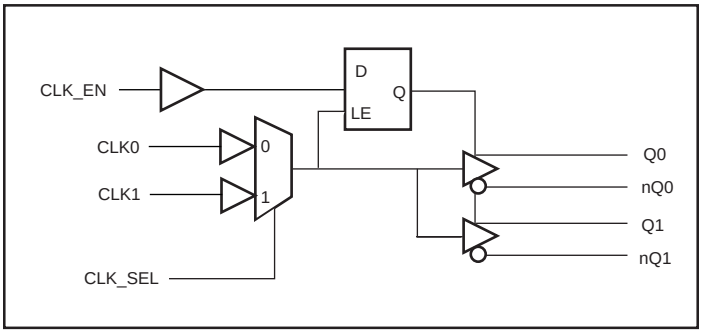
Block Diagram PI6C41204/A



Pin Configuration PI6C41204/A



Block Diagram PI6C41202



Pin Configuration PI6C41202

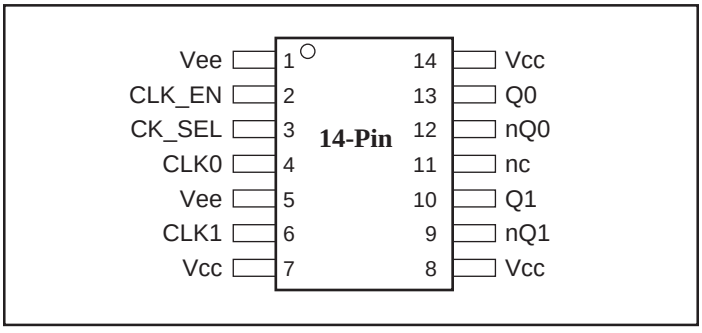


Table 1a. Pin Description for PI6C41204

Number	Name	Type		Description
1	Vee	Power		Ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q are low, nQ are high. LVCMOS or LVTTL input level.
3	CLK_SEL	Input	Pulldown	Clock select input: LOW = CLK0, HIGH = CLK1 LVCMOS or LVTTL input level.
4	CLK0	Input	Pulldown	LVCMOS or LVTTL clock input.
6	CLK1	Input	Pulldown	LVCMOS or LVTTL input level.
5, 7, 8, 9	NC	Unused		No Connect
10, 13, 18	Vcc	Power		3.3V supply
11, 12	nQ3, Q3	Output		LVPECL output pair.
14, 15	nQ2, Q2	Output		LVPECL output pair.
16, 17	nQ1, Q1	Output		LVPECL output pair.
19, 20	nQ0, Q0	Output		LVPECL output pair.

Table 1b. Pin Description for PI6C41204A

Number	Name	Type		Description
1, 5, 7, 8	Vee	Power		Ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q are low, nQ are high. LVCMOS or LVTTL input level.
3	CLK_SEL	Input	Pulldown	Clock select input: LOW = CLK0, HIGH = CLK1 LVCMOS or LVTTL input level
4	CLK0	Input	Pulldown	LVCMOS or LVTTL clock input.
6	CLK1	Input	Pulldown	LVCMOS or LVTTL input level.
9, 10, 13, 18	Vcc	Power		3.3V supply
11, 12	nQ3, Q3	Output		LVPECL output pair.
14, 15	nQ2, Q2	Output		LVPECL output pair.
16, 17	nQ1, Q1	Output		LVPECL output pair.
19, 20	nQ0, Q0	Output		LVPECL output pair.

Table 1c. Pin Description for PI6C41202

Number	Name	Type		Description
1, 5	Vee	Power		Ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q are low, nQ are high. LVCMOS or LVTTL input level.
3	CLK_SEL	Input	Pulldown	Clock select input: LOW = CLK0, HIGH = CLK1 LVCMOS or LVTTL input level.
4	CLK0	Input	Pulldown	LVCMOS or LVTTL clock input.
6	CLK1	Input	Pulldown	LVCMOS or LVTTL input level.
7, 8, 14	Vcc	Power		3.3V supply
9, 10	nQ1, Q1	Output		LVPECL output pair.
12, 13	nQ0, Q0	Output		LVPECL output pair.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	CLK0, CLK1			3.2		pF
		CLK_EN CLK_SEL			2.7		
R_{PULLUP}	Input Pullup Resistor				80		K ohm
$R_{PULLDOWN}$	Input Pulldown Resistor				80		

Table 3a. Control Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0 thru Q3*	nQ0 thru nQ3*
0	0	CLK0	Disabled ; LOW	Disabled ; HIGH
0	1	CLK1	Disabled ; LOW	Disabled ; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in figure1. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3b.

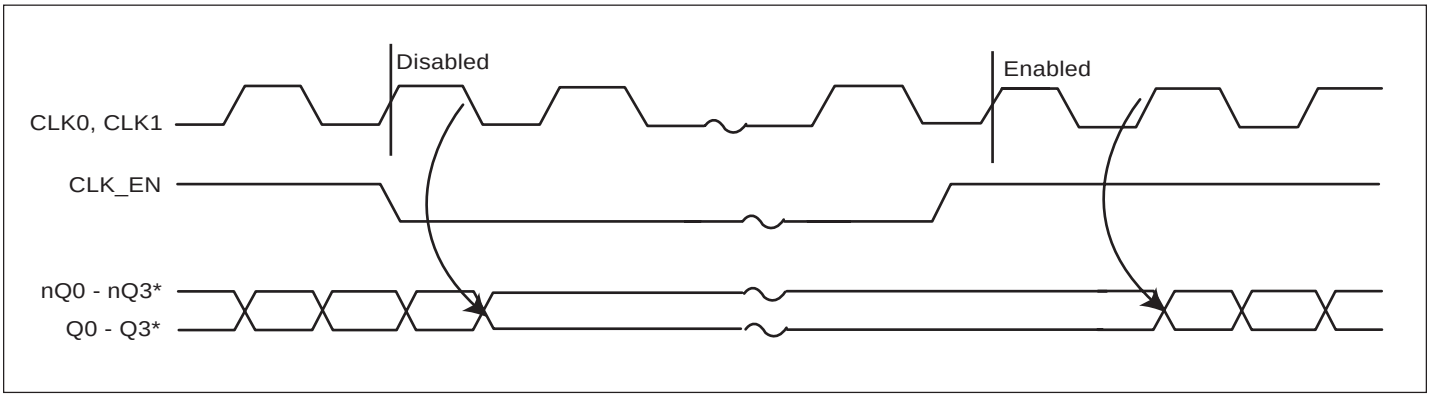


Figure 1. CLK_EN Timing Diagram

Table 3b. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	Q0 thru Q3*	nQ0 thru nQ3*
0	LOW	HIGH
1	HIGH	LOW

Note:
*PI6C41204 and PI6C41204A have four differential outputs. Q0 through Q3 and nQ0 through nQ3. PI6C41202 has two differential outputs. Q0 through Q1 and nQ0 through nQ1.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage, V_{CC}	+4.6V
Input/Output Voltage	–0.5V to V_{CC} + 0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4a. Operating Conditions (Commercial)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	3.135	3.3	3.465	V
I_{EE}	Supply Current			50	mA
T_A	Ambient Temperature	0		70	°C

Table 4b. LVCMOS/LVTTL DC Characteristics, (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	CLK0,CLK1		2		3.765	V
		CLK_EN CLK_SEL		2		3.765	
V_{IL}	Input Low Voltage	CLK0, CLK1		— 0.3		0.8	
		CLK_EN CLK_SEL		— 0.3		0.8	
I_{IH}	Input High Current	CLK0,CLK1 CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	
I_{IL}	Input Low Current	CLK0, CLK1 CLK_SEL	V_{IN} =0V, V_{CC} = 3.465V	— 5			
		CLK_EN	V_{IN} =0V, V_{CC} = 3.465V	— 150			

Table 4c. LVPECL DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Note 1	V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage	Note 1	V_{CC} - 2.0		V_{CC} - 1.7	
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	

Note:
1. Outputs terminated with 50ohm to V_{CC} - 2V

Table 5. AC Characteristics, (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C (Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Input Frequency				266	MHz
t_{PLH}	Propagation Delay Low to High : Note 4	V_{CC} to V_{OX}	1.0		1.9	ns
t_{PHL}	Propagation Delay High to Low : Note 4	V_{CC} to V_{OX}	1.0		1.9	
ts(o)	Output Skew : Note 5			11	30	ps
tsk(pp)	Part to Part Skew : Note 6				150	
t_{DC}	Output Duty Cycle		48	50	52	%
t_r/t_f	Output Rise / Fall time 20% to 80%		100		400	ps

Notes:
3. All parameters measured at 266MHz unless noted otherwise. The part does not add jitter.
4. Measured from the $V_{DD}/2$ point of the input to the differential output crossing point.
5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output crossing points differential.
6. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Measured at the output crossing points differential.

Table 5a. Operating Conditions (Industrial)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	3.135	3.3	3.465	V
I_{EE}	Supply Current			50	mA
T_A	Ambient Temperature	–40		85	°C

Table 5b. LVCMOS/LVTTL DC Characteristics, (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	CLK0,CLK1		2		3.765	V
		CLK_EN CLK_SEL		2		3.765	
V_{IL}	Input Low Voltage	CLK0, CLK1		— 0.3		0.8	
		CLK_EN CLK_SEL		— 0.3		0.8	
I_{IH}	Input High Current	CLK0,CLK1 CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	
I_{IL}	Input Low Current	CLK0, CLK1 CLK_SEL	V_{IN} =0V, V_{CC} = 3.465V	— 5			
		CLK_EN	V_{IN} =0V, V_{CC} = 3.465V	— 150			

Table 5c. LVPECL DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Note 1	V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage	Note 1	V_{CC} - 2.0		V_{CC} - 1.7	
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	

Note:
1. Outputs terminated with 50ohm to V_{CC} - 2V

Table 6. AC Characteristics, (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C, See Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Input Frequency				266	MHz
t_{PLH}	Propagation Delay Low to High : Note 4	V_{CC} to V_{OX}	1.0		1.9	ns
t_{PHL}	Propagation Delay High to Low : Note 4	V_{CC} to V_{OX}	1.0		1.9	
ts(o)	Output Skew : Note 5			11	100	ps
tsk(pp)	Part to Part Skew : Note 6				150	
t_{DC}	Output Duty Cycle		45	50	55	%
t_r/t_f	Output Rise / Fall time 20% to 80%		100		400	ps

Notes:
3. All parameters measured at 266MHz unless noted otherwise. The part does not add jitter.
4. Measured from the $V_{DD}/2$ point of the input to the differential output crossing point.
5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output crossing points differential.
6. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Measured at the output crossing points differential.

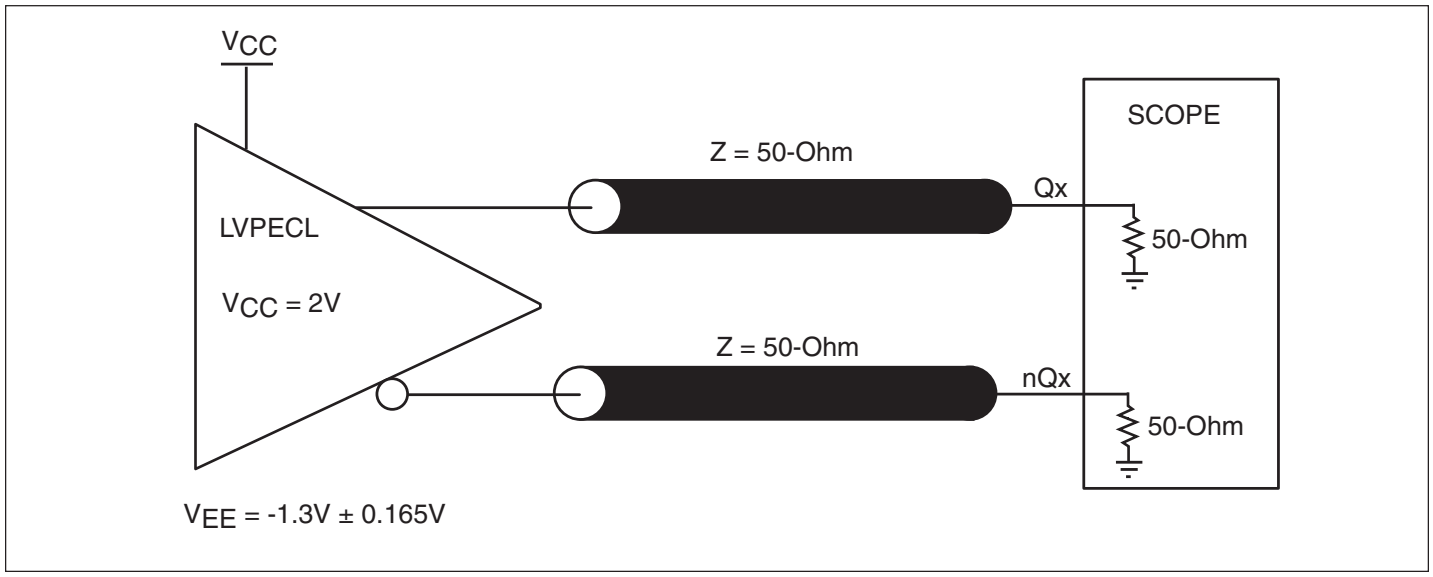


Figure2. 2-3.3V Output Load Test Circuit

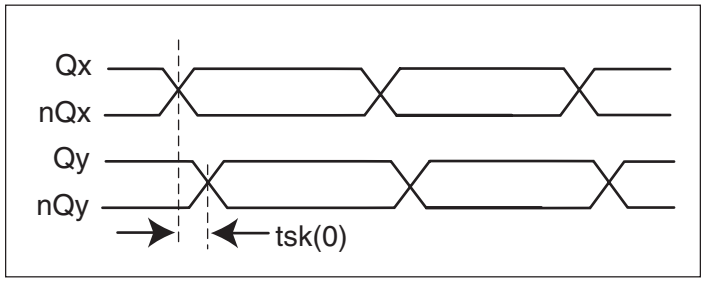


Figure 3. Output Skew

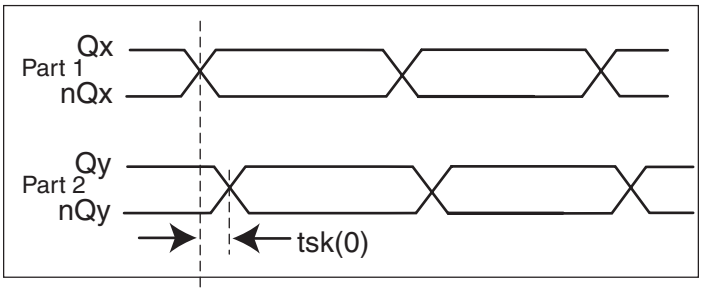


Figure 4. Part-to-Part Skew

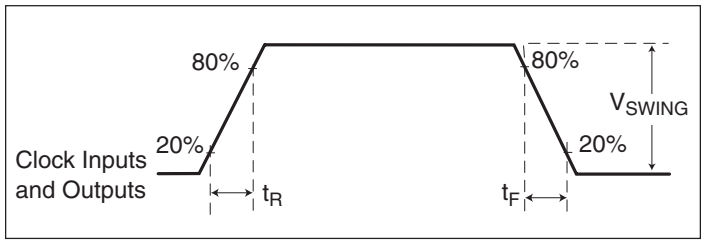


Figure 5. Input and Output Rise and Fall Time

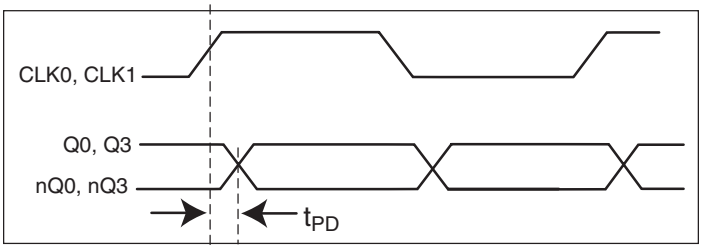


Figure 6. Propagation Delay

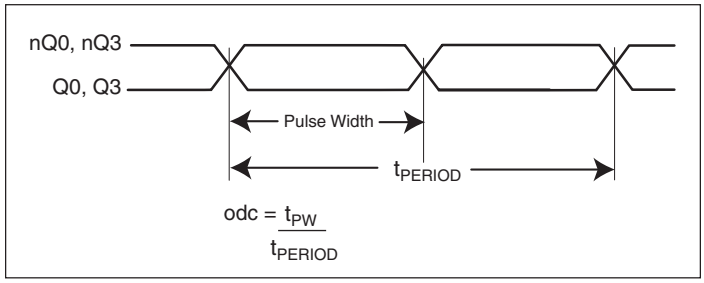
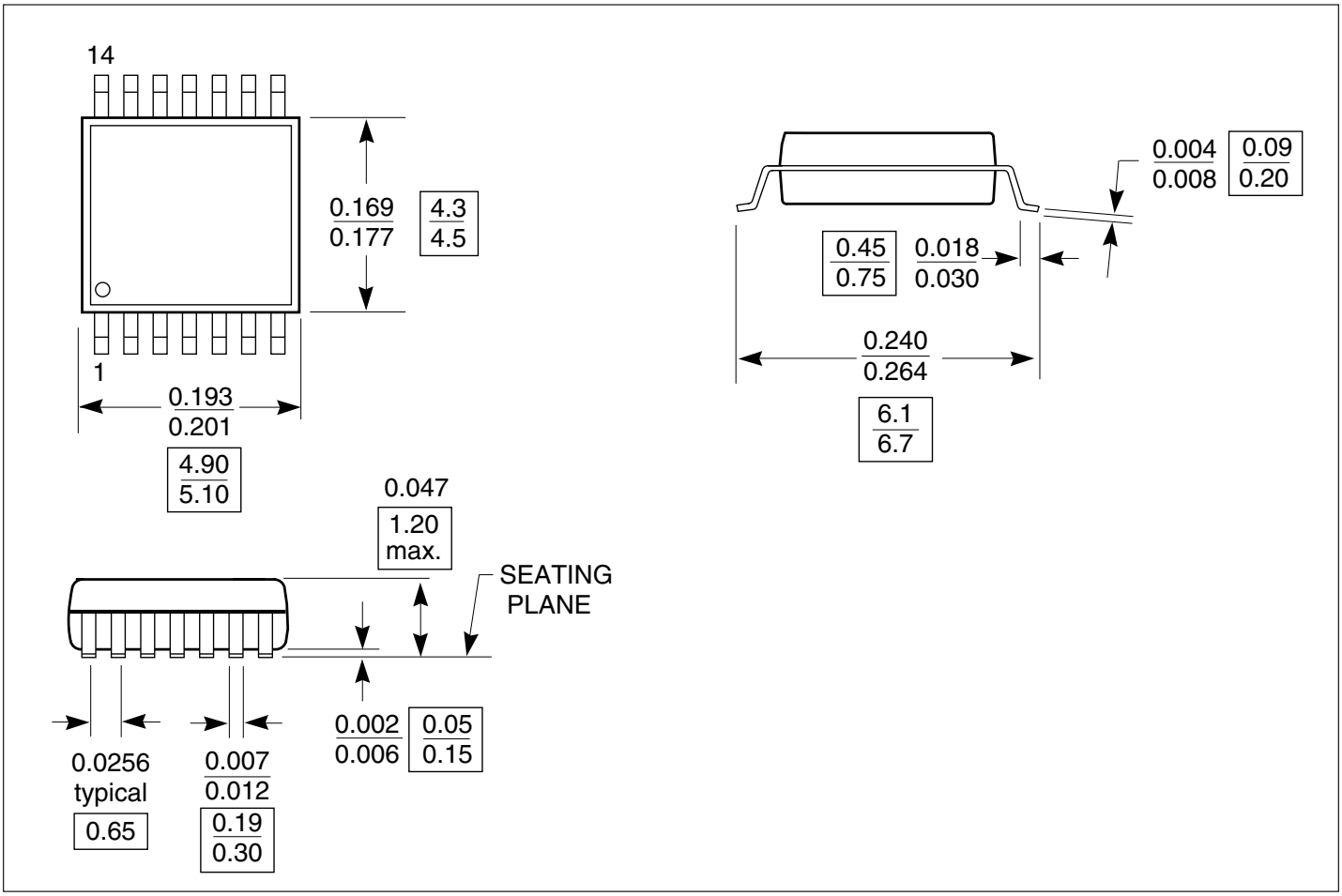
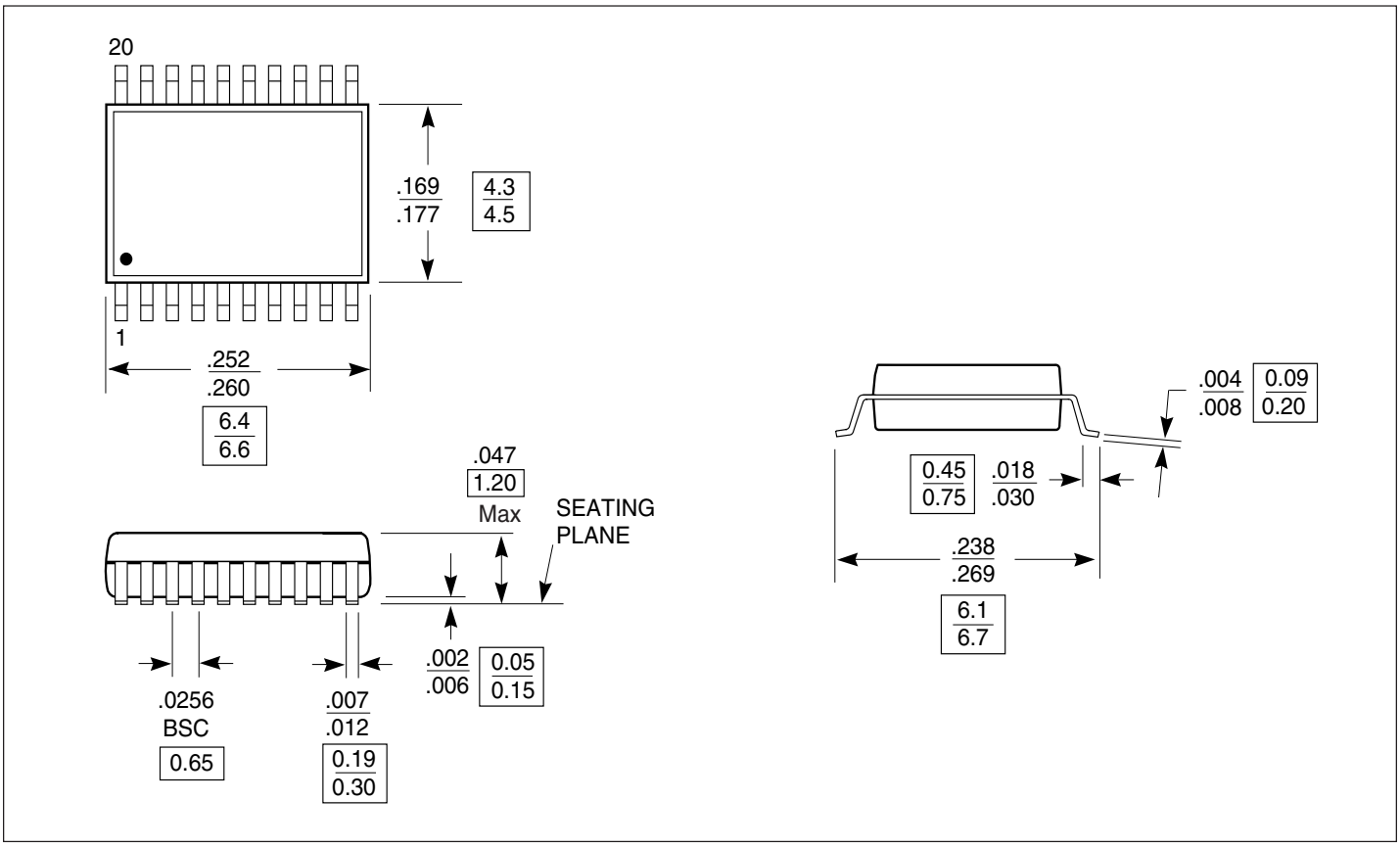


Figure 7. odc & t_{PERIOD}

Packaging Mechanical: 14-Pin TSSOP (L)



Packaging Mechanical: 20-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C41202L	L	14-pin173-mil TSSOP	Commercial
PI6C41202LE	L	Pb-free & Green, 14-pin173-mil TSSOP	Commercial
PI6C41204L	L	20-pin173-mil TSSOP	Commercial
PI6C41204LE	L	Pb-free & Green, 20-pin173-mil TSSOP	Commercial
PI6C41204LI	L	20-pin173-mil TSSOP	Industrial
PI6C41204LIE	L	Pb-free & Green, 20-pin173-mil TSSOP	Industrial
PI6C41204AL	L	20-pin173-mil TSSOP	Commercial
PI6C41204ALE	L	Pb-free & Green, 20-pin173-mil TSSOP	Commercial

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

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