THE DATASHEET OF

PT8A2648PE

www.win-source.net 0086-755-83957316

PIR Sensor Light Switch

Product Features

- Operating voltage: 5V (Typ.)
- Average supply current: 120μA (Typ.)
- 2 stage op-amp for filter.
- Build-in noise rejection circuit.
- On-chip regulator.
- Adjustable output duration
- Override function.
- ON/AUTO/OFF selectable by MODE pin
- Apply to AC 220V/50Hz and 110V/60Hz.
- Auto-reset if the ZC signal disappears over 3 seconds
- Output pulse (PT8A2641/5/7) to drive triac or output level (PT8A2642/6/8) to drive relay.
- CDS to enable/disable output.
- 40 second warm-up.
- Quick check mode for installation.

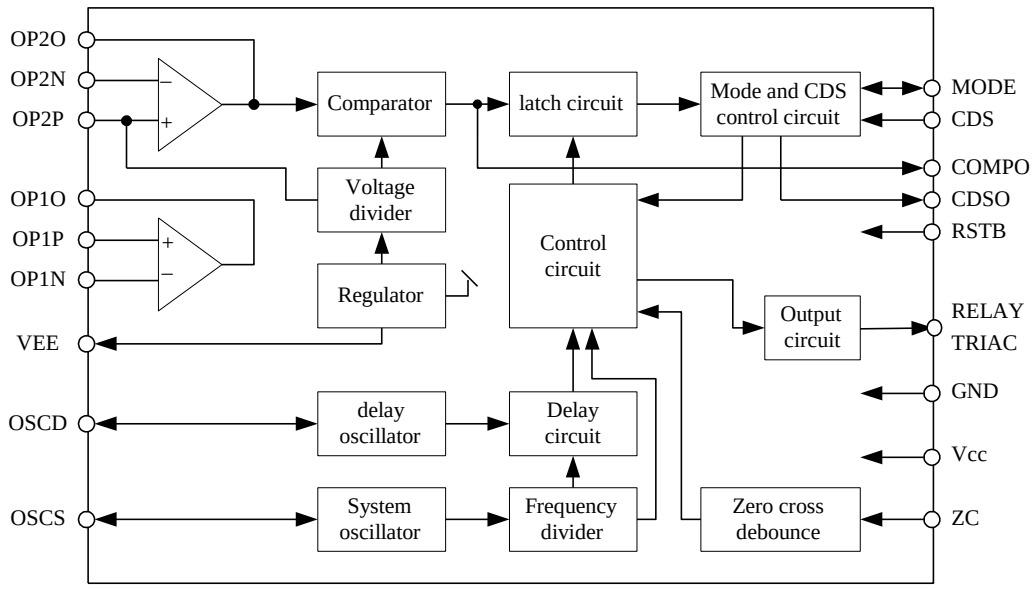
Product Description

The PT8A264X is a CMOS LSI chip designed for use in automatic PIR lamp control. It can operate with a 2-wire configuration for triac applications or with a 3-wire configuration for relay applications. The chip is equipped with operational amplifiers, a comparator, timer, a zero crossing detector, control circuit, a voltage regulator, a system oscillator, and an output timing oscillator.

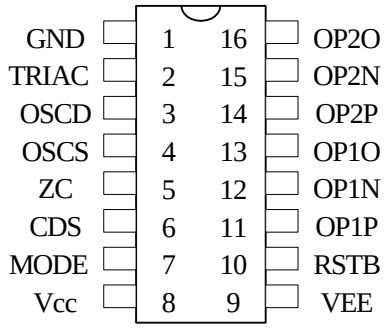
Its PIR sensor detects infrared power variations induced by the motion of a human body and transforms it to a voltage variation. If the PIR output voltage variation conforms to the criteria (refer to the functional description), the lamp is turned on with an adjustable duration. The PT8A264X offers three operating modes (ON, AUTO, OFF) which can be set through the MODE pin. While the chip is working in the AUTO mode the user can override it and switch to the quickly install mode, or manual ON mode, or return to the AUTO mode by switching the power switch.

Block Diagram

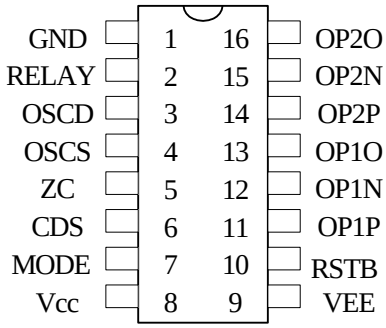
Figure 1 Block Diagram



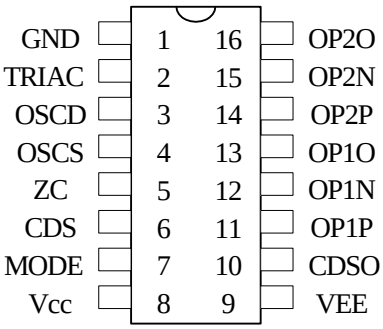
Pin Configuration



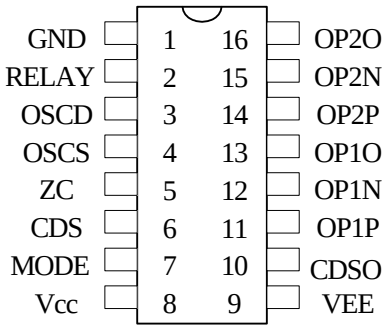
PT8A2641P/2641W



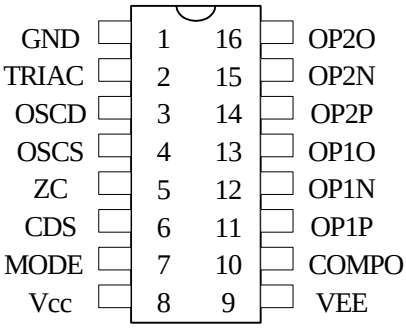
PT8A2642P/2642W



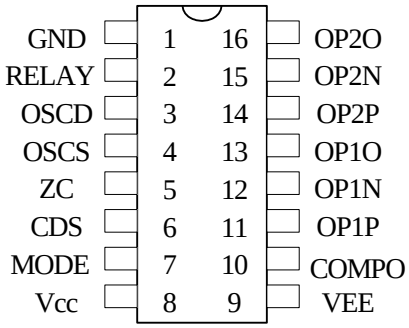
PT8A2645P/2645W



PT8A2646P/2646W



PT8A2647P/2647W



PT8A2648P/2648W

Pin Description

Part number						Pin name	I/O	Description
2641	2642	2645	2646	2647	2648			
1	1	1	1	1	1	GND	I	Ground
-	2	-	2	-	2	RELAY	O	RELAY drive output through an external NPN transistor, active high
2	-	2	-	2	-	TRIAC	O	TRIAC drive to output two negative pulses, active negative pulse.
3	3	3	3	3	3	OSCD	I/O	Output timing oscillator I/O It is connected to an external RC to adjust output duration.
4	4	4	4	4	4	OSCS	I/O	System oscillator I/O OSCS is connected to an external RC to set the system frequency. The system frequency =16KHz for normal application.
5	5	5	5	5	5	ZC	I	Schmitt input for AC zero crossing detection
6	6	6	6	6	6	CDS	I	CDS is connected to a CDS voltage divider for daytime/night auto-detection. Low input to this pin can disable the PIR input. CDS is a schmitt trigger input with 5-second input debounce time.
7	7	7	7	7	7	MODE	I/O	Operating mode selection input: V_{CC}: TRIAC/RELAY is always ON GND: TRIAC/RELAY is always OFF Open: Auto detection, outputs 31.25Hz square wave
8	8	8	8	8	8	Vcc	I	Positive power supply
9	9	9	9	9	9	VEE	O	Regulated voltage output The output voltage is about 3.6V with respect to GND.
10	10	-	-	-	-	RSTB	I	Chip reset input, active low
-	-	10	10	-	-	CDSO		CDS control circuit output signal, active high
-	-	-	-	10	10	COMPO		output of comparator, active high
11	11	11	11	11	11	OP1P	I	Noninverting input of OP1
12	12	12	12	12	12	OP1N	I	Inverting input of OP1
13	13	13	13	13	13	OP1O	O	Output of OP1
14	14	14	14	14	14	OP2P	I	Noninverting input of OP2, internal 1.8V default.
15	15	15	15	15	15	OP2N	I	Inverting input of OP2
16	16	16	16	16	16	OP2O	O	Output of OP2

Note: The active output width of COMPO is inversely proportional to the system frequency.

Maximum Ratings

Storage temperature	-40℃ to +125℃
Supply Voltage to Grourd Potential (Input & V_{CC} Only)	-GND -0.5V to Vcc+0.5V
Supply Voltage to Grourd Potential (output & D/O Only)	GND -0.5V to Vcc+0.5V
DC Input Voltage	-0.5V to + 6.0V
DC Output Current	20mA
Power Dissipation	500mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{CC}	Condition				
V_{CC}	Operating Voltage	-	-	4.75	5.0	6.0	V
V_{IH}	"H" Input Voltage	-	-	0.8	-	-	V_{CC}
V_{IL}	"L" Input Voltage	-	-	-	-	0.2	V_{CC}
F_{SYS}	System Oscillator Frequency	5V	ROSCS=430K COSCS=180P	12.8	16	19.2	KHz
T_A	Operating temperature	-	-	-20	25	70	℃

Electrical Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{CC}	Condition				
VTH1	CDS "H" Transfer Voltage	5V		3.0	3.3	3.6	V
VTL1	CDS "L" Transfer Voltage	5V		0.9	1.2	1.5	V
VTH2	ZC "H" Transfer Voltage	5V		2.6	2.9	3.2	V
VTL2	ZC "L" Transfer Voltage	5V		1.1	1.4	1.7	V
VTH3	OSCS "H" Transfer Voltage	5V		2.7	3	3.3	V
VTL3	OSCS "L" Transfer Voltage	5V		0.8	1	1.2	V
VTH4	OSCD "H" Transfer Voltage	5V		2.7	3	3.3	V
VTL4	OSCD "L" Transfer Voltage	5V		0.8	1	1.2	V
I_{IH}	High level leakage current (ZC,CDS)	5V	V_{IH}=4.5V	-1	-	1	μA
I_{IL}	Low level leakage current (ZC,CDS)	5V	V_{IL}=0.5V	-1	-	1	μA
I_{IHRSTB}	RSTB Input high level current	5V	V_{IH}=4.5V	-1	-	-5	μA
IOH	Output source current(RELAY, TRIAC)	5V	VOH=4.5V	–6	-	-	mA
IOL	Output sink current(RELAY, TRIAC)	5V	VOL=0.5V	15	-	-	mA
IOH	Output source Current(CDSO,COMPO)	5V	VOH=4.5V	–5	-	-	mA
IOL	Output sink current(CDSO,COMPO)	5V	VOL=0.5V	5	-	-	mA

Voltage regulation circuit

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{CC}	Condition				
VEE	Regulator Output Voltage	5V	No load	3.24	3.6	3.96	V
OP2P	Noninverting input of OP2	5V	No load	1.62	1.8	1.98	V
ΔV_O	Line regulation	-	$4.5 \le V_{CC} \le 5.5V$, I_L =1mA	-	30	50	mV
ΔV_{LDR}	Load regulation	5V	$0.5mA \le I_L \le 2mA$	-	60	100	mV

Operational amplifier and windows comparator

Symbol	Description	Test condition	Min	TYP	Max	Unit
BW	3dB band width	-	10	-	-	KHz
V_H	Threshold of windows comparator	V_{CC}=5V	1.8	2.0	2.2	V
V_L		V_{CC}=5V	1.35	1.5	1.65	V

Frequency of oscillator and Timing of ZC and trigger output

Symbol	Description	Test condition	Min	Typ	Max	Unit
F_{MODE}	Oscillator frequency/512	V_{CC}=5V, RS=430KΩ ,CS=180P (PT8A264X)	25	31.25	37.5	Hz
T_{DZT}	Delay time from ZC to TRIAC		1.16	1.45	1.74	ms
T_{TPW}	TRIAC Pulse Width		50	62.5	75	μs
T_{DZR}	Delay time from ZC rising edge to Relay		-	125	200	μs

Power Dissipation

Symbol	Description	Test condition	Min	Typ	Max	Unit
I_{CC}	Power supply current	V_{CC}=5V, R_S=430KΩ ,C_S=180P, R_D =2MΩ, C_D=104, other Input Pins=GND, all outputs float.	-	120	200	μA

Functional Description

VEE: supplies power to the analog front end circuit, it is about a stable 3.6V with respect to GND normally.

OSCS: a system oscillator input pin. System frequency of 16KHz can be generated when connecting to an external RC shows as figure 2 (R=430K, C=180pf).

Figure 2 System oscillator

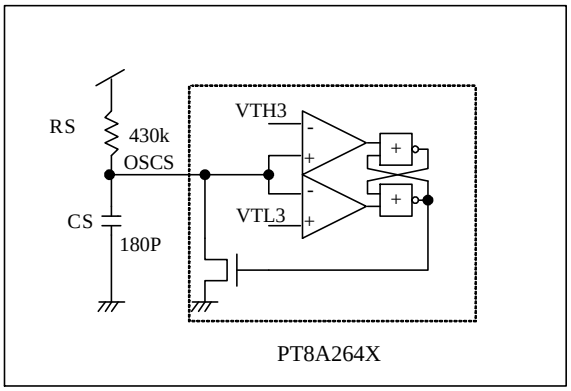
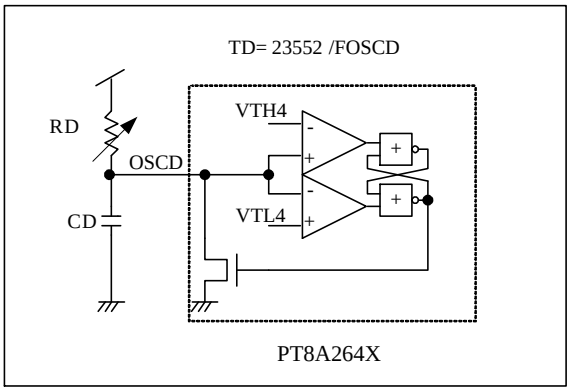


Figure 3 Output timing oscillator



OSCD: input pin of timing oscillator. It's connected to an external RC to obtain the desired output timer. Variable output turn-on duration can be achieved by selecting various values of RC or using a variable resistor, see figure 3.

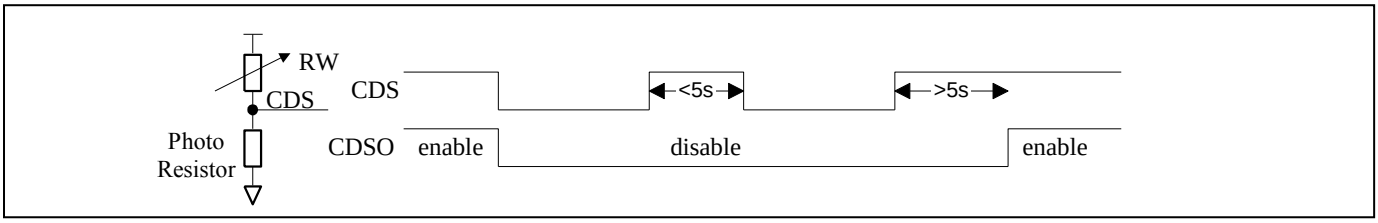
Note: The minimum resistor should be low enough to 2K in order to provide adjustable range about 1000 times between min and max timer (The maximum resistor is 3M). It is recommended that CD is more than 103 in order to guarantee not too bad linearity.

RELAY (TRIAC): an output pin set as a RELAY driving (active high) output for the PT8A2642/6/8, or as a TRIAC driving (active low) output for the PT8A2641/5/7. The output active duration is controlled by the OSCD oscillating period.

CDS and CDSO: CDS has a schmitt trigger input structure. It is used to distinguish lighteness. With a resistor divider including a CDS component, if light is weak enough, CDS is high the PIR input is active. Oppositely, the CDSO will be inactive when CDS is low. The input debounce time from inactive to active is 5 seconds. CDS should be pulled high without using this function. The input of CDS will be ignored once the output is active.

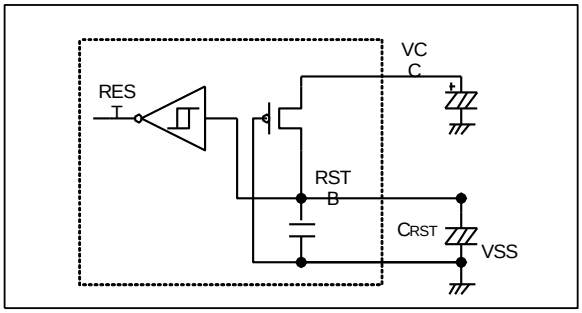
CDS	Status	CDSO
LOW	Day Time	inactive
HIGH	Night	active

Figure 4 CDS input interface and enable debounce



RSTB: used to reset the chip. It is internal pull-high and active low. The use of CRST can extend the power-on initial time. If the RSTB pin is an open circuit (without CRST), the initial time is the default (40 secs).

Figure 5 RSTB application example



Power on initial: Because the band-pass filter and amplifier require a warm up period to reach a stable state after power-on so any inputs should be ignored during this period.

In the AUTO mode within the first 10 seconds of power-on initialization, the system allows override control to access the quickly install mode. However, after 40 seconds of the initial time the system allows override control between ON and AUTO. It will remain in the warm up period if the total initial time has not elapsed after returning to AUTO.

In case that the ZC signal disappears more than 3 seconds, the chip will restart the initialization operation. However, the restart initial time is always 40 seconds and cannot be extended by adding CRST to the RSTB pin as shown in Fig.5.

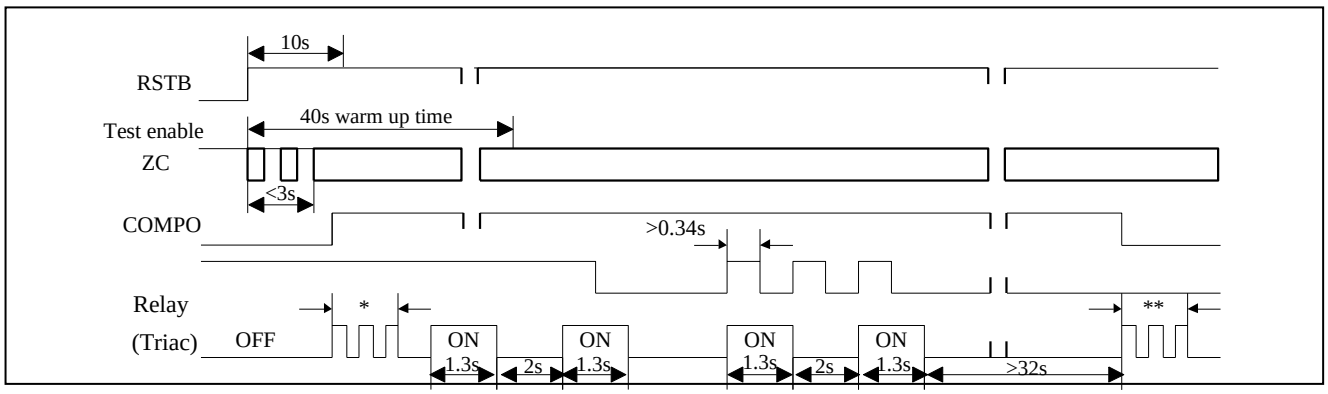
MODE: a tri-state input pin used to select the operating mode.

MODE	Operating Mode	Description
VCC	Output always ON	RELAY outputs high at ZC rising edge TRIAC outputs negative pulse train with synchronizing to ZC
GND	Output always OFF	RELAY outputs low TRIAC outputs high
Open	AUTO	Outputs remain off state until activated by a valid PIR trigger signal. When working in the AUTO mode, the chip allows override control by switching the ZC signal. MODE outputs square wave with frequency of 31.25Hz.

ZC: a CMOS input structure. It receives AC line frequency and generates zero crossing pulses to synchronize the triac/relay driver. With an effective ZC signal switching (switch OFF/ON 2 times within 3 seconds), the system provides the following additional functions:

Quickly install mode: Within 10 seconds after power-on, effective ZC switching will force the chip to enter the quickly install mode. During the mode, the outputs will be active for a duration of 1.3 seconds each time a valid PIR trigger signal is received. If a time interval exceeds 32 seconds without a valid trigger input, the chip will enter the AUTO mode automatically.

Figure 6 Test mode



*&**:flash 3 times at 2Hz rate for 2641/5/7;for 2642/6/8,No flash

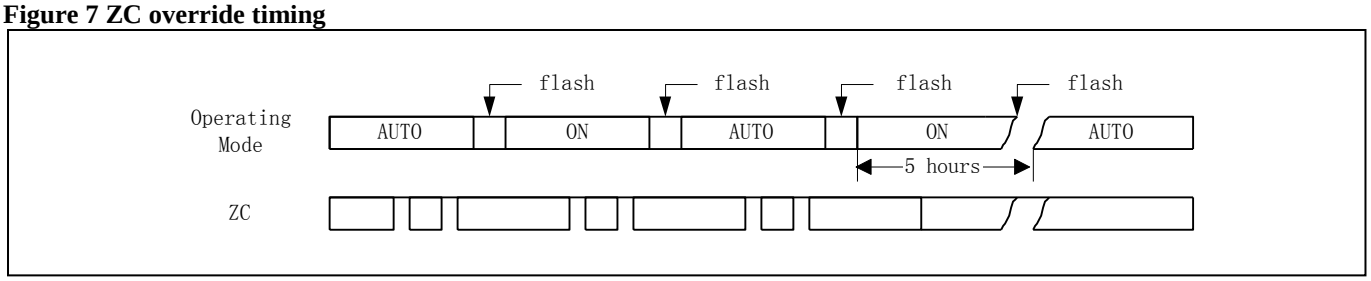
Override control: When the chip is working in the AUTO mode (MODE= open), the output is activated by a valid PIR trigger signal and the active output duration is controlled by the OSCD oscillating period. The lamp can be switched always to "ON" from the AUTO mode by either switching the MODE pin to VCC or switching the ZC signal by an OFF/ON operation of the power switch (OFF/ON twice within 3 seconds). The term "override" refers to the change of operating mode by switching the power switch. The chip can be toggled from ON to AUTO by an override operation. Shows as figure 7.

If the chip is overridden to ON and there is no further override operation, it will return to AUTO automatically after an internal preset ON time duration has elapsed. This override ON time duration is set to 5 hours, refer to fig 7.

The PT8A2641/5/7 will flash on output pin when changing the operating mode. It will flash 3 times at a 1Hz rate each time the chip changes from the AUTO mode to another mode or flash 3 times at a 2Hz rate when returning to the AUTO mode. But
PT8A2642//6/8 does no flash at the same condition.

However, if the AUTO mode is changed by switching the MODE switch output will not flash.

Figure 7 ZC override timing

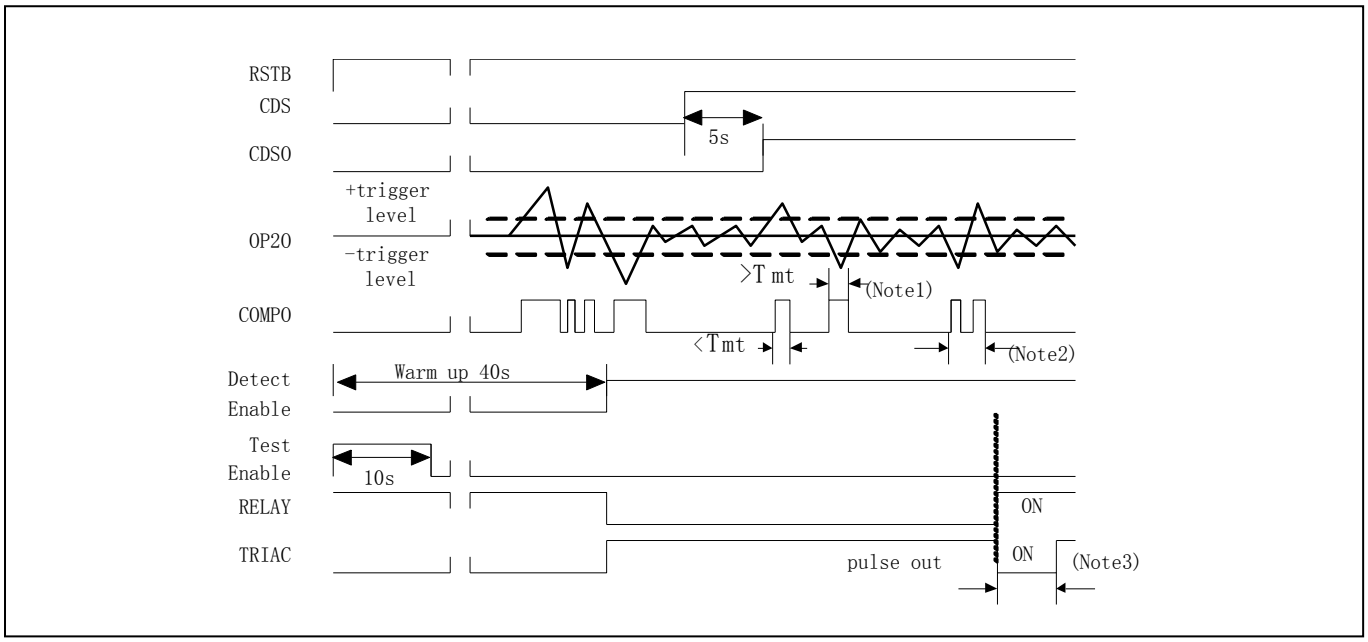


Any operations during flash period are inactive, the flash period is about 3s from AUTO to ON, 3s from ON to AUTO.

COMPO: COMPO is output from comparator, it can be output at pin 10 if needed. Signal from two-stage opamp outputs to a window comparator as pre-operation, COMPO outputs active positive pulses with various width once signal beyond window level. Whether an active PIR signal is detected, see trigger timming diagram below for detail.

Trigger timing

Figure 8 Trigger timing



Note: 1. One measurable trigger width (Tmt) from comparator output is 24ms~ 32ms which varies with frequency of system oscillator (typical system frequency=16KHz).

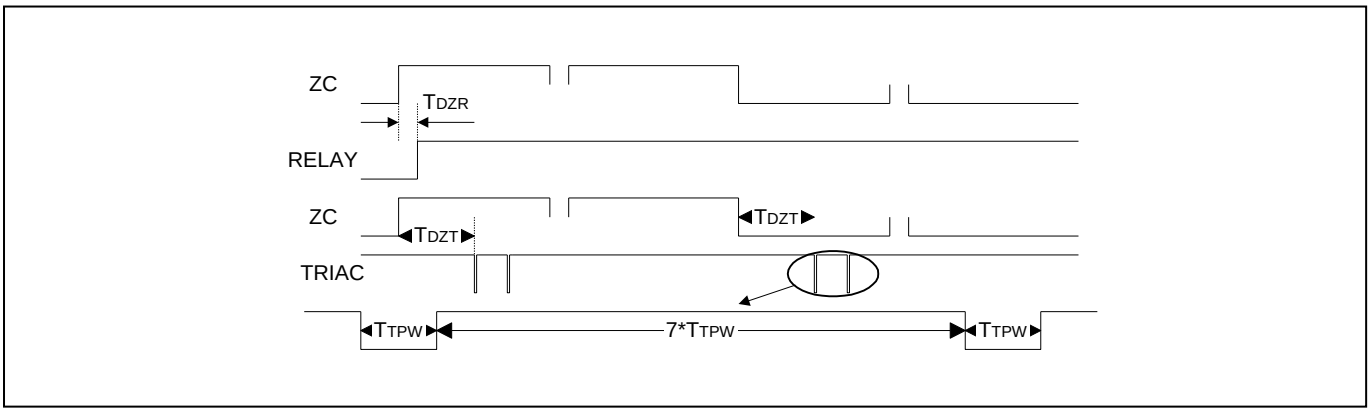
2. The output is activated if the trigger signal conforms to the following criteria:
   - A trigger signal sustain duration:0.34 seconds.
   - 2 trigger signals within 2 seconds with one of the trigger signal sustain:0.16 seconds.
   - More than 3 measurable triggers within 2 seconds.

3. The output duration is set by an external RC that is connected to the OSCD pin.

Retrigger

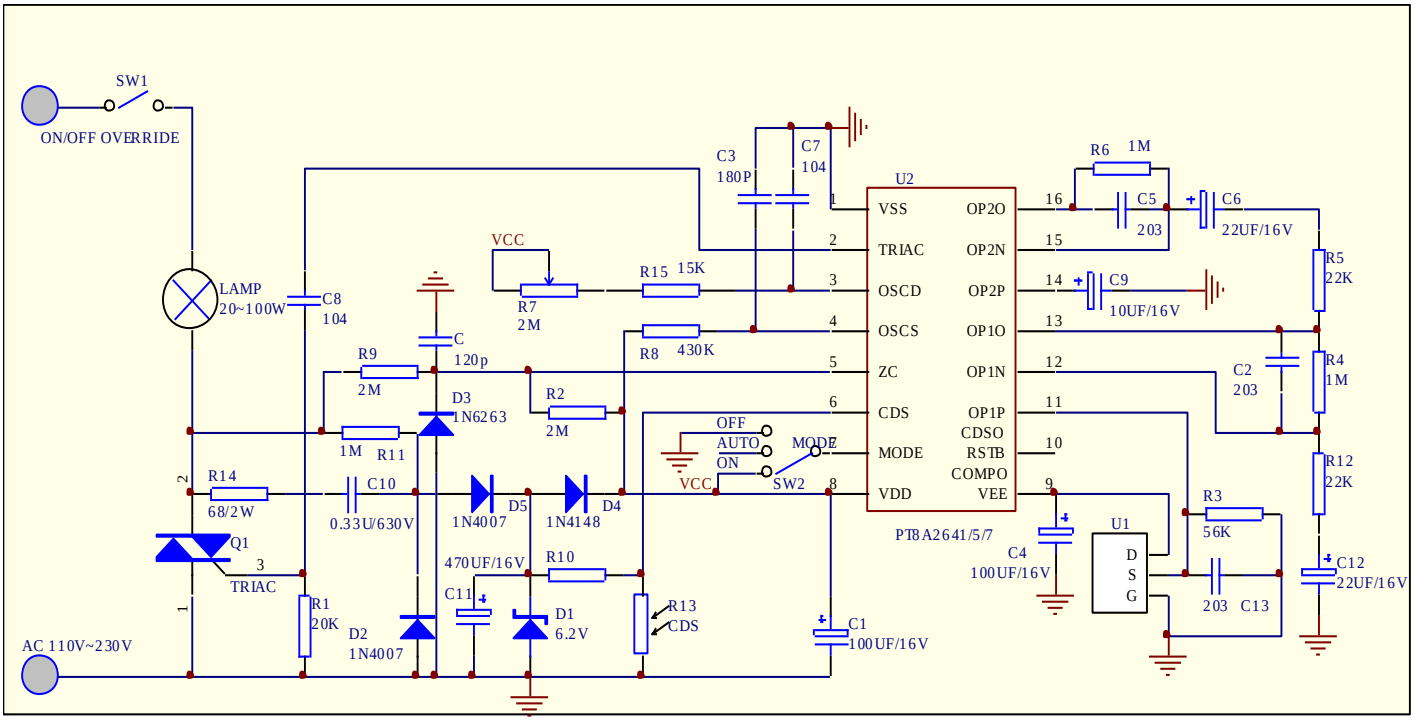
If another signal is attained in trigger hold time, the circuit will be retriggered, and the trigger hold time will be started from this time.

Timing Diagram



Application Circuits

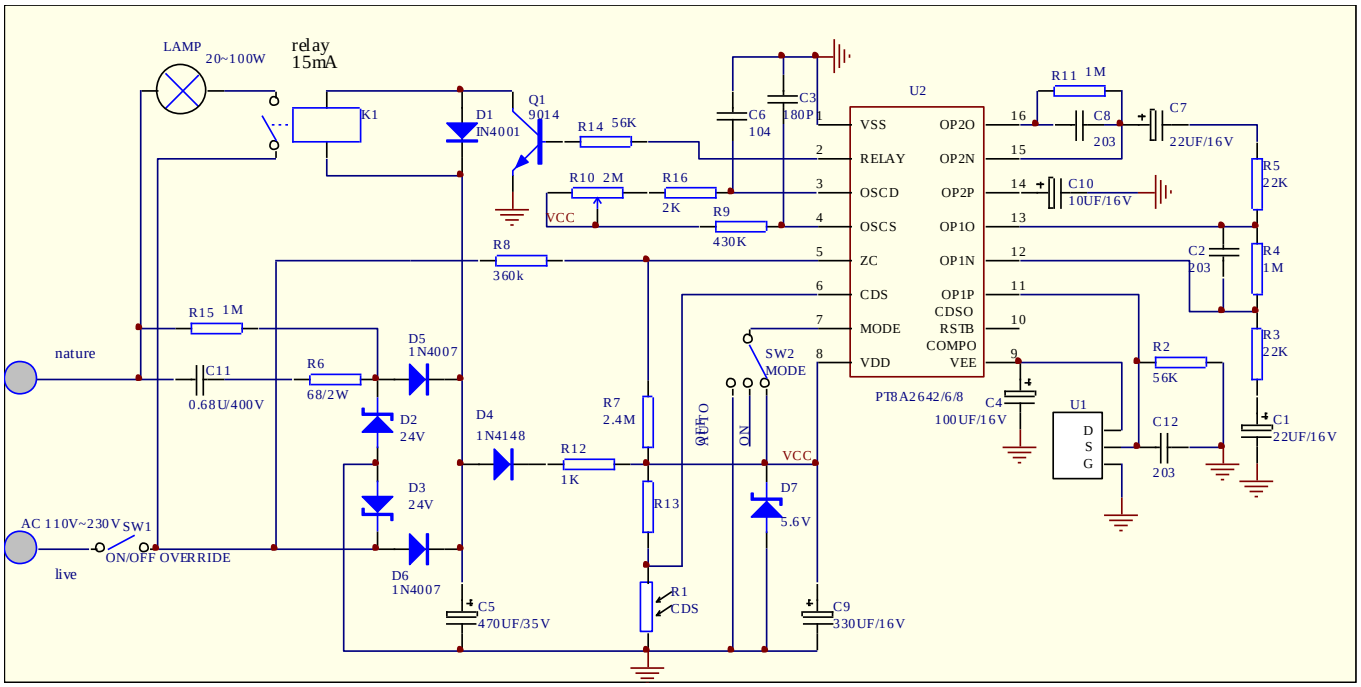
Typical application circuit of two wires PIR detector



Note:

1. Adjust R10 to fit various CDS.
2. Change C7 to obtain the desired adjusting range of output duration.
3. Change the value of C10 to 0.22uf/630V for AC 220V application.

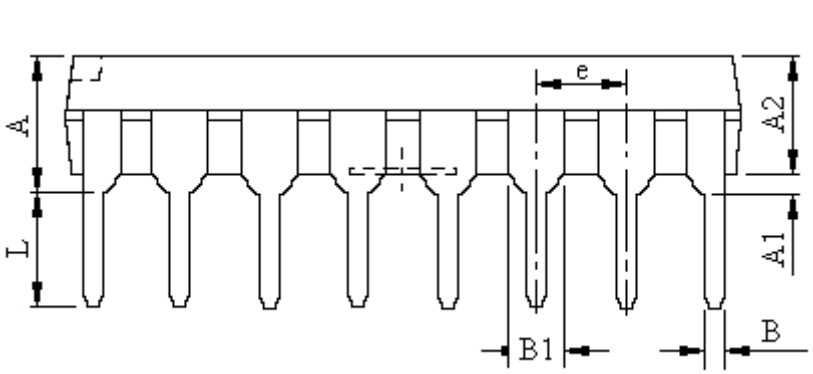
Typical application circuit of three wires PIR detector

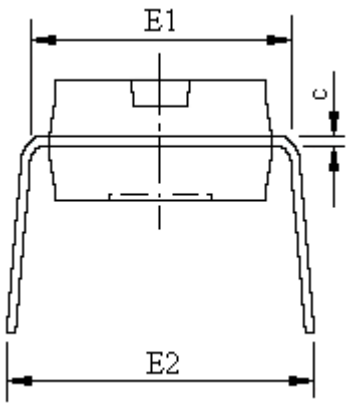


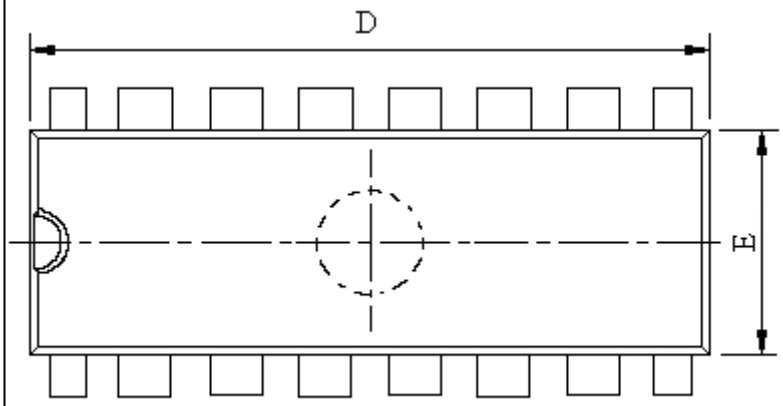
Note: 1.Adjust R13 to fit various CDS.
2.Change C6 to obtain the desired adjusting range of output duration.
3. RSTB pin need a capacitance 104 for PT8A2642 application

Mechanical Information

16-Pin DIP



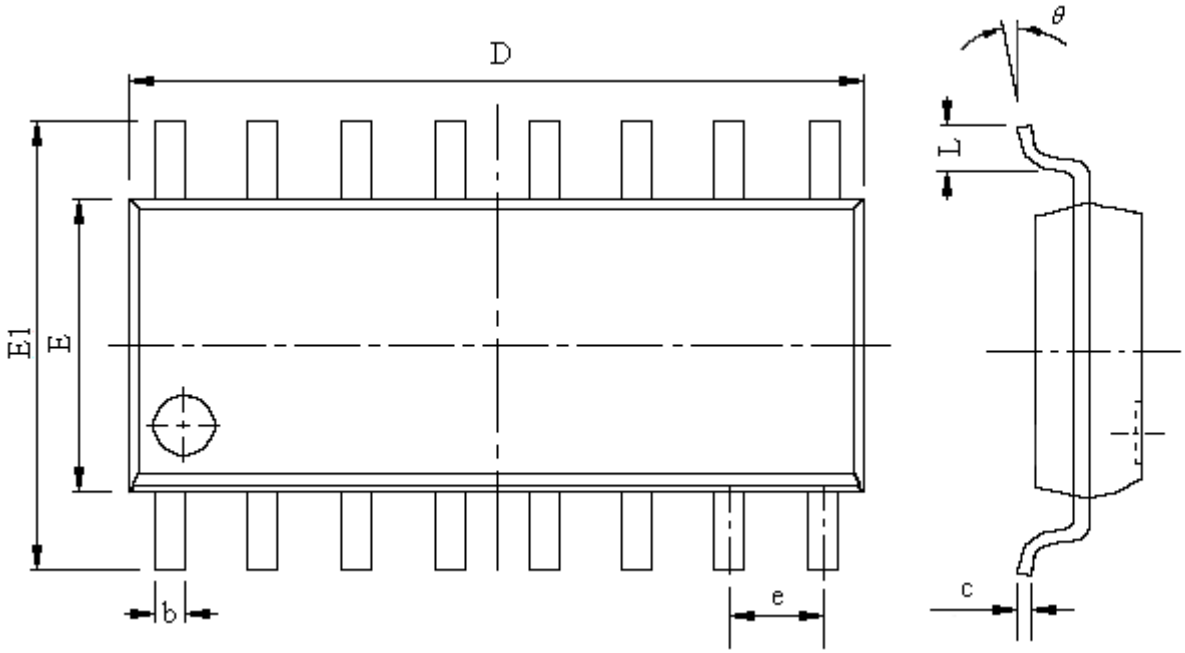


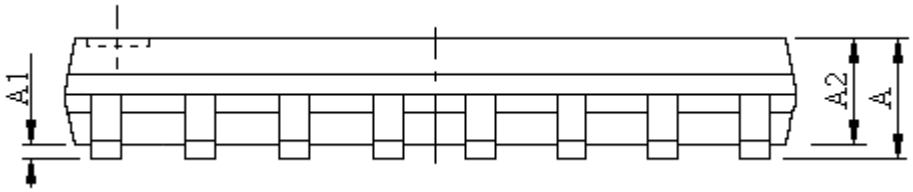


Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-001D/BB

PKG.	DIMENSIONS(MM)	
SYMBOL	Min	Max
A	3.71	4.31
A1	0.51	
A2	3.20	3.60
B	0.38	0.57
B1	1.52 BSC	
c	0.20	0.36
D	18.80	19.20
E	6.20	6.60
E1	7.32	7.92
e	2.54 BSC	
L	3.00	3.60
E2	8.40	9.00

16-Pin SOIC





Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012E/AC

PKG. DIMENSIONS(MM)		
SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	9.80	10.20
E	3.80	4.00
E1	5.80	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

Ordering Information

Part Number	Package code	Package
PT8A2641PE	P	Lead free 16-Pin DIP
PT8A2641WE	W	Lead free 16-Pin SOIC
PT8A2642PE	P	Lead free 16-Pin DIP
PT8A2642WE	W	Lead free 16-Pin SOIC
PT8A2645PE*	P	Lead free 16-Pin DIP
PT8A2645WE*	W	Lead free 16-Pin SOIC
PT8A2646PE*	P	Lead free 16-Pin DIP
PT8A2646WE*	W	Lead free 16-Pin SOIC
PT8A2647PE*	P	Lead free 16-Pin DIP
PT8A2647WE*	W	Lead free 16-Pin SOIC
PT8A2648PE	P	Lead free 16-Pin DIP
PT8A2648WE	W	Lead free 16-Pin SOIC

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- *Contact Pericom for availability.

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