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FOD8001



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FAIRCHILD SEMICONDUCTOR®

December 2010

FOD8001
High Noise Immunity, 3.3V/5V Logic Gate Optocoupler

Features

- High Noise Immunity characterized by Common Mode Rejection (CMR) and Power Supply Rejection (PSR) specifications
  - 20kV/μs Minimum Static CMR @ Vcm = 1000V
  - 25kV/μs Typical Dynamic CMR @ Vcm = 1500V, 20MBaud Rate
  - PSR in excess of 10% of the supply voltages across full operating bandwidth
- High Speed:
  - 25Mbit/sec Date Rate (NRZ)
  - 40ns max. Propagation Delay
  - 6ns max. Pulse Width Distortion
  - 20ns max. Propagation Delay Skew
- 3.3V and 5V CMOS Compatibility
- Extended industrial temperate range, -40°C to 105°C temperature range
- Safety and regulatory pending approvals:
  - UL1577, 3750 VACRMS for 1 min.
  - IEC60747-5-2 (pending)

Applications

- Industrial fieldbus communications
  - Profibus, DeviceNet, CAN, RS485
- Programmable Logic Control
- Isolated Data Acquisition System

Description

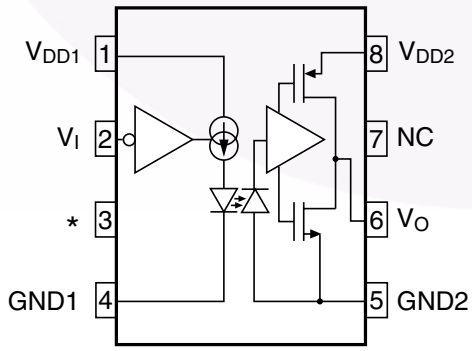
The FOD8001 is a 3.3V/5V high-speed logic gate Optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's proprietary coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection and power supply rejection specifications.

This high-speed logic gate optocoupler, packaged in a compact 8-pin small outline package, consists of a high-speed AlGaAs LED driven by a CMOS buffer IC coupled to a CMOS detector IC. The detector IC comprises an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled to the high efficiency of the LED achieves low power consumption as well as very high speed (40ns propagation delay, 6ns pulse width distortion).

Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/FO/FOD0721.html
- www.fairchildsemi.com/pf/FO/FOD0720.html
- www.fairchildsemi.com/pf/FO/FOD0710.html

Functional Schematic



*: Pin 3 must be left unconnected

Truth Table

V_I	LED	V_O
H	OFF	H
L	ON	L

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Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	V_{DD1}	Input Supply Voltage
2	V_I	Input Data
3		LED Anode – Must be left unconnected
4	GND1	Input Ground
5	GND2	Output Ground
6	V_O	Output Data
7	NC	Not Connected
8	V_{DD2}	Output Supply Voltage

Absolute Maximum Ratings (T_A = 25°C Unless otherwise specified.)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	°C
T_{OPR}	Operating Temperature	-40 to +105	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 sec	°C
V_{DD1}, V_{DD2}	Supply Voltage	0 to 6.0	V
V_I	Input Voltage	-0.5 to V_{DD1} + 0.5	V
I_I	Input DC Current	-10 to +10	µA
V_O	Output Voltage	-0.5 to V_{DD2} + 0.5	V
I_O	Average Output Current	10	mA
PD_I	Input Power Dissipation(1)(3)	90	mW
PD_O	Total Power Dissipation(2)(3)	70	mW

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+105	°C
V_{DD1}, V_{DD2}	Supply Voltages (3.3V Operation)(4)	3.0	3.6	V
	Supply Voltages (5.0V Operation)(4)	4.5	5.5	
V_{IH}	Logic High Input Voltage	2.0	V_{DD}	V
V_{IL}	Logic Low Input Voltage	0	0.8	V
t_r, t_f	Input Signal Rise and Fall Time		1.0	ms

Notes:

1. Derate linearly from 25°C at a rate of tbd W/°C
2. Derate linearly from 25°C at a rate of tbd mW/°C.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. 0.1µF bypass capacitor must be connected between Pin 1 and 4, and 5 and 8.

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Isolation Characteristics (Apply over all recommended conditions, typical value is measured at T_A = 25°C)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
V_{ISO}	Input-Output Isolation Voltage	f = 60Hz, t = 1.0 min, $I_{I-O} \le 10\mu A$ (5)(6)	3750	—	—	Vac_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500V (5)	10^{11}	—	—	Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0V, f = 1.0MHz (5)	—	0.2	—	pF

Notes:

5. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
6. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

Electrical Characteristics (Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3V, V_{DD1} = +3.3V and V_{DD2} = +5.0V, V_{DD1} = +5.0V and V_{DD2} = +3.3V, V_{DD1} = V_{DD2} = +5.0V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
INPUT CHARACTERISTICS						
I_{DD1L}	Logic Low Input Supply Current	V_I = 0V		6.2	10.0	mA
I_{DD1H}	Logic High Input Supply Current	V_I = V_{DD1}		0.8	3.0	mA
I_{IA}, I_{IB}	Input Current		-10		+10	μA
OUTPUT CHARACTERISTICS						
I_{DD2L}	Logic Low Output Supply Current	V_I = 0V		4.5	9.0	mA
I_{DD2H}	Logic High Output Supply Current	V_I = V_{DD1}		4.5	9.0	mA
V_{OH}	Logic High Output Voltage	I_O = -20μA, V_I = V_{IH}, V_{DD2} = +3.3V	2.9	3.3		V
		I_O = -4mA, V_I = V_{IH}, V_{DD2} = +3.3V	1.9	2.9		
		I_O = -20μA, V_I = V_{IH}, V_{DD2} = +5.0V	4.4	5.0		
		I_O = -4mA, V_I = V_{IH}, V_{DD2} = +5.0V	4.0	4.8		
VOL	Logic Low Output Voltage	I_O = 20μA, V_I = V_{IL}		0	0.1	V
		I_O = 4mA, V_I = V_{IL}		0.3	1.0	

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Switching Characteristics (Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3V, V_{DD1} = +3.3V and V_{DD2} = +5.0V, V_{DD1} = +5.0V and V_{DD2} = +3.3V, V_{DD1} = V_{DD2} = +5.0V, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic Low Output	C_L = 15pF		25	40	ns
t_{PLH}	Propagation Delay Time to Logic High Output	C_L = 15pF		25	40	ns
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PWD = 40ns, C_L = 15pF		2	6	ns
	Data Rate				25	Mb/s
t_{PSK}	Propagation Delay Skew	C_L = 15pF(7)			20	ns
t_R	Output Rise Time (10%–90%)			6.5		ns
t_F	Output Fall Time (90%–10%)			6.5		ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	V_I = V_{DD1}, V_O > 0.8 V_{DD1}, V_{CM} = 1000V(8)	20	40		kV/µs
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	V_I = 0V, V_O < 0.8V, V_{CM} = 1000V(8)	20	40		kV/µs
C_{PDI}	Input Dynamic Power Dissipation Capacitance(9)			30		pF
C_{PDO}	Output Dynamic Power Dissipation Capacitance(9)			3		pF

Notes:

7. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
8. Common mode transient immunity at output high is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, Vcm, to assure that the output will remain low.
9. Unloaded dynamic power dissipation is calculated as follows:

   C_{PD} x V_{DD} x *f* + I_{DD} + V_{PD} where *f* is switched time in MHz.

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Typical Performance Curves

Figure 1. Typical Output Voltage vs. Input Voltage

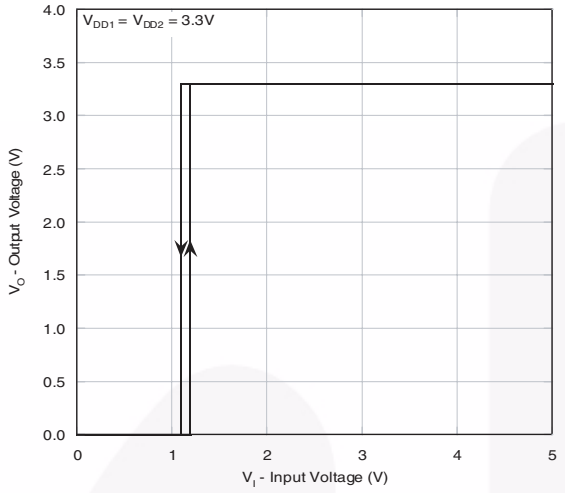


Figure 2. Input Voltage Switching Threshold vs. Input Supply Voltage

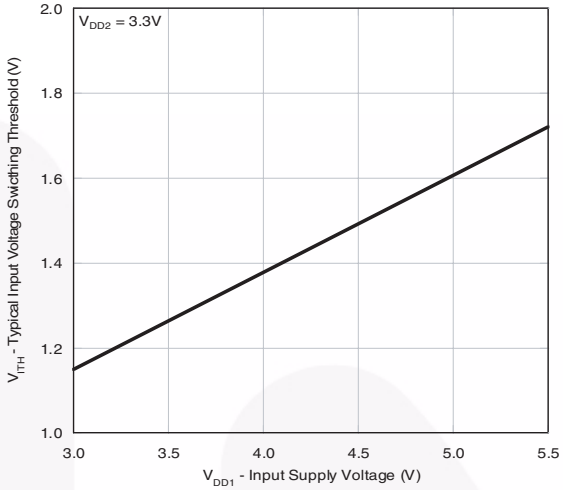


Figure 3. Propogation Delay vs. Ambient Temperature

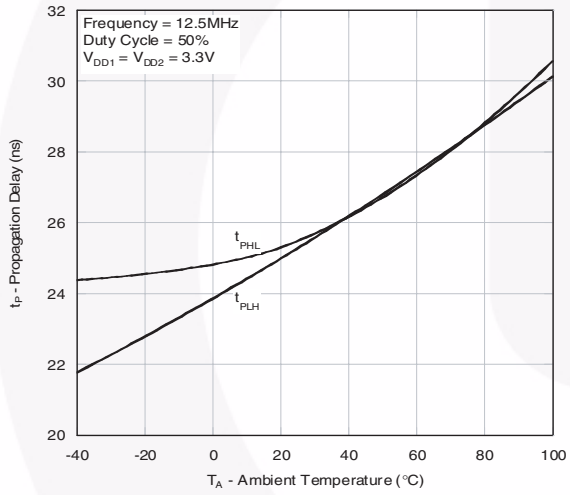


Figure 4. Pulse Width Distortion vs. Ambient Temperature

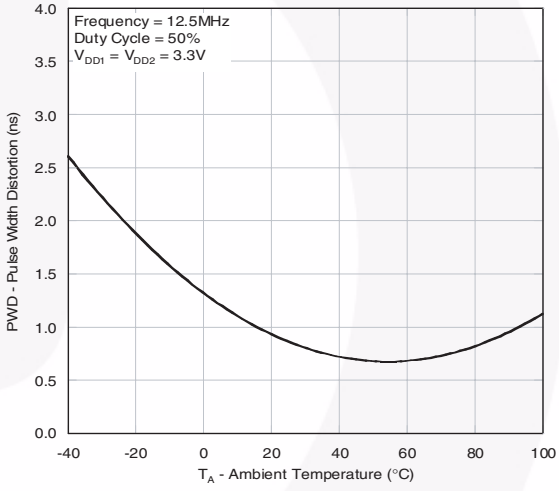


Figure 5. Typical Rise Time vs. Ambient Temperature

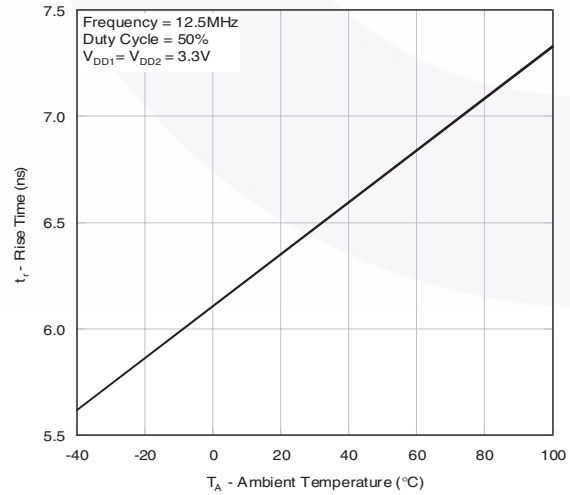
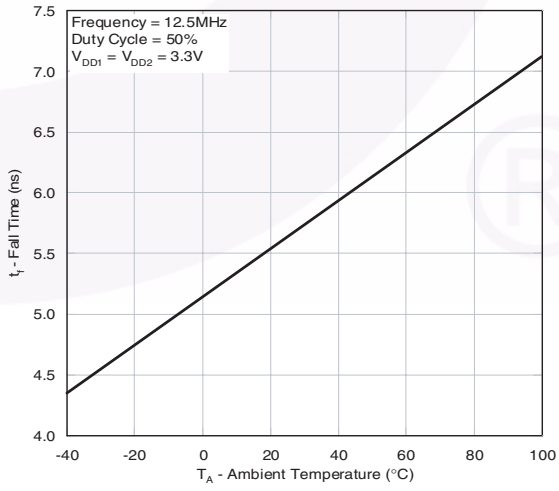


Figure 6. Typical Fall Time vs. Ambient Temperature



Typical Performance Curves (Continued)

Figure 7. Typical Propogation Delay vs. Output Load Capacitance

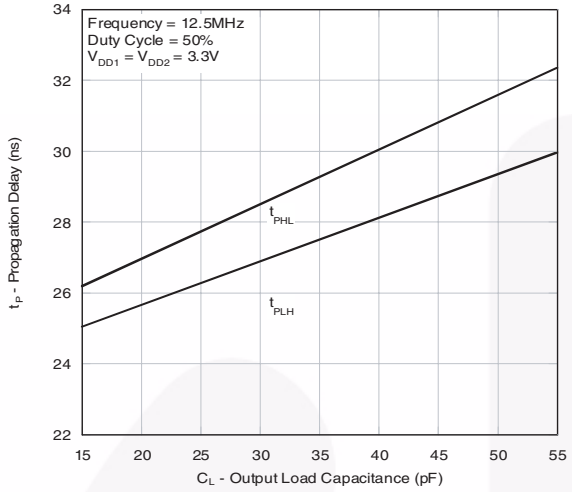


Figure 8. Typical Width Distortion vs. Output Load Capacitance

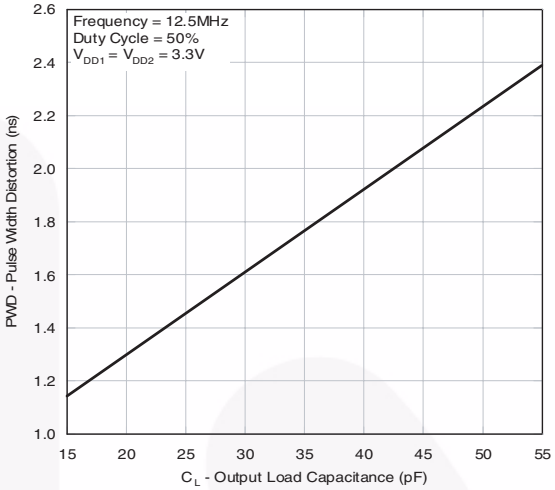


Figure 9. Typical Rise Time vs. Output Load Capacitance

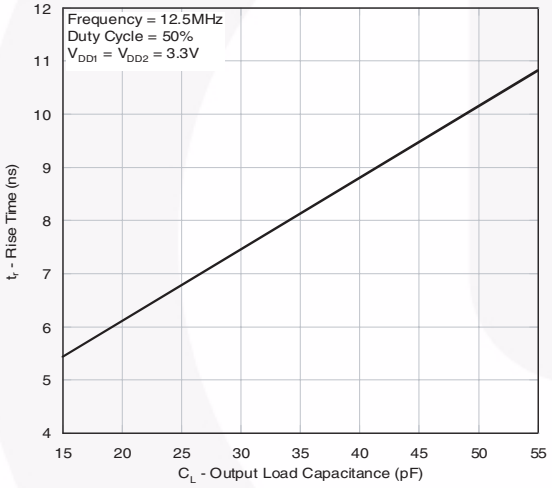


Figure 10. Typical Fall Time vs. Output Load Capacitance

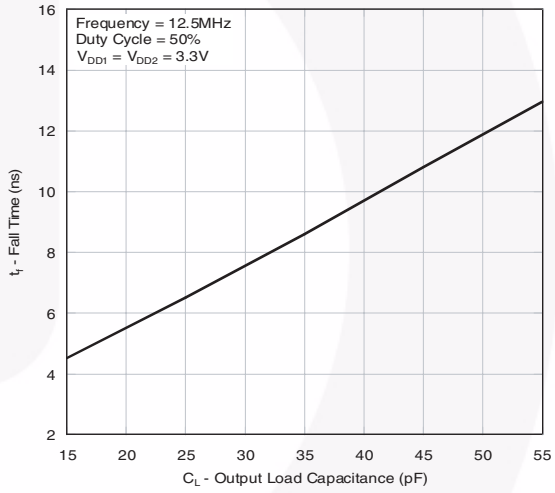


Figure 11. Input Supply Current vs. Frequency

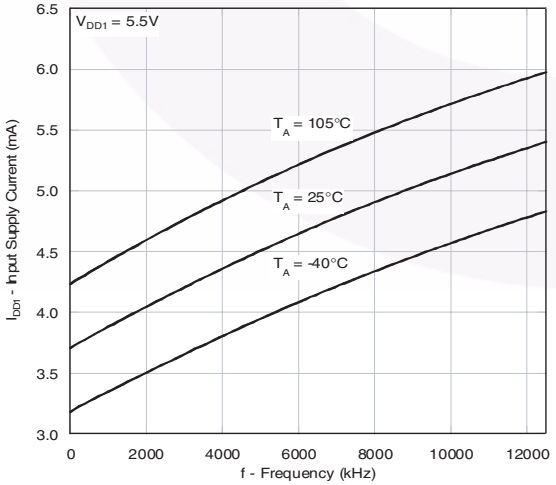
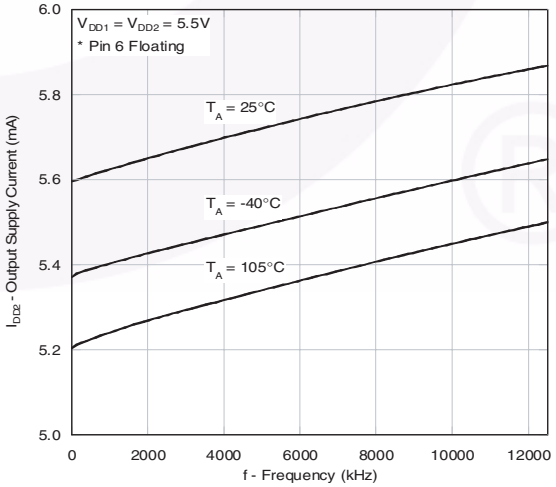


Figure 12. Output Supply Current vs. Frequency



Test Circuits

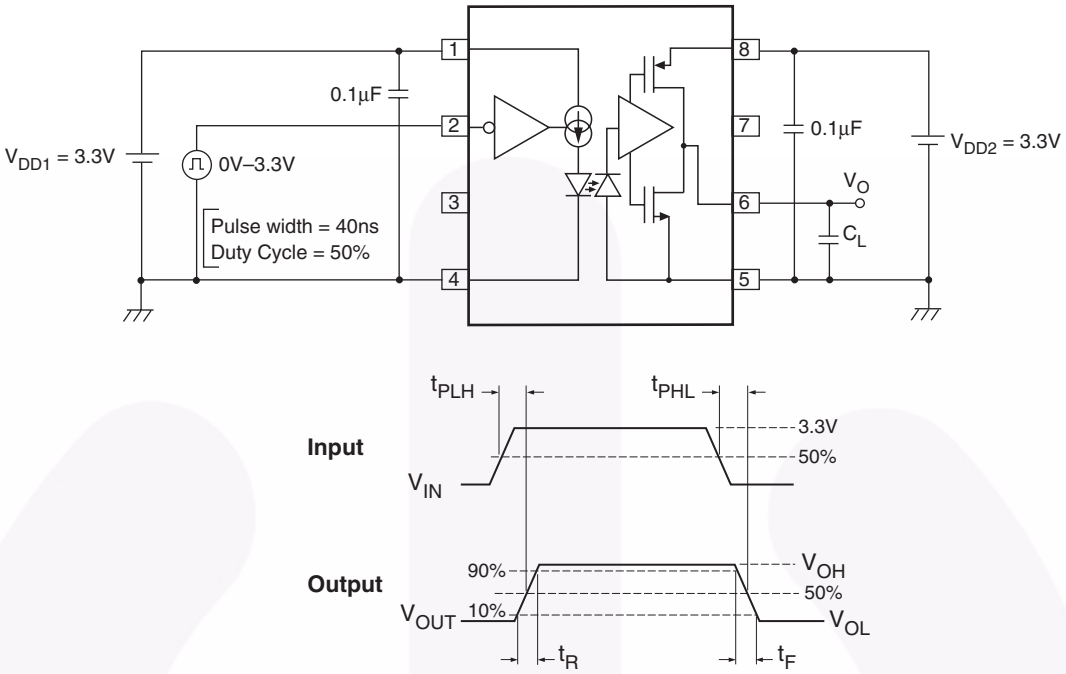


Figure 13. Test Circuit for Propogation Delay Time and Rise Time, Fall Time

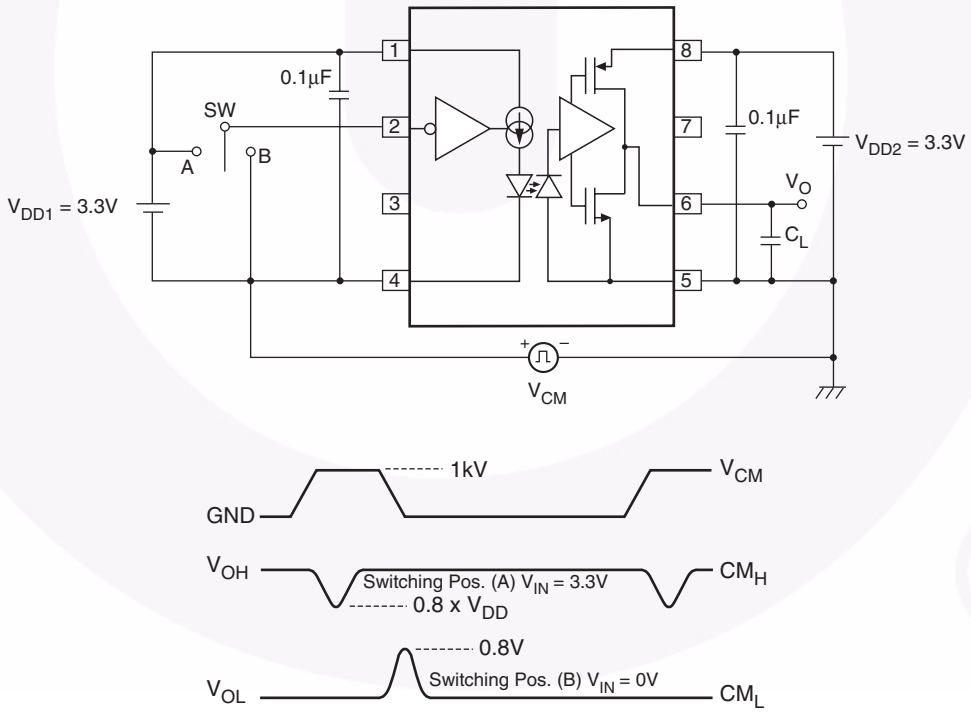


Figure 14. Test Circuit for Instantaneous Common Mode Rejection Voltage

Application Information

Noise is defined as any unwanted signal that degrades or interferes with the operation of a system or circuit. Input-output noise rejection is a key characteristic of an optocoupler, and the performance specification for this noise rejection is called, “Common Mode Transient Immunity or Common Mode Rejection, CMR”. The CMR test configuration is presented in high speed optocoupler datasheets, which tests the optocoupler to a specified rate of interfering signal (dv/dt), at a specified peak voltage (Vcm).

This defined noise signal is applied to the test device while the coupler is a stable logic high or logic low state. This test procedure evaluates the interface device in a constant or static logic state. This type of CMR can be referred to as “**Static CMR**”. Fairchild’s high speed optocouplers, which use an optically transparent, electrically conductive shield, and offer active totem pole logic output have static CMR in excess of 50KV/us at peak amplitudes of 1.5kV to 2.0kV.

Dynamic Common Mode Rejection

The noise susceptibility of an interface while it is actively transferring data is a common requirement in serial data communication. However, the static CMR specification is not adequate in quantifying the electrical noise susceptibility for optocouplers used in isolating high speed data transfer.

A serial data communication network’s noise performance is usually quantified as the number of bit errors per second or as a ratio of the number of bits transmitted in a specified time frame. This describes Bit Error Rate, BER. Test equipment that evaluates BER is called a Bit Error Rate Tester, BERT. When a BERT system is combined with a CMR tester, the active or dynamic noise rejection of an isolated interface can then be quantified. This type of CMR is thus defined as “**Dynamic CMR**”. Therefore, evaluating the common mode rejection while the optocoupler is switching at high speed represents a realistic approach to understand noise interference.

Test circuit functions were built to interface a commercial pseudo-random bit sequence (PRBS) generator and error detector with a pair of high speed optocouplers, FOD8001, connected in a loop-back configuration. With a 10MBaud PRBS serial data stream, no error was detected until the common mode voltage rose above 2.5kV with a dv/dt of 45kV/us. And increasing the data rate beyond 10Mbaud, the test was conducted at 20MBaud, and no error was detected at dv/dt of 25kV/us at common mode voltage of 1.5kV.

The test data for the dynamic CMR is comparable or better than the static CMR specifications found in the datasheet. These excellent noise rejection performances are results of the innovative circuit design and the proprietary coplanar assembly process.

Power Supply Noise Rejection

High levels of electrical noise can cause the optocoupler to register the incorrect logic state. The most commonly discussed noise signal is the common mode noise found between the input and output of the optocoupler. However, common mode noise is not the only path of noise into the input or output of the optocoupler. Due to the high gain and wide bandwidth of the transimpedance amplifier used for the photo detector circuits, power supply noise can cause the optocoupler to change state independent of the LED operation. Power supply noise is typically characterized as either random or periodic pulses with varying amplitudes and rates of rise and fall. The necessary tests have been conducted to understand the influence of the power supply noise and its effect of the proper operation of the FOD8001. The optocoupler under test offered power supply noise rejection in excess of 10% of the supply voltage for a frequency ranging from 100kHz to 35MHz, for logic high and logic low states.

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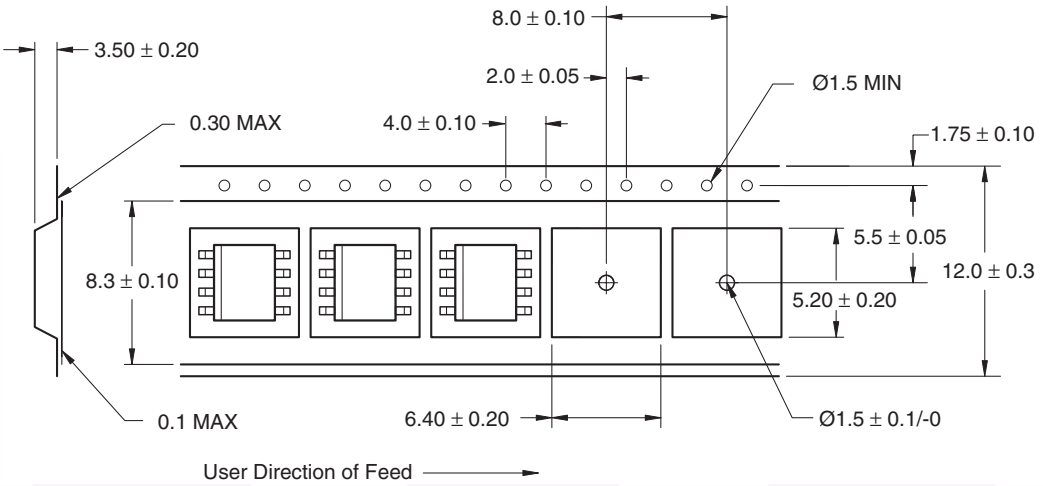
Carrier Tape Specification



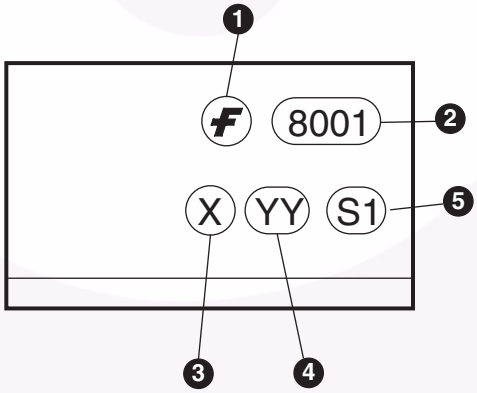
Note:
All dimensions are in millimeters.

Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FOD8001	Small outline 8-pin, shipped in tubes (50 units per tube)
R2	FOD8001R2	Small outline 8-pin, tape and reel (2,500 units per reel)

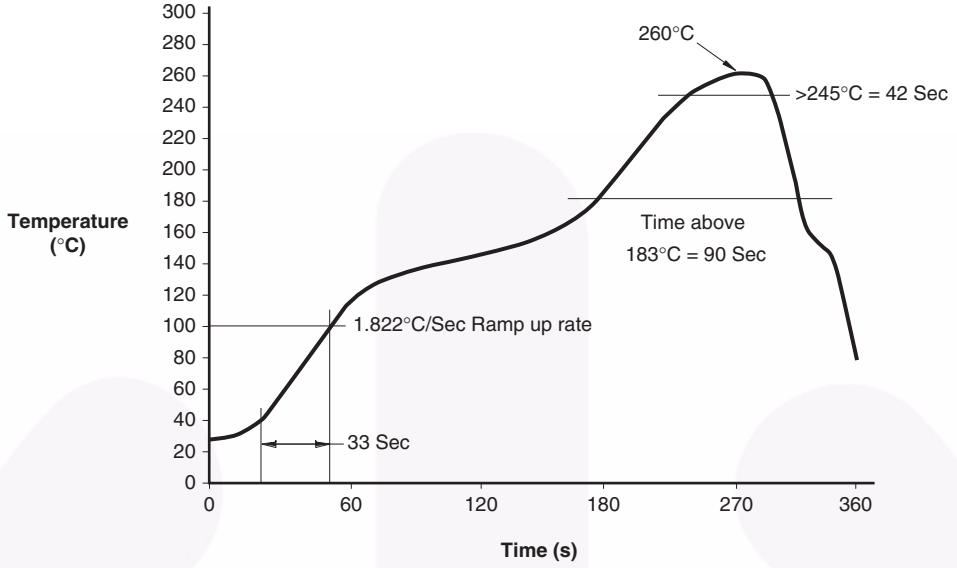
All packages are lead free per JEDEC: J-STD-020B standard.

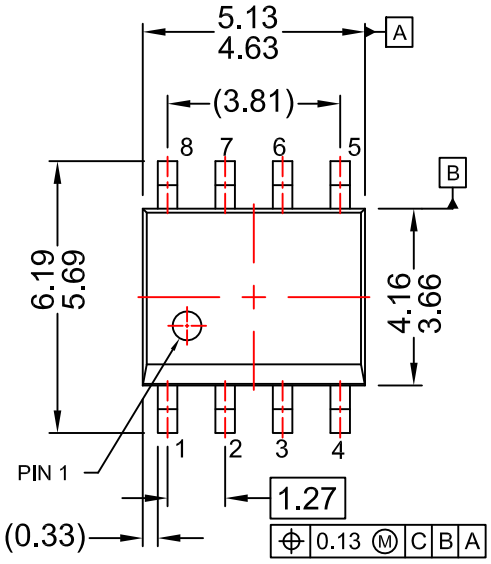
Marking Information

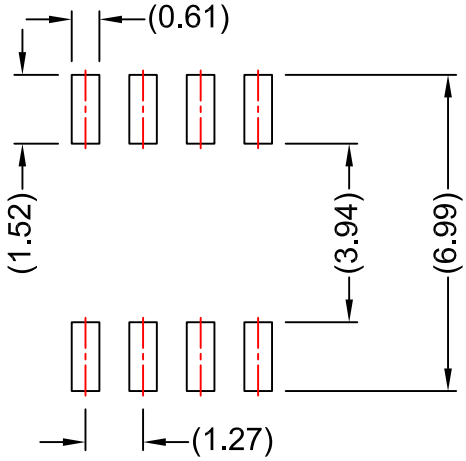


Definitions	
1	Fairchild logo
2	Device number
3	One digit year code, e.g., ‘8’
4	Two digit work week ranging from ‘01’ to ‘53’
5	Assembly package code

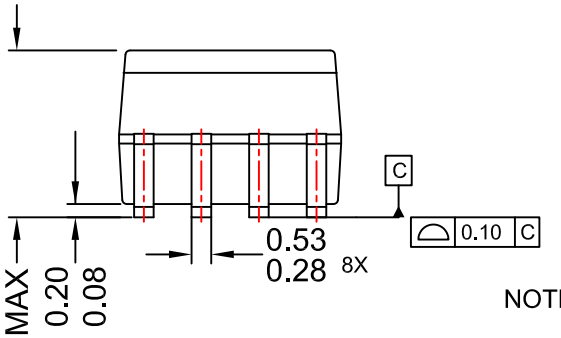
Reflow Profile

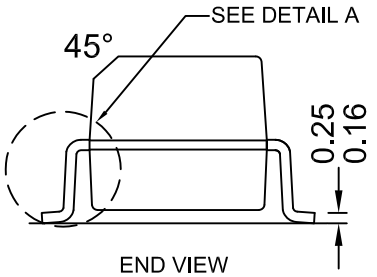




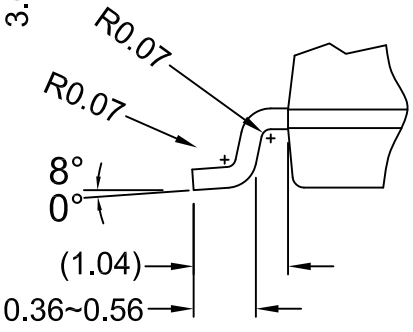


LAND PATTERN RECOMMENDATION





END VIEW



DETAIL A
SCALE: 2:1

NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
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