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www.win-source.net 0086-755-83957316

Freescale Semiconductor
Technical Data

Document Number: MPC8377EEC
Rev. 8, 05/2012

MPC8377E PowerQUICC II Pro Processor Hardware Specifications

This document provides an overview of the MPC8377E PowerQUICC II Pro processor features, including a block diagram showing the major functional components. This chip is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several printing and imaging, consumer, and industrial applications, including main CPUs and I/O processors in printing systems, networking switches and line cards, wireless LANs (WLANs), network access servers (NAS), VPN routers, intelligent NIC, and industrial controllers. This chip extends the PowerQUICC family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

Contents

1. Overview 1
2. Electrical Characteristics 7
3. Power Characteristics 11
4. Clock Input Timing 13
5. RESET Initialization 15
6. DDR1 and DDR2 SDRAM 16
7. DUART 22
8. Ethernet: Enhanced Three-Speed Ethernet (eTSEC) 23
9. USB 33
10. Local Bus 35
11. Enhanced Secure Digital Host Controller (eSDHC) 44
12. JTAG 52
13. I^2C 56
14. PCI 58
15. PCI Express 60
16. Serial ATA (SATA) 69
17. Timers 74
18. GPIO 75
19. IPIC 75
20. SPI 76
21. High-Speed Serial Interfaces (HSSI) 78
22. Package and Pin Listings 88
23. Clocking 107
24. Thermal 114
25. System Design Information 120
26. Ordering Information 122
27. Document Revision History 124

1 Overview

This chip incorporates the e300c4s core, which includes 32 KB of L1 instruction and data caches and on-chip memory management units (MMUs). The device offers two enhanced three-speed 10, 100, 1000 Mbps Ethernet interfaces, a DDR1/DDR2 SDRAM memory controller, a flexible, a 32-bit local bus controller, a 32-bit PCI controller, an optional dedicated security engine, a USB 2.0 dual-role controller, a programmable interrupt

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controller, dual I^2C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.

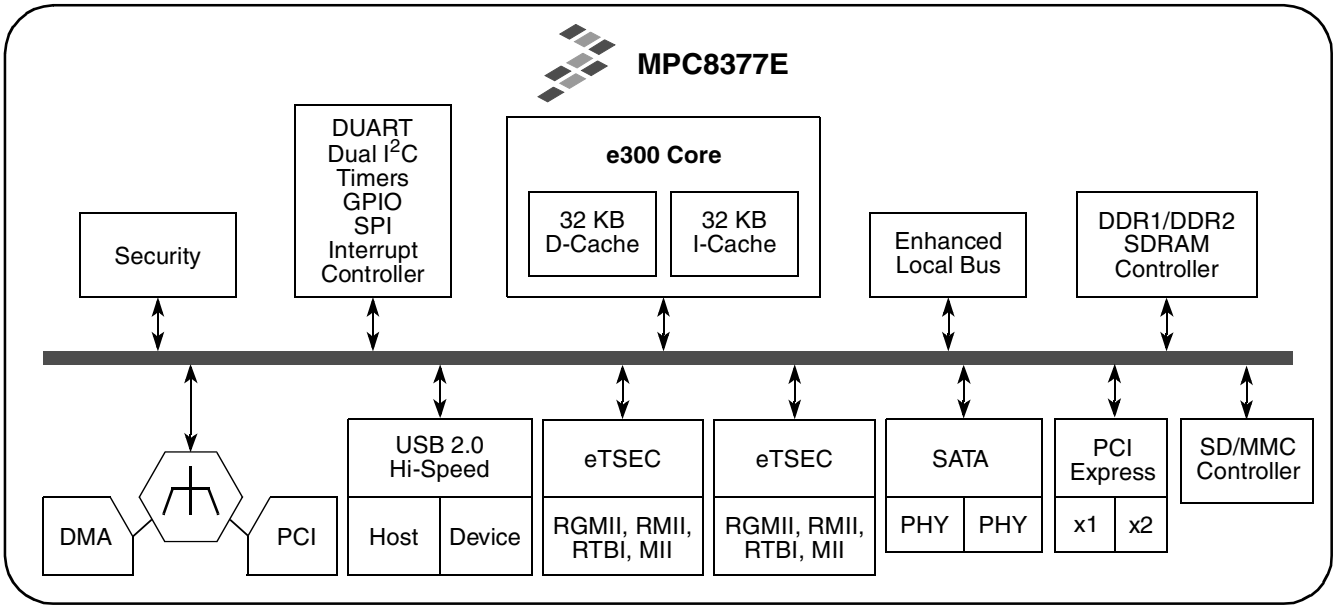


Figure 1. MPC8377E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension “E” at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In addition to the security engine, new high-speed interfaces, such as PCI Express and SATA are included. This table compares the differences between MPC837xE derivatives and provides the number of ports available for each interface.

Table 1. High-Speed Interfaces on the MPC8377E, MPC8378E, and MPC8379E

Descriptions	MPC8377E	MPC8378E	MPC8379E
SGMII	0	2	0
PCI Express®	2	2	0
SATA	2	0	4

1.1 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 32- or 64-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 400-MHz data rate
- Support up to 4 chip selects
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with ×8/×16/×32 data ports (no direct ×4 support)
- Support for up to 32 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.2 USB Dual-Role Controller

The USB controller includes the following features:

- Supports USB on-the-go mode, including both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation; low-speed operation is supported only in host mode
- Supports UTMI + low pin interface (ULPI)

1.3 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two enhanced Ethernet interfaces can be used for RGMII/MII/RMII/RTBI
- Two controllers conform to IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3au, IEEE 802.3ab, and IEEE Std 1588™ standards
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status

1.4 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.5 Power Management Controller (PMC)

The power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, and D3hot states
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports Wake-on-LAN (Magic Packet), USB, GPIO, and PCI (PME input as host)
- Supports MPC8349E backward-compatibility mode

1.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.7 DMA Controller, Dual I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The device provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The main component of the enhanced local bus controller (eLBC) is its memory controller, which provides a seamless interface to many types of memory devices and peripherals. The memory controller is responsible for controlling eight memory banks shared by a NAND Flash control machine (FCM), a general-purpose chip-select machine (GPCM), and up to three user-programmable machines (UPMs). As such, it supports a minimal glue logic interface to SRAM, EPROM, NOR Flash EPROM, NAND Flash, EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. The eLBC external address latch enable (LALE) signal allows multiplexing of addresses with data signals to reduce the device pin count.

The enhanced local bus controller also includes a number of data checking and protection features, such as data parity generation and checking, write protection, and a bus monitor to ensure that each bus cycle is terminated within a user-specified period. The local bus can operate at up to 133 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

1.8 Security Engine

The optional security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.9 PCI Controller

The PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting 5 external masters on PCI
- Selectable hardware-enforced coherency

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two ×1 links or one ×2 link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

1.12 Enhanced Secured Digital Host Controller (eSDHC)

The enhanced SD host controller (eSDHC) has the following features:

- Conforms to *SD Host Controller Standard Specification, Rev 2.0* with Test Event register support.
- Compatible with the *MMC System Specification, Rev 4.0*
- Compatible with the *SD Memory Card Specification, Rev 2.0*, and supports High Capacity SD memory cards
- Compatible with the *SDIO Card Specification Rev, 1.2*
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, MMC 4x, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Supports internal DMA capabilities

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the chip. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (e300 core, eLBC, and system)	AV_{DD}	–0.3 to 1.1	V	—
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}[1,2]	–0.3 to 3.63	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
Local bus	LBV_{DD}	–0.3 to 3.63	V	—
SerDes	L[1,2]_nV_{DD}	–0.3 to 1.1	V	6

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	—
	PCI, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 4, 5
	Local Bus	LB_{IN}	–0.3 to (LBV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. Overshoot/undershoot by OV_{IN} on the PCI interface does not comply to the *PCI Electrical Specification* for 3.3-V operation, as shown in Figure 2.
6. L[1,2]_$n$$V_{DD}$ includes $SDAV_{DD_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

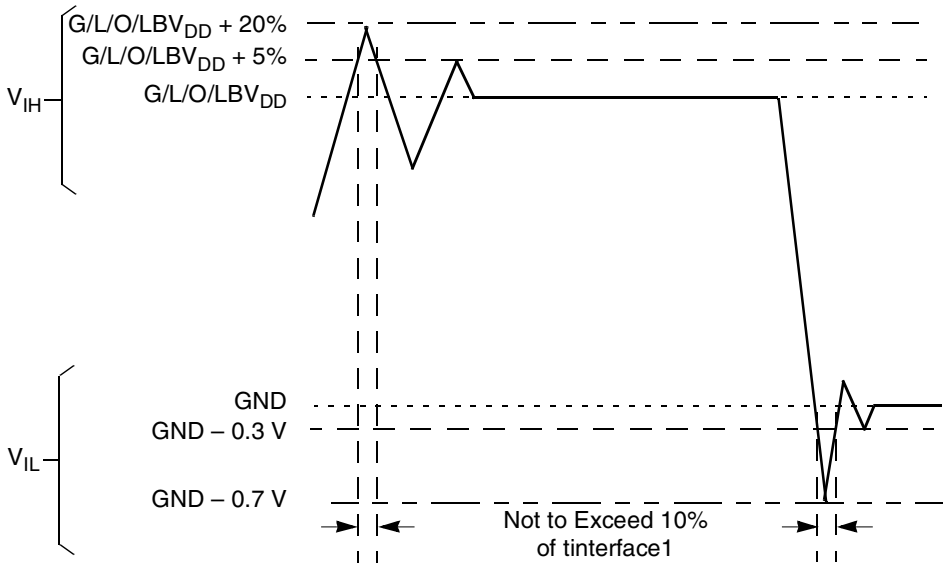
Characteristic		Symbol	Recommended Value	Unit	Note
Core supply voltage	up to 667 MHz	V_{DD}	1.0 ± 50 mV	V	1
	800 MHz		1.05 ± 50 mV	V	1
PLL supply voltage (e300 core, eLBC and system)	up to 667 MHz	AV_{DD}	1.0 ± 50 mV	V	1, 2
	800 MHz		1.05 ± 50 mV	V	1, 2
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Three-speed Ethernet I/O, MII management voltage		LV_{DD}[1,2]	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	1
Local Bus		LBV_{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV 3.3 V ± 165 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
SerDes	up to 667 MHz	L[1,2]_nV_{DD}	1.0 ± 50 mV	V	1, 3
	800 MHz		1.05 V ± 50 mV	V	1, 3
Operating temperature range	commerical	T_a T_j	T_a=0 (min)— T_j=125 (max)	°C	—
	extended temperature	T_a T_j	T_a=–40 (min)— T_j=125 (max)	°C	—

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. AV_{DD} is the input to the filter discussed in Section 25.1, "PLL Power Supply Filtering," and is not necessarily the voltage at the AVDD pin.
3. L[1,2]_nV_{DD}, $SDAV_{DD_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the *PCI Rev. 2.3 Specification* (Section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}

2.1.3 chipOutput Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type[1]	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	45	LBV_{DD} = 2.5 V, 3.3 V
	40	LBV_{DD} = 1.8 V
PCI signals	25	OV_{DD} = 3.3 V
DDR1 signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
eTSEC 10/100/1000 signals	45	LV_{DD} = 2.5 V, 3.3 V
DUART, system control, I^2C, JTAG, SPI, and USB	45	OV_{DD} = 3.3 V
GPIO signals	45	OV_{DD} = 3.3 V

Note:
1. Specialized SerDes output capabilities are described in the relevant sections of these specifications (such as PCI Express and SATA)

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. To avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltages (V_{DD} and AV_{DD}) before the I/O voltages and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. V_{DD} and AV_{DD} must reach 90% of their nominal value before GV_{DD}, LV_{DD}, and OV_{DD} reach 10% of their value, see the following figure. I/O

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

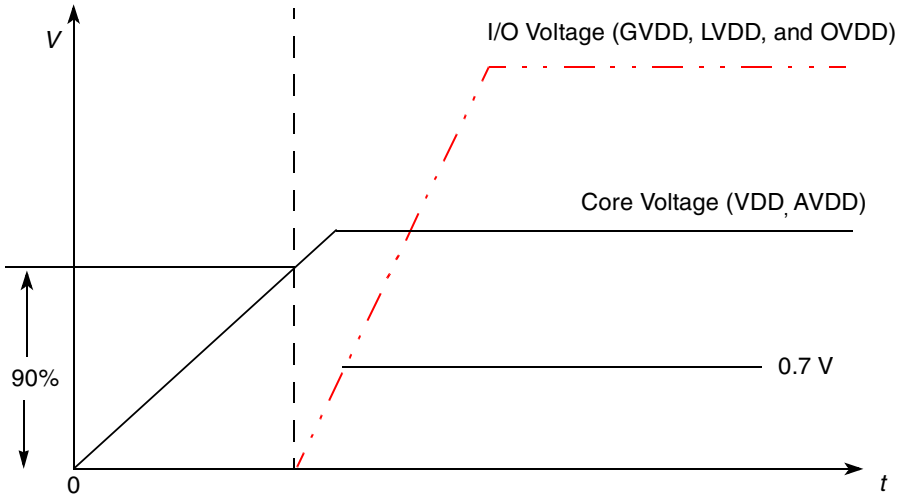


Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_$n$$V_{DD}$ (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	

Table 6. Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	$L[1,2]_nV_{DD}$ (1.0 V)	Unit	Comments
PCI I/O Load = 30 pf	33 MHz, 32-bit	—	—	0.04	—	—	—	W	—
	66 MHz, 32-bit	—	—	0.07	—	—	—	W	
Local Bus I/O Load = 25 pf	167 MHz, 32-bit	0.09	0.17	0.29	—	—	—	W	—
	133 MHz, 32-bit	0.07	0.14	0.24	—	—	—	W	
	83 MHz, 32-bit	0.05	0.09	0.15	—	—	—	W	
	66 MHz, 32-bit	0.04	0.07	0.13	—	—	—	W	
	50 MHz, 32-bit	0.03	0.06	0.1	—	—	—	W	
eTSEC I/O Load = 25 pf	MII or RMII	—	—	—	0.02	—	—	W	Multiply by number of interfaces used.
	RGMII or RTBI	—	—	—	—	0.05	—	W	—
USB (60MHz Clock)	12 Mbps	—	—	0.01	—	—	—	W	—
	480 Mbps	—	—	0.2	—	—	—	W	
SerDes	per lane	—	—		—	—	0.029	W	—
Other I/O	—	—	—	0.01	—	—	—	W	—

Note: The values given are for typical, and not worst case, switching.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the chip. Note that the PCI_CLK/PCI_SYNC_IN signal or CLKIN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. CLKIN is used when the device is in host mode.

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 10	μA	—
PCI_CLK Input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 9. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the chip.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	± 30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

- This table applies for pins $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. The $\overline{\text{PORESET}}$ is input pin, thus stated output voltages are not relevant.
- $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pin, thus V_{OH} is not relevant for these pins.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI_SYNC_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	$t_{PCI_SYNC_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI_SYNC_IN}$	1
$\overline{\text{HRESET}}$ negation to negation (output)	16	—	$t_{PCI_SYNC_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI_SYNC_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI_SYNC_IN}$	1, 3

Notes:

1. $t_{PCI_SYNC_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

Note:

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.9 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.38 V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}				μA	1, 2
DDR1		—	250	600		
DDR2		—	150	400		

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 20. DDR1 and DDR2 SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS-MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz data rate		–500	500		3
333 MHz data rate		–750	750		—
266 MHz data rate		–750	750		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS*n* and any corresponding bit that will be captured with MDQS*n*. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm[T/4 - |t_{CISKEW}|]$ where T is the MCK clock period and $|t_{CISKEW}|$ is the absolute value of t_{CISKEW}.
3. This specification applies only to DDR2 interface.

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in Note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8379E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data MDQ, ECC, or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK*n* at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in Note 1.
7. Clock Control register is set to adjust the memory clocks by 1/2 the applied cycle.
8. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

The minimum frequency for DDR2 is 250 MHz data rate (125 MHz clock), 167 MHz data rate (83 MHz clock) for DDR1. This figure shows the DDR1 and DDR2 SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

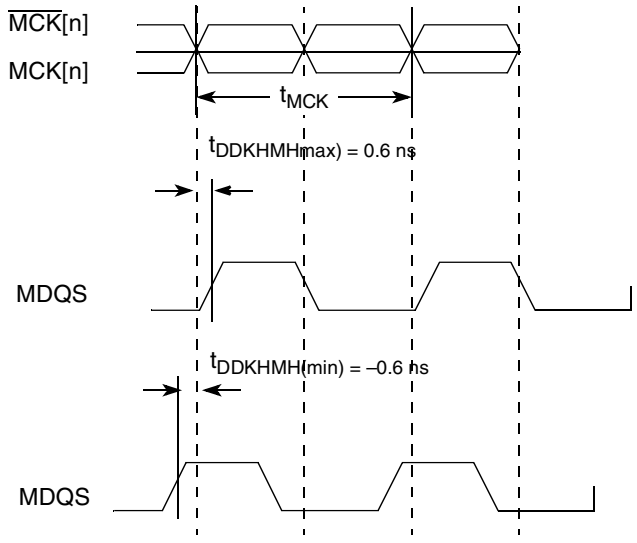


Figure 4. DDR Timing Diagram for t_{DDKHMH}

This figure shows the DDR1 and DDR2 SDRAM output timing diagram.

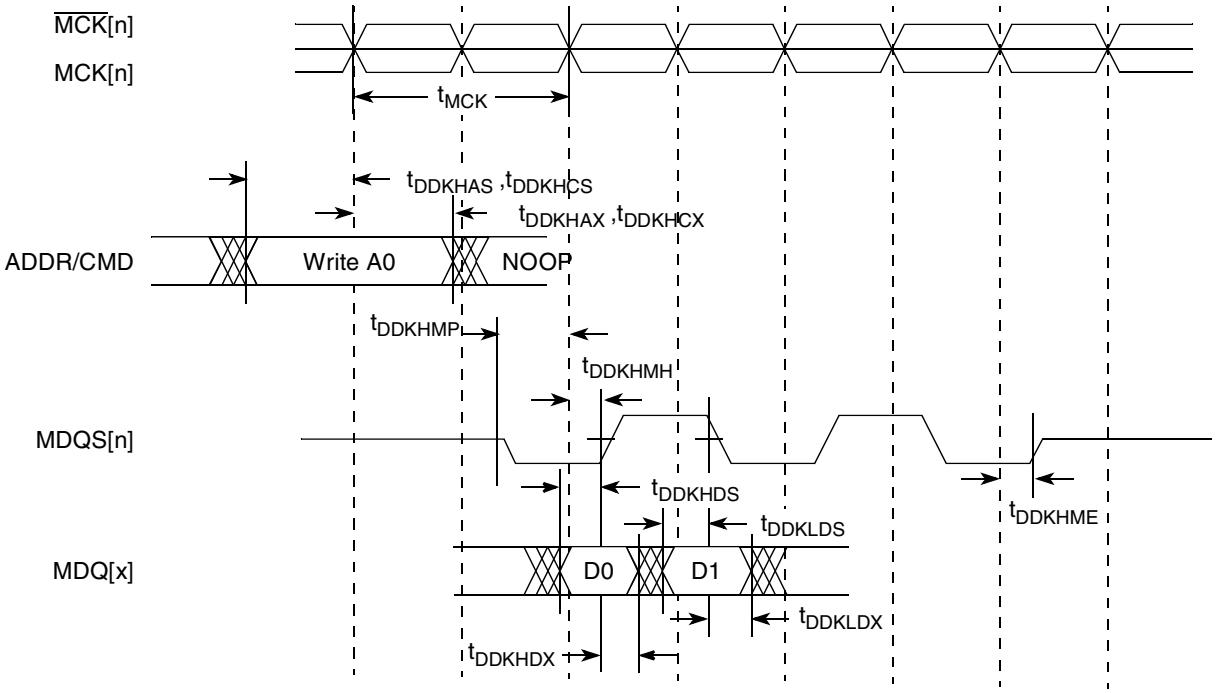


Figure 5. DDR1 and DDR2 SDRAM Output Timing Diagram

This figure provides AC test load for the DDR bus.

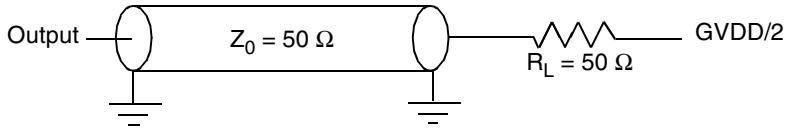


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V

Table 22. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current, (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±30	µA

Note: The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 25. RGMII and RTBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 2.5 V	LV_{DD1} LV_{DD2}	2.37	2.63	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.7	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	–20	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–20	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

8.2 MII, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RGMII, RMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

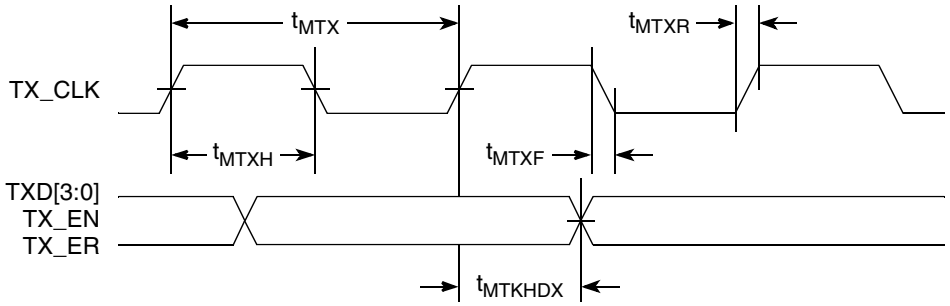


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

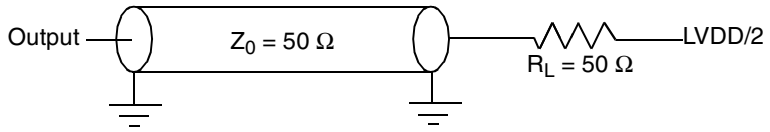


Figure 8. eTSEC AC Test Load

This figure shows the MII receive AC timing diagram.

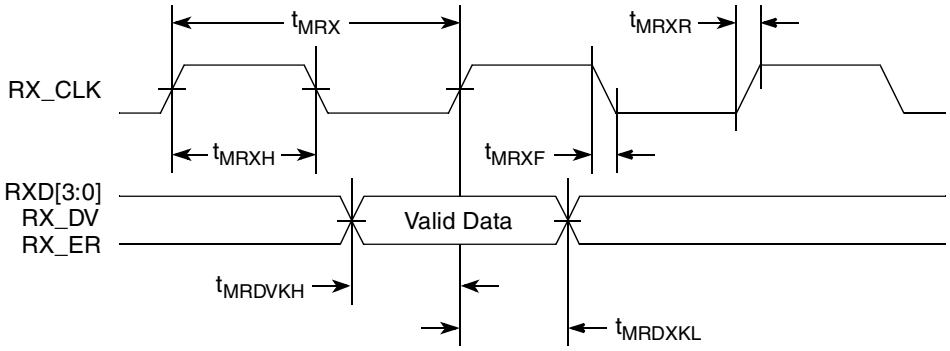


Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—
EC_GTX_CLK125 reference clock period	t_{G12}	—	8.0	—	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at $0.5 \times LV_{DD1}$	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

This figure provides the AC test load for eTSEC.

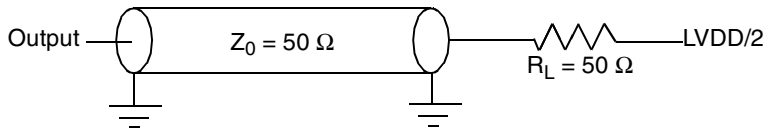


Figure 10. eTSEC AC Test Load

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

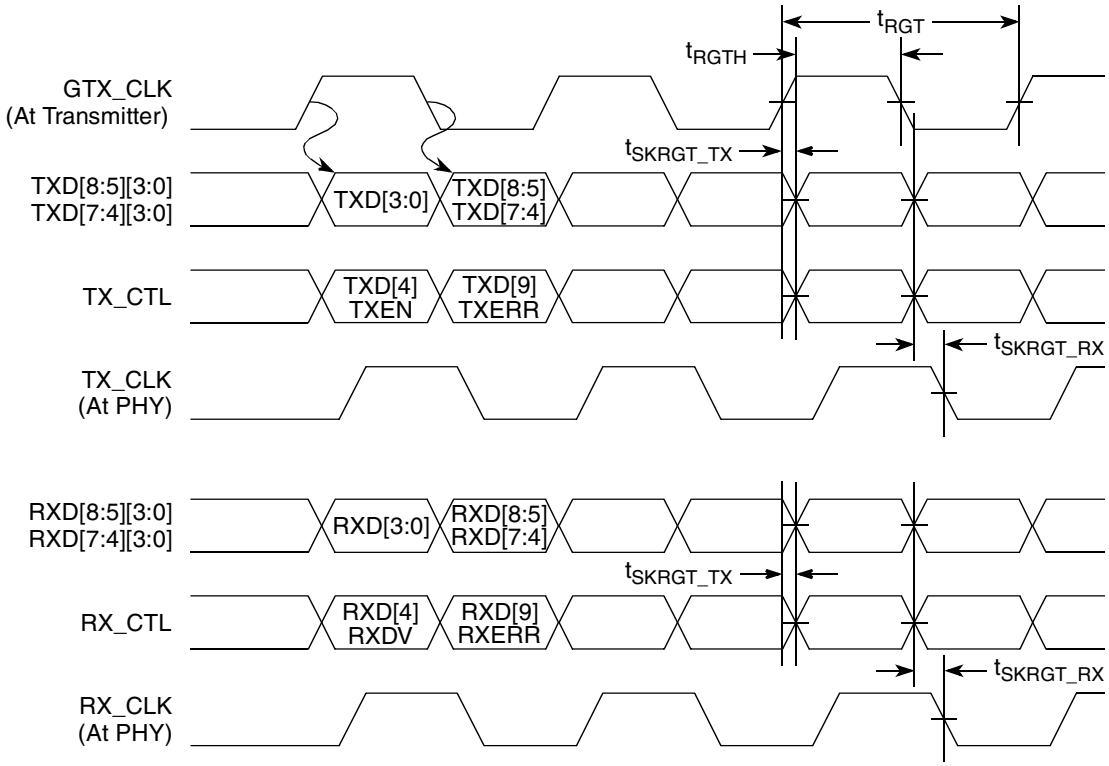


Figure 11. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

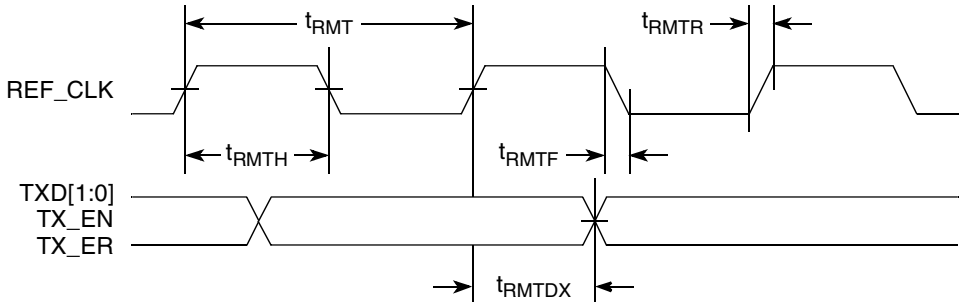


Figure 12. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table shows the RMII receive AC timing specifications.

Table 30. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
Input low voltage at 3.3 LV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage at 3.3 LV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

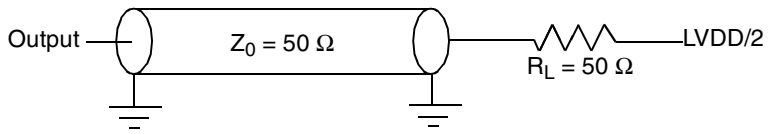


Figure 13. eTSEC AC Test Load

This figure shows the RMII receive AC timing diagram.

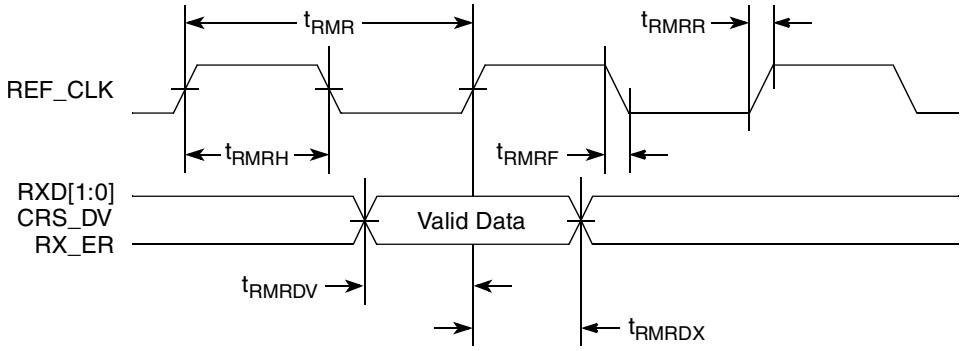


Figure 14. RMII Receive AC Timing Diagram

8.3 Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

This figure provides the AC test load for eTSEC.

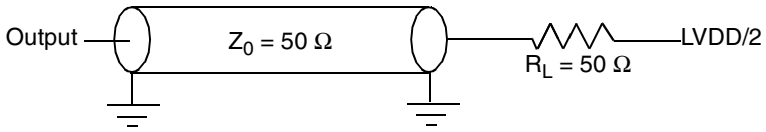


Figure 15. eTSEC AC Test Load

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (2.5 V)	—		LV_{DD1}	2.37	2.63	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.00	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND – 0.3	0.40	V
Input high voltage	—	LV_{DD1} = Min	V_{IH}	1.7	—	V
Input low voltage	—	LV_{DD1} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} = LV_{DD1}		I_{IH}	—	20	μA
Input low current	V_{IN} = LV_{DD1}		I_{IL}	–15	—	μA

Table 32. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (3.3 V)	—		LV_{DD1}	3.135	3.465	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.10	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND	0.50	V
Input high voltage	—		V_{IH}	2.00	—	V
Input low voltage	—		V_{IL}	—	0.80	V
Input high current	LV_{DD1} = Max	V_{IN} [1] = 2.1 V	I_{IH}	—	30	μA
Input low current	LV_{DD1} = Max	V_{IN} = 0.5 V	I_{IL}	–600	—	μA

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 33. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	80	—	400	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$2 \times (t_{plb_clk} \times 8)$	—	—	ns	4
MDC to MDIO delay	t_{MDKHDX}	10	—	$2 \times (t_{plb_clk} \times 8)$	ns	2, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time (20%–80%)	t_{MDCR}	—	—	10	ns	3
MDC fall time (80%–20%)	t_{MDCF}	—	—	10	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed.
3. Guaranteed by design.
4. t_{plb_clk} is the platform (CSB) clock divided according to the SCCR[TSEC1CM].

This figure shows the MII management AC timing diagram.

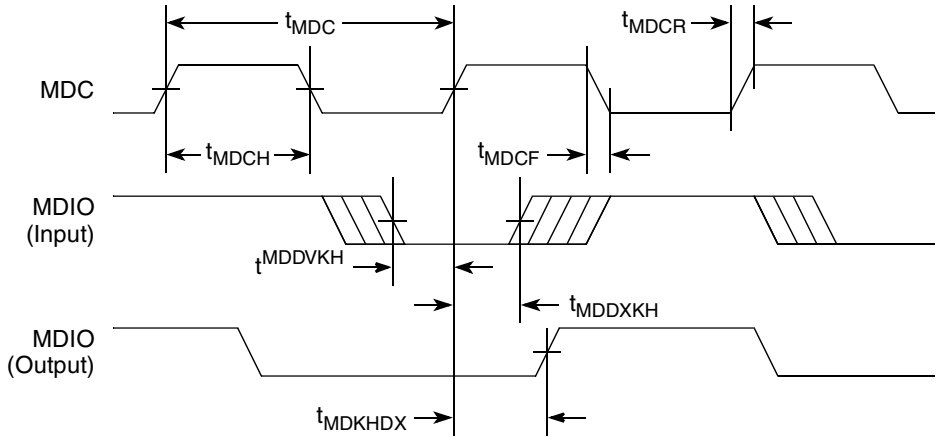


Figure 16. MII Management Interface Timing Diagram

9 USB

This section provides the AC and DC electrical characteristics for the USB dual-role controllers.

9.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the ULPI interface at recommended OV_{DD} = 3.3 V ± 165 mV.

Table 34. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	1
Low-level input voltage	V_{IL}	–0.3	0.8	V	1
Input current	I_{IN}	—	±30	μA	2
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V	—
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V	—

Notes:
1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply and is referenced in Table 3.

9.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 35. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the USB clock, USBDR_CLK.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

These two figures provide the AC test load and signals for the USB, respectively.

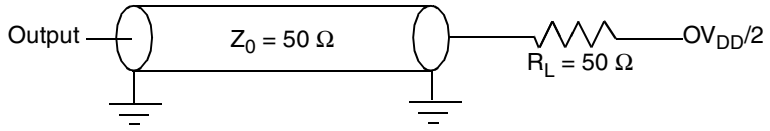


Figure 17. USB AC Test Load

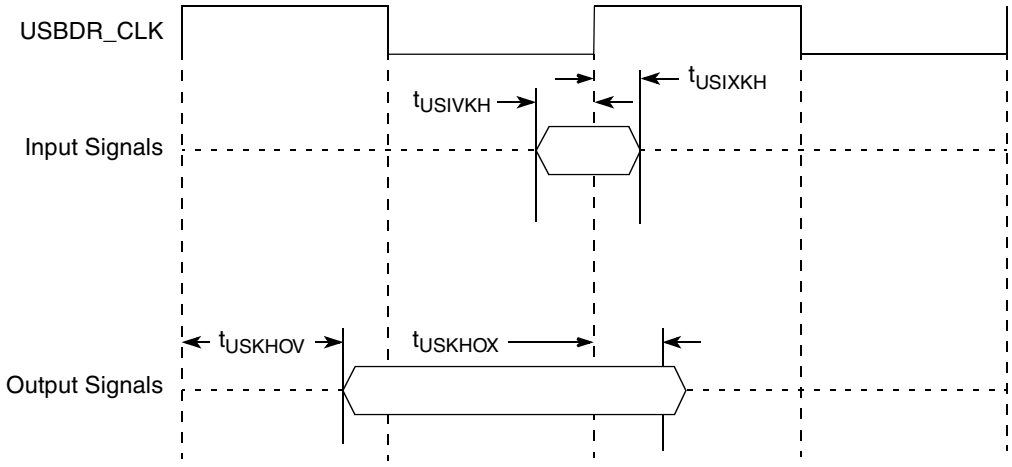


Figure 18. USB Interface Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

10.1 Local Bus DC Electrical Characteristics

This tables provide the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics (LBV_{DD} = 3.3 V)

At recommended operating conditions with LBV_{DD} = 3.3 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 3.3 V	—		LBV_{DD}	3.135	3.465	V
Output high voltage	I_{OH} = –4.0 mA	LBV_{DD} = Min	V_{OH}	2.40	—	V
Output low voltage	I_{OL} = 4.0 mA	LBV_{DD} = Min	V_{OL}	—	0.50	V
Input high voltage	—	—	V_{IH}	2.0	LBV_{DD} + 0.3	V
Input low voltage	—	—	V_{IL}	–0.3	0.90	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	30	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–30	—	μA

Table 37. Local Bus DC Electrical Characteristics (LBV_{DD} = 2.5 V)

At recommended operating conditions with LBV_{DD} = 2.5 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 2.5 V	—		LBV_{DD}	2.37	2.73	V
Output high voltage	I_{OH} = –1.0 mA	LBV_{DD} = Min	V_{OH}	2.00	—	V
Output low voltage	I_{OL} = 1.0 mA	LBV_{DD} = Min	V_{OL}	—	0.40	V
Input high voltage	—	LBV_{DD} = Min	V_{IH}	1.7	LBV_{DD} + 0.3	V
Input low voltage	—	LBV_{DD} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	20	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–20	—	μA

Table 38. Local Bus DC Electrical Characteristics (LBV_{DD} = 1.8 V)

At recommended operating conditions with LBV_{DD} = 1.8 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 1.8 V	—		LBV_{DD}	1.71	1.89	V
Output high voltage	I_{OH} = –1.0 mA	LBV_{DD} = Min	V_{OH}	LBV_{DD} – 0.45	—	V
Output low voltage	I_{OL} = 1.0 mA	LBV_{DD} = Min	V_{OL}	—	0.45	V
Input high voltage	—	LBV_{DD} = Min	V_{IH}	0.65 × LBV_{DD}	LBV_{DD} + 0.3	V
Input low voltage	—	LBV_{DD} = Min	V_{IL}	–0.3	0.35 × LBV_{DD}	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	10	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–10	—	μA

10.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device when in PLL enable mode.

Table 39. Local Bus General Timing Parameters—PLL Enable Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	7.5	15	ns	2
Input setup to local bus clock (except LUPWAIT/$\overline{\text{LGTA}}$)	t_{LBIVKH}	1.5	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LUPWAIT/$\overline{\text{LGTA}}$ input setup to local bus clock	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LALE)	t_{LBKHOV}	—	4.5	ns	3

Table 39. Local Bus General Timing Parameters—PLL Enable Mode (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3, 8
Output hold from local bus clock for LAD/LDP	t_{LBKHOX}	1	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN at $LBV_{DD}/2$ and the $0.4 \times LBV_{DD}$ of the signal in question.
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LSYNC_IN to $0.5 \times LBV_{DD}$ of the signal in question.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device when in PLL bypass mode.

Table 40. Local Bus General Timing Parameters—PLL Bypass Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7.0	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid	t_{LBKHOV}	—	3.0	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4.0	ns	3, 8

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times LBV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

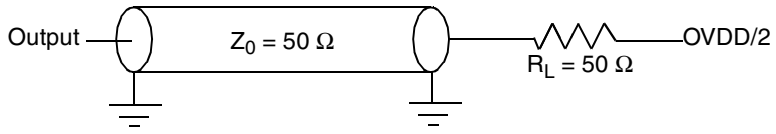


Figure 19. Local Bus AC Test Load

This figures show the local bus signals.

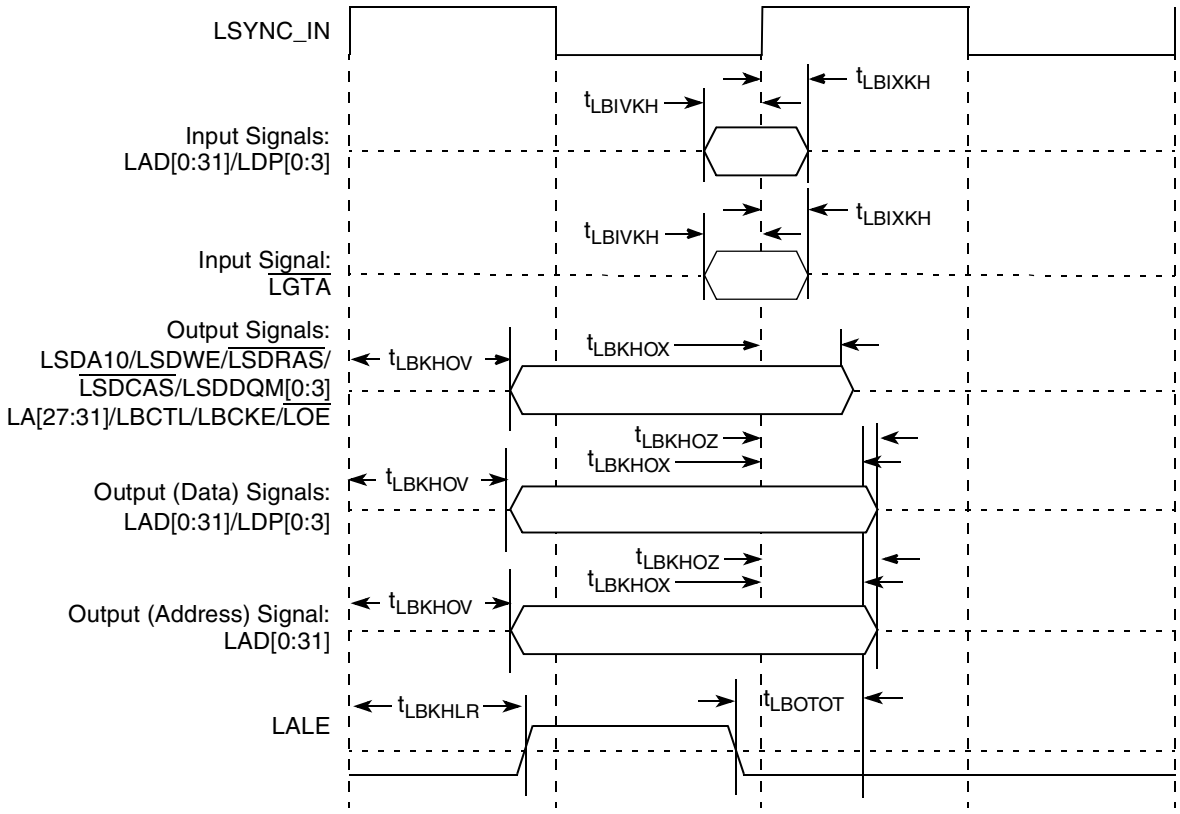


Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

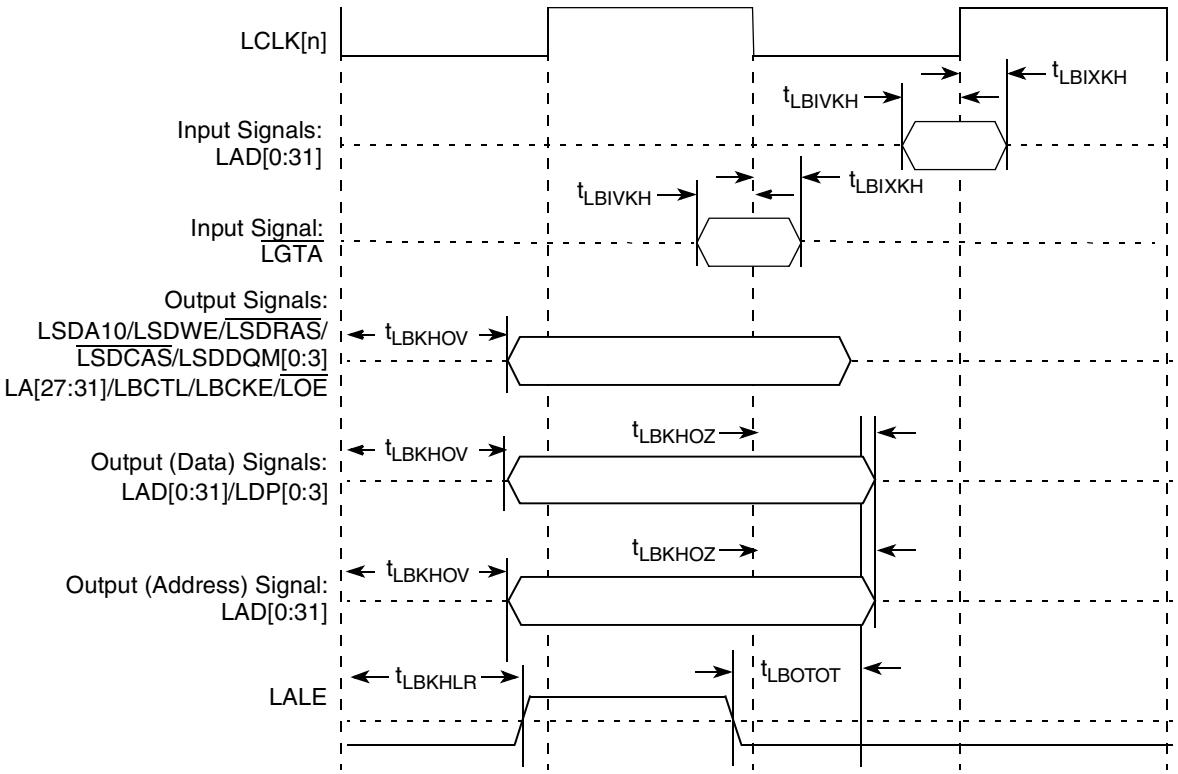


Figure 21. Local Bus Signals, Non-special Signals Only (PLL Bypass Mode)

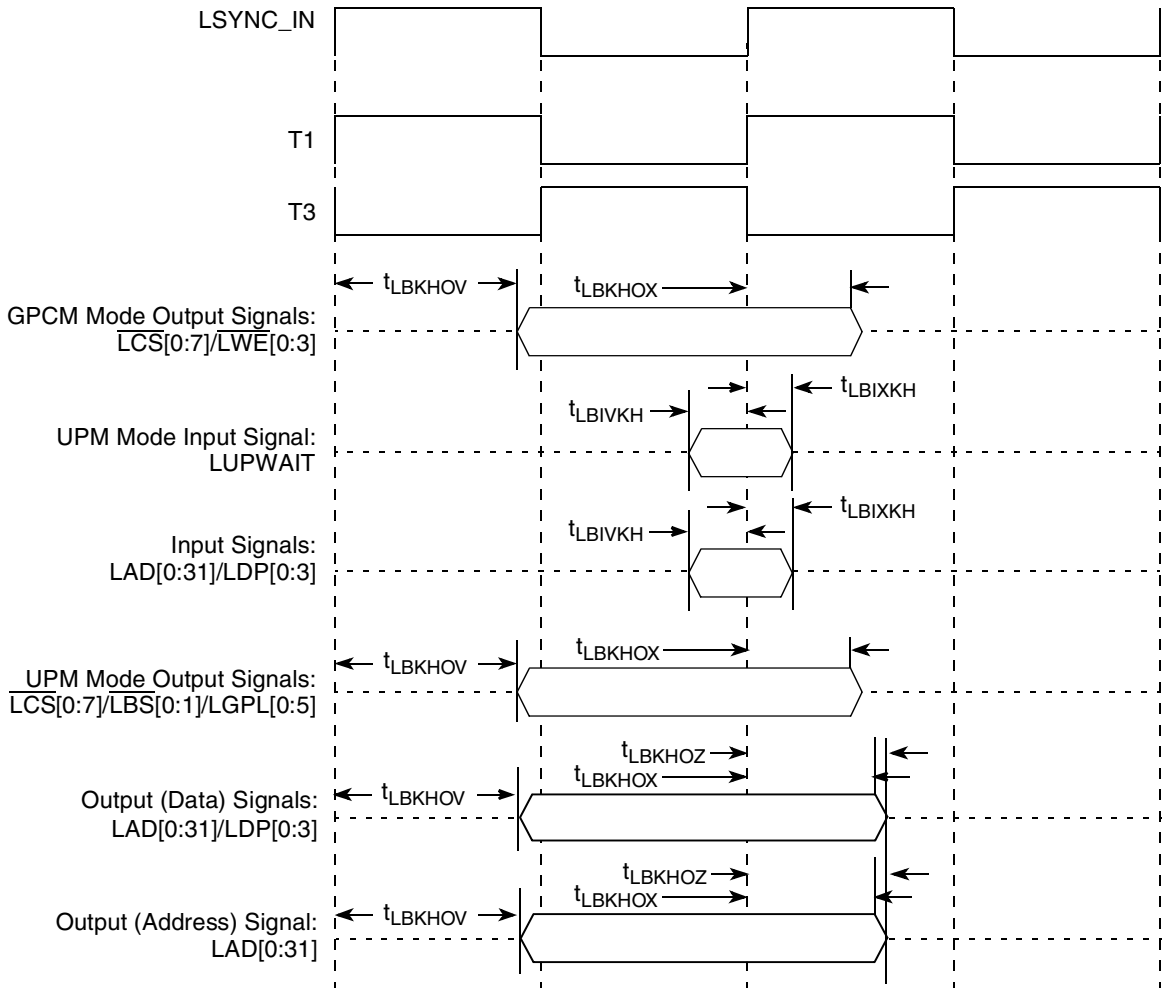


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)

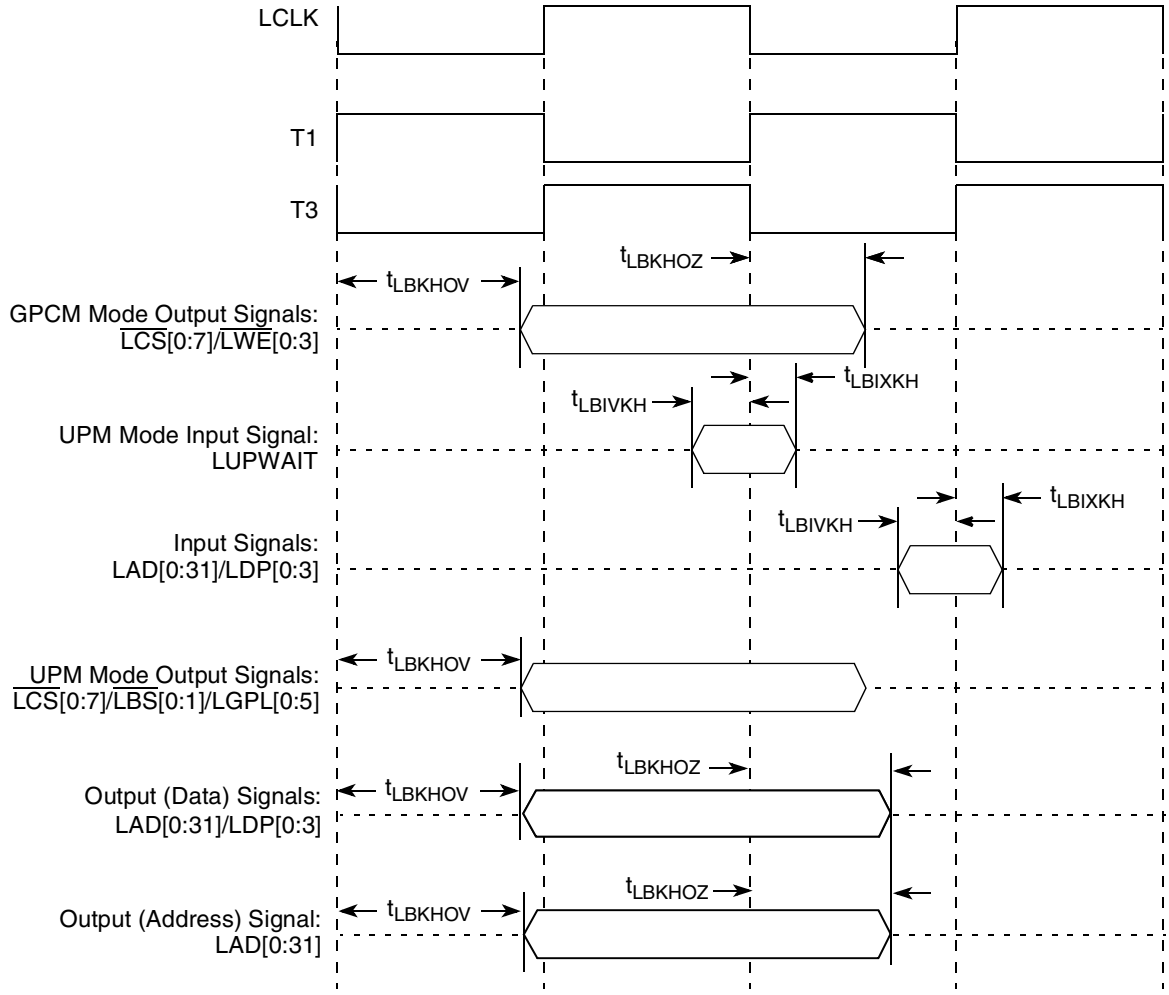


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Bypass Mode)

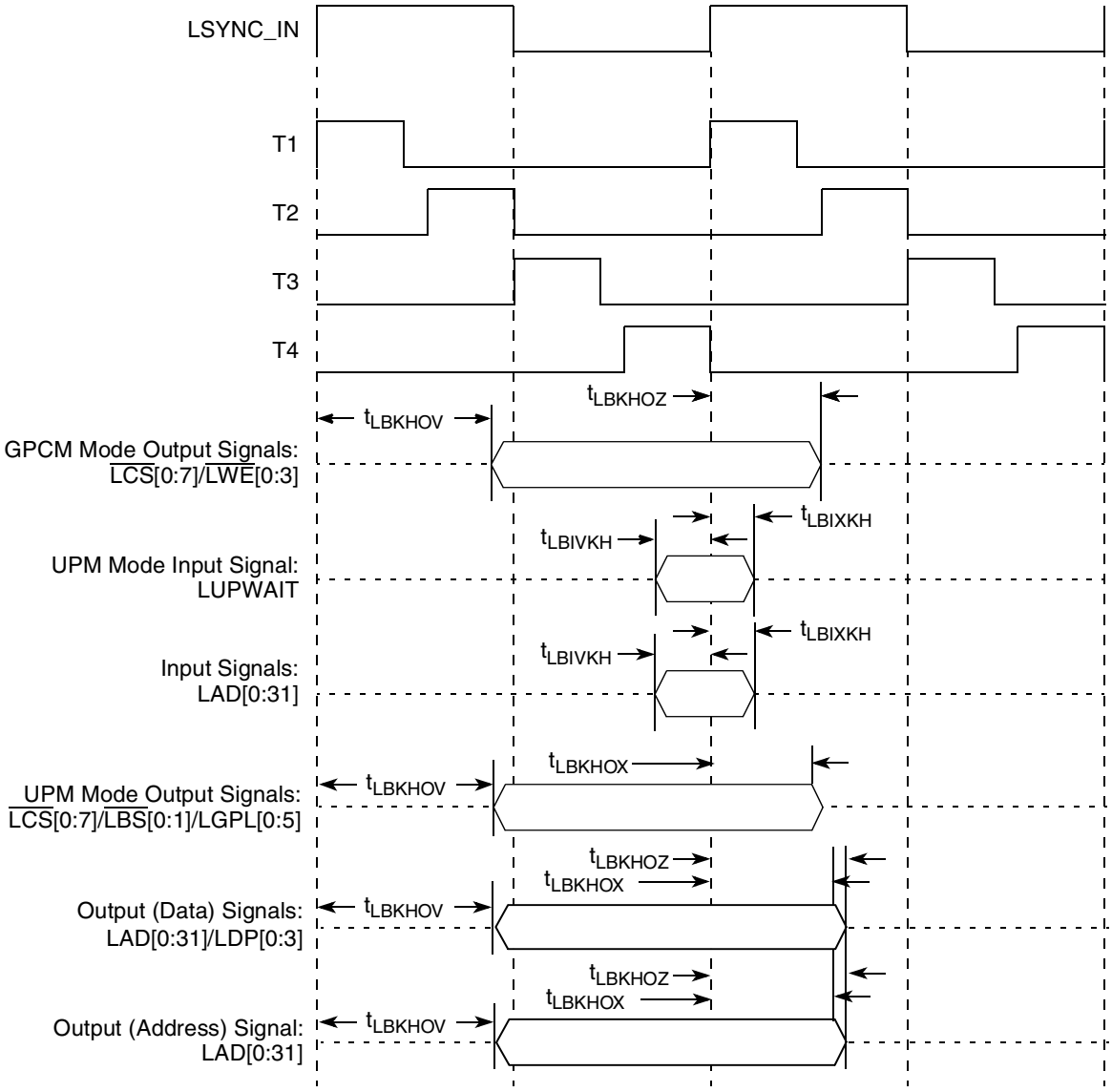


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)

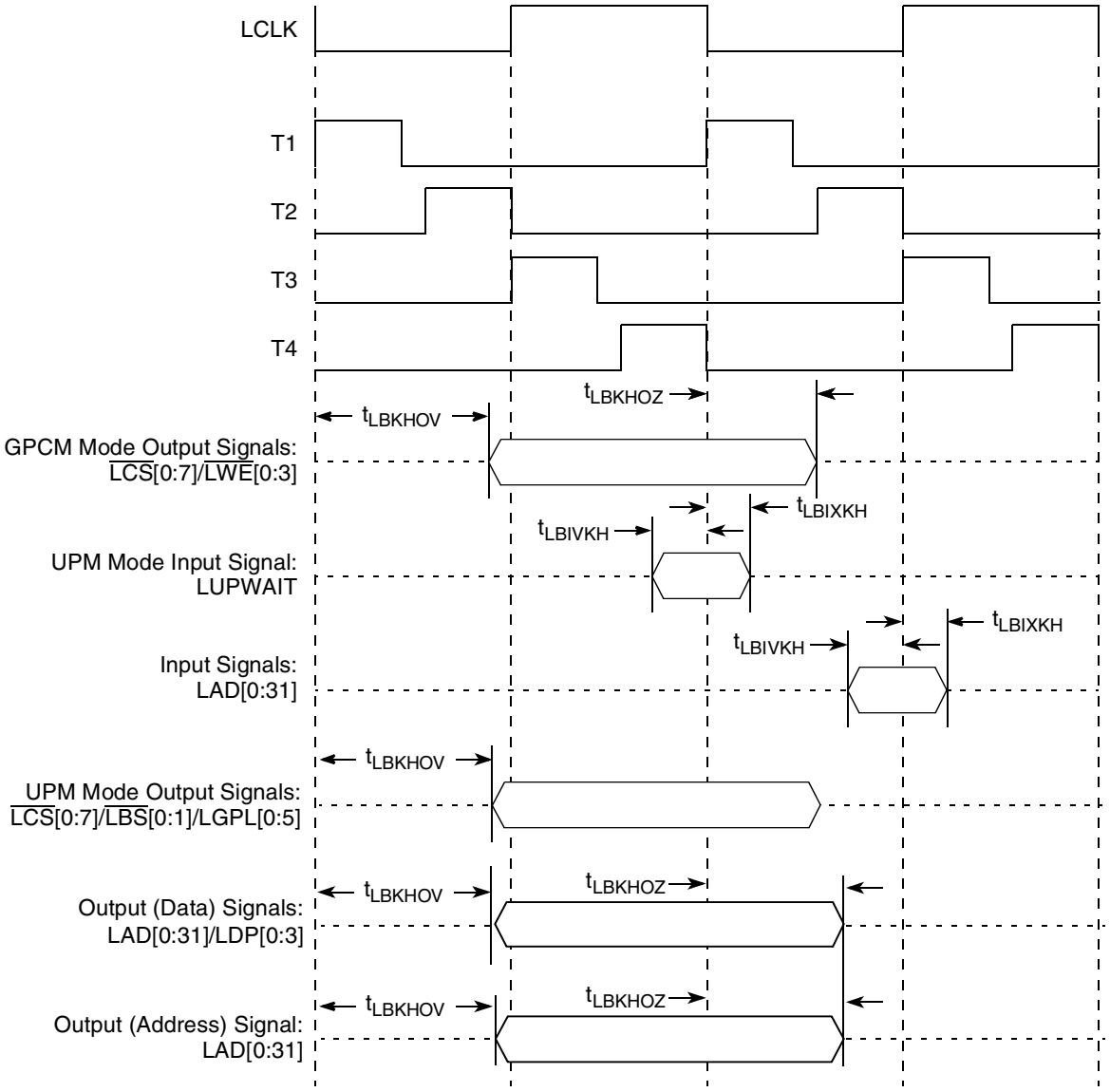


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Bypass Mode)

11 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC) interface of the chip.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and sample the SD_DAT[0:3] as inputs. This behavior is true for both full- and high-speed modes.

Note that this is a non-standard implementation, as the SD card specification assumes that in high-speed mode, data is driven at the rising edge of the clock.

Due to the special implementation of the eSDHC, there are constraints regarding the clock and data signals propagation delay on the user board. The constraints are for minimum and maximum delays, as well as skew between the CLK and DAT/CMD signals.

In full speed mode, there is no need to add special delay on the data or clock signals. The user should make sure to meet the timing requirements as described further within this document.

If the system is designed to support both high-speed and full-speed cards, the high-speed constraints should be fulfilled. If the systems is designed to operate up to 25 MHz only, full-speed mode is recommended.

11.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device.

Table 41. eSDHC interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	$0.625 \times OV_{DD}$	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	–0.3	$0.25 \times OV_{DD}$	V
Input current	I_{IN}	—	—	±30	μA
Output high voltage	V_{OH}	I_{OH} = –100 uA, at OV_{DD}(min)	$0.75 \times OV_{DD}$	—	V
Output low voltage	V_{OL}	I_{OL} = +100 uA, at OV_{DD}(min)	—	$0.125 \times OV_{DD}$	V

11.2 eSDHC AC Timing Specifications (Full-Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full-speed mode as defined in Figure 27 and Figure 28.

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency—full speed mode	f_{SFSCK}	0	25	MHz	—
SD_CLK clock cycle	t_{SFSCK}	40	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	KHz	—
SD_CLK clock low time	t_{SFSCKL}	15	—	ns	2
SD_CLK clock high time	t_{SFSCKH}	15	—	ns	2
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SFSIVKH}$	5	—	ns	2

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode (continued)

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold times: SD_CMD, SD_DAT*x*, SD_CD to SD_CLK	$t_{SFSIXKH}$	0	—	ns	2
SD_CLK delay within device	$t_{INT_CLK_DLY}$	1.5	—	ns	4
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	4	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	0	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

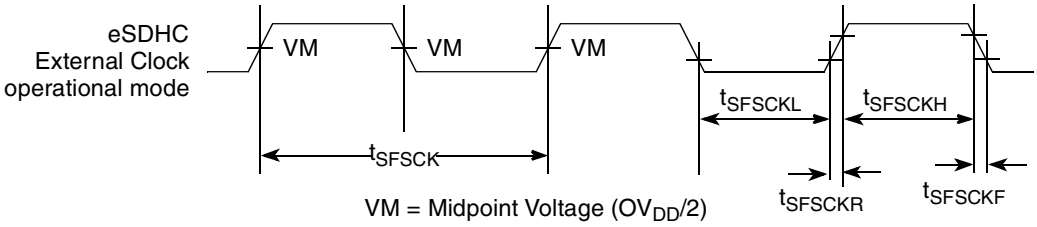


Figure 26. eSDHC Clock Input Timing Diagram

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

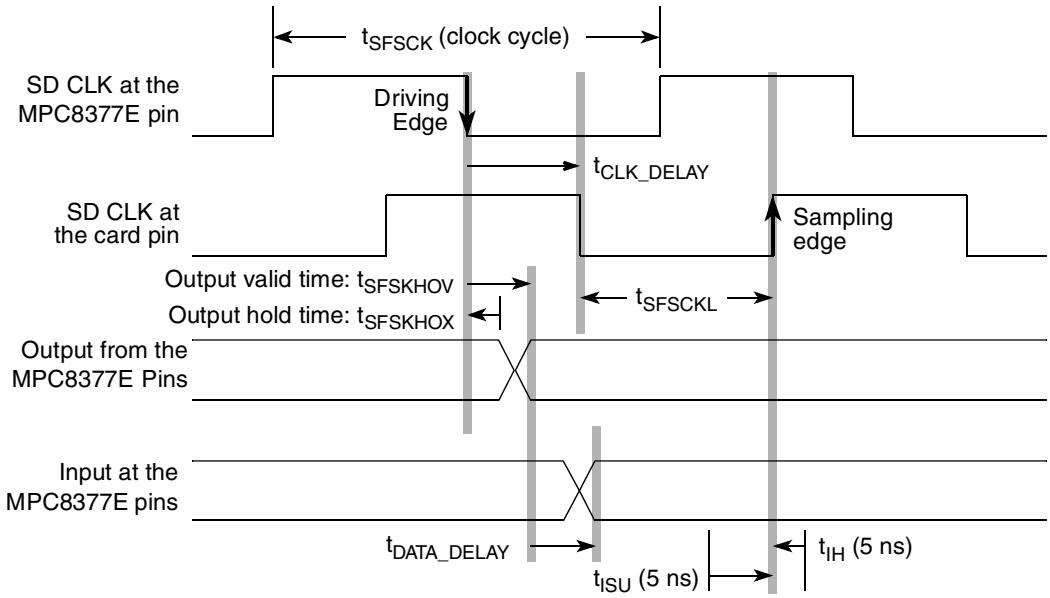


Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA_DELAY} + 20 < 40 + t_{CLK_DELAY} - 5 - 4$

$t_{DATA_DELAY} < 11 + t_{CLK_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

$$t_{CLK_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA_DELAY} \quad \text{Eqn. 5}$$

This means that clock can be delayed versus data up to 15 ns (external delay line) in ideal case of $t_{SFSCLKL}$ = 20 ns:

$t_{CLK_DELAY} + 5 - 0 < 20 + t_{DATA_DELAY}$

$t_{CLK_DELAY} < 15 + t_{DATA_DELAY}$

11.2.1.3 Full-Speed Write Combined Formula

The following equation is the combined formula to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA_DELAY} < t_{SFSCK} + t_{CLK_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \text{Eqn. 6}$$

11.2.2 Full-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

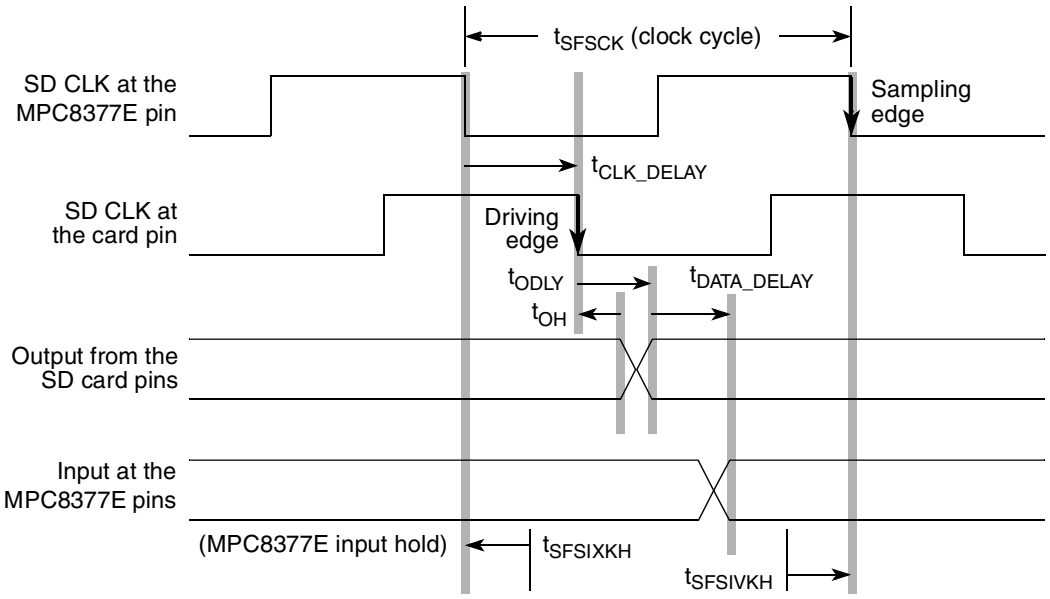


Figure 28. Full Speed Input Path

11.2.2.1 Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} + t_{DATA_DELAY} + t_{ODLY} + t_{SFSIVKH} < t_{SFSCK} \quad \text{Eqn. 7}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < t_{SFSCK} - t_{ODLY} - t_{SFSIVKH} - t_{INT_CLK_DLY} \quad \text{Eqn. 8}$$

11.2.2.2 Full-Speed Read Meeting Hold (Minimum Delay)

There is no minimum delay constraint due to the full clock cycle between the driving and sampling of data.

$$t_{CLK_DELAY} + t_{OH} + t_{DATA_DELAY} > t_{SFSIXKH} \quad \textit{Eqn. 9}$$

This means that Data + Clock delay must be greater than –2 ns. This is always fulfilled.

11.3 eSDHC AC Timing Specifications (High-Speed Mode)

This table provides the eSDHC AC timing specifications for high-speed mode as defined in Figure 30 and Figure 31.

Table 43. eSDHC AC Timing Specifications for High-Speed Mode

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency—high speed mode	f_{SHSCK}	0	50	MHz	—
SD_CLK clock cycle	t_{SHSCK}	20	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	KHz	—
SD_CLK clock low time	t_{SHSCKL}	7	—	ns	2
SD_CLK clock high time	t_{SHSCKH}	7	—	ns	2
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	2
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	0	—	ns	2
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	—	4	ns	2
Output Hold time: SD_CLK to SD_CMD, SD_DATx invalid	$t_{SHSKHOX}$	0	—	ns	2
SD_CLK delay within device	$t_{INT_CLK_DLY}$	1.5	—	ns	4
SD Card Input Setup	t_{ISU}	6	—	ns	3
SD Card Input Hold	t_{IH}	2	—	ns	3
SD Card Output Valid	t_{ODLY}	—	14	ns	3
SD Card Output Hold	t_{OH}	2.5	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

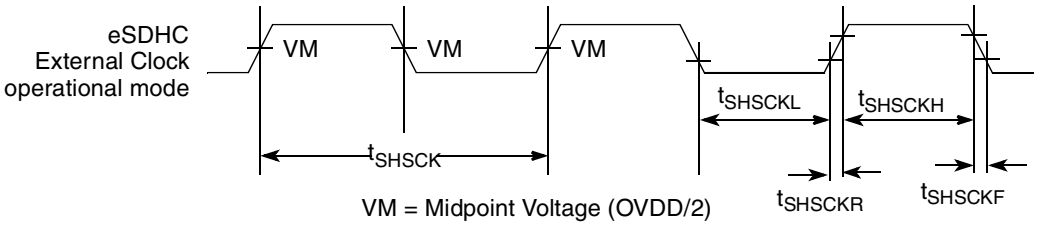


Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

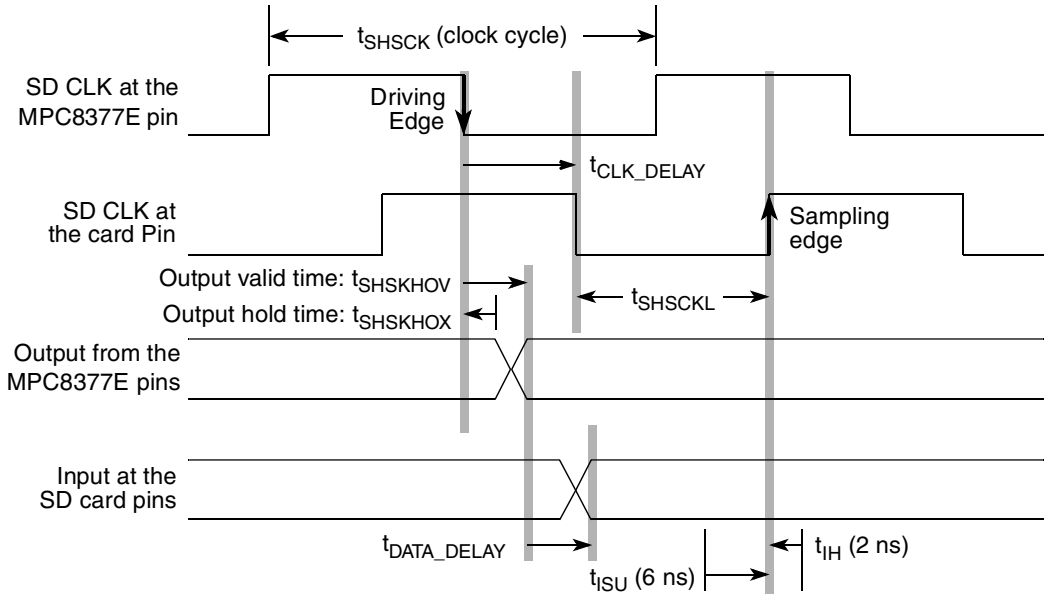


Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

$$t_{SHSKHOV} + t_{DATA_DELAY} + t_{ISU} < t_{SHSCKL} \quad \textit{Eqn. 10}$$

With clock delay:

$$t_{SHSKHOV} + t_{DATA_DELAY} + t_{ISU} < t_{SHSCKL} + t_{CLK_DELAY} \quad \textit{Eqn. 11}$$

$$t_{DATA_DELAY} - t_{CLK_DELAY} < t_{SHSCKL} - t_{ISU} - t_{SHSKHOV} \quad \textit{Eqn. 12}$$

This means that data delay should be equal or less than the clock delay in the ideal case where $t_{SHSCLKL}$ = 10 ns:

$$t_{DATA_DELAY} - t_{CLK_DELAY} < 10 - 6 - 4$$
$$t_{DATA_DELAY} - t_{CLK_DELAY} < 0$$

11.3.1.2 High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} < t_{SHSCKL} + t_{SHSKHOX} + t_{DATA_DELAY} - t_{IH} \quad \textit{Eqn. 13}$$

$$t_{CLK_DELAY} - t_{DATA_DELAY} < t_{SHSCKL} + t_{SHSKHOX} - t_{IH} \quad \textit{Eqn. 14}$$

This means that clock can be delayed versus data up to 8 ns (external delay line) in ideal case of $t_{SHSCLKL}$ = 10 ns:

$$t_{CLK_DELAY} - t_{DATA_DELAY} < 10 + 0 - 2$$
$$t_{CLK_DELAY} - t_{DATA_DELAY} < 8$$

11.3.2 High-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

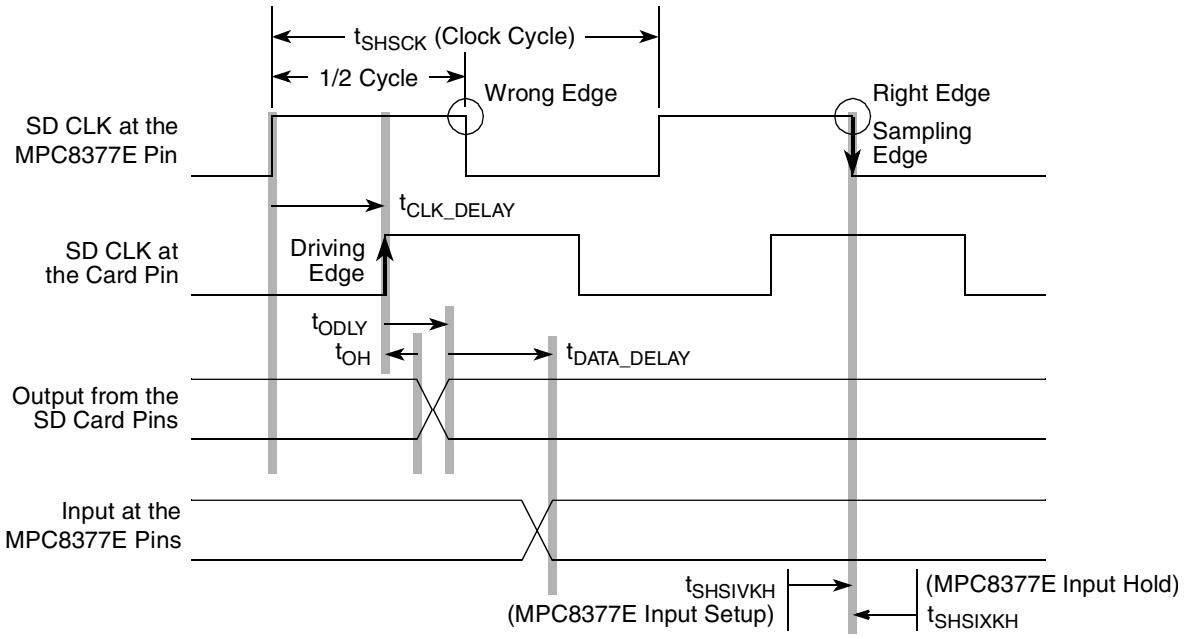


Figure 31. High-Speed Input Path

For the input path, the device eSDHC expects to sample the data 1.5 internal clock cycles after it was driven by the SD card. Since in this mode the SD card drives the data at the rising edge of the clock, a sufficient delay to the clock and the data must exist to ensure it will not be sampled at the wrong internal

clock falling edge. Note that the internal clock which is guaranteed to be 50% duty cycle is used to sample the data, and therefore used in the equations.

11.3.2.1 High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK_DELAY} + t_{DATA_DELAY} + t_{ODLY} + t_{SHSIVKH} < 1.5 \times t_{SHSCK} \quad \text{Eqn. 15}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} < 1.5 \times t_{SHSCK} - t_{ODLY} - t_{SHSIVKH} \quad \text{Eqn. 16}$$

This means that Data + Clock delay can be up to 11 ns for a 20 ns clock cycle:

$t_{CLK_DELAY} + t_{DATA_DELAY} < 30 - 14 - 5$

$t_{CLK_DELAY} + t_{DATA_DELAY} < 11$

11.3.2.2 High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$0.5 \times t_{SHSCK} < t_{CLK_DELAY} + t_{DATA_DELAY} + t_{OH} - t_{SHSIXKH} + t_{INT_CLK_DLY} \quad \text{Eqn. 17}$$

$$0.5 \times t_{SHSCK} - t_{OH} + t_{SHSIXKH} - t_{INT_CLK_DLY} < t_{CLK_DELAY} + t_{DATA_DELAY} \quad \text{Eqn. 18}$$

This means that Data + Clock delay must be greater than ~6 ns for a 20 ns clock cycle:

$10 - 2.5 + (-1.5) < t_{CLK_DELAY} + t_{DATA_DELAY}$

$6 < t_{CLK_DELAY} + t_{DATA_DELAY}$

11.3.2.3 High-Speed Read Combined Formula

The following equation is the combined formula to calculate the propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$0.5 \times t_{SHSCK} - t_{OH} + t_{SHSIXKH} < t_{CLK_DELAY} + t_{DATA_DELAY} < 1.5 \times t_{SHSCK} - t_{ODLY} - t_{SHSIVKH} \quad \text{Eqn. 19}$$

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the chip.

Table 44. JTAG interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device. This table provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1]

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	—
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	—

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 17). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

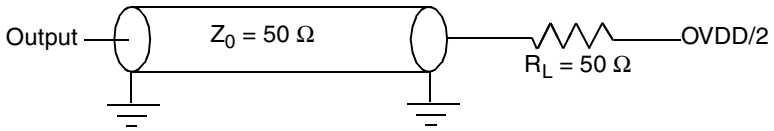


Figure 32. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

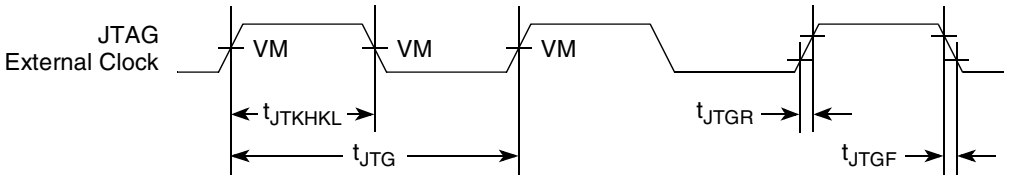


Figure 33. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



Figure 34. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

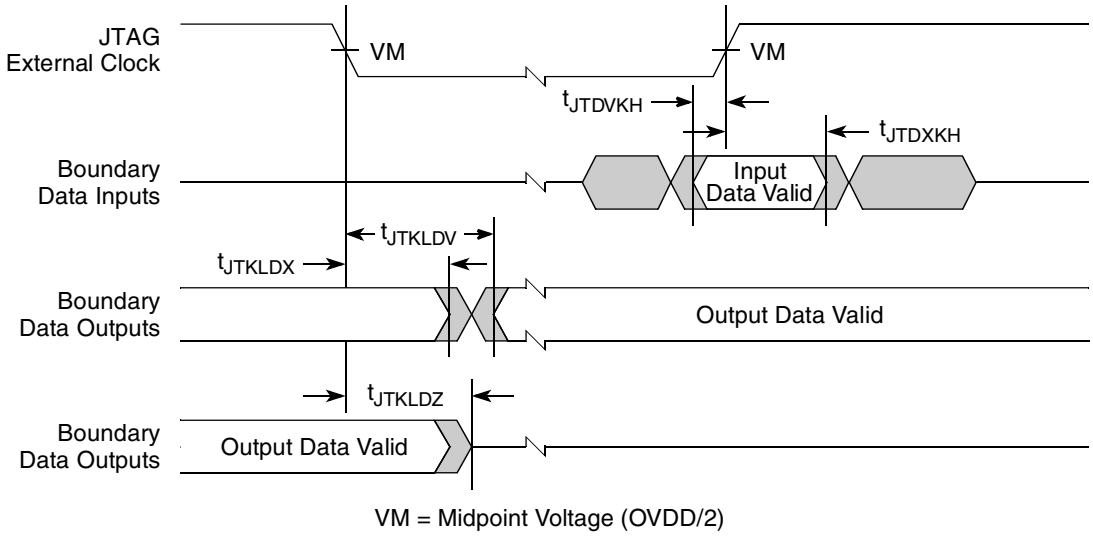


Figure 35. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

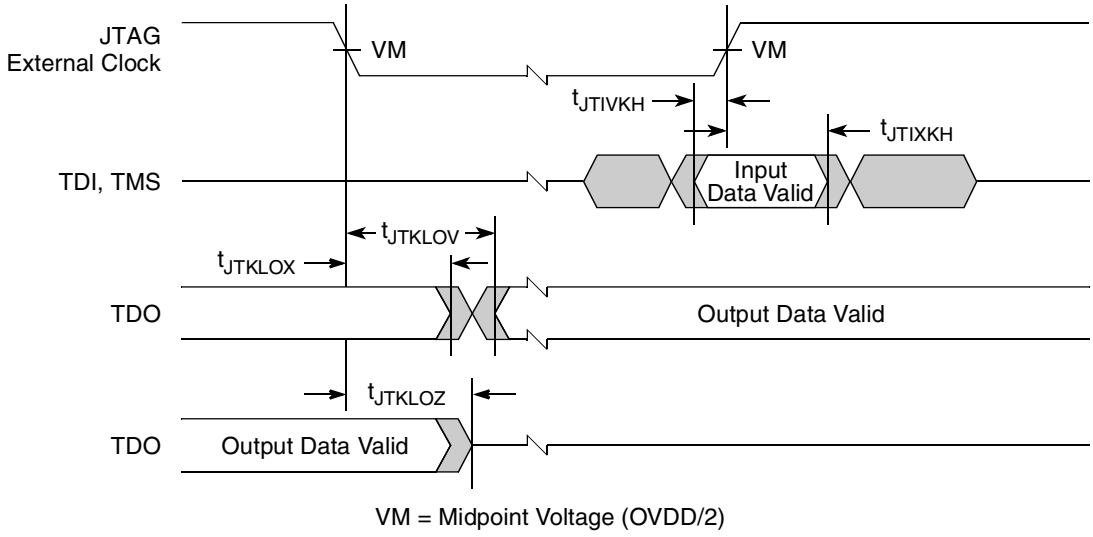


Figure 36. Test Access Port Timing Diagram

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the chip.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the chip.

Table 46. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 165 mV.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	± 30	µA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8379E PowerQUICC II Pro Integrated Host Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface of the device.

Table 47. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	—
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—

Table 47. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol[1]	Min	Max	Unit	Note
Data hold time CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — 0.9	µs	2, 3
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This chip provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

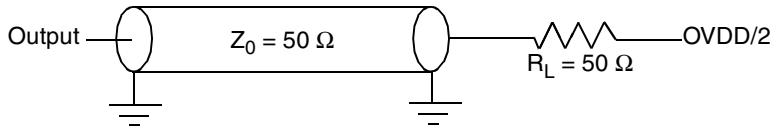


Figure 37. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

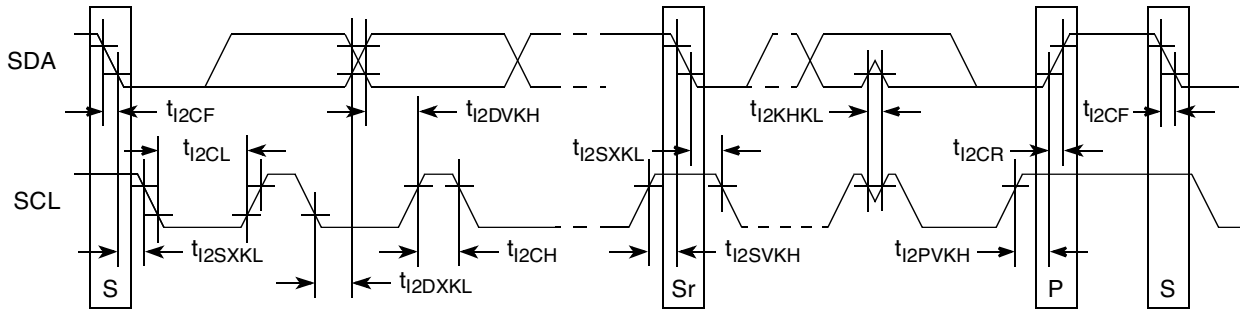


Figure 38. I²C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device. The DC characteristics of the PORESET signal, which can be used as PCI RST in applications where the device is a PCI agent, deviates from the standard PCI levels.

Table 48. PCI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
High-level input voltage	$V_{OUT} \geq V_{OH}$ (min) or	V_{IH}	2.0	OV_{DD} + 0.5	V
Low-level input voltage	$V_{OUT} \leq V_{OL}$ (max)	V_{IL}	–0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	I_{OH} = –500 µA	V_{OH}	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	I_{OL} = 1500 µA	V_{OL}	—	$0.1 \times OV_{DD}$	V
Input current	$0 V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 30	µA

Note:
- The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK/PCI_SYNC_IN or CLKIN signal is used as the PCI input clock depending on whether the chip is configured as a host or agent device. CLKIN is used when the device is in host mode.

This table shows the PCI AC timing specifications at 66 MHz.

Table 49. PCI AC Timing Specifications at 66 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4

Table 49. PCI AC Timing Specifications at 66 MHz (continued)

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold from cock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 1 ns skew for 66 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

This table shows the PCI AC timing specifications at 33 MHz.

Table 50. PCI AC Timing Specifications at 33 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, $V_{IH} = 0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 2 ns skew for 33 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

This figure provides the AC test load for PCI.

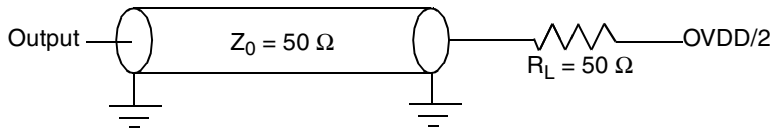


Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

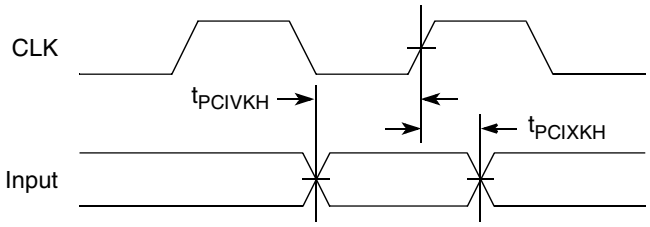


Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

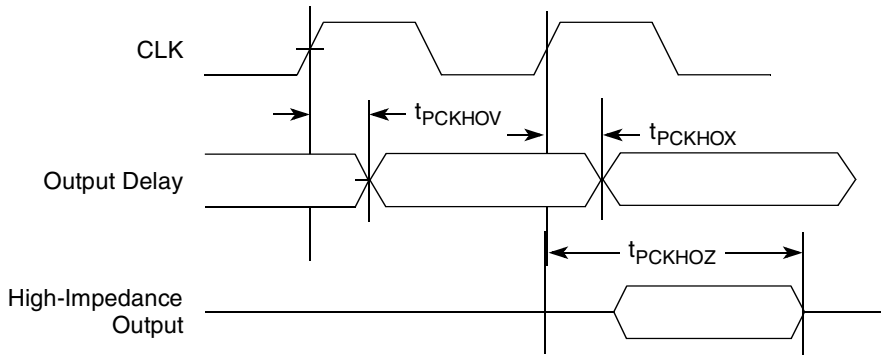


Figure 41. PCI Output AC Timing Measurement Condition

15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

15.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 51. SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ AC Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Note
REFCLK cycle time	t_{REF}	—	10	—	ns	—
REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	t_{REFCJ}	—	—	100	ps	—
REFCLK phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{REFPJ}	–50	—	+50	ps	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CKCJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{CKPJ}	–50	—	+50	ps	2, 3

Notes:
1. All options provide serial interface bit rate of 1.5 and 3.0 Gbps.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10^{-12}.
3. Total peak-to-peak Deterministic Jitter "J_D" should be less than or equal to 50 ps.

15.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

15.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

NOTE

The voltage levels of the transmitter and the receiver depend on the SerDes control registers which should be programmed at the recommended values for PCI Express protocol (that is, L1_nV$_{DD}$ = 1.0 V).

15.4.1 Differential Transmitter (Tx) Output

This table defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 52. Differential Transmitter (Tx) Output Specifications

Parameter	Conditions	Symbol	Min	Typical	Max	Units	Note
Unit interval	Each U_{PETX} is 400 ps ± 300 ppm. U_{PETX} does not account for Spread Spectrum Clock dictated variations.	UI	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{PEDPPTX} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$	$V_{TX-DIFFp-p}$	0.8	—	1.2	V	2
De-emphasized differential output voltage (ratio)	Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition.	$V_{TX-DE-RATIO}$	–3.0	–3.5	–4.0	dB	2
Minimum Tx eye width	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX}$= 0.3 UI.	T_{TX-EYE}	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	2, 3
D+/D– Tx output rise/fall time	—	$T_{TX-RISE}$, $T_{TX-FALL}$	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{PEACPCMTX} = RMS(\lvert V_{TXD+} - V_{TXD-} \rvert/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$	$V_{TX-CM-ACp}$	—	—	20	mV	2
Absolute delta of DC common mode voltage during LO and electrical idle	$\lvert V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)} \rvert <= 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$ [Electrical Idle]	$V_{TX-CM-DC-\ ACTIVE-IDLE-DELTA}$	0	—	100	mV	2

Table 52. Differential Transmitter (Tx) Output Specifications (continued)

Parameter	Conditions	Symbol	Min	Typical	Max	Units	Note
Absolute delta of DC common mode between D+ and D–	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-} \rvert \leq 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} \rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-} \rvert$	$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{PEEIDPTX} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-} \rvert \leq 20$ mV	$V_{TX\text{-}IDLE\text{-}DIFFp}$	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.	$V_{TX\text{-}RCV\text{-}DETECT}$	—	$XPADV_{DD}/2$	600	mV	6
Tx DC common mode voltage	The allowed DC common mode voltage under any conditions.	$V_{TX\text{-}DC\text{-}CM}$	0	$XPADV_{DD}/2$	—	V	6
Tx short circuit current limit	The total current the transmitter can provide when shorted to its ground	$I_{TX\text{-}SHORT}$	—	—	90	mA	—
Minimum time spent in electrical idle	Minimum time a transmitter must be in electrical idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.	$T_{TX\text{-}IDLE\text{-}MIN}$	50	—	—	UI	—
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.	$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	—	—	20	UI	—
Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	Maximum time to meet all Tx specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the Tx to meet all Tx specifications after leaving electrical idle	$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	—	—	20	UI	—
Differential return loss	Measured over 50 MHz to 1.25 GHz.	$RL_{TX\text{-}DIFF}$	12	—	—	dB	4

Table 52. Differential Transmitter (Tx) Output Specifications (continued)

Parameter	Conditions	Symbol	Min	Typical	Max	Units	Note
Common mode return loss	Measured over 50 MHz to 1.25 GHz.	RL_{TX-CM}	6	—	—	dB	4
DC differential Tx impedance	Tx DC differential mode low impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	—
Transmitter DC impedance	Required Tx D+ as well as D– DC impedance during all states	Z_{TX-DC}	40	—	—	Ω	—
Lane-to-Lane output skew	Static skew between any two transmitter lanes within a single link	$L_{TX-SKEW}$	—	—	500 + 2 UI	ps	—
AC coupling capacitor	All transmitters should be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	C_{TX}	75	—	200	nF	—
Crosslink random timeout	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port.	$T_{crosslink}$	0	—	1	ms	7

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 44 and measured over any 250 consecutive Tx UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 42.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance will result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 44 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.

15.4.2 Transmitter Compliance Eye Diagrams

The Tx eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express interconnect + Rx component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

It is recommended that the recovered Tx UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

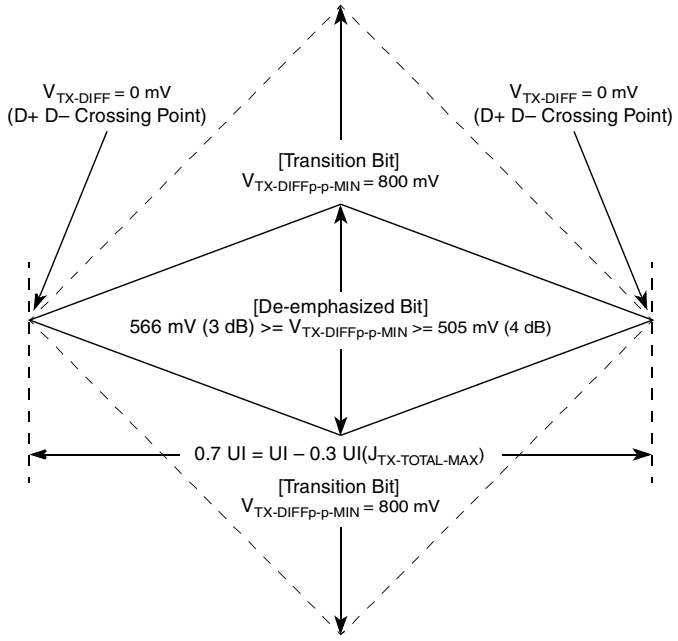


Figure 42. Minimum Transmitter Timing and Voltage Output Compliance Specifications

15.4.3 Differential Receiver (Rx) Input Specifications

This table defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 53. Differential Receiver (Rx) Input Specifications

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unit interval	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	UI	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{PEDPPRX} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$	$V_{RX-DIFFp-p}$	0.175	—	1.200	V	2

Table 53. Differential Receiver (Rx) Input Specifications (continued)

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Minimum receiver eye width	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI.	T_{RX-EYE}	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	2, 3, 7
AC peak common mode input voltage	$V_{PEACPCMRX} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$	$V_{RX-CM-ACp}$	—	—	150	mV	2
Differential return loss	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively.	$RL_{RX-DIFF}$	10	—	—	dB	4
Common mode return loss	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V.	RL_{RX-CM}	6	—	—	dB	4
DC differential input impedance	RX DC differential mode impedance.	$Z_{RX-DIFF-DC}$	80	100	120	Ω	5
DC Input Impedance	Required RX D+ as well as D- DC impedance (50 ± 20% tolerance).	Z_{RX-DC}	40	50	60	Ω	2, 5
Powered down DC input impedance	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power.	$Z_{RX-HIGH-IMP-DC}$	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{PEEIDT} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver	$V_{RX-IDLE-DET-DIFF\ p-p}$	65	—	175	mV	—

Table 53. Differential Receiver (Rx) Input Specifications (continued)

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unexpected Electrical Idle Enter Detect Threshold Integration Time	An unexpected electrical idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	—	—	10	ms	—
Total Skew	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the Rx as well as any delay differences arising from the interconnect itself.	$L_{RX-SKEW}$	—	—	20	ns	—

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the Rx device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 43). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{Rx-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRx-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance will result in a differential return loss greater than or equal to 10 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, C_{Tx}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

15.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 43 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express Rx component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 44) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the

compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. Rx component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 43) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 44). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

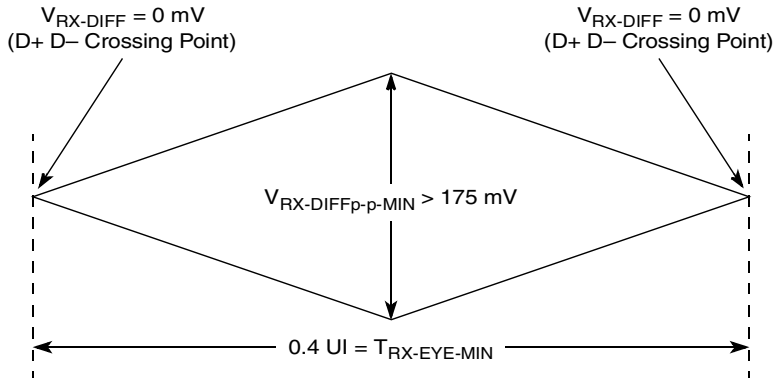


Figure 43. Minimum Receiver Eye Timing and Voltage Compliance Specification

15.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 44.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

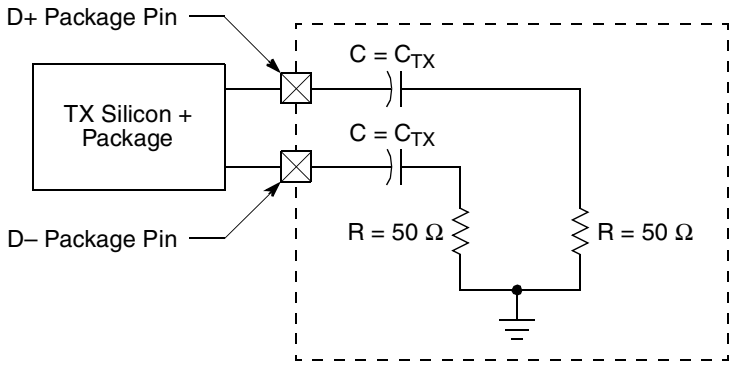


Figure 44. Compliance Test/Measurement Load

16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the MPC8377E. Note that the external cabled applications or long backplane applications (Gen1x and Gen2x) are not supported.

16.1 Requirements for SATA REF_CLK

The reference clock is a single ended input clock required for the SATA interface operation. The AC requirements for the SATA reference clock are listed in the Table 54.

Table 54. SATA Reference Clock Input Requirements

Parameter	Condition	Symbol	Min	Typical	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ frequency range	—	t_{CLK_REF}	—	100/125/150	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ clock frequency tolerance	—	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ reference clock duty cycle	Measured at 1.6V	t_{CLK_DUTY}	40	50	60	%	—

Table 54. SATA Reference Clock Input Requirements (continued)

Parameter	Condition	Symbol	Min	Typical	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ cycle to cycle Clock jitter (period jitter)	Cycle-to-cycle at ref clock input	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ total reference clock jitter, phase jitter (peak-peak)	Peak-to-peak jitter at ref clock input	t_{CLK_PJ}	–50	—	+50	ps	2, 3

Notes:
1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
3. Total peak to peak Deterministic Jitter "D_J" should be less than or equal to 50 ps.

This figure shows the SATA reference clock timing waveform.

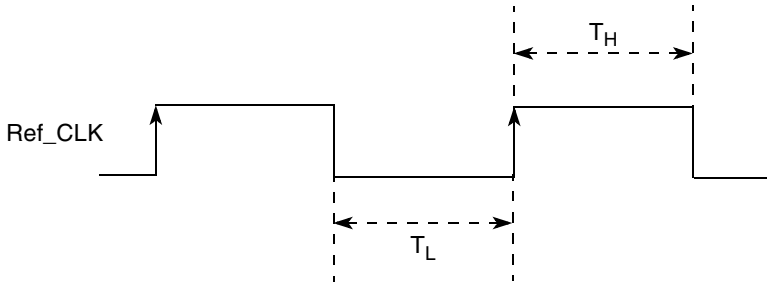


Figure 45. SATA Reference Clock Timing Waveform

16.2 Transmitter (Tx) Output Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G transmitter output characteristics for the SATA interface.

16.2.1 Gen1i/1.5G Transmitter Specifications

This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 55. Gen1i/1.5G Transmitter (Tx) DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 56. Gen1i/1.5G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.355	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.47	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.175	UI_{p-p}	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.22	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.2.2 Gen2i/3G Transmitter Specifications

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 57. Gen 2i/3G Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	550	700	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 58. Gen 2i/3G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB}=f_{BAUD}/10$	$U_{SATA_TXTJfB/10}$	—	—	0.3	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA_TXTJfB/500}$	—	—	0.37	UI_{p-p}	1

Table 58. Gen 2i/3G Transmitter AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.55	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA_TXDJfB/10}$	—	—	0.17	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA_TXDJfB/500}$	—	—	0.19	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3 Differential Receiver (Rx) Input Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G differential receiver input AC characteristics.

16.3.1 Gen1i/1.5G Receiver Specifications

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 59. Gen1i/1.5G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV_{p-p}	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 60. Gen 1i/1.5G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.43	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.60	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.25	UI_{p-p}	1

Table 60. Gen 1i/1.5G Receiver AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3.2 Gen2i/3G Receiver (Rx) Specifications

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 61. Gen2i/3G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	275	500	750	mVp-p	1
Differential RX input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the differential receiver output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 62. Gen 2i/3G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel Speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA_TXTJfB/10}$	—	—	0.46	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA_TXTJfB/500}$	—	—	0.60	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.65	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA_TXDJfB/10}$	—	—	0.35	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA_TXDJfB/500}$	—	—	0.42	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

17 Timers

This section describes the DC and AC electrical specifications for the timers of the chip.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 63. Timers DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 64. Timers Input AC Timing Specifications[1]

Parameter	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the timers.

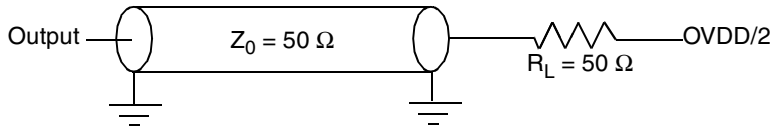


Figure 46. Timers AC Test Load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the chip.

18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 65. GPIO DC Electrical Characteristics

This specification applies when operating at 3.3 V ± 165 mV supply.

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input AC Timing Specifications

Parameter	Symbol	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

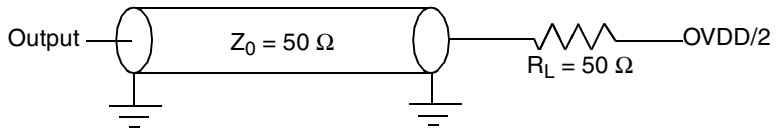


Figure 47. GPIO AC Test Load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the chip.

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 67. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ_OUT}}$, $\overline{\text{MCP_OUT}}$.
2. $\overline{\text{IRQ_OUT}}$ and $\overline{\text{MCP_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	± 30	μA
Output high voltage	I_{OH} = –8.0 mA	V_{OH}	2.4	—	V

Table 69. SPI DC Electrical Characteristics (continued)

Parameter	Condition	Symbol	Min	Max	Unit
Output low voltage	I_{OL} = 8.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

20.2 SPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. The maximum SPICLK input frequency is 66.666 MHz.

This figure provides the AC test load for the SPI.

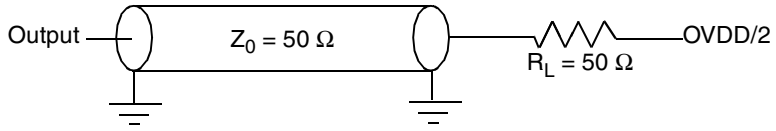
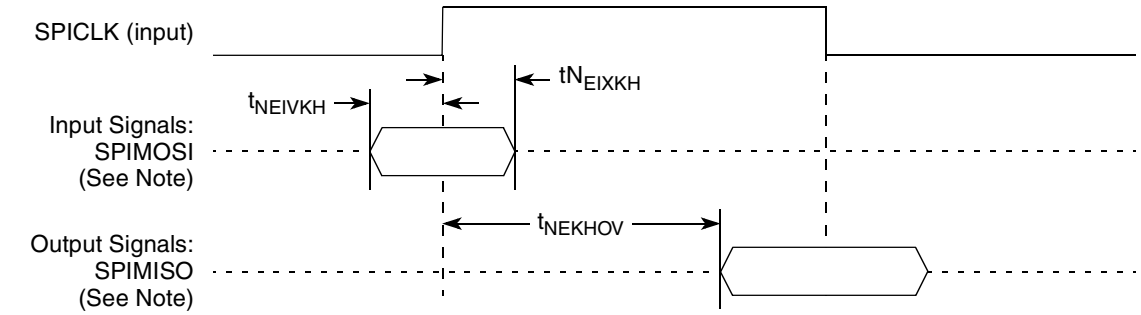


Figure 48. SPI AC Test Load

These figures represent the AC timing from Table 70. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

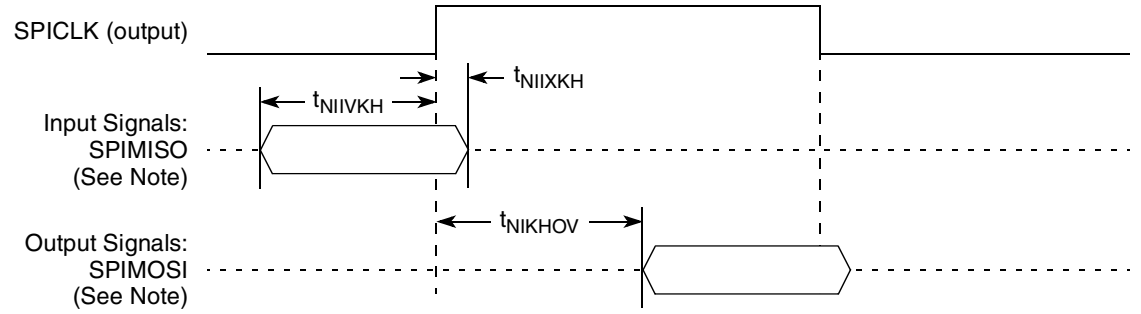
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 49. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 51 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

- **Differential Peak Voltage**, V_{DIFFp}

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

- **Differential Peak-to-Peak**, $V_{DIFFp-p}$

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{_TX}}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 60 as an example for differential waveform.

- **Common Mode Voltage, V_{cm}**

  The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

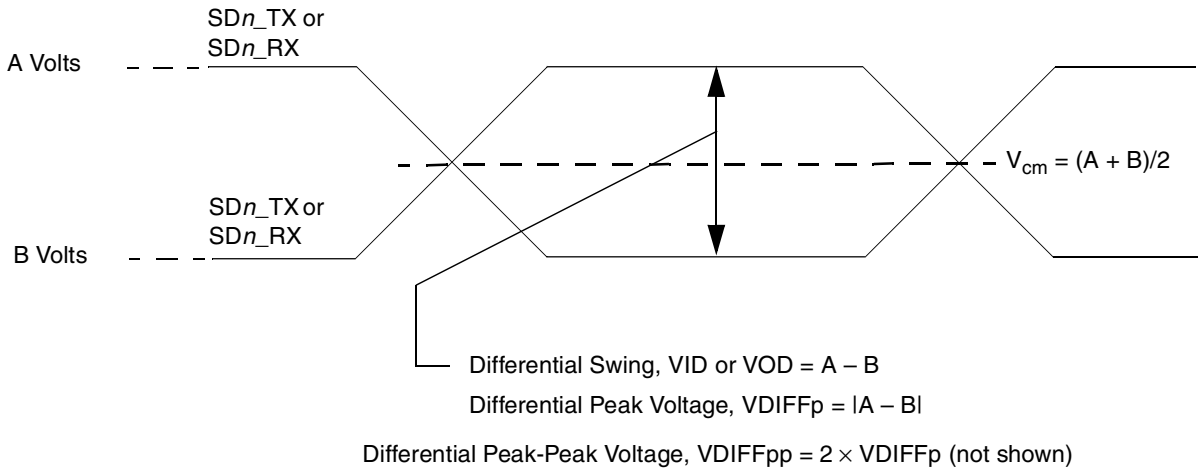


Figure 51. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 $\text{mV}_{\text{p-p}}$, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 $\text{mV}_{\text{p-p}}$.

21.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ for both lanes of SerDes1, and SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ for both lanes of SerDes2.

The following sections describe the SerDes reference clock requirements and some application information.

21.2.1 SerDes Reference Clock Receiver Characteristics

Figure 52 shows a receiver reference diagram of the SerDes reference clocks.

- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 52. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{_REF_CLK}}$) has a 50 Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

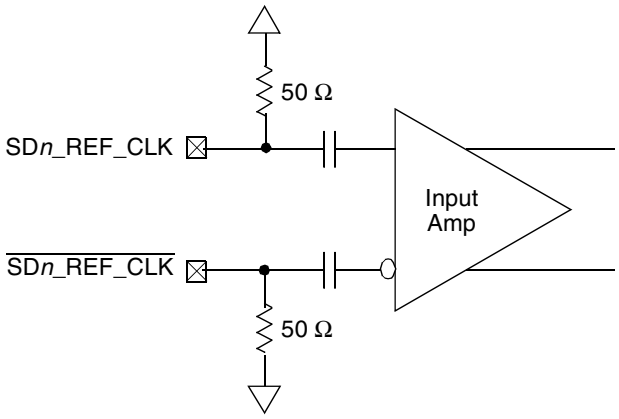


Figure 52. Receiver of SerDes Reference Clocks

21.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the device SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and

greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 21.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 53 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 54 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD _REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV_{p-p} (from V_{min} to V_{max}) with $\overline{SDn_REF_CLK}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 mV and 400 mV. Figure 55 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{SDn_REF_CLK}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

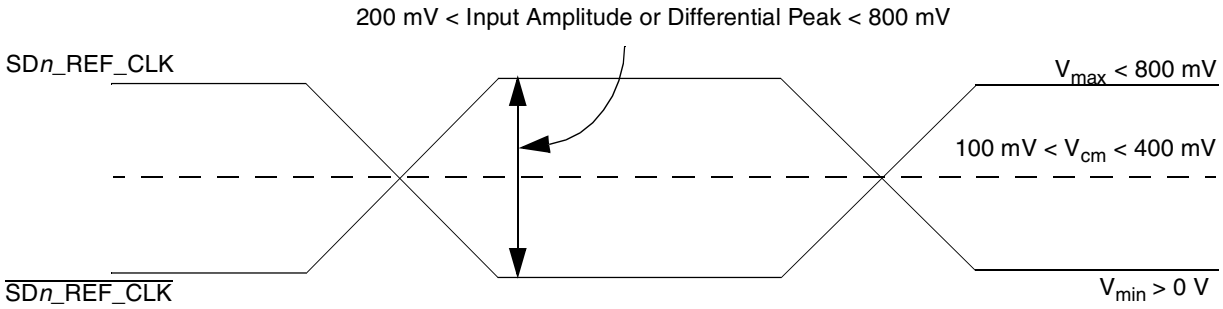


Figure 53. Differential Reference Clock Input DC Requirements (External DC-Coupled)

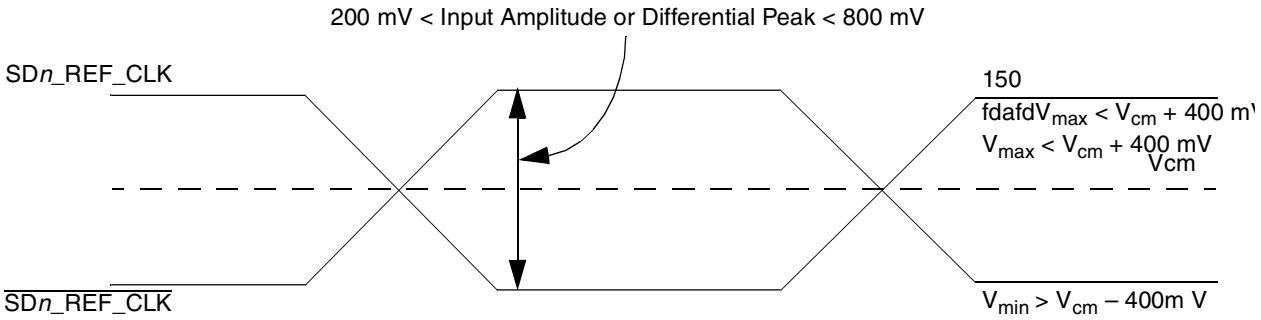


Figure 54. Differential Reference Clock Input DC Requirements (External AC-Coupled)

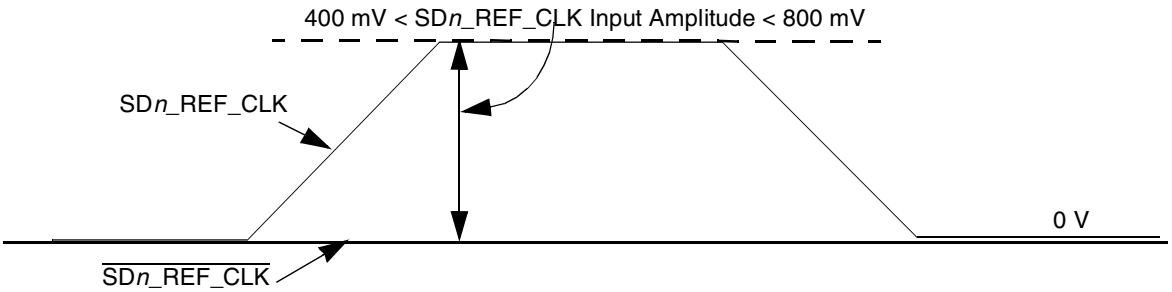


Figure 55. Single-Ended Reference Clock Input DC Requirements

21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 56 to Figure 59 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by the clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the device SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with device SerDes reference clock input's DC requirement.

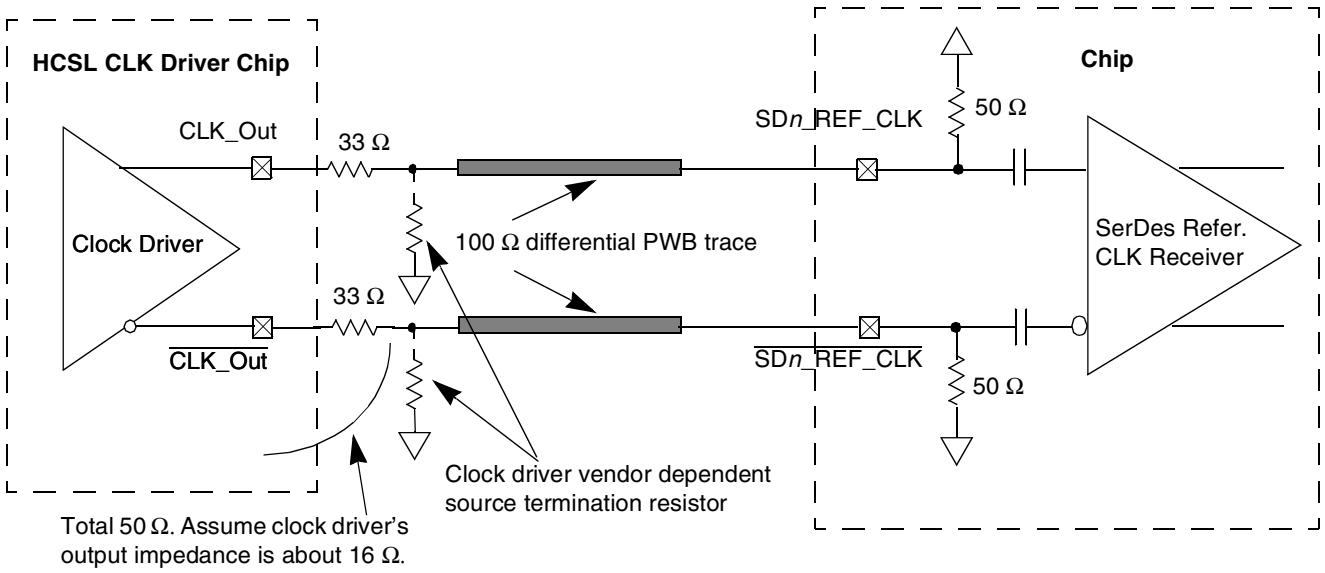


Figure 56. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common-mode voltage is higher than the device SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS

output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

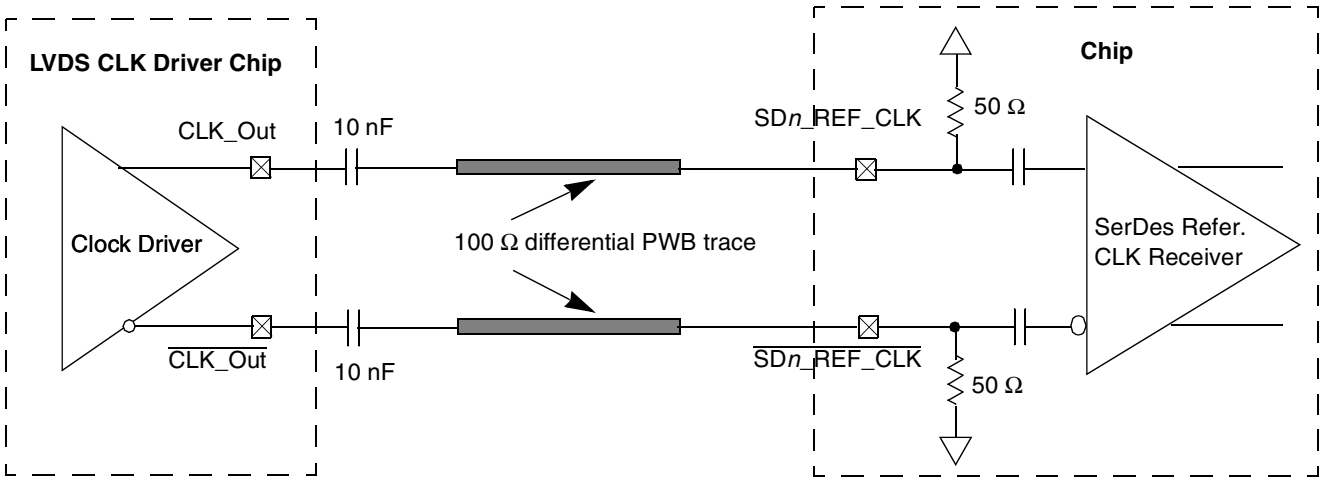


Figure 57. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 58 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with device SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 58 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50 Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the device SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult clock

driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

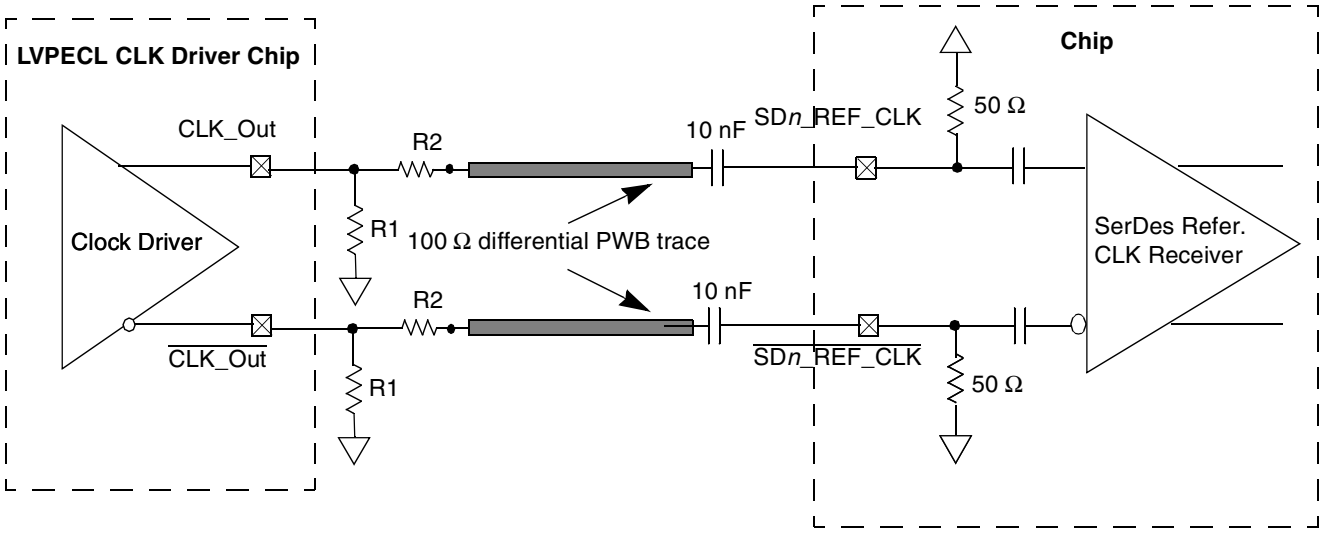


Figure 58. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with device SerDes reference clock input's DC requirement.

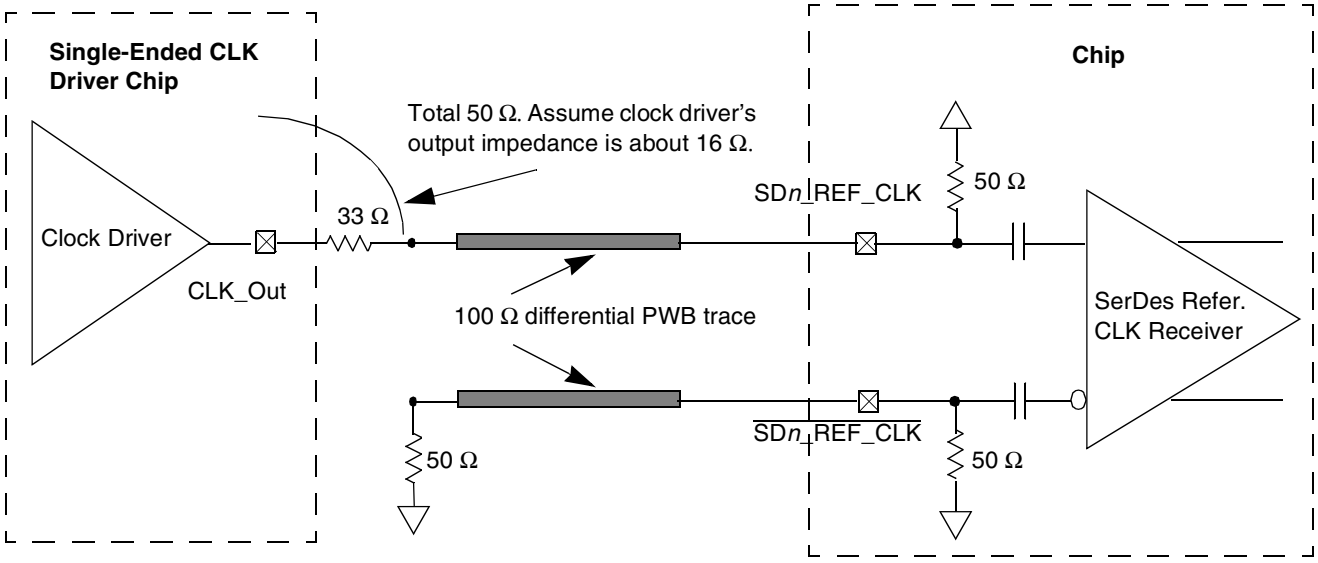


Figure 59. Single-Ended Connection (Reference Only)

21.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for PCI Express .

Table 71. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS} or XV_{DD_SRDS} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{_REF_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 60.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD}n\text{_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 61.

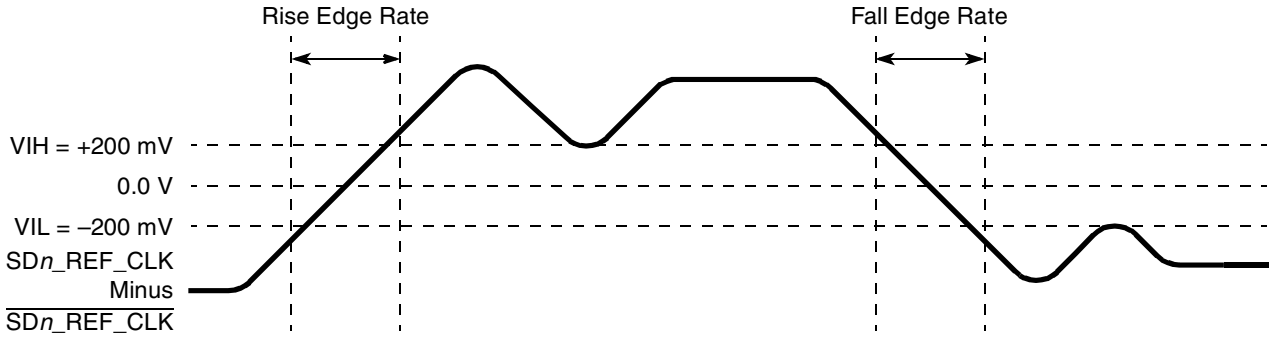


Figure 60. Differential Measurement Points for Rise and Fall Time

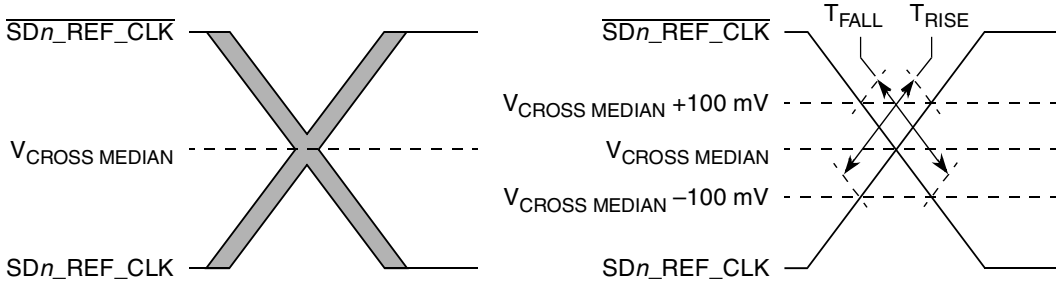


Figure 61. Single-Ended Measurement Points for Rise and Fall Time Matching

21.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

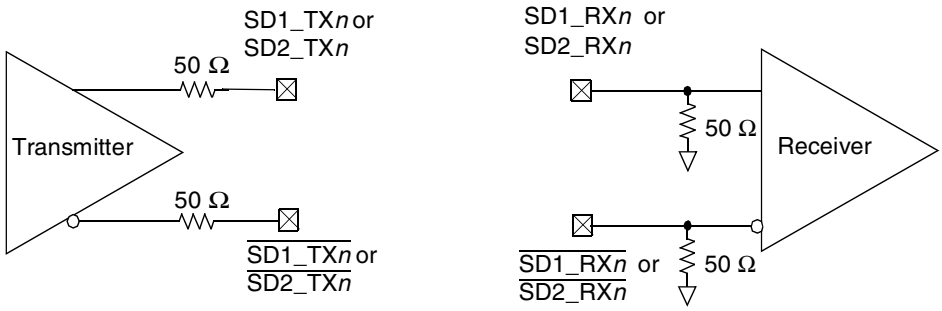


Figure 62. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below in this document based on the application usage:

- Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)"
- Section 15, "PCI Express"
- Section 16, "Serial ATA (SATA)"

Note that an external AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

22 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8377E TePBGA II

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (TePBGA II).

Package outline	31 mm × 31 mm
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm

This figure shows the mechanical dimensions and bottom surface nomenclature of the TEPBGA II package.

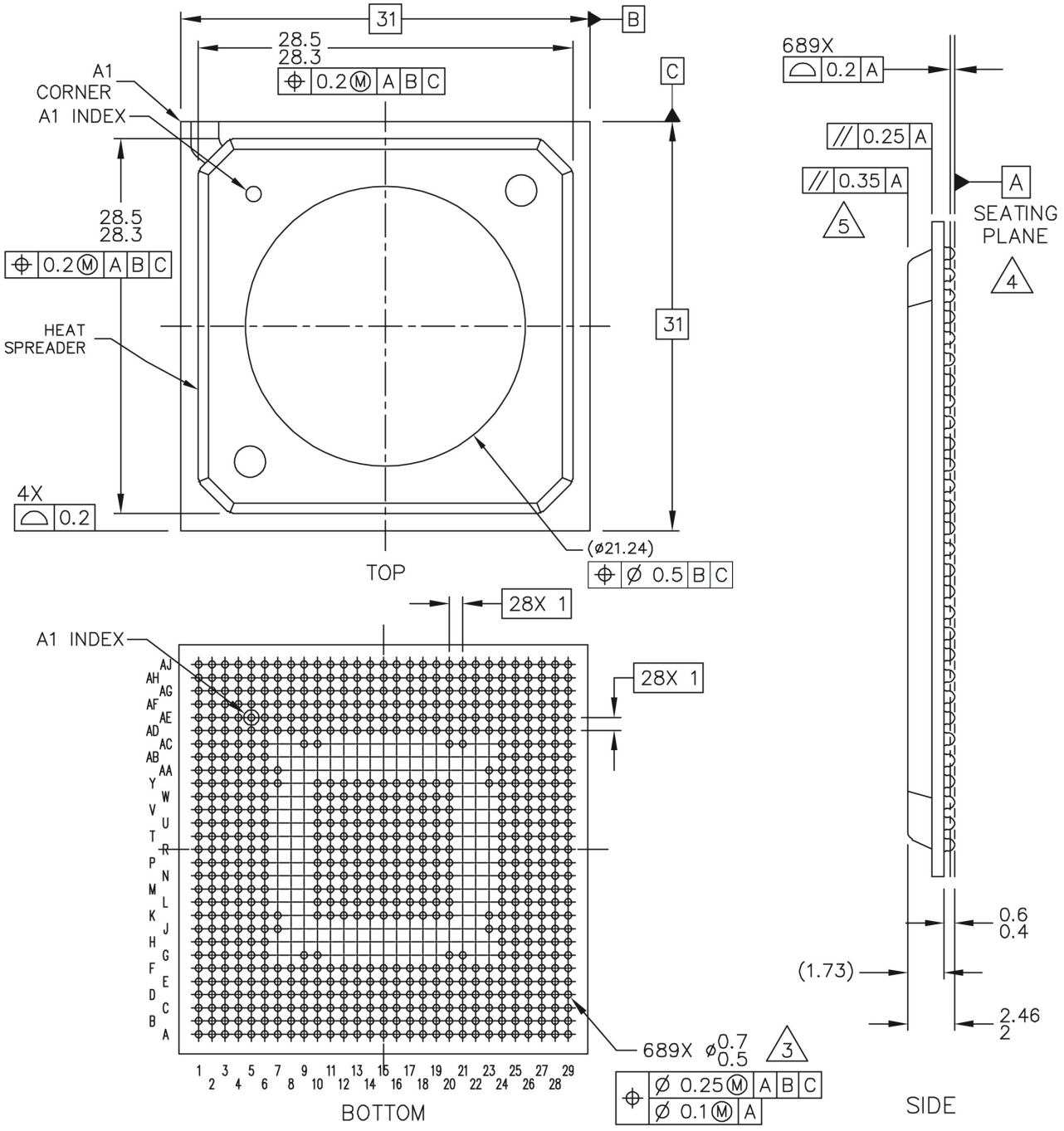


Figure 63. Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II

Note:

1 All dimensions are in millimeters.

2 Dimensioning and tolerancing per ASME Y14. 5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

[5] Parallelism measurement should exclude any effect of mark on top surface of package.

22.2 Pinout Listings

This table provides the pinout listing for the TePBGA II package.

Table 72. TePBGA II Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
Clock Signals				
CLKIN	K24	I	OVDD	—
PCI_CLK/PCI_SYNC_IN	C10	I	OVDD	—
PCI_SYNC_OUT	N24	O	OVDD	3
PCI_CLK0	L24	O	OVDD	—
PCI_CLK1	M24	O	OVDD	—
PCI_CLK2	M25	O	OVDD	—
PCI_CLK3	M26	O	OVDD	—
PCI_CLK4	L26	O	OVDD	—
RTC/PIT_CLOCK	AF11	I	OVDD	—
DDR SDRAM Memory Interface				
MA0	U3	O	GVDD	—
MA1	U1	O	GVDD	—
MA2	T5	O	GVDD	—
MA3	T3	O	GVDD	—
MA4	T2	O	GVDD	—
MA5	T1	O	GVDD	—
MA6	R1	O	GVDD	—
MA7	P2	O	GVDD	—
MA8	P1	O	GVDD	—
MA9	N4	O	GVDD	—
MA10	V3	O	GVDD	—
MA11	M5	O	GVDD	—
MA12	N1	O	GVDD	—
MA13	M2	O	GVDD	—
MA14	M1	O	GVDD	—
MBA0	U5	O	GVDD	—
MBA1	U4	O	GVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MBA2	M3	O	GVDD	—
MCAS_B	W5	O	GVDD	—
MCK_B0	H1	O	GVDD	—
MCK_B1	K1	O	GVDD	—
MCK_B2	V1	O	GVDD	—
MCK_B3	W2	O	GVDD	—
MCK_B4	AA1	O	GVDD	—
MCK_B5	AB2	O	GVDD	—
MCK0	J1	O	GVDD	—
MCK1	L1	O	GVDD	—
MCK2	V2	O	GVDD	—
MCK3	W1	O	GVDD	—
MCK4	Y1	O	GVDD	—
MCK5	AB1	O	GVDD	—
MCKE0	M4	O	GVDD	3
MCKE1	R5	O	GVDD	3
MCS_B0	W3	O	GVDD	—
MCS_B1	P3	O	GVDD	—
MCS_B2	T4	O	GVDD	—
MCS_B3	R4	O	GVDD	—
MDIC0	AH8	I/O	GVDD	9
MDIC1	AJ8	I/O	GVDD	9
MDM0	B6	O	GVDD	—
MDM1	B2	O	GVDD	—
MDM2	E2	O	GVDD	—
MDM3	E1	O	GVDD	—
MDM4	Y6	O	GVDD	—
MDM5	AC6	O	GVDD	—
MDM6	AE6	O	GVDD	—
MDM7	AJ4	O	GVDD	—
MDM8	L6	O	GVDD	—
MDQ0	A8	I/O	GVDD	11
MDQ1	A6	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ2	C7	I/O	GVDD	11
MDQ3	D8	I/O	GVDD	11
MDQ4	A7	I/O	GVDD	11
MDQ5	A5	I/O	GVDD	11
MDQ6	A3	I/O	GVDD	11
MDQ7	C6	I/O	GVDD	11
MDQ8	D7	I/O	GVDD	11
MDQ9	E8	I/O	GVDD	11
MDQ10	B1	I/O	GVDD	11
MDQ11	D5	I/O	GVDD	11
MDQ12	B3	I/O	GVDD	11
MDQ13	D6	I/O	GVDD	11
MDQ14	C3	I/O	GVDD	11
MDQ15	C2	I/O	GVDD	11
MDQ16	D4	I/O	GVDD	11
MDQ17	E6	I/O	GVDD	11
MDQ18	F6	I/O	GVDD	11
MDQ19	G4	I/O	GVDD	11
MDQ20	F8	I/O	GVDD	11
MDQ21	E4	I/O	GVDD	11
MDQ22	C1	I/O	GVDD	11
MDQ23	G6	I/O	GVDD	11
MDQ24	F2	I/O	GVDD	11
MDQ25	G5	I/O	GVDD	11
MDQ26	H6	I/O	GVDD	11
MDQ27	H4	I/O	GVDD	11
MDQ28	D1	I/O	GVDD	11
MDQ29	G3	I/O	GVDD	11
MDQ30	H5	I/O	GVDD	11
MDQ31	F1	I/O	GVDD	11
MDQ32	W6	I/O	GVDD	11
MDQ33	AC1	I/O	GVDD	11
MDQ34	AC3	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ35	AE1	I/O	GVDD	11
MDQ36	V6	I/O	GVDD	11
MDQ37	Y5	I/O	GVDD	11
MDQ38	AA4	I/O	GVDD	11
MDQ39	AB6	I/O	GVDD	11
MDQ40	AD3	I/O	GVDD	11
MDQ41	AC4	I/O	GVDD	11
MDQ42	AD4	I/O	GVDD	11
MDQ43	AF1	I/O	GVDD	11
MDQ44	AE4	I/O	GVDD	11
MDQ45	AC5	I/O	GVDD	11
MDQ46	AE2	I/O	GVDD	11
MDQ47	AE3	I/O	GVDD	11
MDQ48	AG1	I/O	GVDD	11
MDQ49	AG2	I/O	GVDD	11
MDQ50	AG3	I/O	GVDD	11
MDQ51	AF5	I/O	GVDD	11
MDQ52	AE5	I/O	GVDD	11
MDQ53	AD7	I/O	GVDD	11
MDQ54	AH2	I/O	GVDD	11
MDQ55	AG4	I/O	GVDD	11
MDQ56	AH3	I/O	GVDD	11
MDQ57	AG5	I/O	GVDD	11
MDQ58	AF8	I/O	GVDD	11
MDQ59	AJ5	I/O	GVDD	11
MDQ60	AF6	I/O	GVDD	11
MDQ61	AF7	I/O	GVDD	11
MDQ62	AH6	I/O	GVDD	11
MDQ63	AH7	I/O	GVDD	11
MDQS0	C8	I/O	GVDD	11
MDQS1	C4	I/O	GVDD	11
MDQS2	E3	I/O	GVDD	11
MDQS3	G2	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQS4	AB5	I/O	GVDD	11
MDQS5	AD1	I/O	GVDD	11
MDQS6	AH1	I/O	GVDD	11
MDQS7	AJ3	I/O	GVDD	11
MDQS8	G1	I/O	GVDD	11
MECC0/MSRCID0	J6	I/O	GVDD	—
MECC1/MSRCID1	J3	I/O	GVDD	—
MECC2/MSRCID2	K2	I/O	GVDD	—
MECC3/MSRCID3	K3	I/O	GVDD	—
MECC4/MSRCID4	J5	I/O	GVDD	—
MECC5/MDVAL	J2	I/O	GVDD	—
MECC6	L5	I/O	GVDD	—
MECC7	L2	I/O	GVDD	—
MODT0	N5	O	GVDD	6
MODT1	U6	O	GVDD	6
MODT2	M6	O	GVDD	6
MODT3	P6	O	GVDD	6
MRAS_B	AA3	O	GVDD	—
MVREF1	K4	I	GVDD	11
MVREF2	W4	I	GVDD	11
MWE_B	Y2	O	GVDD	—
DUART Interface				
UART_SIN1/ MSRCID2/LSRCID2	L28	I/O	OVDD	—
UART_SOUT1/ MSRCID0/LSRCID0	L27	O	OVDD	—
UART_CTS_B[1]/ MSRCID4/LSRCID4	K26	I/O	OVDD	—
UART_RTS_B1	N27	O	OVDD	—
UART_SIN2/ MSRCID3/LSRCID3	K27	I/O	OVDD	—
UART_SOUT2/ MSRCID1/LSRCID1	K28	O	OVDD	—
UART_CTS_B[2]/ MDVAL/LDVAL	K29	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA25/LAD30	D29	I/O	LBVDD	—
LA26/LAD31	E20	I/O	LBVDD	—
LA27	H26	O	LBVDD	—
LA28	C29	O	LBVDD	—
LA29	E28	O	LBVDD	—
LA30	B26	O	LBVDD	—
LA31	J25	O	LBVDD	—
LA10/LALE	H29	O	LBVDD	—
LBCTL	A22	O	LBVDD	—
LCLK0	B22	O	LBVDD	—
LCLK1	C23	O	LBVDD	—
LCLK2	B23	O	LBVDD	—
LCS_B0	D25	O	LBVDD	—
LCS_B1	F19	O	LBVDD	—
LCS_B2	C27	O	LBVDD	—
LCS_B3	D24	O	LBVDD	—
LCS_B4/LDP0	C24	I/O	LBVDD	—
LCS_B5/LDP1	B29	I/O	LBVDD	—
LA7/LCS_B6/LDP2	E29	I/O	LBVDD	—
LA8/LCS_B7/LDP3	F29	I/O	LBVDD	—
LFCLE/LGPL0	D21	O	LBVDD	—
LFALE/LGPL1	A26	O	LBVDD	—
LFRE_B/LGPL2/LOE_B	F22	O	LBVDD	—
LFWP_B/LGPL3	C21	O	LBVDD	—
LGPL4/LFRB_B/LGTA_B/ LUPWAIT/LPBSE	J29	I/O	LBVDD	16
LA9/LGPL5	G29	O	LBVDD	—
LSYNC_IN	A21	I	LBVDD	—
LSYNC_OUT	D23	O	LBVDD	—
LWE_B0/LFWE0/LBS_B0	E22	O	LBVDD	—
LWE_B1/LFWE1/LBS_B1	B25	O	LBVDD	—
LWE_B2/LFWE2/LBS_B2	E27	O	LBVDD	—
LWE_B3/LFWE3/LBS_B3	F28	O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
eTSEC1/GPIO1/GPIO2/CFG_RESET Interface				
TSEC1_COL/GPIO2[20]	AF22	I/O	LVDD1	16
TSEC1_CRS/GPIO2[21]	AE20	I/O	LVDD1	16
TSEC1_GTX_CLK	AJ25	O	LVDD1	16
TSEC1_RX_CLK	AG22	I	LVDD1	16
TSEC1_RX_DV	AD19	I	LVDD1	16
TSEC1_RX_ER/GPIO2[25]	AD20	I/O	LVDD1	16
TSEC1_RXD0	AD22	I	LVDD1	16
TSEC1_RXD1	AE21	I	LVDD1	16
TSEC1_RXD2	AE22	I	LVDD1	16
TSEC1_RXD3	AD21	I	LVDD1	16
TSEC1_TX_CLK	AJ22	I	LVDD1	16
TSEC1_TX_EN	AG23	O	LVDD1	16
TSEC1_TX_ER/CFG_LBMUX	AH22	I/O	LVDD1	16
TSEC1_TXD0/ CFG_RESET_SOURCE[0]	AD23	I/O	LVDD1	16
TSEC1_TXD1/ CFG_RESET_SOURCE[1]	AE23	I/O	LVDD1	16
TSEC1_TXD2/ CFG_RESET_SOURCE[2]	AF23	I/O	LVDD1	16
TSEC1_TXD3/ CFG_RESET_SOURCE[3]	AJ24	I/O	LVDD1	16
EC_GTX_CLK125	AH24	I	LVDD1	16
EC_MDC/CFG_CLKIN_DIV	AJ21	I/O	LVDD1	16
EC_MDIO	AH21	I/O	LVDD1	16
eTSEC2/GPIO1 Interface				
TSEC2_COL/GPIO1[21]/ TSEC1_TMR_TRIG1	AJ27	I/O	LVDD2	16
TSEC2_CRS/GPIO1[22]/ TSEC1_TMR_TRIG2	AG29	I/O	LVDD2	16
TSEC2_GTX_CLK	AF28	O	LVDD2	16
TSEC2_RX_CLK/ TSEC1_TMR_CLK	AF25	I	LVDD2	16
TSEC2_RX_DV/GPIO1[23]	AF26	I/O	LVDD2	16
TSEC2_RX_ER/GPIO1[25]	AG25	I/O	LVDD2	16

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_RXD0/GPIO1[16]	AE28	I/O	LVDD2	16
TSEC2_RXD1/GPIO1[15]	AE29	I/O	LVDD2	16
TSEC2_RXD2/GPIO1[14]	AH26	I/O	LVDD2	16
TSEC2_RXD3/GPIO1[13]	AH25	I/O	LVDD2	16
TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK	AG28	I/O	LVDD2	16
TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2	AJ26	I/O	LVDD2	16
TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1	AG26	I/O	LVDD2	16
TSEC2_TXD0/GPIO1[20]	AH28	I/O	LVDD2	16
TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1	AF27	I/O	LVDD2	16
TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2	AJ28	I/O	LVDD2	16
TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3	AF29	I/O	LVDD2	16
GPIO1 Interface				
GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B	P25	I/O	OVDD	—
GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B	N25	I/O	OVDD	—
GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B	N26	I/O	OVDD	—
GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B	B9	I/O	OVDD	—
GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B	N29	I/O	OVDD	—
GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B	M29	I/O	OVDD	—
GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B	A9	I/O	OVDD	—
GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B	B10	I/O	OVDD	—
GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B	J26	I/O	OVDD	—
GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B	J24	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GPIO1[10]/GTM1_TGATE4_B/ GTM2_TGATE3_B/DACK3_B	J27	I/O	OVDD	—
GPIO1[11]/GTM1_TOUT4_B/ GTM2_TOUT3_B/DDONE3_B	P24	I/O	OVDD	—
USB/GPIO2 Interface				
USBDR_CLK/GPIO2[23]	AJ11	I/O	OVDD	—
USBDR_DIR_DPPULLUP/ GPIO2[9]	AG12	I/O	OVDD	—
USBDR_NXT/GPIO2[8]	AJ10	I/O	OVDD	—
USBDR_PCTL0/GPIO2[11]/ SD_DAT2	AF10	I/O	OVDD	—
USBDR_PCTL1/GPIO2[22]/ SD_DAT3	AE9	I/O	OVDD	—
USBDR_PWRFAULT/ GPIO2[10]/SD_DAT1	AG13	I/O	OVDD	—
USBDR_STP_SUSPEND	AH12	O	OVDD	12
USBDR_D0_ENABLEN/ GPIO2[0]	AG10	I/O	OVDD	—
USBDR_D1_SER_TXD/ GPIO2[1]	AF13	I/O	OVDD	—
USBDR_D2_VMO_SE0/ GPIO2[2]	AG11	I/O	OVDD	—
USBDR_D3_SPEED/GPIO2[3]	AH11	I/O	OVDD	—
USBDR_D4_DP/GPIO2[4]	AG9	I/O	OVDD	—
USBDR_D5_DM/GPIO2[5]	AF9	I/O	OVDD	—
USBDR_D6_SER_RCV/ GPIO2[6]	AH13	I/O	OVDD	—
USBDR_D7_DRVVBUS/ GPIO2[7]	AH10	I/O	OVDD	—
I^2C Interface				
IIC1_SCL	C12	I/O	OVDD	2
IIC1_SDA	B12	I/O	OVDD	2
IIC2_SCL	A10	I/O	OVDD	2
IIC2_SDA	A12	I/O	OVDD	2
JTAG Interface				
TCK	B13	I	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TDI	E14	I	OVDD	4
TDO	C13	O	OVDD	3
TMS	A13	I	OVDD	4
TRST_B	E11	I	OVDD	4
PCI Signals				
PCI_AD0	P26	I/O	OVDD	—
PCI_AD1	N28	I/O	OVDD	—
PCI_AD2	P29	I/O	OVDD	—
PCI_AD3	P27	I/O	OVDD	—
PCI_AD4	R26	I/O	OVDD	—
PCI_AD5	R29	I/O	OVDD	—
PCI_AD6	T24	I/O	OVDD	—
PCI_AD7	T25	I/O	OVDD	—
PCI_AD8	R27	I/O	OVDD	—
PCI_AD9	P28	I/O	OVDD	—
PCI_AD10	U25	I/O	OVDD	—
PCI_AD11	R28	I/O	OVDD	—
PCI_AD12	U26	I/O	OVDD	—
PCI_AD13	U24	I/O	OVDD	—
PCI_AD14	T29	I/O	OVDD	—
PCI_AD15	V24	I/O	OVDD	—
PCI_AD16	Y26	I/O	OVDD	—
PCI_AD17	V28	I/O	OVDD	—
PCI_AD18	AA25	I/O	OVDD	—
PCI_AD19	AA26	I/O	OVDD	—
PCI_AD20	W29	I/O	OVDD	—
PCI_AD21	AA24	I/O	OVDD	—
PCI_AD22	AA27	I/O	OVDD	—
PCI_AD23	AC26	I/O	OVDD	—
PCI_AD24	AB25	I/O	OVDD	—
PCI_AD25	AB24	I/O	OVDD	—
PCI_AD26	AA28	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD27	AA29	I/O	OVDD	—
PCI_AD28	AC24	I/O	OVDD	—
PCI_AD29	AC25	I/O	OVDD	—
PCI_AD30	AB28	I/O	OVDD	—
PCI_AD31	AE24	I/O	OVDD	—
PCI_C_BE_B0	T26	I/O	OVDD	—
PCI_C_BE_B1	T28	I/O	OVDD	—
PCI_C_BE_B2	V29	I/O	OVDD	—
PCI_C_BE_B3	Y29	I/O	OVDD	—
PCI_DEVSEL_B	U28	I/O	OVDD	5
PCI_FRAME_B	V27	I/O	OVDD	—
PCI_GNT_B0	AE27	I/O	OVDD	—
PCI_GNT_B[1]/ CPCI_HS_LED	AC28	O	OVDD	—
PCI_GNT_B[2]/ CPCI_HS_ENUM	AD27	O	OVDD	—
PCI_GNT_B[3]/PCI_PME	AC27	O	OVDD	—
PCI_GNT_B[4]	AE25	O	OVDD	—
PCI_IDSEL	W28	I	OVDD	5
PCI_INTA_B/IRQ_OUT_B	AD29	O	OVDD	2
PCI_IRDY_B	U29	I/O	OVDD	5
PCI_PAR	V25	I/O	OVDD	—
PCI_PERR_B	Y25	I/O	OVDD	5
PCI_REQ_B0	AE26	I/O	OVDD	—
PCI_REQ_B[1]/CPCI_HS_ES	AC29	I	OVDD	—
PCI_REQ_B2	AB29	I	OVDD	—
PCI_REQ_B3	AD26	I	OVDD	—
PCI_REQ_B4	W27	I	OVDD	—
PCI_RESET_OUT_B	AD28	O	OVDD	—
PCI_SERR_B	V26	I/O	OVDD	5
PCI_STOP_B	W26	I/O	OVDD	5
PCI_TRDY_B	Y24	I/O	OVDD	5
M66EN	AD15	I	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Programmable Interrupt Controller (PIC) Interface				
MCP_OUT_B	AD14	O	OVDD	2
IRQ_B0/MCP_IN_B/GPIO2[12]	F9	I/O	OVDD	—
IRQ_B1/GPIO2[13]	E9	I/O	OVDD	—
IRQ_B2/GPIO2[14]	F10	I/O	OVDD	—
IRQ_B3/GPIO2[15]	D9	I/O	OVDD	—
IRQ_B4/GPIO2[16]/SD_WP	C9	I/O	OVDD	—
IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT	AE10	I/O	OVDD	—
IRQ_B6/GPIO2[18]	AD10	I/O	OVDD	—
IRQ_B7/GPIO2[19]	AD9	I/O	OVDD	—
PMC Interface				
QUIESCE_B	D13	O	OVDD	—
SerDes1 Interface				
L1_SD_IMP_CAL_RX	AJ14	I	L1_XPADVDD	—
L1_SD_IMP_CAL_TX	AG19	I	L1_XPADVDD	—
L1_SD_REF_CLK	AJ17	I	L1_XPADVDD	—
L1_SD_REF_CLK_B	AH17	I	L1_XPADVDD	—
L1_SD_RXA_N	AJ15	I	L1_XPADVDD	—
L1_SD_RXA_P	AH15	I	L1_XPADVDD	—
L1_SD_RXE_N	AJ19	I	L1_XPADVDD	—
L1_SD_RXE_P	AH19	I	L1_XPADVDD	—
L1_SD_TXA_N	AF15	O	L1_XPADVDD	—
L1_SD_TXA_P	AE15	O	L1_XPADVDD	—
L1_SD_TXE_N	AF18	O	L1_XPADVDD	—
L1_SD_TXE_P	AE18	O	L1_XPADVDD	—
L1_SDAVDD_0	AJ18	SerDes PLL Power (1.0 or 1.05 V)	—	—
L1_SDAVSS_0	AG17	SerDes PLL GND	—	—
L1_XCOREVDD	AH14, AJ16, AF17, AH20, AJ20	SerDes Core Power (1.0 or 1.05 V)	—	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
L1_XCOREVSS	AG14, AG15, AG16, AH16, AG18, AG20	SerDes Core GND	—	—
L1_XPADVDD	AE16, AF16, AD18, AE19, AF19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L1_XPADVSS	AF14, AE17, AF20	SerDes I/O GND	—	—
SerDes2 Interface				
L2_SD_IMP_CAL_RX	C19	I	L2_XPADVDD	—
L2_SD_IMP_CAL_TX	C15	I	L2_XPADVDD	—
L2_SD_REF_CLK	B17	I	L2_XPADVDD	—
L2_SD_REF_CLK_B	A17	I	L2_XPADVDD	—
L2_SD_RXA_N	A19	I	L2_XPADVDD	—
L2_SD_RXA_P	B19	I	L2_XPADVDD	—
L2_SD_RXE_N	A15	I	L2_XPADVDD	—
L2_SD_RXE_P	B15	I	L2_XPADVDD	—
L2_SD_TXA_N	D18	O	L2_XPADVDD	—
L2_SD_TXA_P	E18	O	L2_XPADVDD	—
L2_SD_TXE_N	D15	O	L2_XPADVDD	—
L2_SD_TXE_P	E15	O	L2_XPADVDD	—
L2_SDAVDD_0	A16	SerDes PLL Power (1.0 or 1.05 V)	—	—
L2_SDAVSS_0	C17	SerDes PLL GND	—	—
L2_XCOREVDD	A14, B14, D17, B18, B20	SerDes Core Power (1.0 or 1.05 V)	—	—
L2_XCOREVSS	C14, C16, A18, C18, A20, C20	SerDes Core GND	—	—
L2_XPADVDD	D14, E16, F18, D19, E19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L2_XPADVSS	D16, E17, D20	SerDes I/O GND	—	—
SPI Interface				
SPICLK/SD_CLK	AH9	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPIMISO/SD_DAT0	AD11	I/O	OVDD	—
SPIMOSI/SD_CMD	AJ9	I/O	OVDD	—
SPISEL_B/SD_CD	AE11	I	OVDD	—
System Control Interface				
SRESET_B	AD12	I/O	OVDD	2
HRESET_B	AE12	I/O	OVDD	1
PORESET_B	AE14	I	OVDD	—
Test Interface				
TEST	E10	I	OVDD	10
TEST_SEL0	D10	I	OVDD	13
TEST_SEL1	D12	I	OVDD	13
Thermal Management				
Reserved	F15	I	—	14
Power Supply Signals				
LVDD1	AC21, AG21, AH23	Power for eTSEC 1 I/O (2.5 V, 3.3 V)	LVDD1	—
LVDD2	AG24, AH27, AH29	Power for eTSEC 2 I/O (2.5 V, 3.3 V)	LVDD2	—
LBVDD	G20, D22, A24, G26, D27, A28	Power for eLBC (3.3, 2.5, or 1.8 V)	LBVDD	—
VDD	K10, L10, M10, N10, P10, R10, T10, U10, V10, W10, Y10, K11, R11, Y11, K12, Y12, K13, Y13, K14, Y14, K15, L15, W15, Y15, K16, Y16, K17, Y17, K18, Y18, K19, R19, Y19, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20	Power for Core (1.0 V or 1.5 V)	VDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GND (VSS)	A1, AJ1, H2, N2, AA2, AD2, D3, R3, AF3, A4, F4, J4, L4, V4, Y4, AB4, B5, E5, P5, AH5, K6, T6, AA6, AD6, AG6, F7, J7, Y7, AJ7, B8, AE8, AG8, G9, AC9,B11, D11, F11, L11, M11, N11, P11, T11, U11, V11, W11,L12, M12, N12, P12, R12, T12, U12, V12, W12, E12, E13, L13, M13, N13, P13, R13, T13, U13, V13, W13, AE13, AJ13, F14, L14, M14, N14, P14, R14, T14, U14, V14, W14, M15, N15, P15, R15, T15, U15, V15, L16, M16, N16, P16, R16, T16, U16, V16, W16, L17, M17, N17, P17, R17, T17, U17, V17, W17, L18, M18, N18, P18, R18, T18, U18, V18, W18, L19, M19, N19, P19, T19, U19, V19, W19, AC20, G21, AF21, C22, J23, AA23, AJ23, B24, W24, AF24, K25, R25, AD25, D26, G27, M27, T27, Y27, AB27, AG27, A29, AJ29	—	—	—
AVDD_C	AD13	Power for e300 core PLL (1.0 V or 1.05 V)	—	15
AVDD_L	F13	Power for eLBC PLL (1.0 V or 1.05 V)	—	15
AVDD_P	F12	Power for system PLL (1.0 V or 1.05 V)	—	15
GVDD	A2, D2, R2, U2, AC2, AF2, AJ2, F3, H3, L3, N3, Y3, AB3, B4, P4, AF4, AH4, C5, F5, K5, V5, AA5, AD5, N6, R6, AJ6, B7, E7, K7, AA7, AE7, AG7, AD8	Power for DDR SDRAM I/O Voltage (2.5 or 1.8 V)	GVDD	—
OVDD	AC10, AF12, AJ12, K23, Y23, R24, AD24, L25, W25, AB26, U27, M28, Y28, G10, A11, C11	PCI, USB, and other Standard (3.3 V)	OVDD	—
No Connect				
NC	F16, F17, AD16, AD17	—	—	8
Pull Down				

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Pull Down	B16, AH18	—	—	7

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OVDD.
3. This output is actively driven during reset rather than being released to high impedance during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI Specification recommendation and see AN3665, “MPC837xE Design Checklist,” for more details.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND using a 0 Ω resistor.
8. This pin must always be left not connected.
9. For DDR2 operation, it is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.
10. This pin must always be tied low. If it is left floating it may cause the device to malfunction.
11. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.
12. This pin must not be pulled down during PORESET.
13. This pin must always be tied to OVDD.
14. Open or tie to GND.
15. Voltage settings are dependent on the frequency used; see Table 3.
16. See AN3665, “MPC837xE Design Checklist,” for proper termination.

23 Clocking

This figure shows the internal distribution of clocks within this chip.

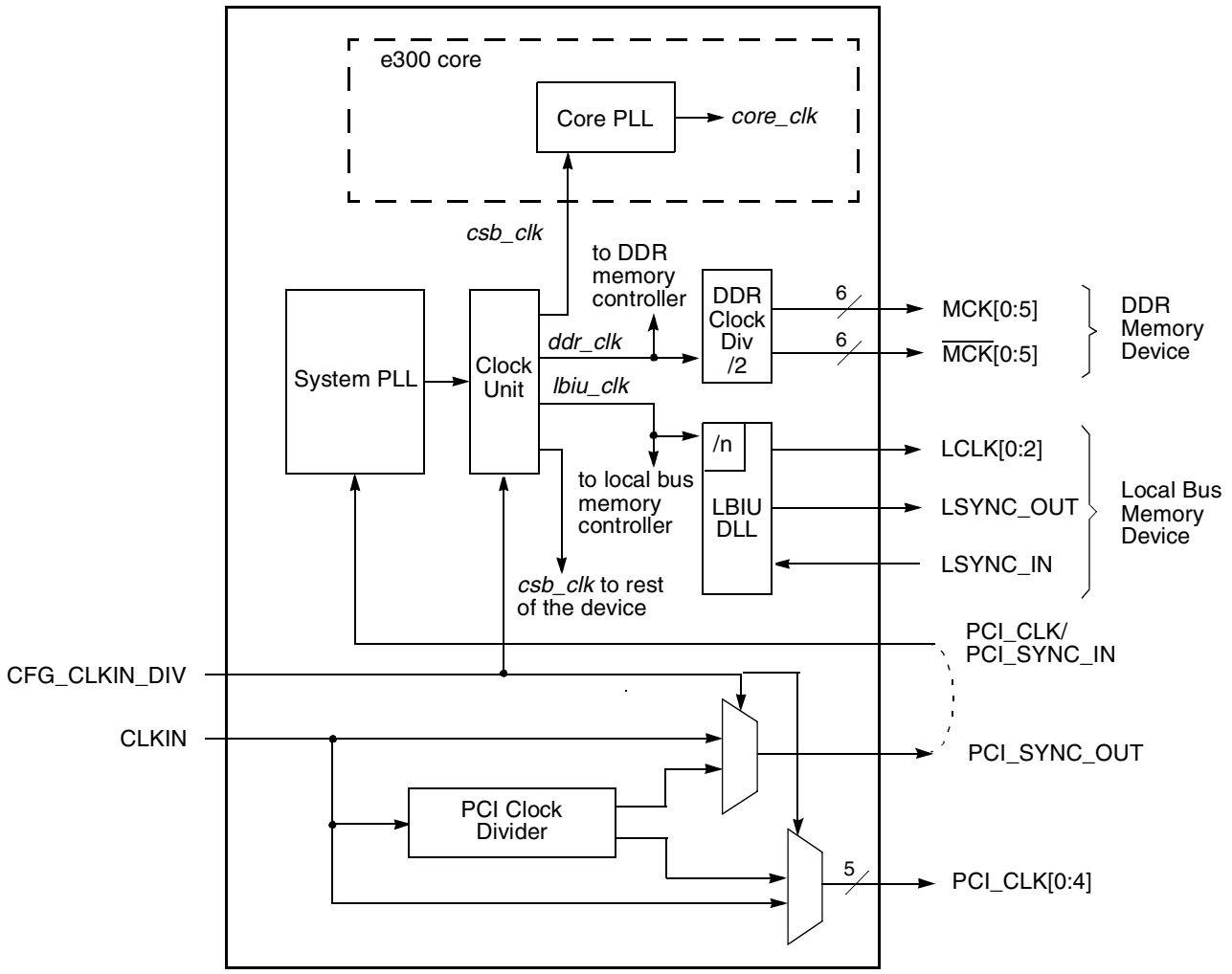


Figure 64. Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether CFG_CLKIN_DIV is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the CLKIN signal should be tied to GND.

As shown in Figure 64, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF \qquad \text{Eqn. 20}$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low register (RCWLR) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8379E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr_clk = csb_clk \times (1 + RCWLR[DDRCM]) \qquad \text{Eqn. 21}$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu_clk = csb_clk \times (1 + RCWLR[LBCM]) \qquad \text{Eqn. 22}$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:2]). The eLBC clock divider ratio is controlled by LCRR[CLKDIV].

Some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 73 specifies which units have a configurable clock frequency.

Table 73. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1, eTSEC2	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
eSDHC and I^2C1[1]	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security block	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	csb_clk	Off, *csb_clk*

Table 73. Configurable Clock Units (continued)

Unit	Default Frequency	Options
PCI Express1, 2	csb_clk/3	Off, c*sb_clk, csb_clk/2, csb_clk/3*
SATA1, 2	csb_clk/3	Off, *csb_clk*

1 This only applies to I^2C1 (I^2C2 clock is not configurable).

This table provides the operating frequencies for the TePBGA II package under recommended operating conditions (see Table 3).

Table 74. Operating Frequencies for TePBGA II

Parameter[1]	Minimum Operating Frequency (MHz)	Maximum Operating Frequency (MHz)
e300 core frequency (*core_clk*)	333	800
Coherent system bus frequency (*csb_clk*)	133	400
DDR2 memory bus frequency (MCK)[1]	250	400
DDR1 memory bus frequency (MCK) [2]	167	333
Local bus frequency (LCLK*n*)[1]	—	133
Local bus controller frequency (*lbc_clk*)	—	400
PCI input frequency (CLKIN or PCI_CLK)	25	66
eTSEC frequency	133	400
Security encryption controller frequency	—	200
USB controller frequency	—	200
eSDHC controller frequency	—	200
PCI Express controller frequency	—	400
SATA controller frequency	—	200

Notes:
1. The CLKIN frequency, RCWLR[SPMF], and RCWLR[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[xCM] must be programmed such that the maximum internal operating frequency of the Security core, USB modules, SATA, and eSDHC will not exceed their respective value listed in this table.
2. The DDR data rate is 2× the DDR memory bus frequency.
3. The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWLR[LBCM]).

23.1 System PLL Configuration

The system PLL is controlled by the RCWLR[SPMF] parameter. The system PLL VCO frequency depends on RCWLR[DDRCM] and RCWLR[LBCM]. Table 75 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWLR[DDRCM] and RCWLR[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWLR[DDRCM] or RCWLR[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 400–800 MHz.

Table 75. System PLL Multiplication Factors

RCWLR[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	× 7 to × 15

As described in Section 23, “Clocking,” The LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 77 and Table 78 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

The RCWLR[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 76.

Table 76. System PLL VCO Divider

RCWLR[SVCOD]	VCO Division Factor
00	4
01	8
10	2
11	1

Table 77. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1			200
High	0100	4 : 1		133	267
High	0101	5 : 1		167	333
High	0110	6 : 1	150	200	400
High	0111	7 : 1	175	233	
High	1000	8 : 1	200	267	
High	1001	9 : 1	225	300	
High	1010	10 : 1	250	333	
High	1011	11 : 1	275	367	
High	1100	12 : 1	300	400	
High	1101	13 : 1	325		
High	1110	14 : 1	350		
High	1111	15 : 1	375		

Notes:
1. CFG_CLKIN_DIV select the ratio between CLKIN and PCI_SYNC_OUT.
2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 78. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
Low	0010	2 : 1			133
Low	0011	3 : 1			200
Low	0100	4 : 1		133	267
Low	0101	5 : 1		167	333
Low	0110	6 : 1	150	200	400

Table 78. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
Low	0111	7 : 1	175	233	
Low	1000	8 : 1	200	267	
Low	1001	9 : 1	225	300	
Low	1010	10 : 1	250	333	
Low	1011	11 : 1	275	367	
Low	1100	12 : 1	300	400	
Low	1101	13 : 1	325		
Low	1110	14 : 1	350		
Low	1111	15 : 1	375		

Notes:
1. CFG_CLKIN_DIV doubles csb_clk if set high.
2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

23.2 Core PLL Configuration

RCWLR[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 79 shows the encodings for RCWLR[COREPLL]. COREPLL values that are not listed in Table 79 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider
VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

Table 79. e300 Core PLL Configuration

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	**nnnn**	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2

Table 79. e300 Core PLL Configuration (continued)

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	2–5	6		
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8
00	**0011**	1	3.5:1	2
01	**0011**	1	3.5:1	4
10	**0011**	1	3.5:1	8
00	**0100**	0	4:1	2
01	**0100**	0	4:1	4
10	**0100**	0	4:1	8

Notes:
1. Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

23.3 Suggested PLL Configurations

This table shows suggested PLL configurations for different input clocks (LBCM = 0).

Table 80. Example Clock Frequency Combinations

								eLBC [1]			e300 Core [1]				
Ref [1]	**LBCM**	**DDRCM**	**SVCOD**	**SPMF**	**Sys VCO[1,2]**	**CSB[1,3]**	**DDR data rate[1,4]**	**/2**	**/4**	**/8**	**× 1**	**× 1.5**	**× 2**	**× 2.5**	**× 3**
25.0	0	1	2	5	500	125	250	62.5	31.3	15.6	—	—	—	—	375
25.0	0	1	2	6	600	150	300	75 [6]	37.5	18.8	—	—	—	375	450
33.3	0	1	2	5	667	167	333	83.3 [6]	41.6	20.8	—	—	333	416	500
33.3	0	1	2	4	533	133	267	66.7	33.3	16.7	—	—	—	333	400

Table 80. Example Clock Frequency Combinations (continued)

								eLBC [1]			e300 Core [1]				
Ref [1]	LBCM	DDRCM	SVCOD	SPMF	Sys VCO[1,2]	CSB[1,3]	DDR data rate[1,4]	/2	/4	/8	× 1	× 1.5	× 2	× 2.5	× 3
48.0	0	1	2	3	576	144	288	72 [6]	36	18	—	—	—	360	432
66.7	0	1	2	2	533	133	266	66.7	33.3	16.7	—	—	—	333	400
25.0	0	0	4	8	800	200	200	100 [6]	50	25	—	—	400	500	600
33.3	0	0	2	8	533	266.7	267	133 [6]	66.7	33.3	—	400	533	667	800
50.0	0	0	4	4	800	200	200	100 [6]	50	25	—	—	400	500	600
50.0	0	0	2	8	800	400	400 [5]	—	100 [6]	50	—	600	800	—	—
66.7	0	0	2	4	533	266.7	267	133 [6]	66.7	33.3	—	400	533	667	800
66.7	0	0	2	5	667	333	333	—	83.3 [6]	41.6	333	500	667	—	—
66.7	0	0	2	6	800	400	400 [5]	—	100 [6]	50	400	600	800	—	—

Notes:
1. Values in MHz.
2. System PLL VCO range: 400–800 MHz.
3. CSB frequencies less than 133 MHz will not support Gigabit Ethernet rates.
4. Minimum data rate for DDR2 is 250 MHz and for DDR1 is 167 MHz.
5. Applies to DDR2 only.
6. Applies to eLBC PLL-enabled mode only.

24 Thermal

This section describes the thermal specifications of this chip.

24.1 Thermal Characteristics

This table provides the package thermal characteristics for the 689 31 × 31mm TePBGA II package.

Table 81. Package Thermal Characteristics for TePBGA II

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient natural convection on single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four layer board (2s2p)	$R_{\theta JA}$	15	°C/W	1, 2, 3
Junction-to-ambient (at 200 ft/min) on single layer board (1s)	$R_{\theta JMA}$	16	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	6	°C/W	5

Table 81. Package Thermal Characteristics for TePBGA II (continued)

Parameter	Symbol	Value	Unit	Note
Junction-to-package natural convection on top	ψ_{JT}	6	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

NOTE

The heat sink cannot be mounted on the package.

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JB} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

24.2.3 Experimental Determination of Junction Temperature

NOTE

The heat sink cannot be mounted on the package.

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

For the power values the device is expected to operate at, it is anticipated that a heat sink will be required. A preliminary estimate of heat sink performance can be obtained from the following first-cut approach.

The thermal resistance is expressed as the sum of a junction to case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

This first-cut approach overestimates the heat sink size required, since heat flow through the board is not accounted for, which can be as much as one-third to one-half of the power generated in the package.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling through the package and board and the convection cooling due to the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because of the wide variety of application environments, a single standard heat sink applicable to all cannot be specified.

This table shows the heat sink thermal resistance for TePBGA II package with heat sinks, simulated in a standard JEDEC environment, per JESD 51-6.

Table 82. Thermal Resistance with Heat Sink in Open Flow (TePBGA II)

Heat Sink Assuming Thermal Grease	Air Flow	Thermal Resistance (°/W)
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.1
	0.5 m/s	10.6
	1 m/s	9.3
	2 m/s	8.2
	4 m/s	7.5
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.1
	0.5 m/s	8.5
	1 m/s	7.7
	2 m/s	7.2
	4 m/s	6.8
AAVID 43× 41× 16.5mm Pin Fin	Natural Convection	11.3
	0.5 m/s	9.0
	1 m/s	7.8
	2 m/s	7.0
	4 m/s	6.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.7
	0.5 m/s	7.7
	1 m/s	6.8
	2 m/s	6.4
	4 m/s	6.1

Heat sink vendors include the following:

Aavid Thermalloy
www.aavidthermalloy.com

Alpha Novatech
www.alphanovatech.com

International Electronic Research Corporation (IERC)
www.ctscorp.com

Millennium Electronics (MEI)
www.mei-thermal.com

Tyco Electronics
Chip Coolers™
www.chipcoolers.com

Wakefield Engineering
www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.
www.chomerics.com

Dow-Corning Corporation
Dow-Corning Electronic Materials
www.dowcorning.com

Shin-Etsu MicroSi, Inc.
www.microsi.com

The Bergquist Company
www.bergquistcompany.com

24.3 Heat Sink Attachment

The device requires the use of heat sinks. When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum compressive force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

24.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

P_D = power dissipation (W)

25 System Design Information

This section provides electrical and thermal design recommendations for successful application of this chip.

25.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 65, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

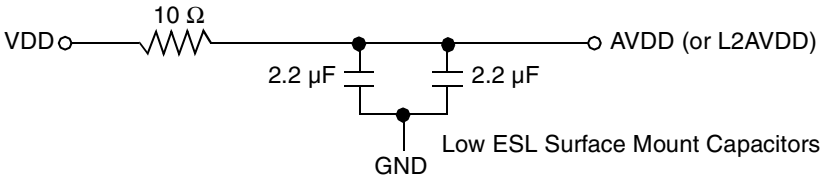


Figure 65. PLL Power Supply Filter Circuit

25.2 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, OVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, OVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, OVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.3 Connection Recommendations

To ensure reliable operation, it is highly recommended that unused inputs be connected to an appropriate signal level. Unused active low inputs should be tied to OVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external VDD, GVDD, LVDD, OVDD, and GND pins of the device.

25.4 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OVDD or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

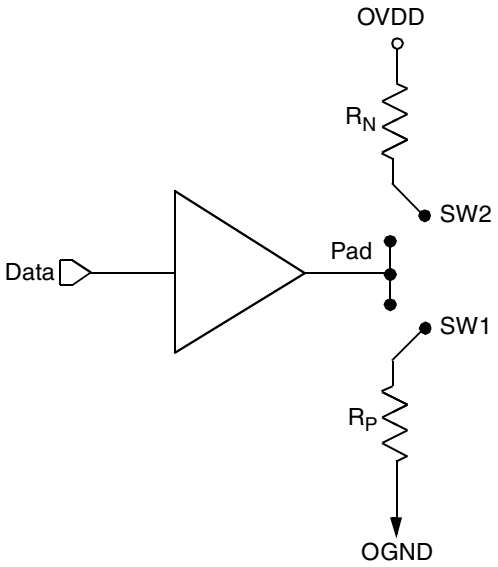


Figure 66. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 83. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI output clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	W
Differential	NA	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 2, T_j = 105°C.

25.5 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

25.6 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3665, "MPC837xE Design Checklist."

26 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 26.1, "Part Numbers Fully Addressed by This Document."

26.1 Part Numbers Fully Addressed by This Document

Table 84 provides the Freescale part numbering nomenclature for this chip. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 84. Part Numbering Nomenclature

MPC	*8377*	*E*	*C*	*ZQ*	*AF*	*D*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [1]**	**Package [2]**	**e300 core Frequency [3]**	**DDR Data Rate**	**Revision Level [4]**
MPC	8377	Blank = Not included E = included	Blank = 0°C (T_a) to 125°C (T_j) C = –40°C (T_a) to 125°C (T_j)	VR = Pb-free 689 TePBGA II	AN = 800 MHz AL = 667 MHz AJ = 533 MHz AG = 400 MHz	G = 400 MHz F = 333 MHz D = 266 MHz	Blank = Freescale ATMC fab A = GlobalFoundries fab

Note:

1 Contact local Freescale office on availability of parts with an extended temperature range.

2 See Section 22, "Package and Pin Listings," for more information on the available package type.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

4 No design changes occurred between initial parts and the revision "*A*" parts. Only the fab source has changed in moving to revision "*A*" parts. Initial revision parts and revision "*A*" parts are form, fit, function, and reliability equivalent.

This table lists the available core and DDR data rate frequency combinations.

Table 85. Available Parts (Core/DDR Data Rate)

MPC8377E	MPC8378E	MPC8379E
800 MHz/400 MHz	800 MHz/400 MHz	800 MHz/400 MHz
667 MHz/400 MHz	667 MHz/400 MHz	667 MHz/400 MHz
533 MHz/333 MHz	533 MHz/333 MHz	533 MHz/333 MHz
400 MHz/266 MHz	400 MHz/266 MHz	400 MHz/266 MHz

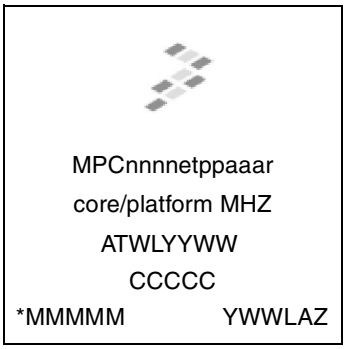
This table shows the SVR and PVR settings by device.

Table 86. SVR and PVR Settings by Product Revision

Device	Package	SVR		PVR	
		Rev 1.0	Rev. 2.1	Rev. 1.0	Rev. 2.1
MPC8377	TePBGA II	0x80C7_0010	0x80C7_0021	0x8086_1010	0x8086_1011
MPC8377E		0x80C6_0010	0x80C6_0021		
MPC8378		0x80C5_0010	0x80C5_0021		
MPC8378E		0x80C4_0010	0x80C4_0021		
MPC8379		0x80C3_0010	0x80C3_0021		
MPC8379E		0x80C2_0010	0x80C2_0021		

26.2 Part Marking

Parts are marked as in the example as shown in this figure.



TePBGA II

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 67. Freescale Part Marking for TePBGA II Devices

27 Document Revision History

This table provides a revision history for this document.

Table 87. Document Revision History

Revision	Date	Substantive Change(s)
8	05/2012	In Table 15, “DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V,” updated Output leakage current (I_{OZ}) min and max values.
7	10/2011	• In Table 84, “Part Numbering Nomenclature,” updated “Revision Level description”and added footnote 4.In Section 21.2.4, “AC Requirements for SerDes Reference Clocks,” modified the introductory sentence for Table 71, “SerDes Reference Clock Common AC Parameters.”

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
6	07/2011	In Section 2.2, "Power Sequencing," updated power down sequencing information.
5	07/2011	• In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from LB_{IN} to OV_{IN}. Also, corrected footnote 5. • In Table 3, "Recommended Operating Conditions," added footnote 2 to AV_{DD}. • In Figure 2, "Overshoot/Undershoot Voltage for $GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}$," added LBV_{DD}. • In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," updated I_{OZ} min/max to –50/50. • In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between t_{SKRGT_RX} and t_{SKRGT_TX} signals. • In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3. • In Table 48, "PCI DC Electrical Characteristics," updated V_{IH} min value to 2.0. • In Table 72, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist." • In Table 74, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values.
4	11/2010	• In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated V_{IH} min value to 1.7. • In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for t_{LBKHLR}. • In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 23, "Clocking," updated LCCR to LCRR. • In Table 72, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality.
3	03/2010	• Added Section 4.3, "eTSEC Gigabit Reference Clock Timing." • In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes . • In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$. • In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN. • In Figure 63, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader. • In Section 25.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins. • In Table 72, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins. • in Table 72, "TePBGA II Pinout Listing," added Note 16 to eTSEC pins. • In Table 77, "CSB Frequency Options for Host Mode," and Table 78, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available. • In Table 84, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency."

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2	10/2009	• In Table 3, “Recommended Operating Conditions,” added “Operating temperature range” values. • In Table 5, “Power Dissipation [1],” corrected maximal application for 800/400 MHz to 4.3 W. • In Table 5, “Power Dissipation [1],” added a column for “Typical Application at T_j = 65°C (W)”. • In Table 5, “Power Dissipation [1],” added a column for “Sleep Power at T_j = 65°C (W)”. • In Table 11, removed overbar from CFG_CLKIN_DIV. • In Table 17, “Current Draw Characteristics for MV_{REF},” updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” column headings renamed to “Min” and “Max”. Footnote 2 updated to state “T is the MCK clock period”. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” and Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” clarified that the frequency parameters are data rates. • In Table 29, “RMII Transmit AC Timing Specifications,” updated t_{RMTDX}I to 2.0 ns. • In Table 60, Gen 1i/1.5G Transmitter AC Specifications,” and Table 62, Gen 2i/3G Transmitter AC Specifications,” corrected titles from “Transmitter” to “Receiver”. • In Table 72, “TePBGA II Pinout Listing,” removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. • In Table 74, “Operating Frequencies for TePBGA II,” corrected “DDR2 memory bus frequency (MCK)” range to 125–200. • In Table 79, “e300 Core PLL Configuration,” added 3.5:1 and 4:1 core_clk: csb_clk ratio options. • In Table 80, “Example Clock Frequency Combinations,” updated column heading to “DDR data rate” . • In Section 20.2, “SPI AC Timing Specifications,” corrected t_{NIKHOX} and t_{NEKHOX} to t_{NIKHOV} and t_{NEKHOV}, respectively.
1	02/2009	• In Table 3, “Recommended Operating Conditions,” added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. • In Table 5, “Power Dissipation [1],” added Notes 4 and 5. In addition, changed 666 to 667 MHz. • In Table 13, “DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V,” Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” and Table 72, “TePBGA II Pinout Listing,” added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, *MPC837xE Design Checklist*. • In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. • In Table 72, “TePBGA II Pinout Listing,” added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 14. • In Table 74, “Operating Frequencies for TePBGA II,” changed 667 to 800 MHz for *core_clk*. • In Table 80, “Example Clock Frequency Combinations,” added 800 MHz cells for e300 core. • Updated part numbering information in AF column in Table 84, “Part Numbering Nomenclature.” In addition, modified extended temperature information in notes 1 and 4. • In Table 85, “Available Parts (Core/DDR Data Rate),” added new row for 800/400 MHz.
0	12/2008	Initial public release.

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Document Number: MPC8377EEC
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