THE DATASHEET OF

HIP1011BCBZA

HIP1011B

PCI Hot Plug Controller

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contact our Technical Support Center at
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FN4640
Rev 5.00
November 18, 2004

The HIP1011B, the third product in the HIP1011 family, is an electronic circuit breaker that monitors, reports and protects circuits from excessive load currents. As a pin-for-pin drop-in alternative offering similar functionality to the widely used HIP1011, the HIP1011B is compatible with CompactPCI peripheral boards and PCI Hot Plug systems where voltage “health” monitoring and reporting are centralized by the system controller IC. The HIP1011B does not monitor nor respond to under voltage conditions thus making control of a wide range of voltages possible.

The HIP1011B creates a small and simple yet complete power control solution to control the four independent supplies (+5V, +3.3V, +12V, and -12V) found in PCI and CompactPCI systems. For the +12V and -12V supplies, overcurrent protection is provided internally with integrated current sensing FET switches. For the +5V and +3.3V supplies, overcurrent protection is provided by sensing the voltage across the external current-sense resistors. The PWRON input controls the state of both internal and external switches. During an overcurrent condition on any output, all MOSFETs are latched-off and a LOW (0V) is asserted on the FLTN output. The FLTN latch is cleared when the PWRON input is toggled low again. During initial power-up of the main V_{CC} supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the Reset state until the V_{CC} input is greater than 10V.

User programmability of the overcurrent threshold, response time and turn-on slew rate is provided. A resistor connected to the OCSET pin programs the overcurrent thresholds. A capacitor may be added to the FLTN pin to adjust the fault reporting and power-supply latch-off response times after an over-current event. Capacitors connected to the gate pins determine the turn-on rate.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
HIP1011BCB	0 to 70	16 Ld SOIC	M16.15
HIP1011BCB-T	0 to 70	Tape and Reel	
HIP1011BCBZA (See Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
HIP1011BCBZA-T (See Note)	0 to 70	Tape and Reel (Pb-free)	

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

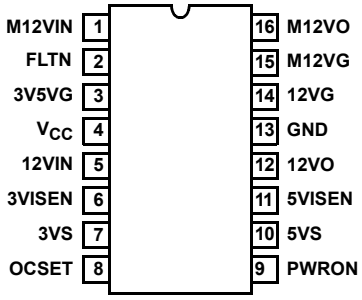
- Allows for System Centralized Voltage Monitoring
- Adjustable Delay to Fault Notification and Latch-Off
- Controls Four Supplies: +5V, +3.3V, +12V, and -12V
- Internal MOSFET Switches for +12V and -12V Outputs
- µP Interface for On/Off Control and Fault Reporting
- Adjustable Overcurrent Protection for All Supplies
- Provides Overcurrent Fault Isolation
- Adjustable Turn-On Slew Rate
- Minimum Parts Count Solution
- No Charge Pump
- Pb-Free Available (RoHS Compliant)

Applications

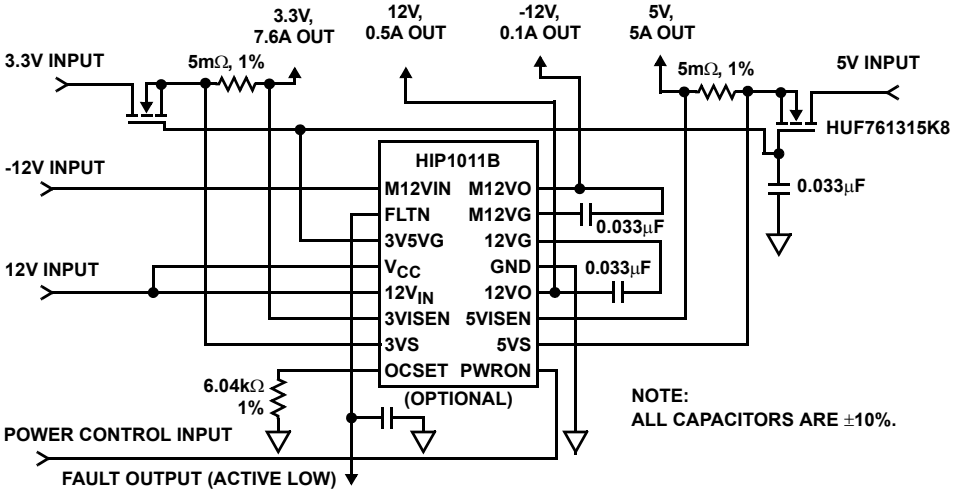
- PCI Hot Plug
- CompactPCI

Pinout

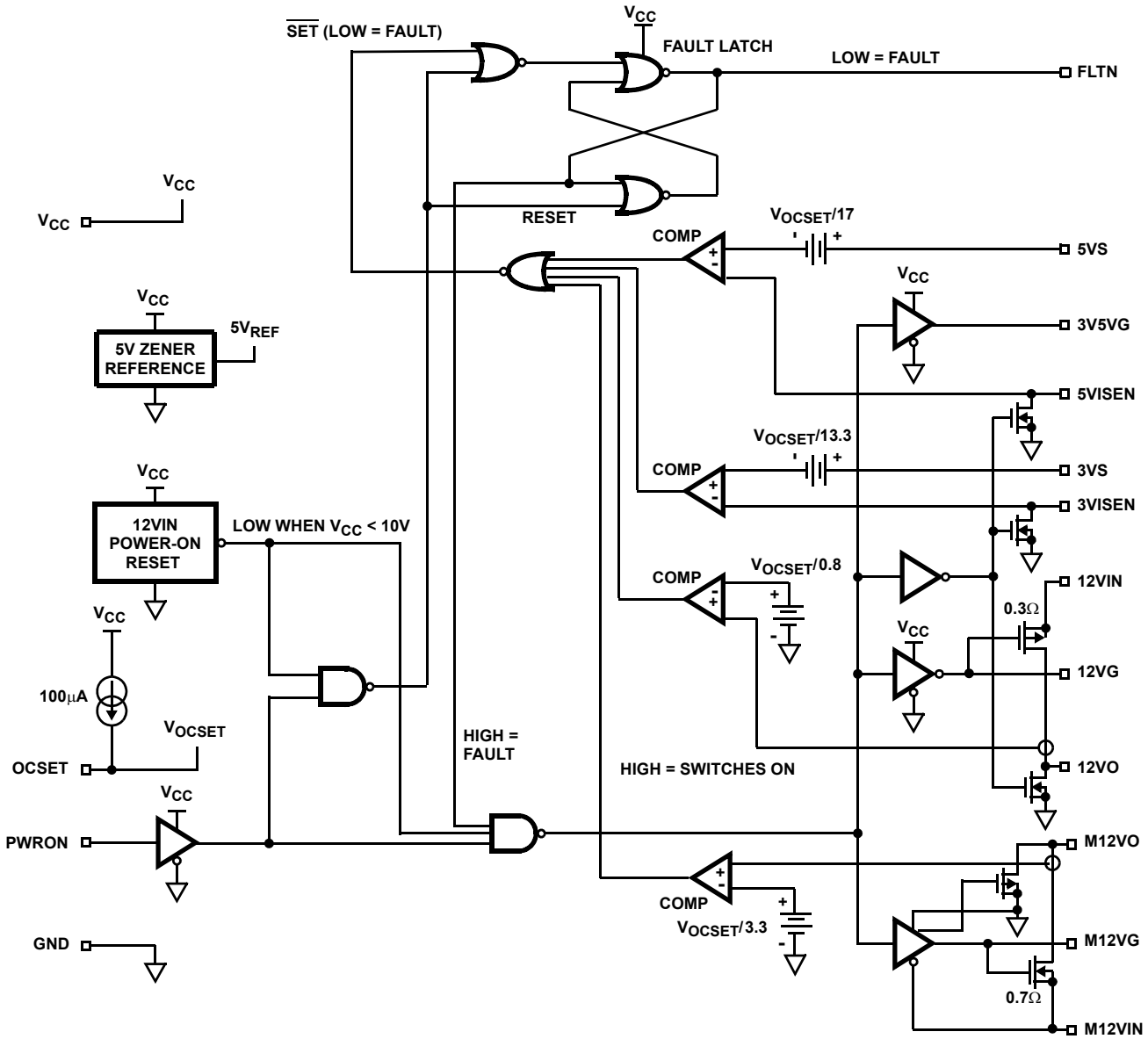
HIP1011B
(SOIC)
TOP VIEW



Typical Application



Simplified Schematic



Pin Descriptions

PIN	DESIGNATOR	FUNCTION	DESCRIPTION
1	M12VIN	-12V Input	-12V Supply Input. Also provides power to the -12V overcurrent circuitry.
2	FLTN	Fault Output	5V CMOS Fault Output; LOW = FAULT. A capacitor may be placed from this pin to ground to provide delay time to fault notification and power supply latch-off.
3	3V5VG	3.3V/5V Gate Output	Drive the Gates of the 3.3V and 5V MOSFETs. Connect a capacitor to ground to set the start-up ramp. During turn on, this capacitor is charged with a 25µA current source.
4	V_{CC}	12V V_{CC} Input	Connect to unswitched 12V supply.
5	$12V_{IN}$	12V Input	Switched 12V supply input.
6	3VISEN	3.3V Current Sense	Connect to the load side of the current sense resistor in series with source of external 3.3V MOSFET. This pin tied to GND when FET switch outputs disabled.
7	3VS	3.3V Source	Connect to Source of 3.3V MOSFET. This connection along with pin 6 (3VISEN) senses the voltage drop across the sense resistor.
8	OCSET	Overcurrent Set	Connect a resistor from this pin to ground to set the overcurrent trip point of all four switches. All four over current trips can be programmed by changing the value of this resistor. The default (6.04kΩ, 1%) is compatible with the maximum allowable currents as outlined in the PCI specification.
9	PWRON	Power On Control	Controls all Four Switches. High to Turn Switches ON, Low to turn them OFF.
10	5VS	5V Source	Connect to Source of 5V MOSFET Switch. This connection along with pin 11 (5VISEN) senses the voltage drop across the sense resistor.
11	5VISEN	5V Current Sense	Connect to the load side of the current sense resistor in series with source of external 5V MOSFET. This pin tied to GND when FET switch outputs disabled.
12	12VO	Switched 12V Output	Switched 12V output. This pin tied to GND when FET switch outputs disabled.
13	GND	Ground	Connect to common of power supplies.
14	12VG	Gate of Internal PMOS	Connect a capacitor between 12VG and 12VO to set the start up ramp for the +12V supply. This capacitor is charged with a 25µA current source during start-up.
15	M12VG	Gate of Internal NMOS	Connect a capacitor between M12VG and M12VO to set the start-up ramp for the M12V supply. This capacitor is charged with 25µA during start-up.
16	M12VO	Switched -12V Output	Switched 12V Output. This pin tied to GND when FET switch outputs disabled.

Absolute Maximum Ratings

V_{CC}, 12VIN . . . . . -0.5V to +14.0V
12VO . . . . . -0.5V to $V12V_{IN}$ + 0.5V
12VO, 12VG, 3V5VG . . . . . -0.5V to V_{CC} + 0.5V
M12VIN . . . . . -15.0V to + 0.5V
M12VO, M12VG. . . . . V_{M12VIN}-0.5V to + 0.5V
3VISEN, 5VISEN . . . . . -0.5V to the lesser of V_{CC} or + 7.0V
Voltage, Any Other Pin . . . . . -0.5V to + 7.0V
12VO Output Current 3A
M12VO Output Current 0.8A
ESD Classification . . . . . 4KeV (HBM)

Operating Conditions

VCC Supply Voltage Range. . . . . +10.8V to +13.2V
12VO Output Current . . . . . 0 to +0.5A
M12VO Output Current . . . . . 0 to +0.1A
Temperature Range (T_A) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	68
Maximum Junction Temperature	125^oC
Maximum Storage Temperature Range	-65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300^oC

Die Characteristics

Number of Transistors 250

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal 5V and 3.3V Input Supply Voltages,
V_{CC} = 12VIN = 12V, M12VIN = -12V, $T_A = T_J$ = 0 to 70^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V/3.3V SUPPLY CONTROL						
5V Overcurrent Threshold	I_{OC5V}	See Figure 1, Typical Application	-	8	-	A
5V Overcurrent Threshold Voltage	V_{OC5V_1}	V_{OCSET} = 0.6V	30	36	42	mV
5V Overcurrent Threshold Voltage	V_{OC5V_2}	V_{OCSET} = 1.2V	66	72	79	mV
5V Turn-On Time (PWRON High to 5VOUT = 4.75V)	t_{ON5V}	C_{3V5VG} = 0.022µF, C_{5VOUT} = 2000µF, R_L = 1Ω	-	6.5	-	ms
5VS Input Bias Current	IB_{5VS}	PWRON = High	-40	-26	-20	µA
5VISEN Input Bias Current	IB_{5VISEN}	PWRON = High	-160	-140	-110	µA
3V Overcurrent Threshold	I_{OC3V}	See Figure 1, Typical Application		10		A
3V Overcurrent Threshold Voltage	V_{OC3V_1}	V_{OCSET} = 0.6V	42	49	56	mV
3V Overcurrent Threshold Voltage	V_{OC3V_2}	V_{OCSET} = 1.2V	88	95	102	mV
3V Turn-On Time (PWRON High to 3VOUT = 3.00V)	t_{ON3V}	C_{3V5VG} = 0.022µF, C_{3VOUT} = 2000µF, R_L = 0.43Ω	-	6.5	-	ms
3VS Input Bias Current	IB_{3VS}	PWRON = High	-40	-26	-20	µA
3VISEN Input Bias Current	IB_{3VISEN}	PWRON = High	-160	-140	-110	µA
3V5VG V_{OUT} High	$V_{OUT_HI_35VG}$	3V5VG IOUT = 5µA	11	11.7	-	V
Gate Output Charge Current	IC_{3V5VG}	PWRON = High, V_{3V5VG} = 2V	22.5	25.0	27.5	µA
Gate Turn-On Time (PWRON High to 3V5VG = 11V)	t_{ON3V5V}	C_{3V5VG} = 0.1µF	-	280	500	µs
Gate Turn-Off Time	$t_{OFF3V5V}$	C_{3V5VG} = 0.1µF, 3V5VG from 9.5V to 1V	-	13	17	µs
Gate Turn-Off Time		C_{3V5VG} = 0.022µF, 3V5VG Falling 90% to 10%	-	2	-	µs

Electrical Specifications Nominal 5V and 3.3V Input Supply Voltages, V_{CC} = 12VIN = 12V, M12VIN = -12V, $T_A = T_J$ = 0 to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
+12V SUPPLY CONTROL						
On Resistance of Internal PMOS	$r_{DS(ON)12}$	PWRON = High, I_D = 0.5A, $T_A = T_J$ = 25°C	0.18	0.3	0.35	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.6	0.75	0.9	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	1.25	1.50	1.8	A
Gate Charge Current	IC_{12VG}	PWRON = High, V_{12VG} = 3V	22.5	25	28.5	µA
Turn-On Time (PWRON High to 12VG = 1V)	t_{ON12V}	C_{12VG} = 0.022µF	-	16	20	ms
Turn-Off Time	t_{OFF12V}	C_{12VG} = 0.1µF, 12VG	-	9	12	µs
Turn-Off Time		C_{12VG} = 0.022µF, 12VG Rising 10% - 90%	-	3	-	µs
-12V SUPPLY CONTROL						
On Resistance of Internal NMOS	$r_{DS(ON)M12}$	PWRON = High, I_D = 0.1A, $T_A = T_J$ = 25°C	0.5	0.7	0.9	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.15	0.18	0.25	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	0.30	0.37	0.50	A
Gate Output Charge Current	IC_{M12VG}	PWRON = High, V_{3VG} = -4V	22.5	25	28.5	µA
Turn-On Time (PWRON High to M12VG = -1V)	t_{ONM12V}	C_{M12VG} = 0.022µF	-	160	300	µs
Turn-On Time (PWRON High to M12VO = -10.8V)	t_{ONM12V}	C_{M12VG} = 0.022µF, C_{M12VO} = 50µF, R_L = 120Ω	-	16	-	ms
Turn-Off Time	$t_{OFFM12V}$	C_{M12VG} = 0.1µF, M12VG	-	18	23	µs
Turn-Off Time		C_{M12VG} = 0.022µF, M12VG Falling 90% to 10%	-	3	-	µs
M12VIN Input Bias Current	IB_{M12VIN}	PWRON = High	-	2	2.6	mA
CONTROL I/O PINS						
Supply Current	I_{VCC}		4	5	5.8	mA
OCSET Current	I_{OCSET}		95	100	105	µA
Overcurrent Fault Response Time	t_{OC}		-	500	960	ns
PWRON Threshold Voltage	$V_{THPWRON}$		0.8	1.6	2.1	V
FLTN Output Low Voltage	$V_{FLTN,OL}$	I_{FLTN} = 2mA	-	0.6	0.9	V
FLTN Output High Voltage	$V_{FLTN,OH}$	I_{FLTN} = 0 to -4mA	3.9	4.3	4.9	V
FLTN Output Latch Threshold	$V_{FLTN,TH}$		1.45	1.8	2.25	V
12V Power On Reset Threshold	$V_{POR,TH}$	V_{CC} Voltage Falling	8.7	9.4	9.9	V

Typical Performance Curves

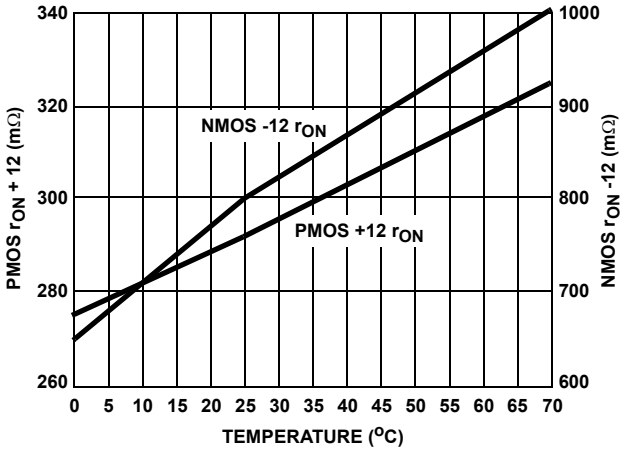


FIGURE 1. r_{ON} vs TEMPERATURE

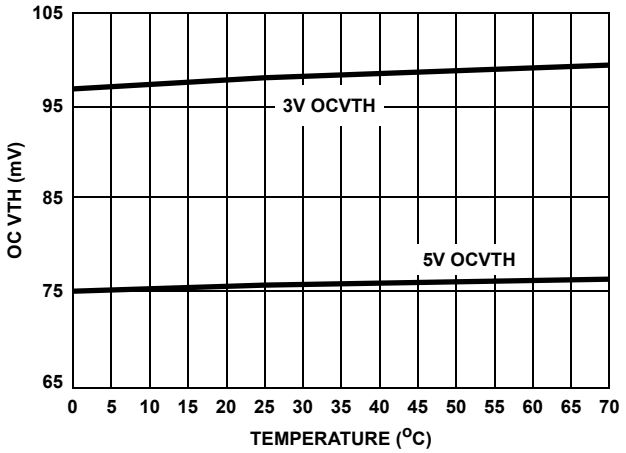


FIGURE 2. OC VTH vs TEMPERATURE (VR_{OCSET} = 1.21V)

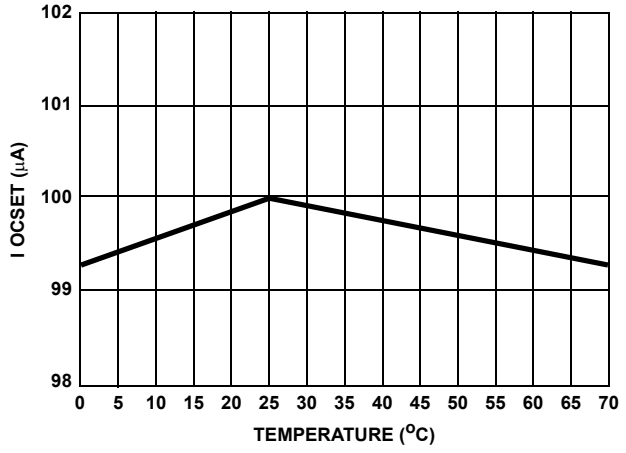


FIGURE 3. OCSET CURRENT vs TEMPERATURE

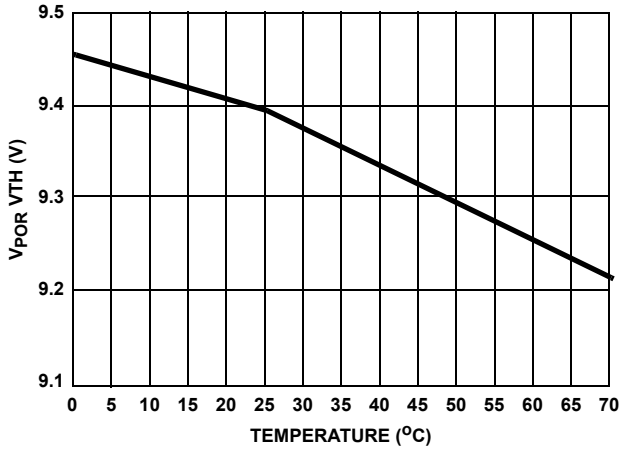


FIGURE 4. V_{CC} POWER ON RESET VTH vs TEMPERATURE

Adjusting the Fault Reporting and Power Supply Latch-Off Delay Times

Figure 5 illustrates the relationship between the FLTN signal and the gate drive outputs. Duration **a**, indicates the time between FLTN starting to transition from High to Low, (indicating a fault has occurred) and the start of the gate drive outputs latching off. The latch-off is initiated by the falling FLTN signal reaching the output latch threshold voltage, VFLTN, TH. For additional details and wave forms see HIP1011A Data Sheet FN4631. Table 1 illustrates the effect of the FLTN capacitor on the response times.

TABLE 1. RESPONSE TIME TABLE

	0.001μF	0.1μF	10μF
3V5VG Response **a**	0.85μs	37μs	3.8ms

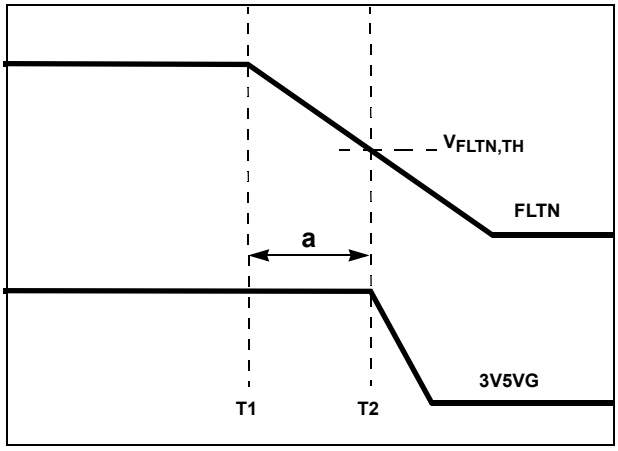


FIGURE 5. TIMING DIAGRAM

Applications

Implementing the HIP1011B in the CompactPCI Hot Swap Application

This application offers to the CompactPCI peripheral board designer programmable Over Current (OC) protection, programmable delays to latch off, and soft start ramp turn on for all four supplies with simultaneous latch off upon OC fault detection.

Figure 6 illustrates the HIP1011EVAL2 evaluation board for CompactPCI Hot Swap implementation. The shaded components are the external components necessary to accomplish both controlled power up and turn-on. For minimum PCB area single gate logic can be used.

Insertion Sequence

Because of the staggered pin lengths in the CompactPCI connector, as the board is inserted into the slot, the ground bus plane is connected first via the longest pins referencing the HIP1011B by way of the PWRON, OCSET and GND pins through R4 and R3. Additionally the three-state driver, U1 address line is referenced through R6.

Subsequently the medium length pins engage to connect the +3.3V, +5V, +12V, -12V lines to the inputs, activating the HIP1011B, and the 2 logic devices, U1 and U2. At this time the HIP1011B is in control holding off all the MOSFET switches, as PWRON is being held low. With the logic devices powered the inverter U2 input is pulled high putting a low on the three-state driver U1 input which is passed through to the PWRON pin.

Upon complete insertion the shortest length pin, “board present” which is tied to ground on the backplane finally contacts the inverter input. The inverter output pulls high turning on the HIP1011B through U1 thus, the board is fully powered on only upon complete insertion.

Fault Reset

If an overcurrent condition is detected on the board by the HIP1011B the FLTN signal transitions low, once the $V_{FLTN,TH}$ is reached all the switches are simultaneously switched off protecting the system, the board and its components. The system controller is notified of the fault occurrence by the FLTN signal.

Reset of the faulted card is accomplished by a positive pulse on the three-state $\overline{oe}$ input. The pulse puts U1 output into a high Z state allowing R4 to pull the HIP1011B PWRON pin low, resetting the HIP1011B. The HIP1011B switches turn back on when U1 $\overline{oe}$ input returns to a low state resulting in PWRON going high. The reset pulse can be generated by either the system restart/reset to the master board or from the master system board to any of the peripheral boards in the system.

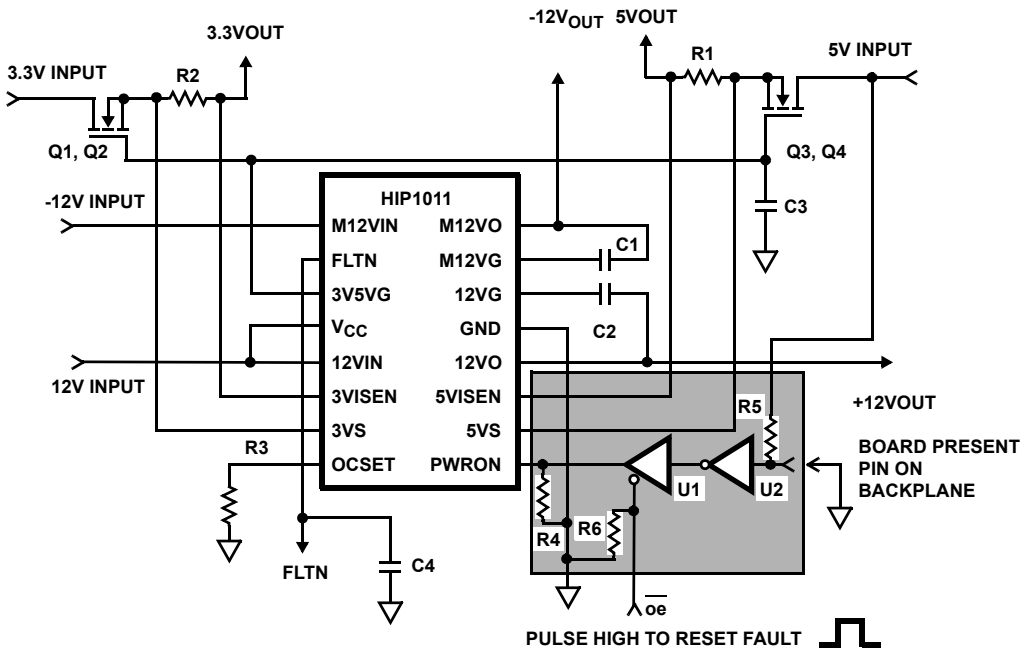


FIGURE 6. HIP1011B CompactPCI APPLICATION CIRCUIT

NOTES:

3. Each test point (TP) on HIP1011EVAL2 refers to device pin number.
4. SIGNAL_GND, SHIELD_GND and SHORTPIN_GND can be jumpered together for ease of evaluation.
5. HIP1011B devices can be placed into HIP1011EVAL2 board for evaluation or contact INTERSIL for a HIP1011B equipped evaluation board.

HIP1011 Split Load Application

All of the members of the HIP1011 family, including the HIP1011B, can be used in an application where two electrically isolated loads are to be powered from a common bus. This may occur in a system that has a power management feature controlled by a system controller IC invoking a sleep or standby state. Thus one load can be shut down while maintaining power to a second isolated circuit. The circuit shown in Figure 7 shows the external FETs, and sense resistor configuration for the 3.3V and/or 5V load that has such a requirement. The HIP1011 is represented by pin names in rectangles. Q1 and Q2 are the N-Channel FETs for each load on this rail, these are sized appropriately for each load. R1 and R2 are needed to pull down the supply slot pins or load when slot power is disabled as the load discharge FETs (Q3) on the VISEN pins are no longer attached to the load. When power is turned off to the load these (~100Ω) FETs turn on, thus some low current, (10mA) continues to be drawn from the supply in addition to the sleep load current resulting in a 4^{O}C die temperature rise.

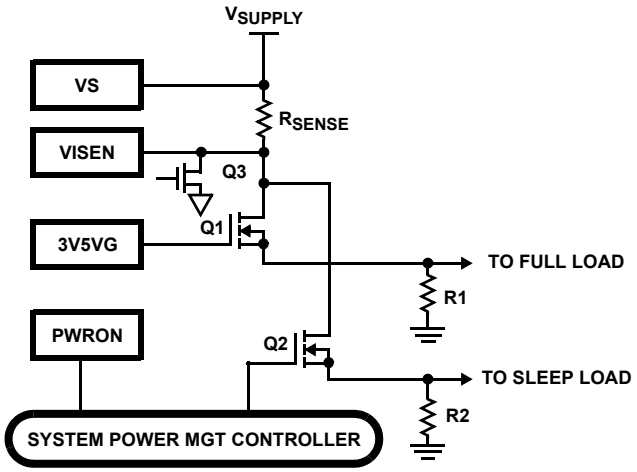


FIGURE 7. SPLIT LOAD CIRCUIT

HIP1011 High Power Circuit

Instances occur when a noncompliant card is designed for use in a PCI environment. Although the HIP1011 family has proven to be very design flexible, controlling high power +12V supplies requires special attention. This is due to thermal considerations that limit the integrated power device on the +12V supply to about 1.5A. To address this an external add on circuit as shown in Figure 8 enables the designer to add the OC monitoring and control of a high power +12V supply in addition to the 3 other power supplies. The HIP1011 is represented by pin names in rectangles.

This circuit primarily requires that an external P-Channel MOSFET be connected in parallel to the internal HIP1011 PMOS device and that the discrete device have a much lower $r_{DS(ON)}$ value than the internal PMOS device in order to carry the majority of the current load. By monitoring the voltage across the sense resistor carrying the combined load current of both the internal and external FETs and by using a comparator with a common mode input voltage range to the positive rail and a low input voltage threshold offset to reduce distribution losses, a high precision OC detector can be designed to control a much higher current load than can be tolerated by the HIP1011.

An alternative circuit for moderate current levels where both accuracy and cost are lowered can be accomplished by a single external P-Channel MOSFET in parallel with the internal P-Channel MOSFET. For example, if 2X the OC level is desired a 0.3Ω $r_{DS(ON)}$ P-Channel MOSFET can be used thus approximately doubling the +12 IOUT before latch-off. $IOC_{TOTAL} = IOC_{INTERNAL}$ (1 + $r_{DS(ON)}$ of internal FET/$r_{DS(ON)}$ of external FET).

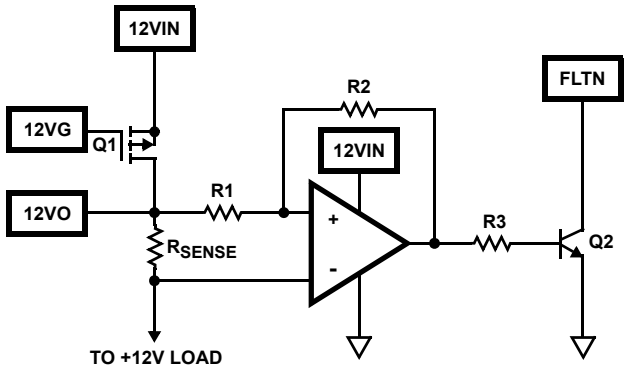
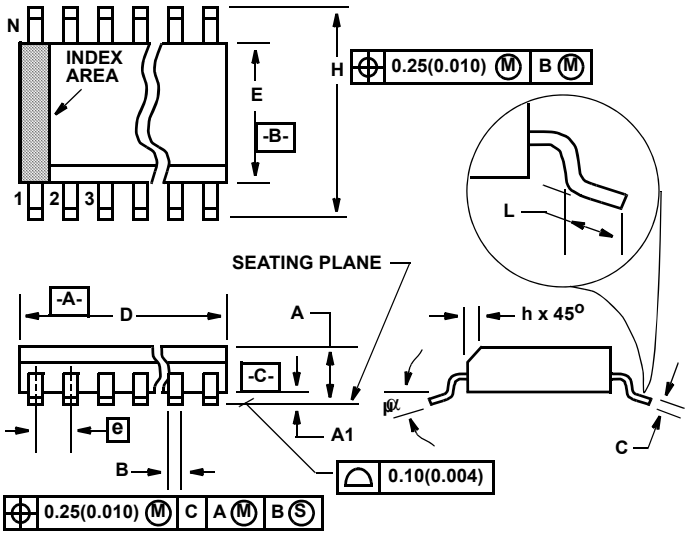


FIGURE 8. HIGH POWER +12V CIRCUIT

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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