THE DATASHEET OF

ISL59481IRZ

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ISL59481

Dual, 500MHz Triple, Multiplexing Amplifiers

FN6208
Rev 4.00
May 18, 2007

The ISL59481 contains two independent unity gain triple 4:1 MUX amplifiers that feature high slew rate and excellent bandwidth for RGB video switching. Each RGB 4:1 MUX contains binary coded, channel select logic inputs (S0, S1), and separate logic inputs for High Impedance output (HIZ) and power-down ($\overline{EN}$) modes. The HIZ state presents a high impedance at the output so that both RGB MUX outputs can be wired together to form an 8:1 RGB MUX amplifier or they can be used in R-R, G-G, and B-B pairs to form a 4:1 differential input/output MUX. Separate power-down mode controls ($\overline{EN1}$, $\overline{EN2}$) are included to turn off unused circuitry in power sensitive applications. With both $\overline{EN}$ pins pulled high, the ISL59481 enters a standby power mode - consuming just 36mW.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
ISL59481IRZ	ISL59481 IRZ	-	48 Ld Exposed Pad 7x7 QFN	L48.7x7B
ISL59481IRZ-T13	ISL59481 IRZ	13”	48 Ld Exposed Pad 7x7 QFN	L48.7x7B
ISL59481EVAL1Z	Evaluation PCB			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

TABLE 1. CHANNEL SELECT LOGIC TABLE ISL59481

S1-1, 2	S0-1, 2	$\overline{EN1}$, $\overline{EN2}$	HIZ1, 2	OUTPUT1, 2
0	0	0	0	IN0 (A, B, C)
0	1	0	0	IN1 (A, B, C)
1	0	0	0	IN2 (A, B, C)
1	1	0	0	IN3 (A, B, C)
X	X	1	X	Power-down
X	X	0	1	High Z

Features

- Dual, triple 4:1 multiplexers for RGB
- Externally configurable for various video MUX circuits including
  - 8:1 RGB MUX
  - Two separate 4:1 RGB MUX
  - 4:1 differential RGB video MUX
- Internally set gain-of-1
- High impedance outputs (HIZ)
- Power-down mode ($\overline{EN}$)
- ±5V operation
- ±870V/µs slew rate
- 500MHz bandwidth
- Supply current 16mA/CH
- Pb-free plus anneal (RoHS compliant)

Applications

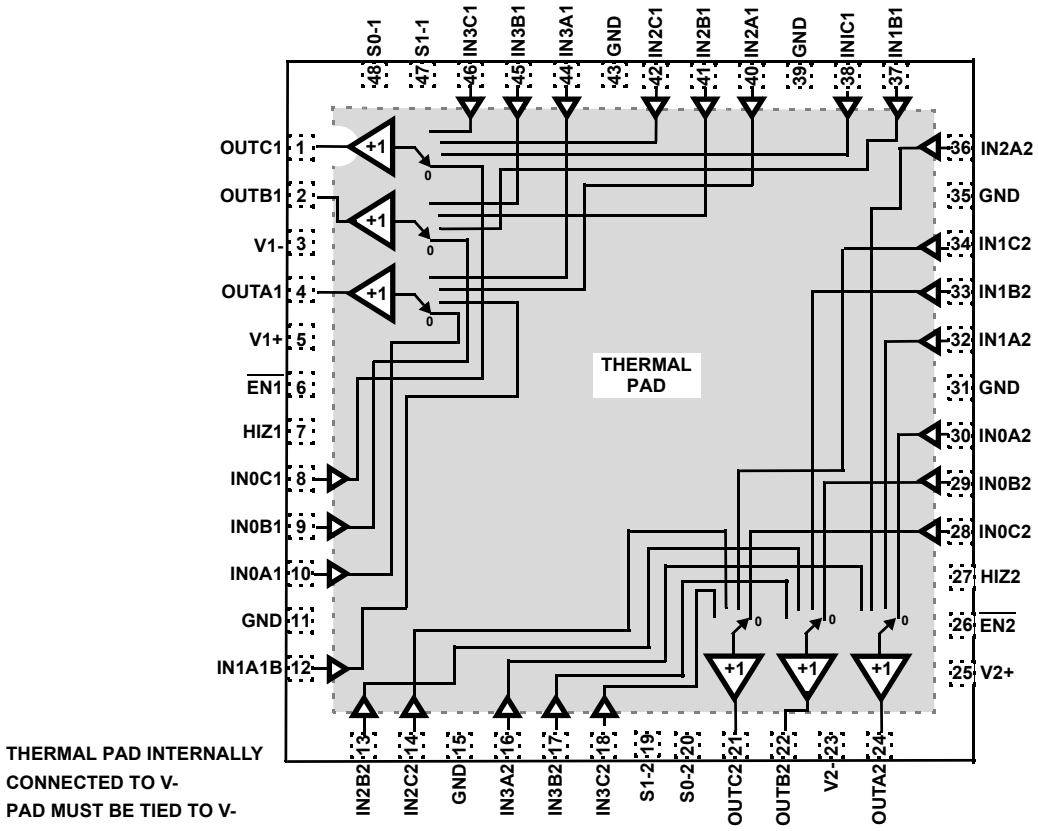
- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set-top boxes
- Security video
- Broadcast video equipment

Related Literature

- Application Note AN1235 “ISL59481EVAL1 Evaluation Board User’s Guide”

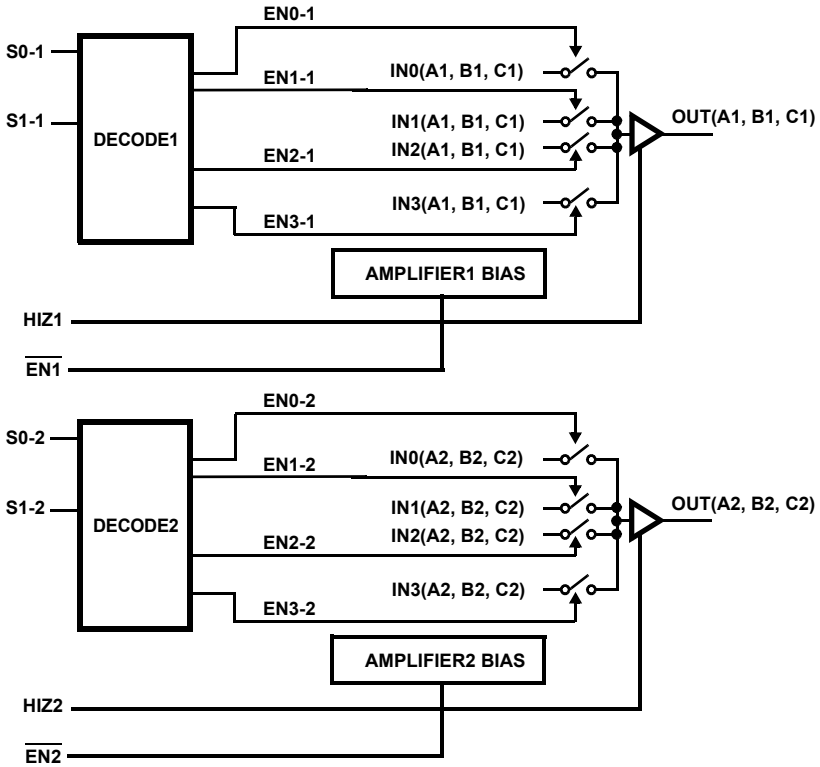
Pinout

ISL59481
(48 LD QFN)
TOP VIEW



THERMAL PAD INTERNALLY CONNECTED TO V-
PAD MUST BE TIED TO V-

Functional Diagram ISL59481



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to V-). 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). . . .2500V
Machine Model 300V

Thermal Information

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .-40°C to +125°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V1+ = V2+ = +5V, V1- = V2- = -5V, GND = 0V, T_A = +25°C, Input Video = $1V_{P-P}$ and R_L = 500Ω to GND, C_L = 5pF unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
$+I_S$ Enabled	Enabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ Low	75	92	100	mA
$-I_S$ Enabled	Enabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ Low	-96	-92	-68	mA
$+I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ High	5	6.2	8	mA
$-I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ High	-250	-20		µA
V_{OUT}	Positive and Negative Output Swing	V_{IN} = ±3.5V, R_L = 500Ω	3.1	3.4		|V|
I_{OUT}	Output Current	R_L = 10Ω to GND	80	135		|mA|
V_{OS}	Output Offset Voltage	V_{IN} = 0V	-10		14	mV
Ib	Input Bias Current	V_{IN} = 0V	-10	-2	+10	µA
R_{OUT}	HIZ Output Resistance	HIZ = Logic High		1.2		MΩ
R_{OUT}	Enabled Output Resistance	HIZ = Logic Low		0.1		Ω
R_{IN}	Input Resistance	V_{IN} = ±3.5V		10		MΩ
A_{CL} or A_V	Voltage Gain	V_{IN} = ±1.5V, R_L= 500Ω	0.98	0.99	1.02	V/V
I_{HIZ}	Output Current in High Impedance state	V_{OUT} = 0V		1.2		µA
LOGIC						
V_{IH}	Input High Voltage (Logic Inputs)		2			V
V_{IL}	Input Low Voltage (Logic Inputs)				0.8	V
I_{IH}	Input High Current (Logic Inputs)	V_H = 5V	215	270	320	µA
I_{IL}	Input Low Current (Logic Inputs)	V_L = 0V	-10	-1	+10	µA
AC GENERAL						
t_S	0.1% Settling Time	R_L= 500Ω, C_L = 1.5pF, Step = 1V		10		ns
PSRR	Power Supply Rejection Ratio	DC, PSRR V+ and V- combined	52	56		dB
ISO	Channel Isolation	f = 10MHz, Ch to Ch Crosstalk and Off Isolation, C_L = 1.5pF		75		dB
dG	Differential Gain Error	NTC-7, R_L = 150, C_L = 1.5pF		0.02		%
dP	Differential Phase Error	NTC-7, R_L = 150, C_L = 1.5pF		0.02		°
BW	-3dB Bandwidth	C_L = 1.5pF		500		MHz

Electrical Specifications V1+ = V2+ = +5V, V1- = V2- = -5V, GND = 0V, T_A = +25°C, Input Video = $1V_{P-P}$ and R_L = 500Ω to GND, C_L = 5pF unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
FBW	0.1dB Bandwidth	C_L = 1.5pF		60		MHz
	0.1dB Bandwidth	C_L = 4.7pF		120		MHz
SR	Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L = 1.5pF		±870		V/µs
SWITCHING CHARACTERISTICS						
V_{GLITCH}	Channel-to-Channel Switching Glitch	V_{IN} = 0V C_L = 1.5pF		20		mV_{P-P}
	$\overline{EN}$ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		200		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		200		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		18		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		20		ns
tr, tf	Rise and Fall Time	10% to 90%		1.1		ns
tpd	Propagation Delay	10% to 10%		0.9		ns

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified.

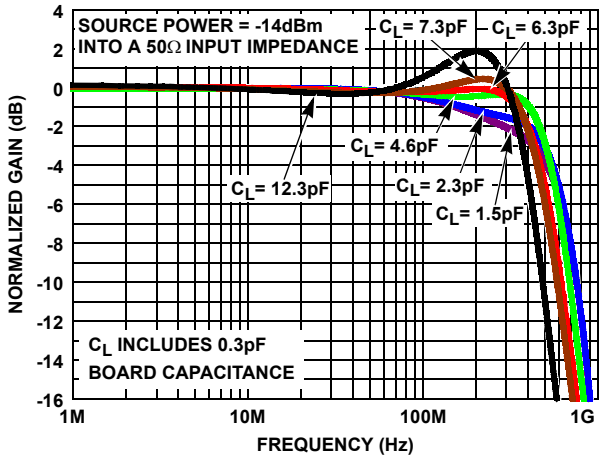


FIGURE 1. GAIN vs FREQUENCY vs C_L

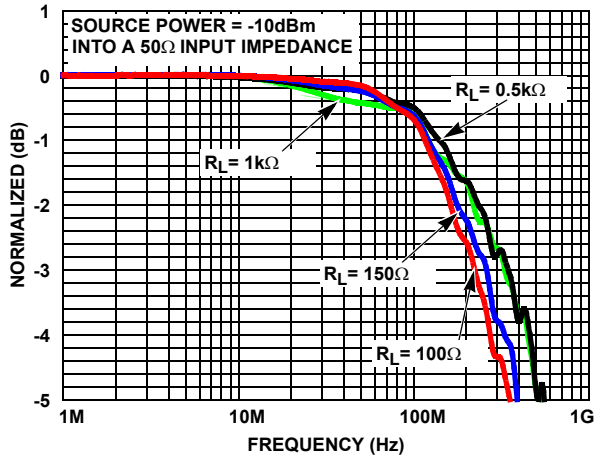


FIGURE 2. GAIN vs FREQUENCY vs R_L

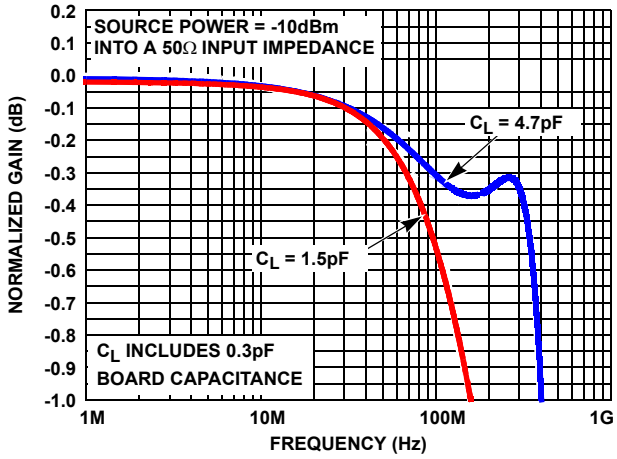


FIGURE 3. 0.1dB GAIN vs FREQUENCY

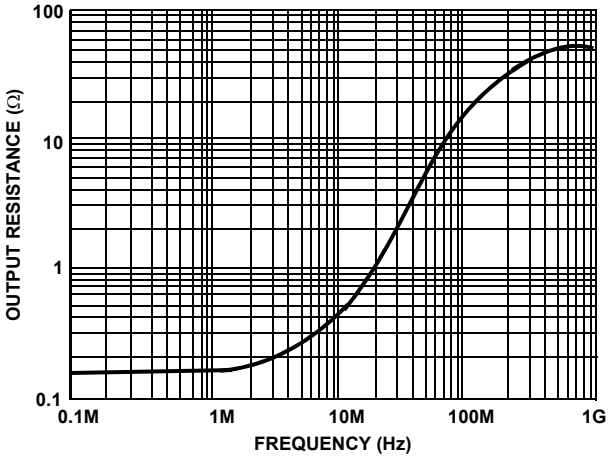


FIGURE 4. R_{OUT} vs FREQUENCY

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

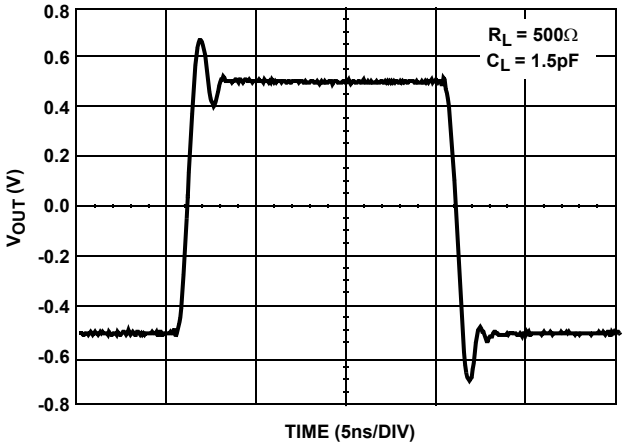


FIGURE 5. TRANSIENT RESPONSE

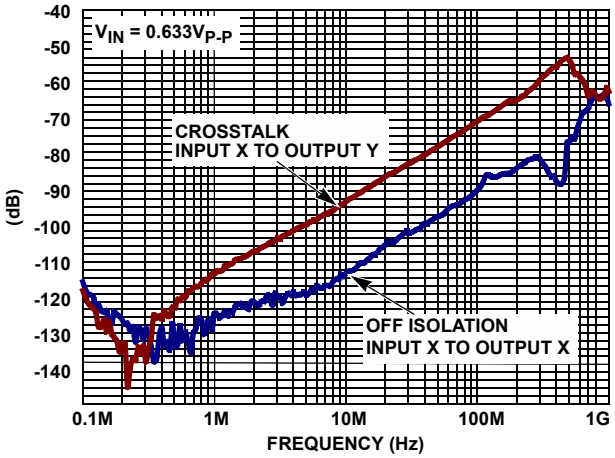


FIGURE 6. CROSSTALK AND OFF ISOLATION

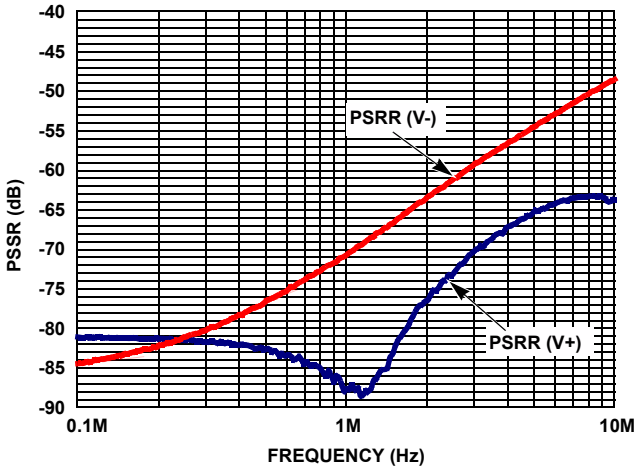


FIGURE 7. PSRR CHANNELS A, B, C

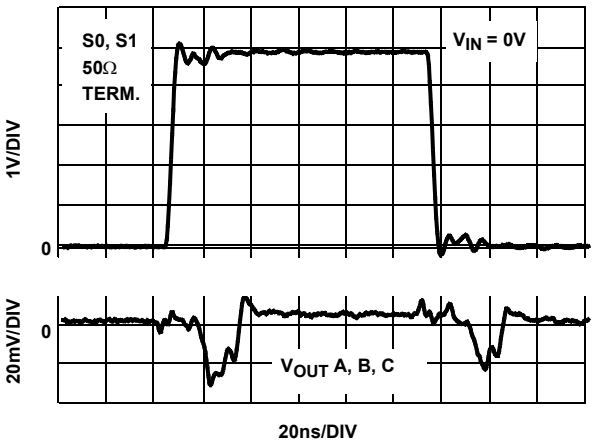


FIGURE 8. CHANNEL-TO-CHANNEL SWITCHING GLITCH (V_{IN} = 0V)

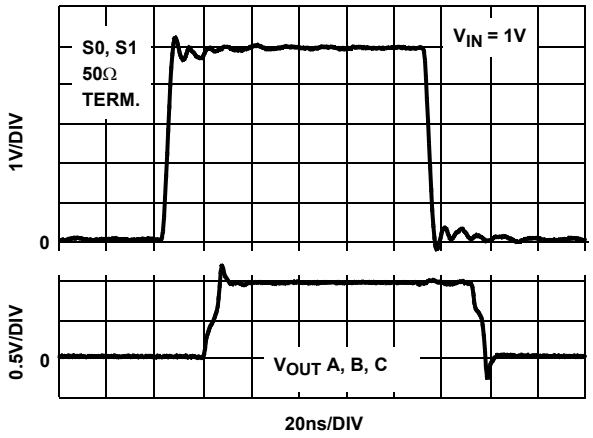


FIGURE 9. CHANNEL TO CHANNEL TRANSIENT RESPONSE (V_{IN} = 1V)

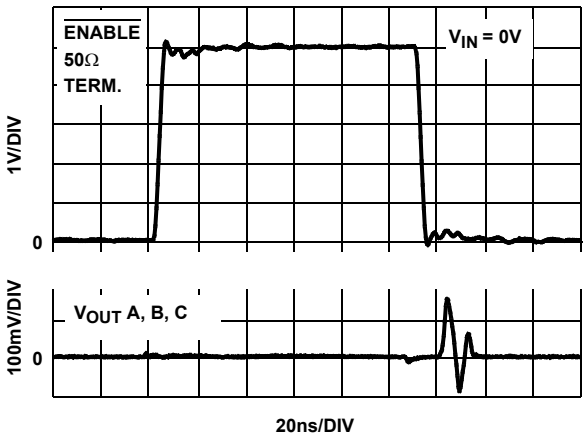


FIGURE 10. $\overline{\text{ENABLE}}$ SWITCHING GLITCH (V_{IN} = 0V)

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

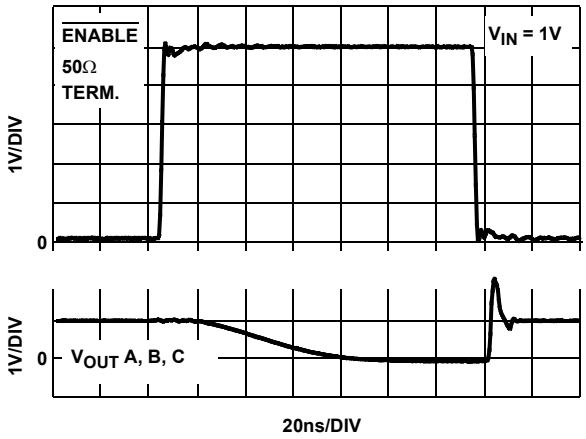


FIGURE 11. $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE (V_{IN} = 1V)

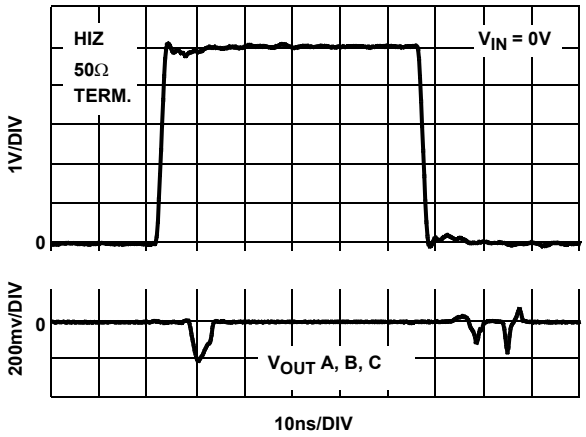


FIGURE 12. HIZ SWITCHING GLITCH (V_{IN} = 0V)

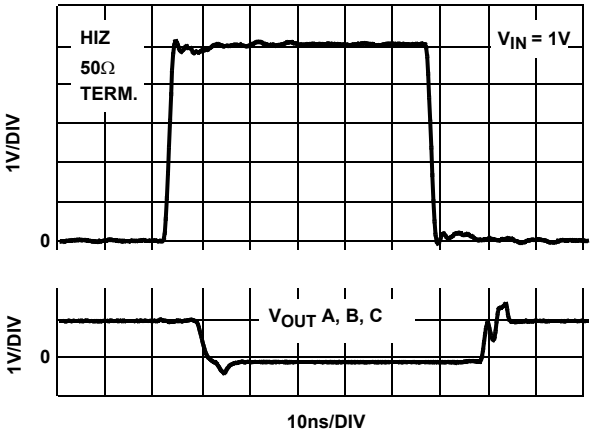


FIGURE 13. HIZ TRANSIENT RESPONSE (V_{IN} = 1V)

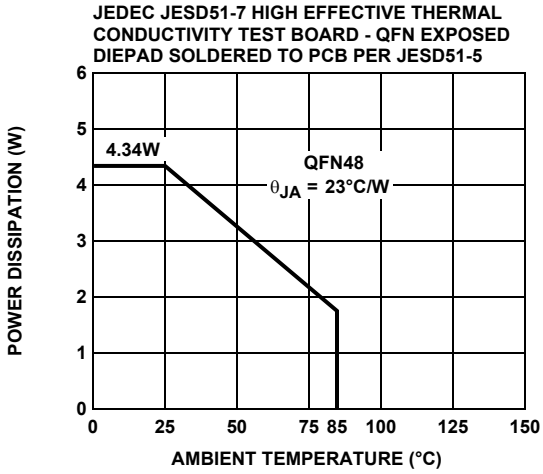
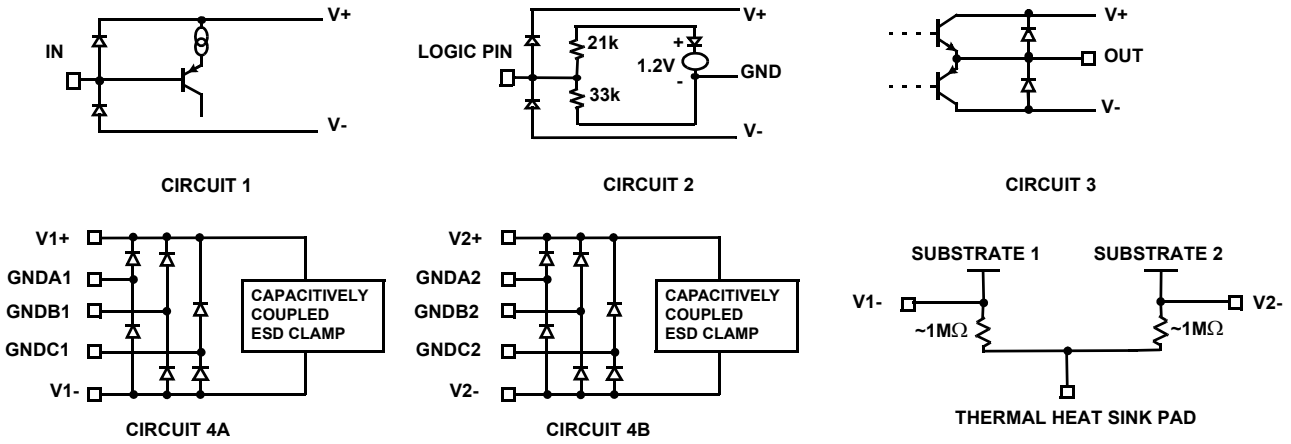


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Description

ISL59481 (48 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUTC1	Circuit 3	Output of amplifier C1
2	OUTB1	Circuit 3	Output of amplifier B1
3, 23	V1-, V2-	Circuit 4A	Negative power supply #1 and #2
4	OUTA1	Circuit 3	Output of amplifier A1
5, 25	V1+, V2+	Circuit 4A	Positive Power Supply #1 and #2
6	$\overline{EN1}$	Circuit 2	Device enable (active low) with internal pull-down resistor. A logic High puts device into power-down mode leaving the logic circuitry active. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
26	$\overline{EN2}$		
7	HIZ1	Circuit 2	Output disable (active high) with internal pull-down resistor. A logic high puts the output in a high impedance state. Use this state when more than one MUX-amp share the same video output line.
27	HIZ2		
8	IN0C1	Circuit 1	Channel 0 input for amplifier C1
9	IN0B1	Circuit 1	Channel 0 input for amplifier B1
10	IN0A1	Circuit 1	Channel 0 input for amplifier A1
11	GND	Circuit 4A	Ground pin for amplifier A1
12	IN1A1	Circuit 1	Channel 1 input for amplifier A1
13	IN2B2	Circuit 1	Channel 2 input for amplifier B2
14	IN2C2	Circuit 1	Channel 2 input for amplifier C2
15	GND	Circuit 4B	Ground pin for amplifier C2
16	IN3A2	Circuit 1	Channel 3 input for amplifier A2
17	IN3B2	Circuit 1	Channel 3 input for amplifier B2
18	IN3C2	Circuit 1	Channel 3 input for amplifier C2
19, 47	S1-2, S1-1	Circuit 2	Channel select pin MSB (binary logic code) for amplifiers A2, B2, C2 (S1-2) and A1, B1, C1 (S1-1)
20, 48	S0-2, S0-1	Circuit 2	Channel select pin LSB (binary logic code) for amplifiers A2, B2, C2 (S0-2) and A1, B1, C1 (S0-1)
21	OUTC2	Circuit 2	Output of amplifier C2
22	OUTB2	Circuit 1	Output of amplifier B2
24	OUTA2	Circuit 1	Output of amplifier A2
28	IN0C2	Circuit 1	Channel 0 input for amplifier A2
29	IN0B2	Circuit 1	Channel 0 input for amplifier B2
30	IN0A2	Circuit 1	Channel 0 input for amplifier C2
31	GND	Circuit 4B	Ground pin for amplifier C2
32	IN1A2	Circuit 1	Channel 1 input for amplifier A2
33	IN1B2	Circuit 1	Channel 1 input for amplifier B2
34	IN1C2	Circuit 1	Channel 1 input for amplifier C2
35	GND	Circuit 4B	Ground pin for amplifier B2
36	IN2A2	Circuit 1	Channel 2 input for amplifier A2
37	IN1B1	Circuit 1	Channel 1 input for amplifier B1
38	IN1C1	Circuit 1	Channel 1 input for amplifier C1
39	GND	Circuit 4A	Ground pin for amplifier B1
40	IN2A1	Circuit 1	Channel 2 input for amplifier A1
41	IN2B1	Circuit 1	Channel 2 input for amplifier B1
42	IN2C1	Circuit 1	Channel 2 input for amplifier C1
43	GND	Circuit 4A	Ground pin for amplifier C1
44	IN3A1	Circuit 1	Channel 3 input for amplifier A1
45	IN3B1	Circuit 1	Channel 3 input for amplifier B1
46	IN3C1	Circuit 1	Channel 3 input for amplifier C1

Pin Equivalent Circuits



AC Test Circuits

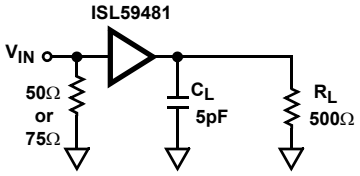


FIGURE 15A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

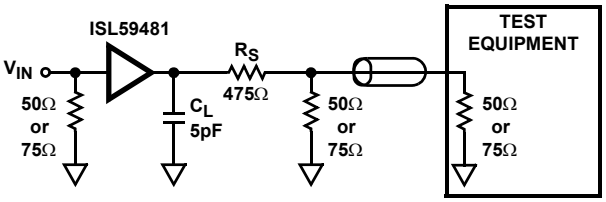


FIGURE 15B. TEST CIRCUIT FOR MEASURING WITH 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

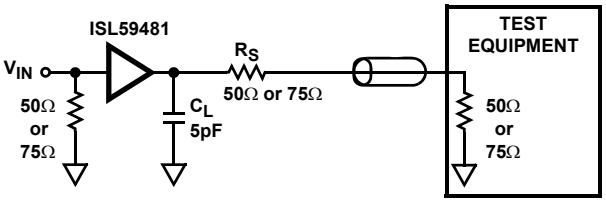


FIGURE 15C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

FIGURE 15. TEST CIRCUITS

Figure 15A illustrates the optimum output load for testing AC performance. Figure 15B illustrates the optimum output load when connecting to 50Ω input terminated equipment.

Application Information

General

The ISL59481 is ideal as the matrix element of high performance switchers and routers. Key features include high impedance buffered analog inputs and excellent AC performance at output loads down to 150Ω for video cable-driving. The unity-gain current feedback output amplifiers are stable operating into capacitive loads and bandwidth is optimized with a load of 5pF in parallel with a 500Ω. Total output capacitance can be split between the PCB capacitance and an external load capacitor.

Ground Connections

For the best isolation and crosstalk rejection, all GND pins must connect to the GND plane.

Power-up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT-triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 16) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply. One Schottky can be used to protect both V+ power supply pins, and a second for the protection of both V- pins.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the

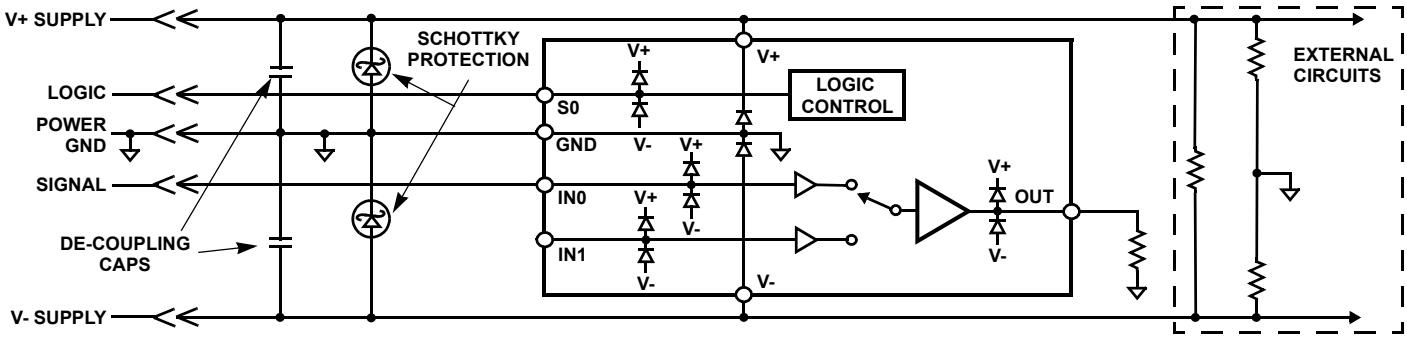


FIGURE 16. SCHOTTKY PROTECTION CIRCUIT

internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

HIZ State

Each internal 4:1 triple MUX-amp has a three-state output control pin (HIZ1 and HIZ2). Each has an internal pull-down resistor to set the output to the enabled state with no connection to the HIZ pin. The HIZ state is established within approximately 15ns by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4MΩ with approximately 1.5pF in parallel with a 10µA bias current from the output. When more than one MUX shares a common output, the high impedance state loading effect is minimized over the maximum output voltage swing and maintains its high Z even in the presence of high slew rates. The supply current during this state is the same as the active state.

$\overline{EN}$ and Power-down States

The $\overline{EN}$ pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{EN}$ pin. The power-down state is established within approximately 80ns, if a logic high (>2V) is placed on the $\overline{EN}$ pin. In the power-down state, supply current is reduced significantly by shutting the three amplifiers off. The output presents a high impedance to the output pin, however, there is a risk that the disabled amplifier output can be back-driven at signal voltage levels exceeding ~$2V_{P-P}$. Under this condition, large incoming slew rates can cause fault currents of tens of mA. Therefore, the parallel connection of multiple outputs is not recommended unless the application can tolerate the limited power-down output impedance.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners. Use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless controlled impedance (50Ω or 75Ω) strip lines or microstrips are used.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of 2 power supply decoupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible. Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to

provide heat sinking for the IC. However, because of the connection to the V1- and V2- supply pins through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Do **not** tie this pin to GND as this could result in large back biased currents flowing between GND and the V- pins. Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

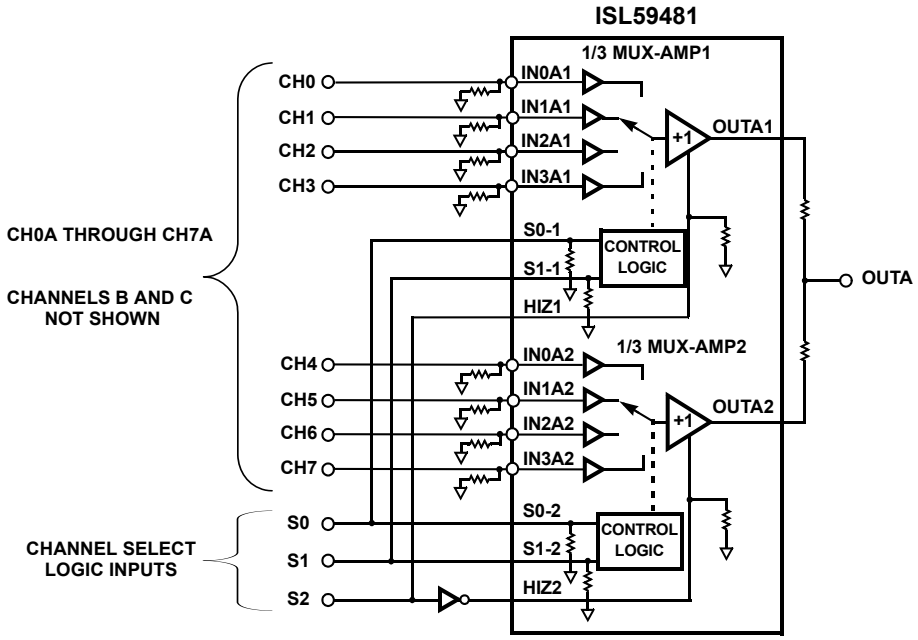
The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible, an isolated thermal pad on another layer should be used. Pad area requirements should be evaluated on a case-by-case basis.

MUX Application Circuits

Each of the two 4:1 triple MUX amplifiers have their own binary-coded, TTL compatible channel select logic inputs (S0-1, 2, and S1-1, 2). All three amplifiers are switched simultaneously from their respective inputs with S0-1 S1-1 controlling MUX-amp1, and S0-2, S1-2 controlling MUX-amp2. The HIZ control inputs (HIZ1, HIZ2) and device enable control inputs ($\overline{EN1}$ and $\overline{EN2}$) control MUX-amp1 and MUX-amp2 in a similar fashion. The individual control for each 4:1 triple MUX enables external connections to configure the device for different MUX applications.

8:1 RGB Video MUX

For a triple input RGB 8:1 MUX (Figure 17), the RGB amplifier outputs of MUX-amp1 are parallel-connected to the RGB amplifier outputs of MUX-amp2 to produce the single RGB video output. Input channels CH0 through CH3 are assigned to MUX-amp1, and channels CH4 through CH7 are assigned to MUX-amp2. Channels CH0 through CH3 are selected by setting HIZ1 low, HIZ2 high (enables MUX-amp1 and three-states MUX-amp2), and the appropriate channel select logic to S0-1, S1-1. Reversing the logic inputs of HIZ1, HIZ2 switches from MUX-amp1 to MUX-amp2 enables the selection of channels CH4 through CH7. The channel select inputs are parallel connected (S0-1 to S0-2) and (S1-1 to S1-2) to form two logic controls S0, S1. A single S2 control is split into complimentary logic inputs for HIZ1 and HIZ2 to produce a chip select function for the MSB. The logic control truth table is shown in Figure 17.



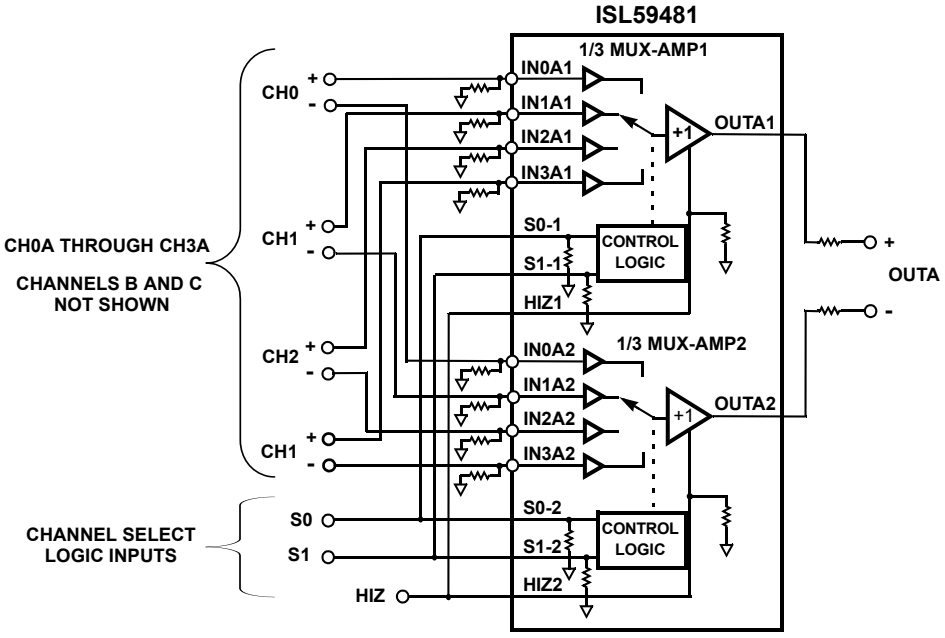
CHANNEL SELECT TRUTH TABLE
8:1 VIDEO MUX

S2	S1	S0	OUTA, B, C
0	0	0	CH0A, B, C
0	0	1	CH1A, B, C
0	1	0	CH2A, B, C
0	1	1	CH3A, B, C
1	0	0	CH4A, B, C
1	0	1	CH5A,B,C
1	1	0	CH6A, B, C
1	1	1	CH7A, B, C

FIGURE 17. APPLICATION CIRCUIT FOR 8:1 RGB VIDEO MUX

4:1 RGB Differential Video MUX

Connecting the channel select pins in parallel (S0-1 to S0-2 and S1-1 to S1-2) converts the 8 individual RGB video inputs into 4 differential RGB input pairs. The amplifier RGB outputs are similarly paired resulting in a fully differential 4:1 RGB MUX amp shown in Figure 18. Connecting HIZ1 and HIZ2 to +5V disables the 4:1 differential MUX, and enables the connection of additional differential-connected MUX amplifiers to the same outputs, thus allowing input expansion to 8:1 or more.



CHANNEL SELECT TRUTH TABLE
4:1 DIFFERENTIAL VIDEO MUX

S1	S0	OUTA, B, C
0	0	CH0A, B, C
0	1	CH1A, B, C
1	0	CH2A, B, C
1	1	CH3A, B, C

FIGURE 18. APPLICATION CIRCUIT FOR 4:1 RGB DIFFERENTIAL VIDEO MUX

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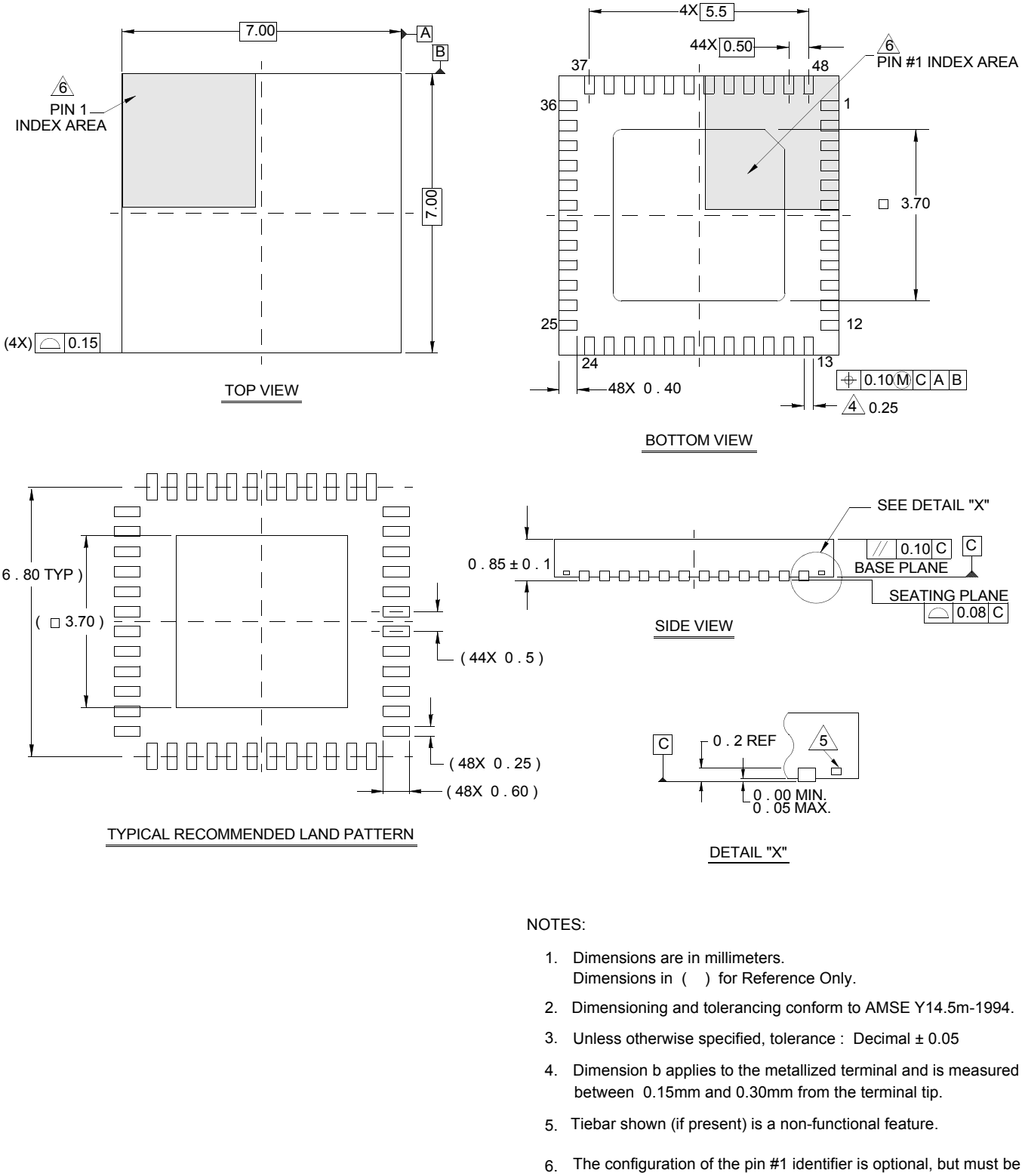
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Package Outline Drawing

L48.7x7B

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 12/06



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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