THE DATASHEET OF

LTC1775CS#PBF

High Power No R_{SENSE}™ Current Mode Synchronous Step-Down Switching Regulator

FEATURES

- **Highest Efficiency Current Mode Controller**
- **No Sense Resistor Required**
- **300mV Maximum Current Sense Voltage**
- **Stable High Current Operation**
- **Dual N-Channel MOSFET Synchronous Drive**
- Wide V_{IN} Range: 4V to 36V
- **Wide V_{OUT} Range: 1.19V to V_{IN}**
- ±1% 1.19V Reference
- Programmable Fixed Frequency with Injection Lock
- Very Low Drop Out Operation: 99% Duty Cycle
- Forced Continuous Mode Control Pin
- Optional Programmable Soft Start
- Pin Selectable Output Voltage
- Foldback Current Limit
- Output Overvoltage Protection
- Logic Controlled Micropower Shutdown: I_Q < 30µA
- Available in 16-Lead Narrow SSOP and SO Packages

APPLICATIONS

- Notebook Computers
- Automotive Electronics
- Battery Chargers
- Distributed Power Systems

DESCRIPTION

The LTC®1775 is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using few external components. Current mode control with MOSFET V_{DS} sensing eliminates the need for a sense resistor and improves efficiency. Largely similar to the LTC1625, the LTC1775 has twice the maximum sense voltage for high current applications. The frequency of a nominal 150kHz internal oscillator can be synchronized to an external clock over a 1.5:1 frequency range.

Burst Mode™ operation at low load currents reduces switching losses and low dropout operation extends operating time in battery-powered systems. A forced continuous mode control pin can assist secondary winding regulation by disabling Burst Mode operation when the main output is lightly loaded.

Fault protection is provided by foldback current limiting and an output overvoltage comparator. An external capacitor attached to the RUN/SS pin provides soft start capability for supply sequencing. A wide supply range allows operation from 4V (4.3V for LTC1775I) to 36V at the input and 1.19V to V_{IN} at the output.

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No R_{SENSE} and Burst Mode are trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

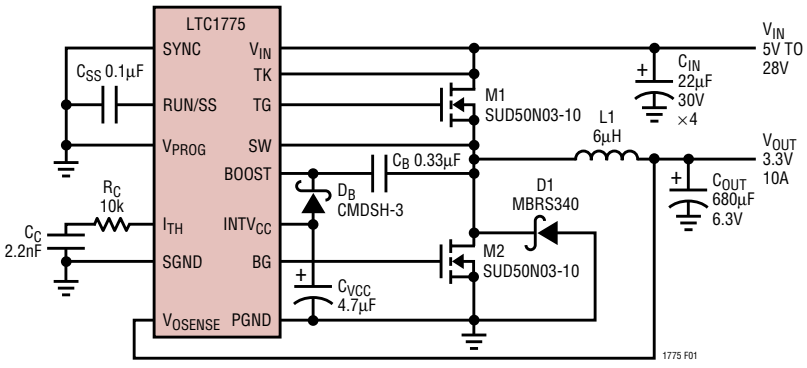
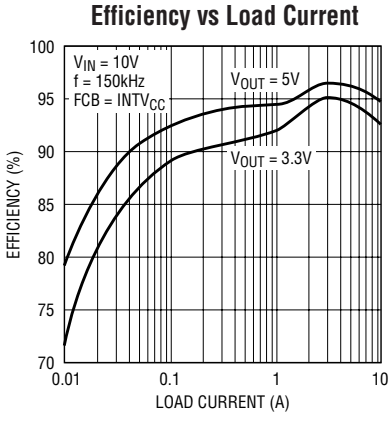


Figure 1. High Efficiency Step-Down Converter

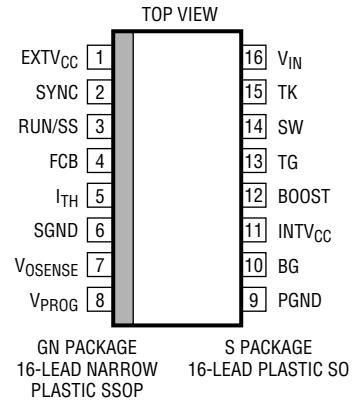


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}, TK) ..... 36V to –0.3V
Boosted Supply Voltage (BOOST) ..... 42V to –0.3V
Boosted Driver Voltage (BOOST – SW) ..... 7V to –0.3V
Switch Voltage (SW) .....36V to –5V
$EXTV_{CC}$ Voltage .....7V to –0.3V
I_{TH} Voltage .....2.7V to –0.3V
FCB, RUN/SS, SYNC Voltages .....7V to –0.3V
V_{OSENSE}, V_{PROG} Voltages .....($INTV_{CC}$ + 0.3V) to –0.3V
Peak Driver Output Current < 10µs (TG, BG) 2A
$INTV_{CC}$ Output Current 50mA
Operating Ambient Temperature Range
LTC1775C ..... 0°C to 70°C
LTC1775I (Note 5) ..... –40°C to 85°C
Junction Temperature (Note 2) .....125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW
PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LTC1775CGN LTC1775CS LTC1775IGN LTC1775IS
GN PART MARKING
1775 1775I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$I_{IN}V_{OSENSE}$	Feedback Current	V_{PROG} Pin Open, I_{TH} = 1.19V (Note 3)			10	50	nA
V_{OUT}	Regulated Output Voltage 1.19V (Adjustable) Selected 3.3V Selected 5V Selected	I_{TH} = 1.19V (Note 3) V_{PROG} Pin Open V_{PROG} = 0V V_{PROG} = $INTV_{CC}$	 ● ● ●	 1.178 3.220 4.900	 1.190 3.300 5.000	 1.202 3.380 5.100	 V V V
$V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 4V to 20V, I_{TH} = 1.19V (Note 3), V_{PROG} Pin Open			0.001	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} = 2V (Note 3) I_{TH} = 0.5V (Note 3)	● ●		–0.020 0.035	–0.2 0.2	% %
V_{FCB}	Forced Continuous Threshold	V_{FCB} Ramping Negative	●	1.16	1.19	1.22	V
I_{FCB}	Forced Continuous Bias Current	V_{FCB} = 1.19V			–1	–2	µA
V_{OVL}	Output Overvoltage Lockout	V_{PROG} Pin Open		1.24	1.28	1.32	V
I_{PROG}	V_{PROG} Input Current 3.3V V_{OUT} 5V V_{OUT}	 V_{PROG} = 0V V_{PROG} = 5V	 	 	 –3.5 3.5	 –7 7	 µA µA
I_Q	Input DC Supply Current Normal Mode Shutdown	 $EXTV_{CC}$ = 5V (Note 4) $V_{RUN/SS}$ = 0V, 4V < V_{IN} < 15V	 	 	 500 15	 30	 µA µA
$V_{RUN/SS}$	RUN/SS Pin Threshold		●	0.8	1.4	2	V
$I_{RUN/SS}$	Soft Start Current Source	$V_{RUN/SS}$ = 0V		–1.2	–2.5	–4	µA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{OSENSE} = 1V, V_{PROG} Pin Open		260	300	340	mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	TG Transition Time	(Note 6)					
TG t_R	Rise Time	C_{LOAD} = 3300pF			50	150	ns
TG t_F	Fall Time	C_{LOAD} = 3300pF			50	150	ns
	BG Transition Time	(Note 6)					
BG t_R	Rise Time	C_{LOAD} = 3300pF			50	150	ns
BG t_F	Fall Time	C_{LOAD} = 3300pF			50	150	ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	5.0	5.2	5.4	V
V_{LDOINT}	$INTV_{CC}$ Load Regulation	I_{CC} = 20mA, V_{EXTVCC} = 4V			–0.2	–1	%
V_{LDOEXT}	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			180	300	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, V_{EXTVCC} Ramping Positive	●	4.5	4.7		V
Oscillator							
f_{OSC}	Oscillator Freqency	SYNC = 0V		135	150	165	kHz
f_H/f_{OSC}	Maximum Synchronized Frequency Ratio				1.5		
V_{SYNC}	SYNC Pin Threshold (Figure 4)	Ramping Positive			0.9	1.2	V
R_{SYNC}	SYNC Pin Input Resistance				50		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1775CGN/LTC1775IGN: $T_J = T_A + (P_D \bullet 130°C/W)$

LTC1775CS/LTC1775IS: $T_J = T_A + (P_D \bullet 110°C/W)$

Note 3: The LTC1775 is tested in a feedback loop that adjusts V_{OSENSE} to achieve a specified error amplifier output voltage (I_{TH}).

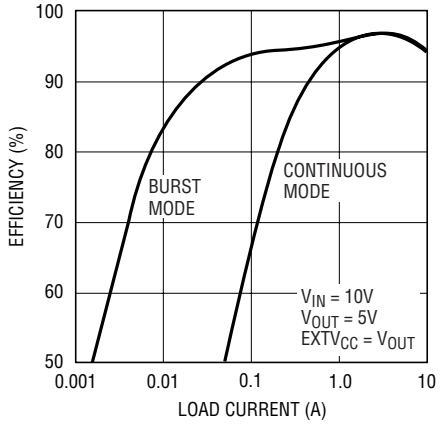
Note 4: Typical in application circuit with $EXTV_{CC}$ tied to V_{OUT} = 5V, I_{OUT} = 0A and FCB = $INTV_{CC}$. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: Minimum input supply voltage is 4.3V at –40°C for industrial grade parts.

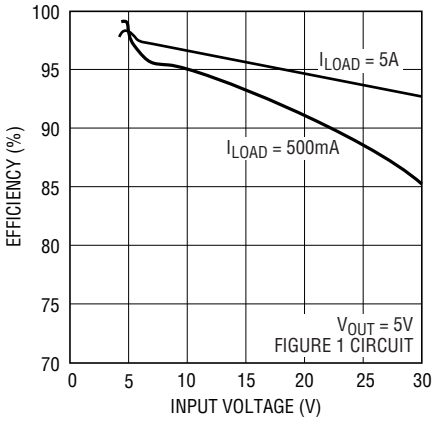
Note 6: Rise and fall times are measured at 10% to 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

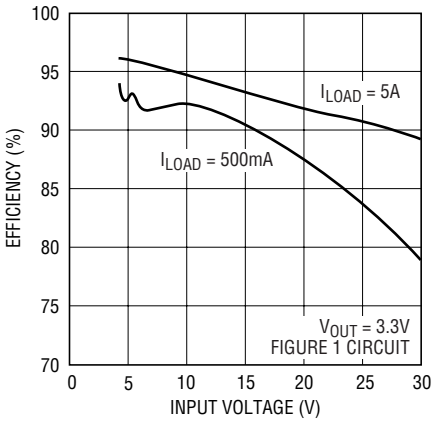
Efficiency vs Load Current



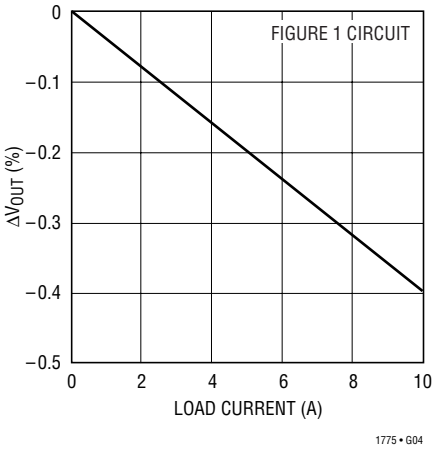
Efficiency vs Input Voltage



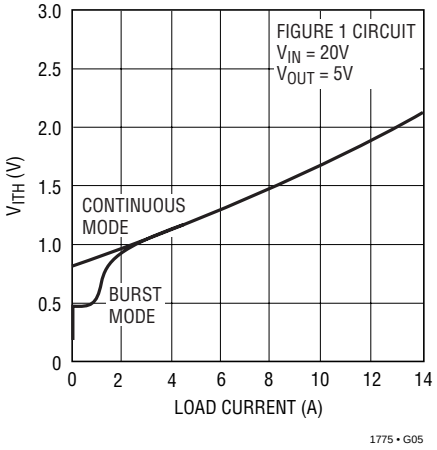
Efficiency vs Input Voltage



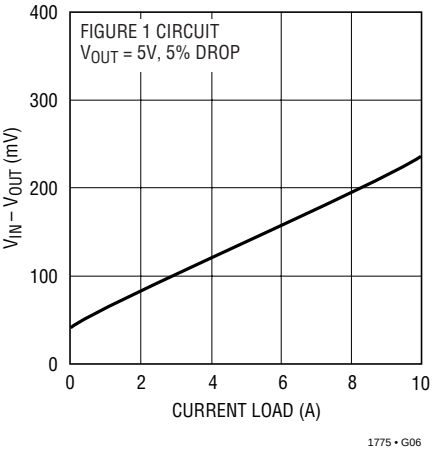
Load Regulation



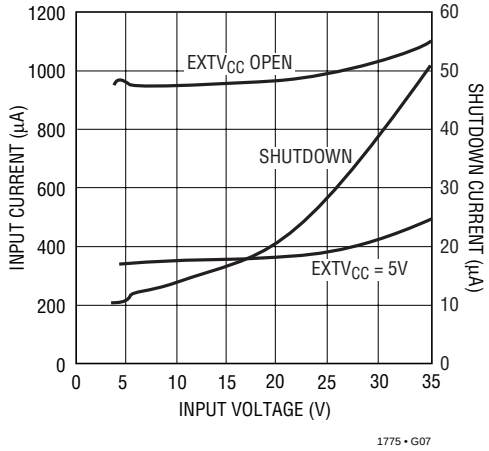
ITH Pin Voltage vs Load Current



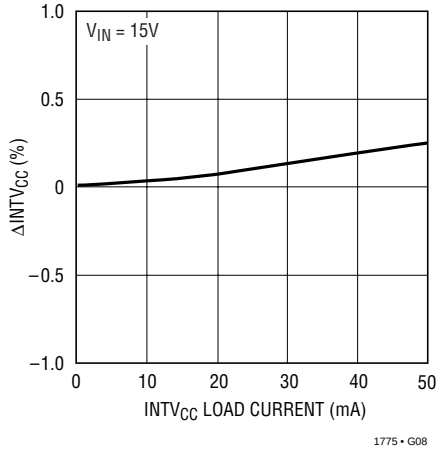
VIN – VOUT Dropout Voltage vs Load Current



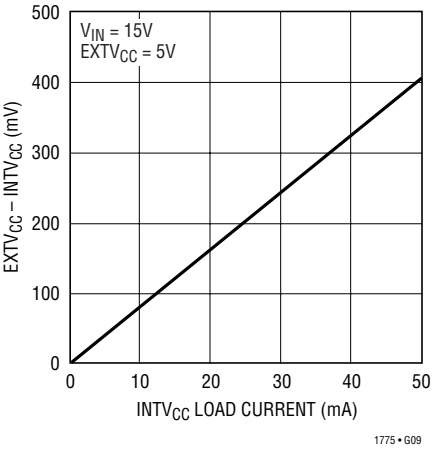
Input and Shutdown Current vs Input Voltage



INTVCC Load Regulation

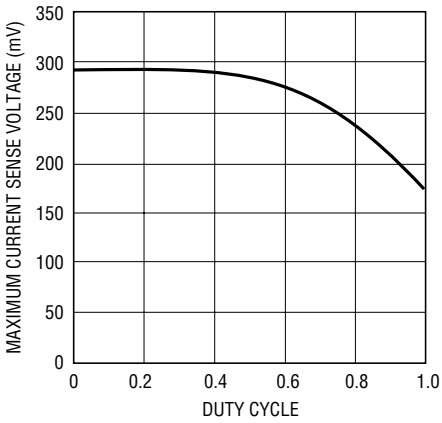


EXTVCC Switch Drop vs INTVCC Load Current



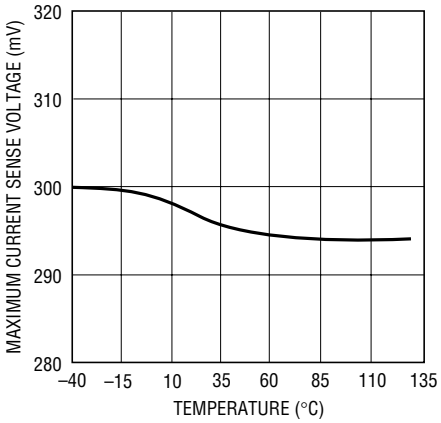
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Voltage vs Duty Cycle



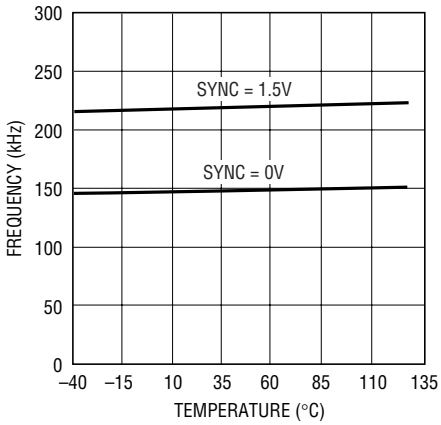
1775 • G10

Maximum Current Sense Voltage vs Temperature



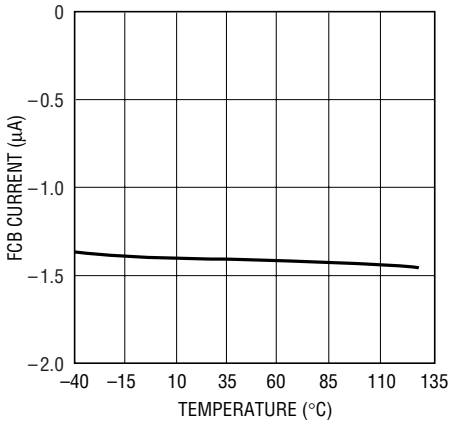
1775 • G11

Oscillator Frequency vs Temperature



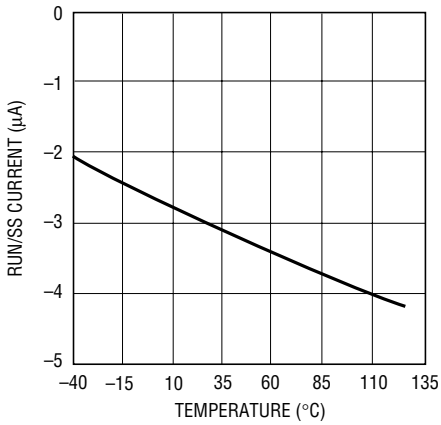
1775 • G12

FCB Pin Current vs Temperature



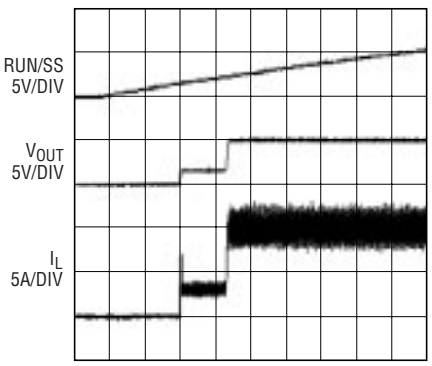
1775 • G13

RUN/SS Pin Current vs Temperature



1775 • G14

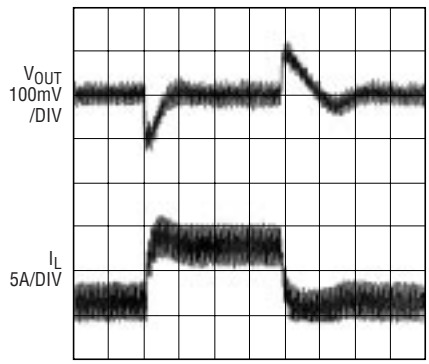
Soft Start



V_{IN} = 20V 20ms/DIV
V_{OUT} = 5V
R_{LOAD} = 0.5Ω
FIGURE 1 CIRCUIT

1530 G16

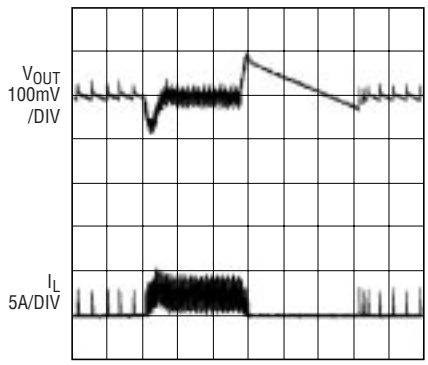
Transient Response



V_{IN} = 20V 100µs/DIV
V_{OUT} = 5V
I_{LOAD} = 2A TO 8A
FIGURE 1 CIRCUIT

1530 G18

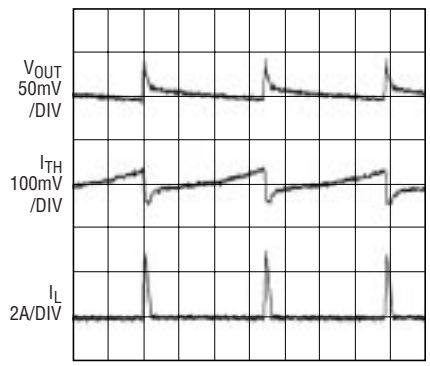
Transient Response (Burst Mode Operation)



V_{IN} = 20V 200µs/DIV
V_{OUT} = 5V
I_{LOAD} = 100mA TO 2A
FIGURE 1 CIRCUIT

1530 G17

Burst Mode Operation



V_{IN} = 20V 20µs/DIV
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 1 CIRCUIT

1530 G15

PIN FUNCTIONS

$EXTV_{CC}$ (Pin 1): $INTV_{CC}$ Switch Input. When the $EXTV_{CC}$ voltage is above 4.7V, the switch closes and supplies $INTV_{CC}$ power from $EXTV_{CC}$. Do not exceed 7V at this pin.

SYNC (Pin 2): Synchronization Input for Internal Oscillator. The oscillator will nominally run at 150kHz when open, 225kHz when tied above 1.2V, and will lock over a 1.5:1 clock frequency range.

RUN/SS (Pin 3): Run Control and Soft Start Input. A capacitor to ground at this pin sets the ramp time to full current output (approximately 1s/µF). Forcing this pin below 1.4V shuts down the device.

FCB (Pin 4): Forced Continuous Input. Tie this pin to ground to force synchronous operation at low load currents, to a resistive divider from the secondary output when using a secondary winding, or to $INTV_{CC}$ to enable Burst Mode operation at low load currents.

I_{TH} (Pin 5): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage, forcing inductor current to be roughly proportional to V_{ITH}. Nominal voltage range for this pin is 0V to 2.4V.

SGND (Pin 6): Signal Ground. Connect to the (–) terminal of C_{OUT}.

V_{OSENSE} (Pin 7): Output Voltage Sense. Feedback input from the remotely sensed output voltage or from an external resistive divider across the output.

V_{PROG} (Pin 8): Output Voltage Programming. When V_{OSENSE} is connected to the output, $V_{PROG} < 0.8V$ selects a 3.3V output and $V_{PROG} > 3.5V$ selects a 5V output. Leaving V_{PROG} open allows the output voltage to be set by an external resistive divider between the output and V_{OSENSE}.

PGND (Pin 9): Driver Power Ground. Connects to the source of the bottom N-channel MOSFET, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

BG (Pin 10): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

$INTV_{CC}$ (Pin 11): Internal 5.2V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF tantalum or other low ESR capacitor.

BOOST (Pin 12): Topside Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. This pin swings from a Schottky diode drop below $INTV_{CC}$ to V_{IN} + $INTV_{CC}$.

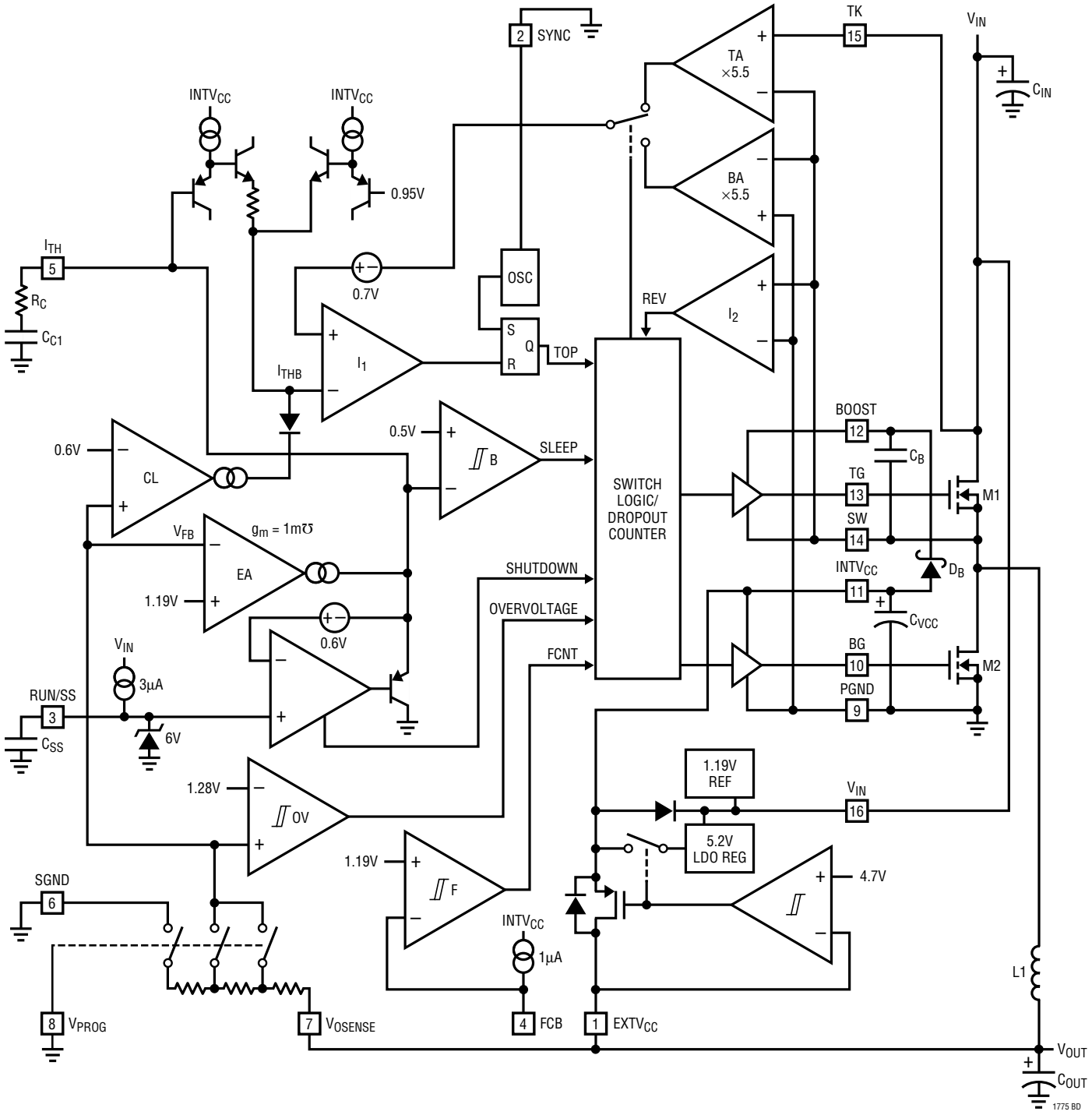
TG (Pin 13): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

SW (Pin 14): Switch Node. The (–) terminal of the bootstrap capacitor connects here. This pin swings from a diode drop below ground up to V_{IN}.

TK (Pin 15): Top MOSFET Kelvin Sense. MOSFET V_{DS} sensing requires this pin to be routed to the drain of the top MOSFET separately from V_{IN}.

V_{IN} (Pin 16): Main Supply Input. Decouple this pin to ground with an RC filter (1Ω, 0.1µF) for applications above 3A.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC1775 is a constant frequency, current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on when the RS latch is set by the on-chip oscillator and is turned off when the current comparator I_1 resets the latch. While the top MOSFET is turned off, the bottom MOSFET is turned on until either the inductor current reverses, as determined by the current reversal comparator I_2, or the next cycle begins. Inductor current is measured by sensing the V_{DS} potential across the conducting MOSFET. The output of the appropriate sense amplifier (TA or BA) is selected by the switch logic and applied to the current comparator. The voltage on the I_{TH} pin sets the comparator threshold corresponding to peak inductor current. The error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} from the output voltage with the internal 1.19V reference. The V_{PROG} pin selects whether the feedback voltage is taken directly from the V_{OSENSE} pin or is derived from an on-chip resistive divider. When the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

The internal oscillator can be synchronized to an external clock applied to the SYNC pin and can lock to a frequency between 100% and 150% of its nominal 150kHz rate. When the SYNC pin is left open, it is pulled low internally and the oscillator runs at its normal rate. If this pin is taken above 1.2V, the oscillator will run at its maximum 225kHz rate.

Pulling the RUN/SS pin low forces the controller into its shutdown state and turns off both MOSFETs. Releasing the RUN/SS pin allows an internal 3μA current source to charge up an external soft start capacitor C_{SS}. When this voltage reaches 1.4V, the controller begins switching, but with the I_{TH} voltage clamped at approximately 0.8V. As C_{SS} continues to charge, the clamp is raised until full range operation is restored.

The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is normally recharged from $INTV_{CC}$ through a diode D_B when the top MOSFET is turned off. As V_{IN} decreases towards V_{OUT}, the converter will attempt to turn on the top MOSFET continuously (''dropout''). A dropout counter detects this condition and forces the top MOSFET to turn off for about 500ns every tenth cycle to recharge the bootstrap capacitor.

An overvoltage comparator OV guards against transient overshoots and other conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback current limiting for an output shorted to ground is provided by a transconductance amplifer CL. As V_{FB} drops below 0.6V, the buffered I_{TH} input to the current comparator is gradually pulled down to a 0.95V clamp. This reduces peak inductor current to about one fifth of its maximum value.

Low Current Operation

The LTC1775 is capable of Burst Mode operation at low load currents. If the error amplifier drives the I_{TH} voltage below 0.95V, the buffered I_{TH} input to the current comparator will remain clamped at 0.95V. The inductor current peak is then held at approximately $60mV/R_{DS(ON)(TOP)}$. If I_{TH} then drops below 0.5V, the Burst Mode comparator B will turn off both MOSFETs. The load current will be supplied solely by the output capacitor until I_{TH} rises above the 50mV hysteresis of the comparator and switching is resumed. Burst Mode operation is disabled by comparator F when the FCB pin is brought below 1.19V. This forces continuous operation and can assist secondary winding regulation.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal circuitry of the LTC1775 is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open, an internal 5.2V low dropout regulator supplies the $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is raised above 4.7V, the internal regulator is turned off and an internal switch connects $EXTV_{CC}$ to $INTV_{CC}$. This allows a high efficiency source, such as the primary or a secondary output of the converter itself, to provide the $INTV_{CC}$ power.

APPLICATIONS INFORMATION

The basic LTC1775 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance for the desired current level. Since the LTC1775 senses current using the on-resistance of the power MOSFET, the maximum application current primarily determines the choice of MOSFET. The operating frequency and the inductor are chosen based largely on the desired amount of ripple current. Finally, C_{IN} is selected for its ability to handle the RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple specification.

Power MOSFET Selection

The LTC1775 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{D(MAX)}$.

The gate drive voltage is set by the 5.2V $INTV_{CC}$ supply. Consequently, logic level threshold MOSFETs must be used in LTC1775 applications. If low input voltage operation is expected ($V_{IN} < 5V$), then sub-logic level threshold MOSFETs should be used. Pay close attention to the $V_{(BR)DSS}$ specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

The MOSFET on-resistance is chosen based on the required load current. The maximum average output current $I_{O(MAX)}$ is equal to the peak inductor current less half the peak-to-peak ripple current ΔI_L. The peak inductor current is inherently limited in a current mode controller by the current threshold I_{TH} range. The corresponding maximum V_{DS} sense voltage is about 300mV under normal conditions. The LTC1775 will not allow peak inductor current to exceed $300mV/R_{DS(ON)(TOP)}$. The following equation is a good guide for determining the required $R_{DS(ON)(MAX)}$ at 25°C (manufacturer's specification), allowing some margin for ripple current, current limit and variations in the LTC1775 and external component values:

$$R_{DS(ON)(MAX)} \cong \frac{240mV}{(I_{O(MAX)})(\rho_T)}$$

The ρ_T is a normalized term accounting for the significant variation in $R_{DS(ON)}$ with temperature, typically about 0.4%/°C as shown in Figure 2. Junction to ambient temperature T_{JA} is around 20°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{90°C} \cong 1.3$ in the above equation is a reasonable choice. This equation is plotted in Figure 3 to illustrate the dependence of maximum output current on $R_{DS(ON)}$. Some popular MOSFETs are shown as data points.

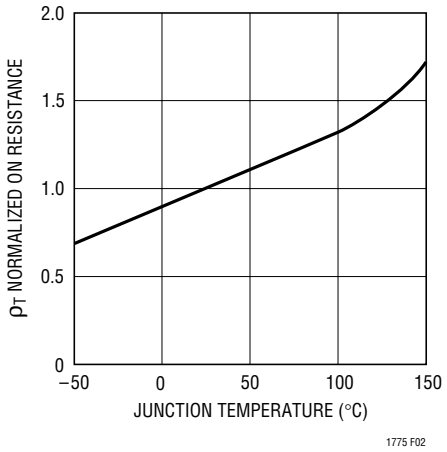


Figure 2. $R_{DS(ON)}$ vs Temperature

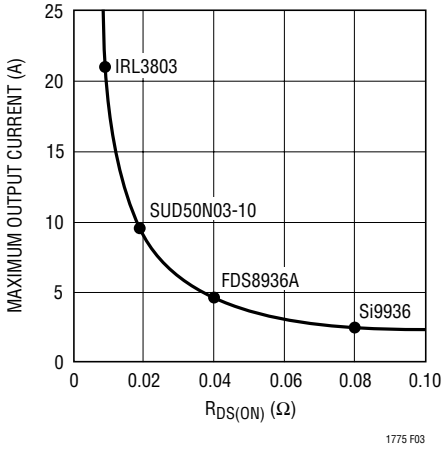


Figure 3. Maximum Output Current vs $R_{DS(ON)}$ at V_{GS} = 4.5V

The 300mV maximum sense voltage of the LTC1775 allows a large current to be obtained from power MOSFET switches. It also causes a significant amount of power dissipation in those switches and careful attention must be

APPLICATIONS INFORMATION

paid to the resulting thermal issues. Under DC conditions, the maximum power that can be dissipated by a MOSFET switch limits the current through it:

$$I_{DS(MAX)} = \sqrt{\frac{P}{R_{DS(ON)}}} = \sqrt{\frac{T_{J(MAX)} - T_A}{\theta_{JA} R_{DS(ON)} \rho_{TJ(MAX)}}}$$

For example, the SUD50N03-10 with $T_{J(MAX)}$ = 175°C, T_A =70°, θ_{JA} = 30° C/W, $R_{DS(ON)}$ = 0.019Ω, $\rho_{TJ(MAX)}$ = 1.8 can operate with a maximum DC current of 10A. In a switching application, the actual power dissipation is increased by the transition losses and is reduced by the switch duty cycle. When the LTC1775 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{O(MAX)}{}^2)(\rho_{T(TOP)})(R_{DS(ON)}) + (k)(V_{IN}{}^2)(I_{O(MAX)})(C_{RSS})(f)$$

$$P_{BOT} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)(I_{O(MAX)}{}^2)(\rho_{T(BOT)})(R_{DS(ON)})$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The constant k = 1.7 can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle is nearly 100%. The temperature rise of the MOSFETs depends on the effective thermal resistance θ_{JA} of the heat sink used in the application. Check the temperature of the MOSFET when testing applications and use appropriate heat sinking such as board power planes to spread the heat.

Operating Frequency and Synchronization

The choice of operating frequency and inductor value is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator runs at a nominal 150kHz frequency when the SYNC pin is left open or connected to ground. Pulling the SYNC pin above 1.2V will increase the frequency by 50%. The oscillator will injection lock to a clock signal applied to the SYNC pin with a frequency between 165kHz and 200kHz. The clock high level must exceed 1.2V for at least 1µs and no longer than 4µs as shown in Figure 4. The top MOSFET turn-on will synchronize with the rising edge of the clock.

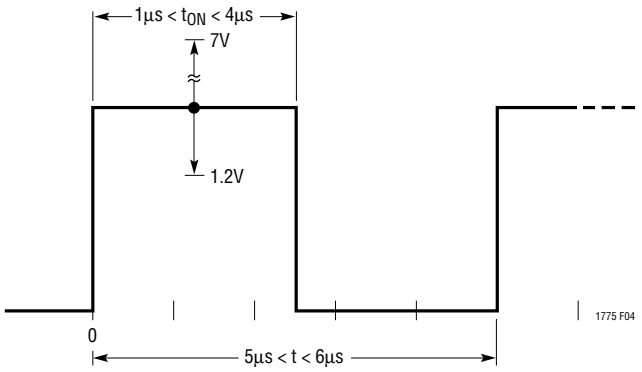


Figure 4. SYNC Clock Waveform

Inductor Value Selection

Given the desired input and output voltages, the inductor value and operating frequency directly determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{(f)(L)}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with small ripple current. To achieve this, however, requires a large inductor.

APPLICATIONS INFORMATION

A reasonable starting point is to choose a ripple current that is about 40% of $I_{O(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \left(\frac{V_{OUT}}{(f)(\Delta I_{L(MAX)})}\right)\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Burst Mode Operation Considerations

The choice of $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC1775 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{60mV}{R_{DS(ON)}}$$

The corresponding average current depends on the amount of ripple current. Lower inductor values (higher ΔI_L) will reduce the load current at which Burst Mode operation begins.

The output voltage ripple can increase during Burst Mode operation if ΔI_L is substantially less than I_{BURST}. This will primarily occur when the duty cycle is very close to unity (V_{IN} is close to V_{OUT}) or if very large value inductors are chosen. This is generally only a concern in applications with $V_{OUT} \geq$ 5V. At high duty cycles, a skipped cycle causes the inductor current to quickly descend to zero. However, it takes multiple cycles to ramp the current back up to $I_{BURST(PEAK)}$. During this interval, the output capacitor must supply the load current and enough charge may be lost to cause significant droop in the output voltage. It is a good idea to keep ΔI_L comparable to $I_{BURST(PEAK)}$. Otherwise, one might need to increase the output capacitance in order to reduce the voltage ripple or else disable Burst Mode operation by forcing continuous operation with the FCB pin.

Fault Conditions: Current Limit and Output Shorts

The LTC1775 current comparator can accommodate a maximum sense voltage of 300mV. This voltage and the sense resistance determine the maximum allowed peak inductor current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{300mV}{(R_{DS(ON)})(\rho_T)} - \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{O(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions which cause the highest power dissipation in the top MOSFET. Note that it is important to check for self-consistency between the assumed junction temperature of the top MOSFET and the resulting value of I_{LIMIT} which heats the junction.

Caution should be used when setting the current limit based upon $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable, but perhaps overly conservative, assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum $R_{DS(ON)}$ lies above it. Consult the MOSFET manufacturer for further guidelines.

The LTC1775 includes current foldback to help further limit load current when the output is shorted to ground. If the output falls by more than half, then the maximum sense voltage is progressively lowered from 300mV to about 80mV. Under short-circuit conditions with very low duty cycle, the LTC1775 will begin skipping cycles in order to limit the short-circuit current. In this situation the bottom MOSFET $R_{DS(ON)}$ will control the inductor current valley rather than the top MOSFET controlling the inductor current peak. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC1775 (approximately 0.5µs), the input voltage, and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\ V_{IN}/L.$$

The resulting short-circuit current is:

$$I_{SC} = \frac{80mV}{(R_{DS(ON)(BOT)})(\rho_T)} + \frac{1}{2}\Delta I_{L(SC)}$$

APPLICATIONS INFORMATION

Normally, the top and bottom MOSFETs will be of the same type. A bottom MOSFET with lower $R_{DS(ON)}$ than the top may be chosen if the resulting increase in short-circuit current is tolerable. However, the bottom MOSFET should never be chosen to have a higher nominal $R_{DS(ON)}$ than the top MOSFET.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses rapidly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Schottky Diode Selection

The Schottky diode D1 shown in Figure 1 conducts during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 1A Schottky diode is generally a good size for 3A to 5A regulators. The diode may be omitted if the efficiency loss can be tolerated.

Parasitic Lead Inductance Effects

Because the LTC1775 is designed to operate with relatively large currents through single (or multiple) MOSFET switches, the lead inductance of these power switches can become a significant concern. The table below shows typical values of lead inductance for some common packages:

MOSFET Package	Lead Inductance
TO-220	4nH to 12nH
DDPAK	4nH
DPAK	1.5nH
SO-8	1nH

Of particular concern are switches in TO-220 packages which can have a series inductance of between 4nH and 12nH depending upon the depth of insertion into the circuit board. When the main (top) switch is turned on, the lead inductance LP forms a voltage divider with the power inductor L1. The voltage V_{LP} across this parasitic adds to the voltage from the switch on-resistance and increases the current sense voltage.

$$V_{LP} = (V_{IN} - V_{OUT})LP/L1$$

The result is lower value of current limit than would have been expected otherwise. For example, a 10nH lead inductance with a 5μH power inductor has 50mV across it when V_{IN} = 30V and V_{OUT} = 5V. Thus, the 300mV current limit will be reached when the switch voltage due to on-resistance is only 250mV, a 17% reduction. This effect is most noticeable at higher input voltages.

Lead inductance also reduces the benefit of the Schottky diode D1 by delaying commutation of the inductor current from the diode over to the synchronous (bottom) switch. With the diode forward biased when the synchronous switch turns on, there is only about 500mV applied across the lead and trace inductance between the switch and the diode. It takes about 400ns to commutate a 20A current in this case. This delay reduces efficiency and can also increase the foldback current limit of the LTC1775. The

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APPLICATIONS INFORMATION

Schottky diode must be placed next to the synchronous switch to minimize this effect. One also might consider using a power switch with an integrated Schottky diode, or omitting the diode altogether in high current applications.

C_{IN} and C_{OUT} Selection

In continuous mode, the drain current of the top MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large input voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{(8)(f)(C_{OUT})} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering and has the required RMS current rating.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON (organic semiconductor dielectric) capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the effect of their lead inductance.

In surface mount applications, multiple capacitors placed in parallel may be required to meet the ESR, RMS current handling and load step requirements. Dry tantalum, special polymer and aluminum electrolytic capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Several excellent surge-tested choices are the AVX TPS and TPSV or the KEMET T510 series. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-driven applications providing that consideration is given to ripple current ratings and long term reliability. Other capacitor types include Nichicon PL, NEC Neocap, Panasonic SP and Sprague 595D series.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5.2V supply which powers the drivers and internal circuitry within the LTC1775. The $INTV_{CC}$ pin can supply a maximum RMS current of 50mA and must be bypassed to ground with a minimum of 4.7µF tantalum or low ESR electrolytic capacitance. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the LTC1775 to exceed its maximum junction temperature rating. Most of the supply current drives the MOSFET gates unless an external $EXTV_{CC}$ source is used. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, the LTC1775CGN is limited to less than 14mA from a 30V supply:

$$T_J = 70°C + (14mA)(30V)(130°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating in continuous mode at high V_{IN}. Relief can be provided by using the $EXTV_{CC}$ pin to provide the gate drive current.

APPLICATIONS INFORMATION

$EXTV_{CC}$ Connection

The LTC1775 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Whenever the $EXTV_{CC}$ pin is above 4.7V the internal 5.2V regulator shuts off, the switch closes and $INTV_{CC}$ power is supplied via $EXTV_{CC}$ until $EXTV_{CC}$ drops below 4.5V. This allows the MOSFET gate drive and control power to be derived from the output or other external source during normal operation. When the output is out of regulation (start-up, short circuit) power is supplied from the internal regulator. Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current supplying the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.2V regulator resulting in a low current efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

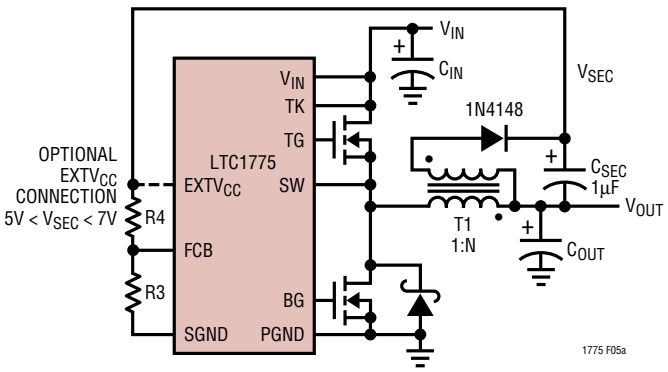


Figure 5a: Secondary Output Loop and $EXTV_{CC}$ Connection

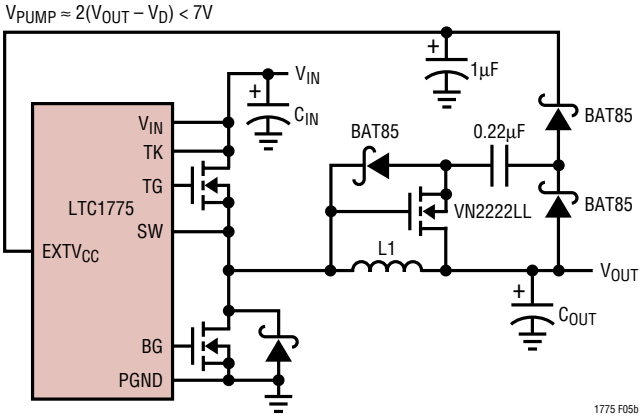


Figure 5b: Capacitive Charge Pump for $EXTV_{CC}$

3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.7V. This can be done with either an inductive boost winding as shown in Figure 5a or a capacitive charge pump as shown in Figure 5b.
4. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 7V range ($EXTV_{CC} < V_{IN}$), it may be used to power $EXTV_{CC}$.

Figure 6 shows how one can easily generate a suitable $EXTV_{CC}$ voltage from V_{IN}. This circuit still derives the gate drive current from V_{IN}, but it removes the power dissipation from the LTC1775 internal regulator and increases the gate drive voltage.

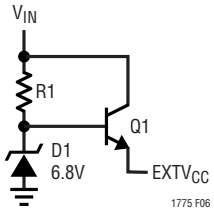


Figure 6. $EXTV_{CC}$ Power Supplied from V_{IN}

Note that $R_{DS(ON)}$ also varies with the gate drive level. If gate drives other than the 5.2V $INTV_{CC}$ are used, this must be accounted for when selecting the MOSFET $R_{DS(ON)}$. Particular care should be taken with applications where $EXTV_{CC}$ is connected to the output. When the output

APPLICATIONS INFORMATION

voltage is between 4.7V and 5.2V, $INTV_{CC}$ will be connected to the output and the gate drive is reduced. The resulting increase in $R_{DS(ON)}$ will also lower the current limit. Even applications with $V_{OUT} > 5.2V$ will traverse this region during start-up and must take into account the reduced current limit.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor (C_B in the functional diagram) connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the SW node is low. Note that the voltage across C_B is about a diode drop below $INTV_{CC}$. When the top MOSFET turns on, the switch node voltage rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + $INTV_{CC}$. During dropout operation, C_B supplies the top driver for as long as ten cycles between refreshes. Thus, the boost capacitance needs to store about 100 times the gate charge required by the top MOSFET. In many applications 0.1µF to 0.47µF is adequate.

When adjusting the gate drive level , the final arbiter is the total input current for the regulator. If you make a change and the input current decreases, then you improved the efficiency. If there is no change in input current, then there is no change in efficiency.

External Gate Drive Buffer

The LTC1775 drivers are adequate for driving up to about 30nC into MOSFET switches. When using large single, or multiple, MOSFET switches, external buffers may be required to provide additional gate drive capability. Special purpose gate driver circuits such as the LTC1693 are ideal in such cases. Alternately, the external buffer circuit shown in Figure 7 can be used. Note that the bipolar devices reduce the signal swing at the gate by a diode drop. Thus, the LTC1775 requires an increased $EXTV_{CC}$ voltage of about 6V (such as provided by the Figure 6 circuit) when using this driver.

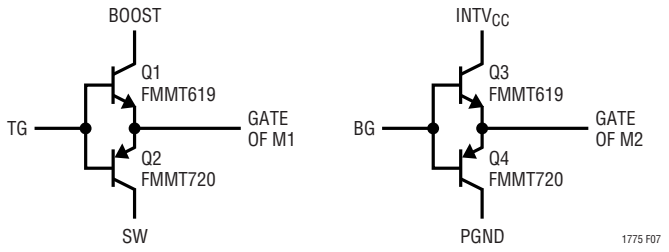


Figure 7. Optional External Gate Driver

Output Voltage Programming

The LTC1775 has a pin selectable output voltage determined by the V_{PROG} pin as follows:

V_{PROG}	V_{OUT}
0V	3.3V
$INTV_{CC}$	5V
Open	Adjustable

Remote sensing of the output voltage is provided by the V_{OSENSE} pin. For fixed 3.3V and 5V output applications an internal resistive divider is used and the V_{OSENSE} pin is connected directly to the output voltage as shown in Figure 8a. When using an external resistive divider, the V_{PROG} pin is left open and the V_{OSENSE} pin is connected to feedback resistors as shown in Figure 8b. The output voltage is set by the divider as:

$$V_{OUT} = 1.19V\left(1+\frac{R2}{R1}\right)$$

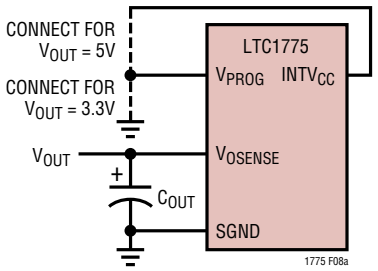


Figure 8a. Fixed 3.3V or 5V V_{OUT}

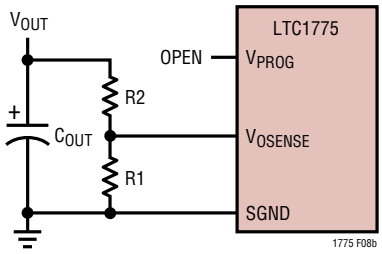


Figure 8b. Adjustable V_{OUT}

APPLICATIONS INFORMATION

Run/Soft Start Function

The RUN/SS pin is a dual purpose pin that provides a soft start function and a means to shut down the LTC1775. Soft start reduces surge currents from V_{IN} by gradually increasing the controller's current limit $I_{TH(MAX)}$. This pin can also be used for power supply sequencing.

Pulling the RUN/SS pin below 1.4V puts the LTC1775 into a low quiescent current shutdown ($I_Q < 30\mu A$). This pin can be driven directly from logic as shown in Figure 9. Releasing the RUN/SS pin allows an internal 3μA current source to charge up the soft-start capacitor C_{SS}. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \left(\frac{1.4V}{3\mu A}\right)C_{SS} = (0.5s/\mu F)C_{SS}$$

When the voltage on RUN/SS reaches 1.4V the LTC1775 begins operating with a clamp on I_{TH} at 0.8V. As the voltage on RUN/SS increases to approximately 3.1V, the clamp on I_{TH} is raised until its full 2.4V range is restored. This takes an additional 0.5s/μF. During this time the load current will be folded back to approximately $80mV/R_{DS(ON)}$ until the output reaches half of its final value.

Diode D1 in Figure 9 reduces the start delay while allowing C_{SS} to charge up slowly for the soft start function. This diode and C_{SS} can be deleted if soft start is not needed. The RUN/SS pin has an internal 6V zener clamp (See Functional Diagram).

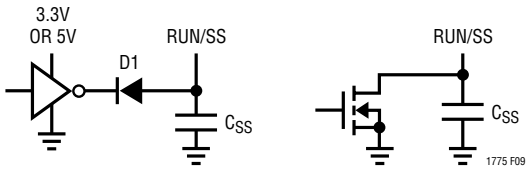


Figure 9. RUN/SS Pin Interfacing

FCB Pin Operation

When the FCB pin drops below its 1.19V threshold, continuous synchronous operation is forced. In this case, the top and bottom MOSFETs continue to be driven regardless of the load on the main output. Burst Mode operation is disabled and current reversal under light loads is allowed in the inductor.

In addition to providing a logic input to force continuous operation, the FCB pin provides a means to regulate a flyback winding output. It can force continuous synchronous operation when needed by the flyback winding, regardless of the main output load.

The secondary output voltage V_{SEC} is normally set as shown in Figure 5a by the turns ratio N of the transformer:

$$V_{SEC} \cong (N + 1)V_{OUT}$$

However, if the controller goes into Burst Mode operation and halts switching due to a light main load current, then V_{SEC} will droop. An external resistor divider from V_{SEC} to the FCB pin sets a minimum voltage $V_{SEC(MIN)}$:

$$V_{SEC(MIN)} \cong 1.19V\left(1 + \frac{R4}{R3}\right)$$

If V_{SEC} drops below this level, the FCB voltage forces continuous operation until V_{SEC} is again above its minimum.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC1775 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{(V_{IN})(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1775 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC1775 is generally about 0.5μs. However, as the peak sense voltage ($I_{L(PEAK)} \bullet R_{DS(ON)}$) decreases, the minimum on-time gradually increases up to about 0.7μs. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of

APPLICATIONS INFORMATION

cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power (×100%). Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1775 circuits:

1. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. The driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched on and then off, a packet of gate charge Q_g moves from $INTV_{CC}$ to ground. The resulting current out of $INTV_{CC}$ is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$.

   By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application at 400mA load, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the loss from 10% (if the driver was powered directly from V_{IN}) to about 3%.

2. DC I^2R Losses. Since there is no separate sense resistor, DC I^2R losses arise only from the resistances of the MOSFETs and inductor. In continuous mode the average output current flows through L, but is "chopped" between the top MOSFET and the bottom MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistance of L to obtain the DC I^2R loss. For example, if each $R_{DS(ON)} = 0.05\Omega$ and $R_L = 0.15\Omega$, then the total resistance is 0.2Ω. This results in losses ranging from 2% to 8% as the output current increases from 0.5A to 2A for a 5V output. I^2R losses cause the efficiency to drop at high output currents.

3. Transition losses apply only to the topside MOSFET, and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7)(V_{IN}^2)(I_{O(MAX)})(C_{RSS})(f)$$

4. LTC1775 V_{IN} supply current. The V_{IN} current is the DC supply current to the controller excluding MOSFET gate drive current. Total supply current is typically about 850μA. If $EXTV_{CC}$ is connected to 5V, the LTC1775 will draw only 330μA from V_{IN} and the remaining 520μA will come from $EXTV_{CC}$. V_{IN} current results in a small (<1%) loss which increases with V_{IN}.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}, and C_{OUT} begins to charge or discharge. The regulator loop acts on the resulting feedback error signal to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} pin external components shown in Figure 1 will provide adequate compensation for most applications.

A second, more severe transient is caused by connecting loads with large (>1μF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive in order to limit the inrush current to the load.

APPLICATIONS INFORMATION

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main power line in an automobile is the source of a number of nasty potential transients, including load dump, reverse and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 10 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC1775 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET $V_{(BR)DSS}$.

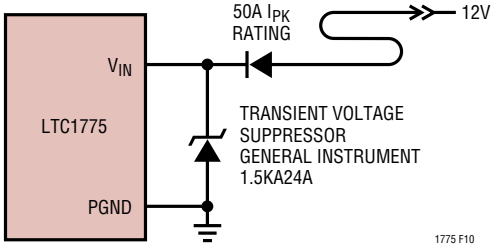


Figure 10. Automotive Application Protection

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 6V to 22V (15V nominal), V_{OUT} = 5V, $I_{O(MAX)}$ = 10A. The required $R_{DS(ON)}$ can immediately be estimated:

$$R_{DS(ON)} = \frac{240mV}{(10A)(1.3)} = 0.018\Omega$$

A 0.019Ω Siliconix SUD50N03-10 MOSFET (θ_{JA} = 30°C/W) is close to this value.

For 40% ripple current at maximum V_{IN} the inductor should be:

$$L \geq \frac{5V}{(150kHz)(0.4)(10A)}\left(1-\frac{5V}{22V}\right) = 6.4\mu H$$

Choosing a Magnetics 55380-A2 core with 8 turns of 15 gauge wire yields a 6µH inductor. The resulting maximum ripple current will be:

$$\Delta I_{L(MAX)} = \frac{5V}{(150kHz)(6\mu H)}\left(1-\frac{5V}{22V}\right) = 4.3A$$

Next, check that the minimum value of the current limit is acceptable. Assume a junction temperature about 20°C above the 70°C ambient with $\rho_{90°C}$ = 1.3.

$$I_{LIMIT} \geq \frac{300mV}{(0.019\Omega)(1.3)} - \left(\frac{1}{2}\right)4.3A = 10A$$

Now double-check the assumed T_J:

$$P_{TOP} = \frac{5V}{22V}(10A)^2(1.3)(0.019\Omega) + (1.7)(22V)^2(10A)(170pF)(150kHz)$$
$$= 0.56W + 0.21W = 0.77mW$$

T_J = 70°C + (0.77W)(30°C/W) = 93°C

Since ρ(93°C) ≅ ρ(90°C), the solution is self-consistent.

APPLICATIONS INFORMATION

A short circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{80mV}{(0.013\Omega)(1.1)} + \left(\frac{1}{2}\right)\frac{(15V)(0.5\mu s)}{6\mu H} = 6.2A$$

with a typical value of $R_{DS(ON)}$ and $\rho(50°C) = 1.1$. The resulting power dissipated in the bottom MOSFET is:

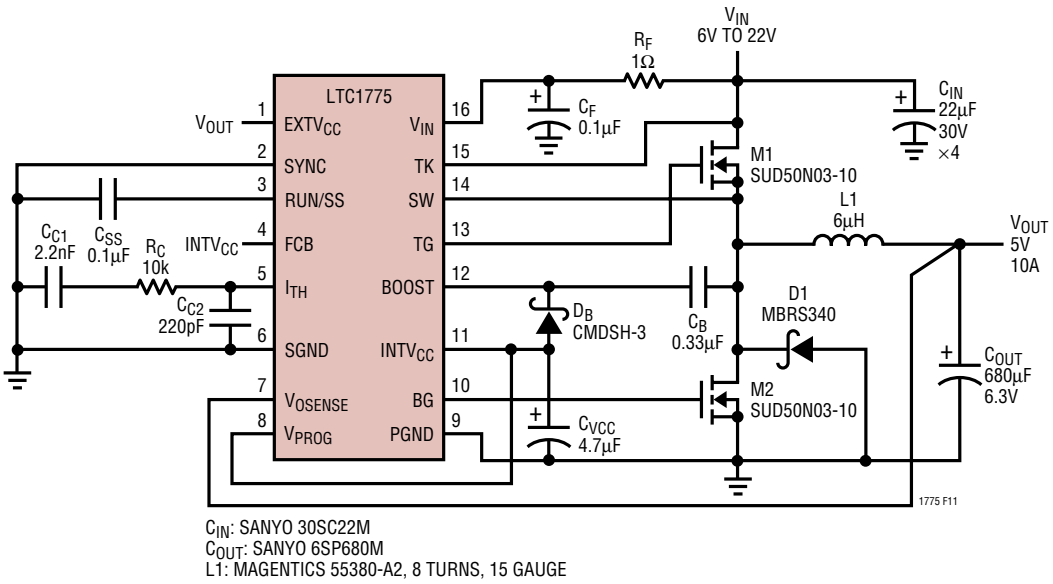
$$P_{BOT} = \frac{15V - 5V}{15V}(6.2A)^2(1.1)(0.013\Omega) = 0.37W$$

which is less than under full load conditions.

C_{IN} is chosen for an RMS current rating of at least 5A at temperature. C_{OUT} is chosen with an ESR of 0.013Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage and is approximately:

$$\Delta V_O = (\Delta I_{L(MAX)})(ESR) = (4.3A)(0.013\Omega) = 56mV$$

The complete circuit is shown in Figure 11.



C_{IN}: SANYO 30SC22M
C_{OUT}: SANYO 6SP680M
L1: MAGENTICS 55380-A2, 8 TURNS, 15 GAUGE

Figure 11. 5V/10A Fixed Output from Design Example

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1775. These items are also illustrated graphically in the layout diagram of Figure 12. Check the following in your layout:

1) Connect the TK lead directly to the drain of the topside MOSFET. Then connect the drain to the (+) plate of C_{IN}. This capacitor provides the AC current to the top MOSFET.

2) The power ground pin connects directly to the source of the bottom N-channel MOSFET. Then connect the source to the anode of the Schottky diode (if used) and (–) plate of C_{IN}, which should have as short lead lengths as possible.

3) The LTC1775 signal ground pin should connect to the (–) plate of C_{OUT}. Connect the (–) plate of C_{OUT} to power ground at the source of the bottom MOSFET. All small-signal components (R2, C_{SS}, C_C, etc.) should return directly to SGND.

4) Keep the switch node SW away from sensitive small-signal nodes. Ideally the switch node should be placed on the opposite side of the power MOSFETs from the LTC1775.

5) Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ pin and the power ground pin. This capacitor carries the MOSFET gate drive current.

6) Does the V_{OSENSE} pin connect as close as possible to the load? In adjustable applications, the resistive divider (R1, R2) must be connected between the load and signal ground. Place the divider near the LTC1775 in order to keep the high impedance V_{OSENSE} node short.

7) For applications with multiple switching power converters connected to the same V_{IN}, ensure that the input filter capacitance for the LTC1775 is not shared with the other converters. AC input current from another converter will cause substantial input voltage ripple that may interfere with proper operation of the LTC1775. A few inches of PC trace or wire ($L_{TRACE} \approx 100nH$) between C_{IN} and the V_{IN} supply is sufficient to prevent sharing.

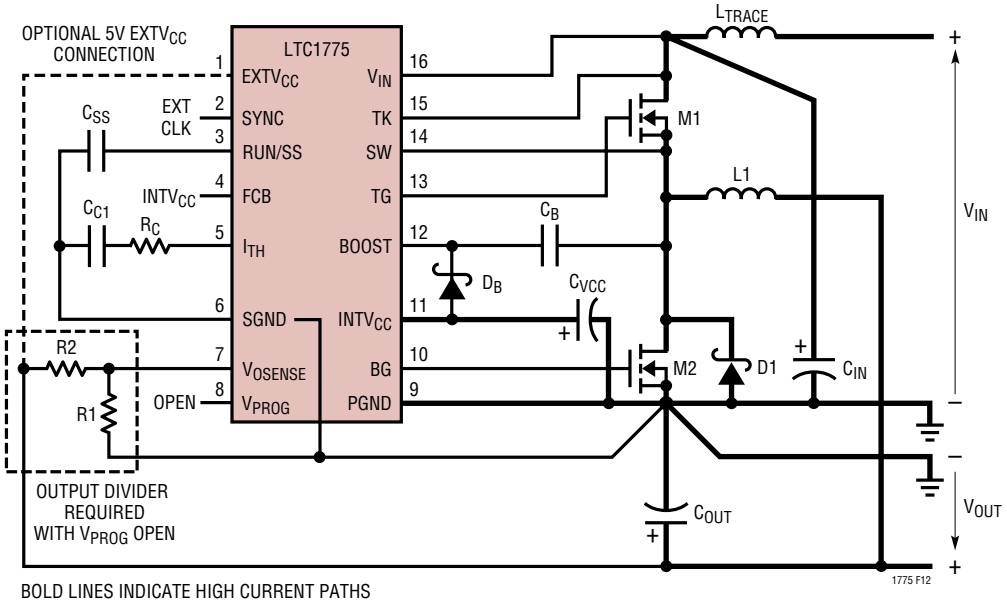
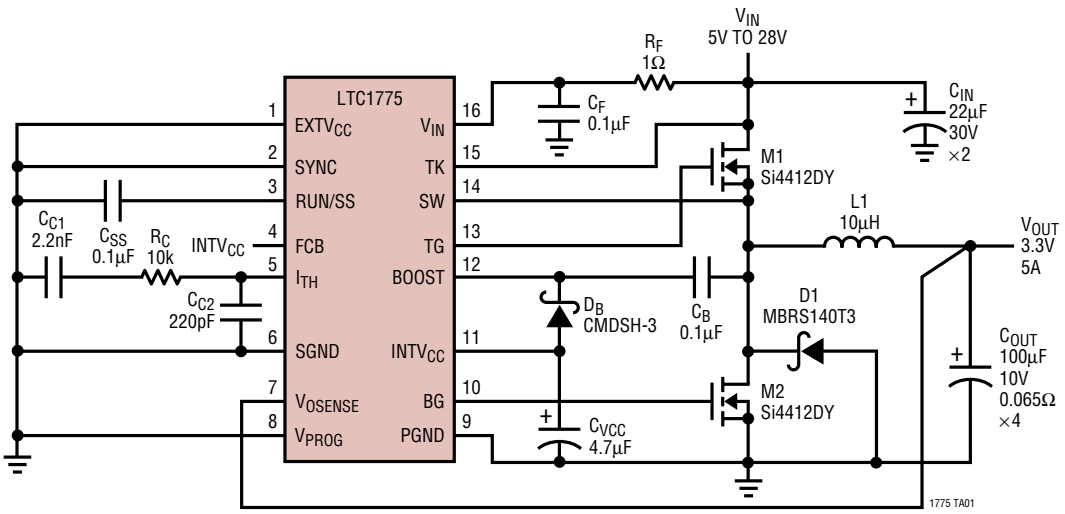


Figure 12. LTC1775 Layout Diagram

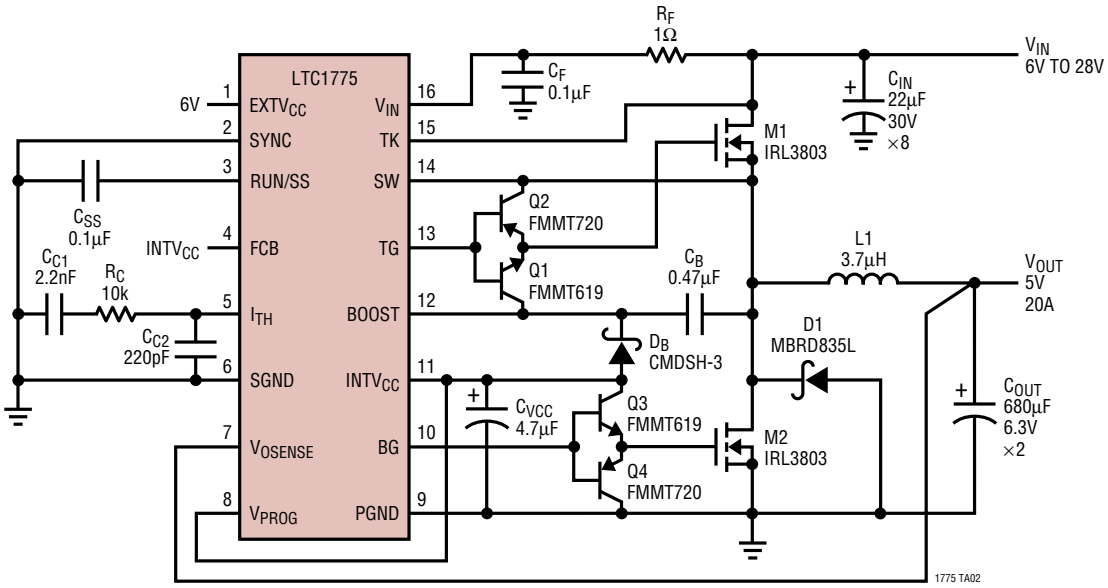
TYPICAL APPLICATIONS

3.3V/5A Fixed Output



CIN: SANYO 30SC22M
COUT: AVX TPSD107M010R0065
L1: SUMIDA CDRH-125

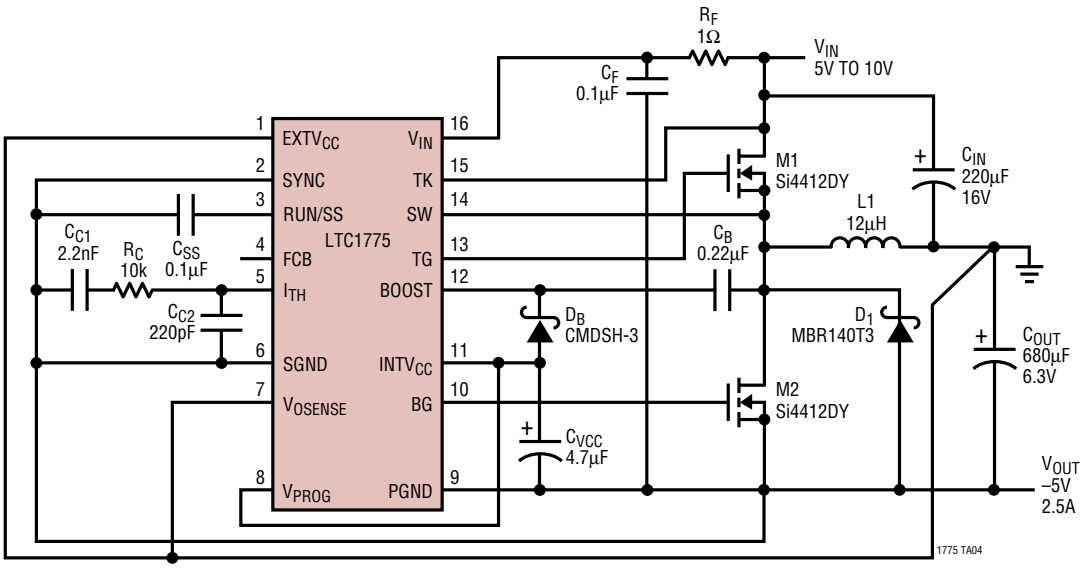
5V/20A Fixed Output



CIN: SANYO 30SC22M
COUT: SANYO 6SP680M
L1: MAGNETICS 55206-A2, 3.7µH, 6 TURNS, 13 GAUGE

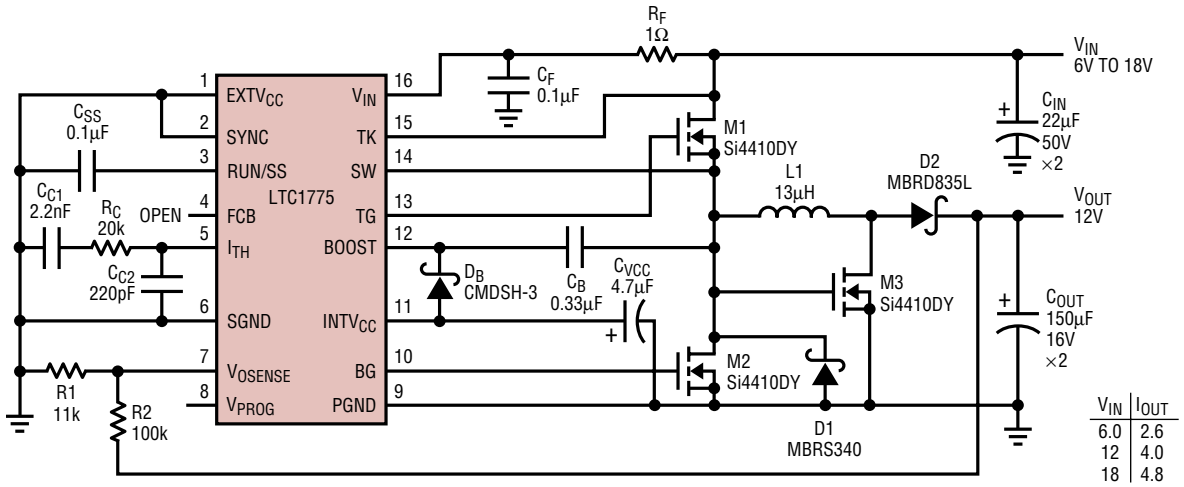
TYPICAL APPLICATIONS

–5V/2.5A Positive to Negative Converter



CIN: SANYO 16SV220M
COUT: SANYO 6SP680M
L1: 12µH, 5A

12V Output, Single Inductor, Buck/Boost Converter



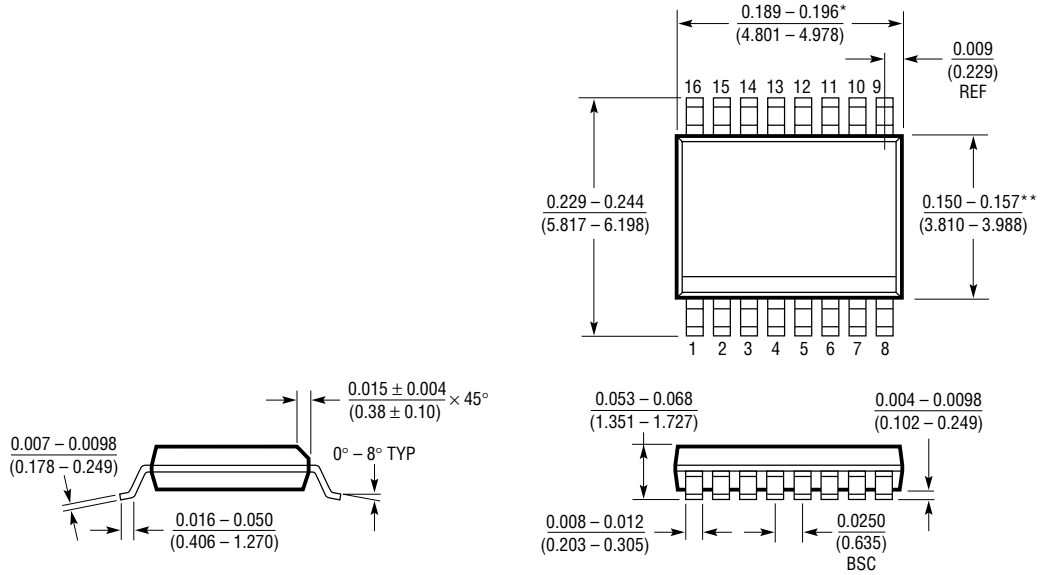
VIN	IOUT
6.0	2.6
12	4.0
18	4.8

CIN: UNITED CHEMICON THCR70E1H226ZT-CBU
COUT: SANYO 165A-150M
L1: 13µH/11A

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

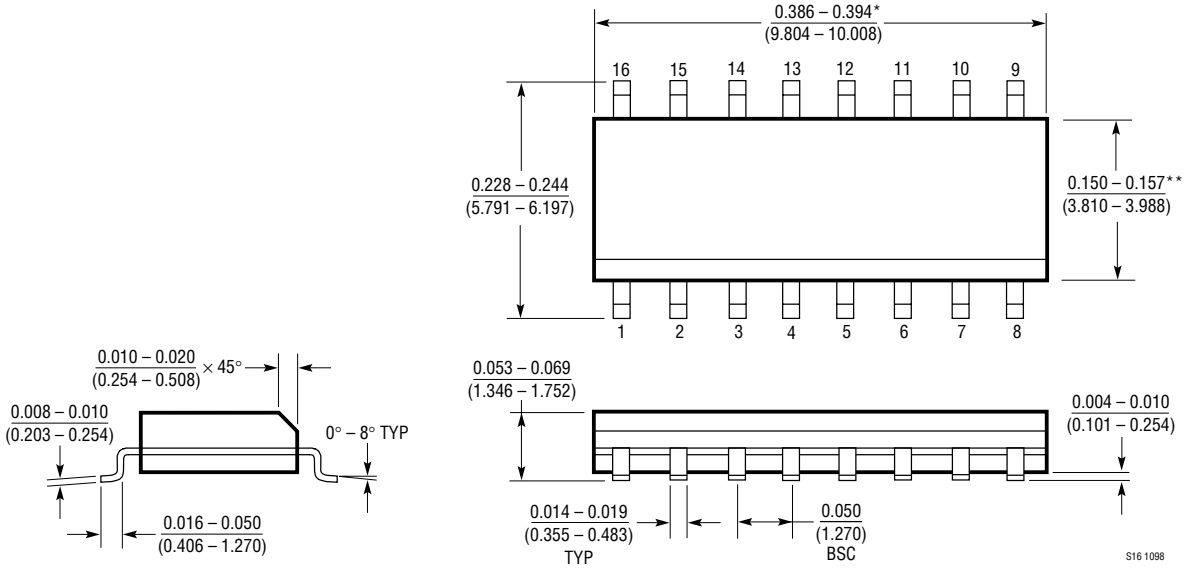


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 1098

LINEAR TECHNOLOGY

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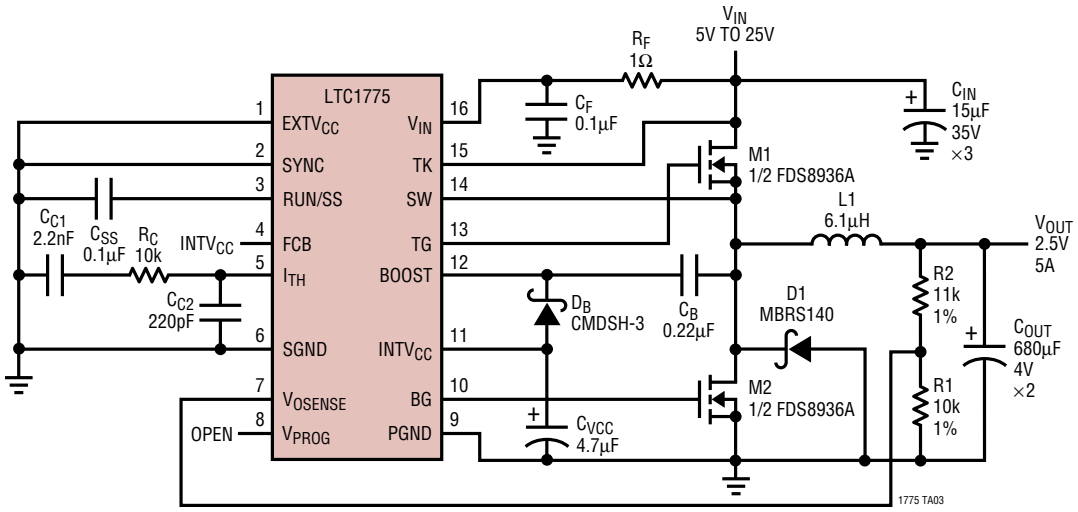
TYPICAL APPLICATIONS

2.5V/5A Adjustable Output



CIN: KEMET T495X156M035AS
COUT: KEMET T510X687K004AS
L1: SUMIDA CDRH127-6R1

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1339	High Power Synchronous DC/DC Controller	60V Maximum Input Voltage
LTC1436A-PLL	High Efficiency Low Noise Synchronous Step-Down Controller	PLL Synchronization and Auxiliary Linear Regulator
LTC1438	Dual High Efficiency Step-Down Controller	Power-On Reset and Low-Battery Comparator
LTC1530	High Power Synchronous Step-Down Controller	SO-8 with Current Limit, No R_{SENSE} Saves Space, Fixed Frequency Ideal for 5V to 3.3V
LTC1538-AUX	Dual High Efficiency Step-Down Controller	5V Standby Output and Auxiliary Linear Regulator
LTC1625	No R_{SENSE} Current Mode Synchronous Step-Down Controller	Burst Mode Operation, 16-Lead GN Package
LTC1628	Dual High Efficiency 2-Phase Step-Down Controller	Antiphase Drive, Standby 5V and 3.3V LDO, Fault Protection, V_{IN} Up to 36V
LTC1629	PolyPhase™ High Efficiency Step-Down Controller	Current Mode Ensures Accurate Current Sharing, Expandable Up to 200A, V_{IN} Up to 36V
LTC1649	3.3V Input High Power Step-Down Controller	2.7V to 5V Input, 90% Efficiency, Ideal for 3.3V to 1.xV – 2.xV Up to 20A
LTC1702	Dual 2-Phase High Frequency, High Efficiency Voltage Mode Synchronous Step-Down Controller	500kHz; V_{IN} Up to 7V; V_{OUT1}, V_{OUT2} as Low as 2.x, 1.x, I_{OUT1}, I_{OUT2} as High as 20A; No Sense Resistor Required
LTC1735	High Efficiency Synchronous Step-Down Controller	Output Fault Protection, 16-Pin GN Package, $4V \le V_{IN} \le 36V$

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- Alternative Solution
- Excess Inventory Management